

## 1 Program Structure and Execution

### 1.1 Information Storage

Computers store information as a series of bits. These bits can be interpreted by users in either source binary, comfortable decimal, or compatible hexadecimal.

Computers also have a default word size, i.e. the largest continuous block of memory the computer can access. Currently, most computers are 32 bit, however more are becoming 64.

Going with word size, each data type also has a typical size in memory:

C Declaration	32 Bit	64 Bit
char	1	1
short int	2	2
int	4	4
long int	4	8
long long int	8	8
char*	4	8
float	4	4
double	8	8

Table 1: Size of C Data Types

Besides the bits themselves, the order also matters, which brings up the distinction between little-endian and big-endian<sup>1</sup>. Big Endian has the highest place values put in the lowest memory location, while Little Endian has the lowest place values put in the lowest memory location.

### 1.2 Integer Arithmetic

Depending on the type of numbers involved in addition, we can get strange or unexpected behavior.

If we're dealing with large numbers, ones that are near to the word size in length, we have to be concerned about overflow. Overflow occurs when the full integer result cannot fit within the word size limits of the given data type.

Unsigned integer addition results in a something that resembles modular addition. If we have signed integers, we need to now concern ourselves with the negative numbers as well. Negative overflow often results in a positive number due to the definition of two's complement<sup>2</sup>.

<sup>1</sup>Names stolen from Gilmore's Travels.

<sup>2</sup>Computers represent negative numbers by essentially inverting the bits. Normal binary adds each place, this system subtracts each place from the highest set bit. For a 4 bit word size, the number 0011 would actually be -5 instead of 3.

### 1.3 Floating Point


The first method of expressing floating point numbers for a computer was through fractional binary numbers. These numbers had the form:

$$\frac{b_{p-1}}{2^{p-1}} \frac{b_{p-2}}{2^{p-2}} \dots \frac{b_2}{2^2} \frac{b_1}{2^1} \frac{b_0}{2^0} \dots \frac{b_{-1}}{2^{-1}} \frac{b_{-2}}{2^{-2}} \dots \frac{b_{-p}}{2^{-p}}$$

The inherent issue with this method, is that it's not very good at dealing with larger numbers. This is where IEEE floating point standard comes in, which has the form:

$$V = (-1)^s \times M \times 2^E$$

Where:

- $s$  determines sign
- $M$  is a fractional binary number ranging from 1 and  $2 - \epsilon$  or between 0 and  $1 - \epsilon$
- $E$  weighs the number by a power of 2.
- Final format looks as such: 

With these floating point numbers, we have three cases to deal with.

1. **Normalized Values** are the most common. This occurs when  $E$  is neither all ones or all zeros.

2. **Denormalized Values** occur when the exponent field is all zeros. These values express zero, as well as numbers that are very close to zero in absolute value.

3. **Special Values** occur when the exponent field is all ones. This either indicates  $\pm\infty$  or NaN when the fractional value is non-zero.

## 2 Machine Level Representation of Programs

Most computers primarily use assembly for a more human-readable machine code. This code is much more explicit than the C that it was derived from.

Several fields that are visible in assembly that we lacked access to before<sup>3</sup>:

- The program counter, referred to as PC, and called %eip, refers to the address in memory of the next instruction to be executed.
- The integer register file contains eight named locations storing 32 bit values.
- Condition code registers
- Floating point registers

<sup>3</sup>The x86 architecture, all memory addresses are for 32 bit platforms only.

halt	stop the program
nop	no operation
movl	register → register
imrml	immediate → register
movm	register → memory
imrm	immediate → memory
cmpl	integer operation
jnz	jump
call	call function
ret	Return
pushl	push onto stack
popl	pop from stack

Table 2: Y86 Instruction Set

## 5 Memory Hierarchy

### 5.1 RAM

RAM comes in two forms, static and dynamic. Static RAM is much more expensive, but way faster.

### 5.1.1 SRAM

Each bit is stored in a bistable memory cell. It can only be in one position or another, never both, or neither. It will also keep its state indefinitely as long as it's kept powered.

### 5.1.2 DRAM

Each bit is stored as a charge on a capacitor. They lose power relatively quickly and are much cheaper.

### 5.2 Disk Storage

Disks have several platters that spin at a fixed rate. The capacity of a disk is determined by

$$\text{Recording Density} \times \text{Track Density} = \text{Areol Density}$$

or

$$\text{Capacity} = \frac{\text{bytes}}{\text{sector}} \times \frac{\text{average sectors}}{\text{track}} \times \frac{\text{tracks}}{\text{surface}} \times \frac{\text{platters}}{\text{platter}} \times \frac{\text{disk}}{\text{disk}}$$

There is an actuator arm responsible for reading and writing from and to the disk.

Virtual address	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Set	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Way	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

(a) 32B Four cache, 32 entries, four way set associative

Way	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
00	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
01	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
02	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
03	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
04	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
05	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
06	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
07	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

(b) 32B Four cache, 32 entries, four way set associative

Way	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
00	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
01	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
02	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
03	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
04	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
05	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
06	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
07	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

(c) 32B Four cache, 32 entries, four way set associative

Way	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
00	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
01	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
02	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
03	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
04	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
05	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
06	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
07	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

(d) 32B Four cache, 32 entries, four way set associative

F	5A	0	...	...	...	...	...
---	----	---	-----	-----	-----	-----	-----

(F) Cache (8Kbytes sets, 4 byte blocks, direct mapped)

**Figure 9.20** TLB, page table, and cache for small memory system. All values are in hexadecimal notation.