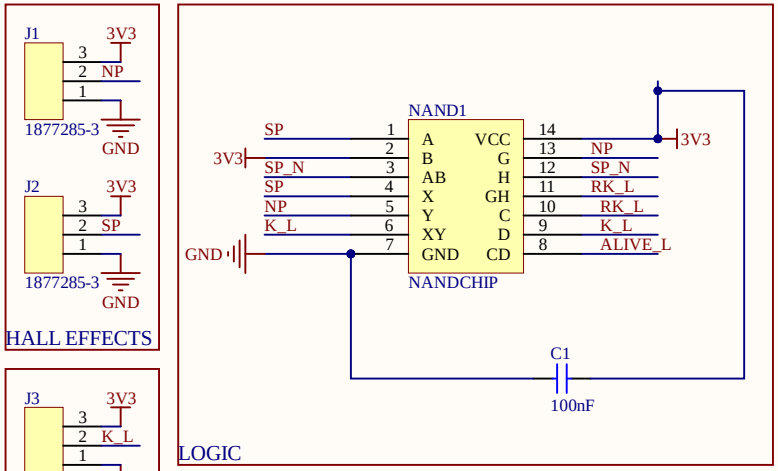
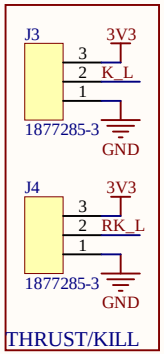
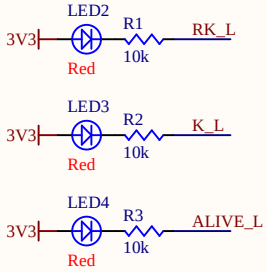
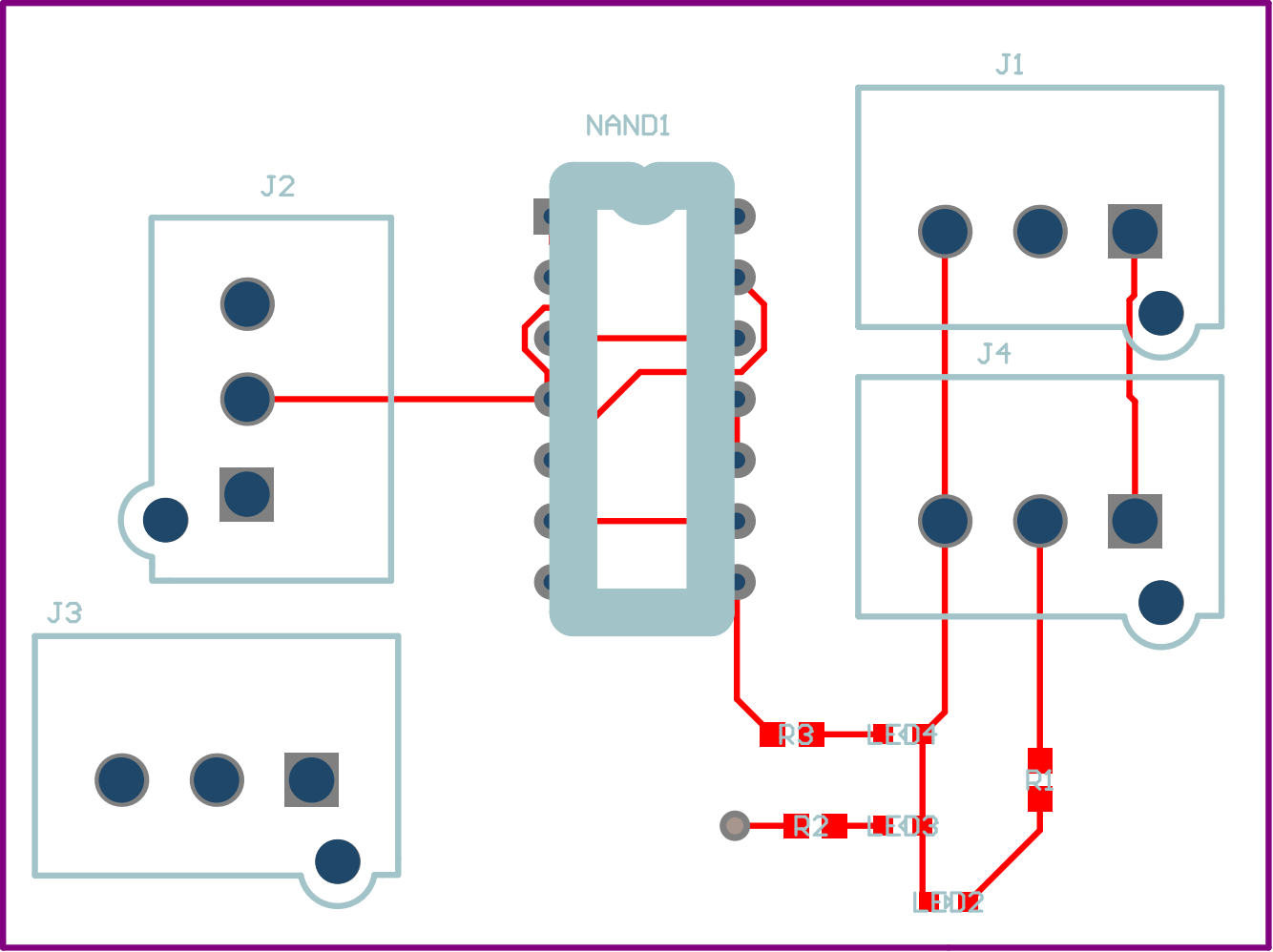


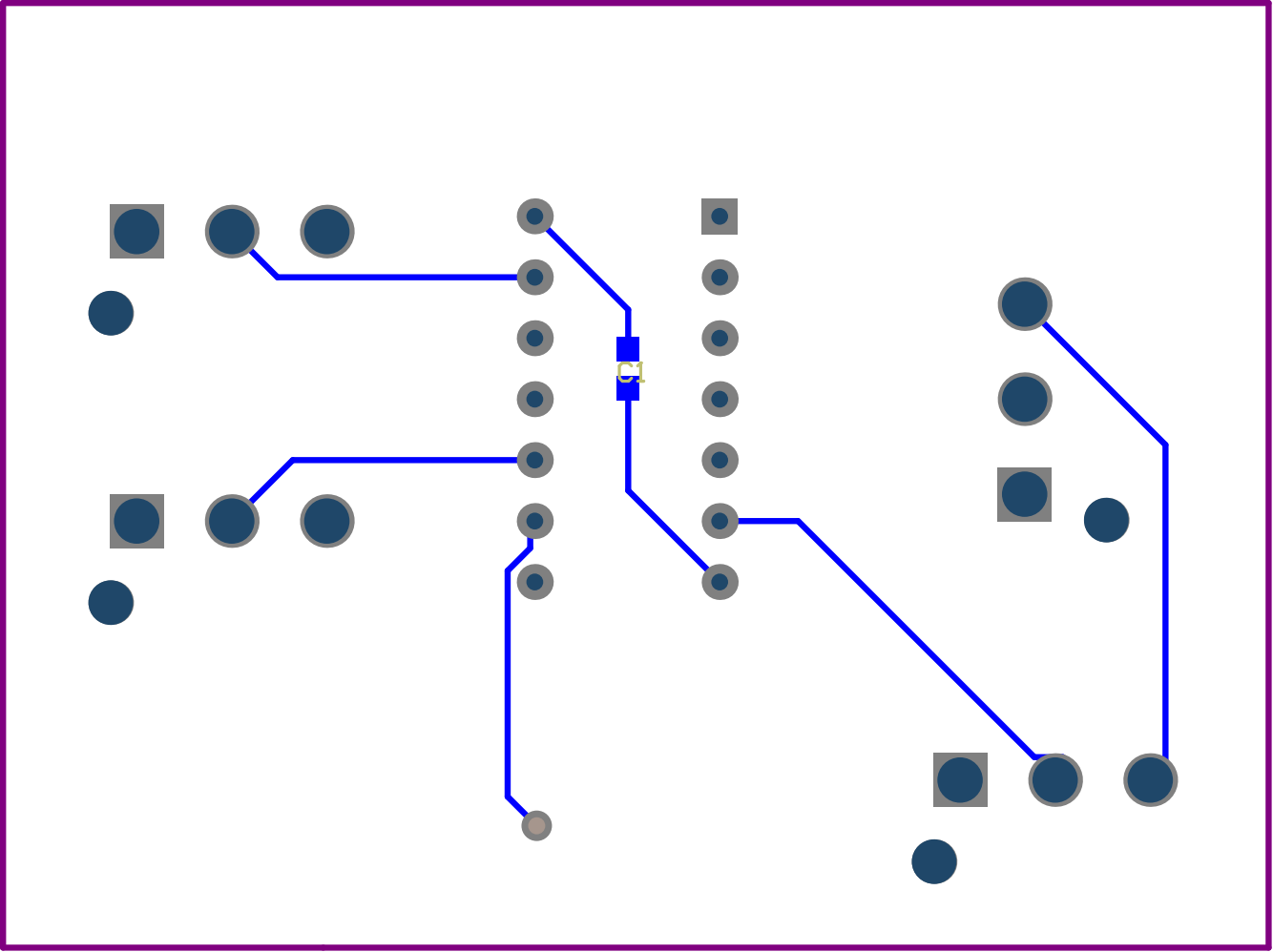




NOTES

Project/Vehicle: SubjuGator 8			Machine Intelligence Laboratory 1889 Museum Rd Room 3001 Gainesville, FL, 32611	
Author(s): -YOUR NAME :) -* -* -*	Revisor(s): -* -* -*		Git Repo: * Git Hash: Not in version control	
Date: 9/13/2024	Revision: A	Size: A	File: Main.SchDoc	Sheet 1 of 1


J1
NAND1
J2
J4
J3
R3
LED4
R1
R2
LED3
LED2


C1

Comment	Description	Designator	Footprint	LibRef	Quantity
Cap		C1	CAPC0603	Cap	1
1877285-3		J1, J2, J3, J4	1877285-3	1877285-3	4
LED		LED2, LED3, LED4	LED0603	LED	3
NANDCHIP	IC GATE NAND 4CH 2-INP 14DIP	NAND1	NAND2	TC74AC00P(F)	1
Res		R1, R2, R3	RES0603	Res	3

Design Rules Verification Report

Filename : C:\Users\jgood\Documents\ALTIUM_THINGS\assignment\AltiumAssignment\Altiu

Warnings 0
Rule Violations 56

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=10mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	47
Silk to Silk (Clearance=10mil) (All),(All)	9
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	56

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C1-1(6825mil,2293.504mil) on Bottom Layer And Text "C1'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C1-2(6825mil,2356.496mil) on Bottom Layer And Text "C1'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad LED2-A(7292.52mil,1450mil) on Top Layer And Text "LED2'
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED2-A(7292.52mil,1450mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED2-A(7292.52mil,1450mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED2-A(7292.52mil,1450mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad LED2-C(7357.48mil,1450mil) on Top Layer And Text "LED2'
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED2-C(7357.48mil,1450mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED2-C(7357.48mil,1450mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad LED3-A(7282.48mil,1575mil) on Top Layer And Text "LED3'
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED3-A(7282.48mil,1575mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED3-A(7282.48mil,1575mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED3-A(7282.48mil,1575mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad LED3-C(7217.52mil,1575mil) on Top Layer And Text "LED3'
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED3-C(7217.52mil,1575mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED3-C(7217.52mil,1575mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad LED4-A(7282.48mil,1725mil) on Top Layer And Text "LED4'
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED4-A(7282.48mil,1725mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED4-A(7282.48mil,1725mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED4-A(7282.48mil,1725mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad LED4-C(7217.52mil,1725mil) on Top Layer And Text "LED4'
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED4-C(7217.52mil,1725mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.311mil < 10mil) Between Pad LED4-C(7217.52mil,1725mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-1(6675mil,2575mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-1(6675mil,2575mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-10(6978.15mil,2175mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-11(6978.15mil,2275mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-12(6978.15mil,2375mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-13(6978.15mil,2475mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-14(6978.15mil,2575mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-14(6978.15mil,2575mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-2(6675mil,2475mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-3(6675mil,2375mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-4(6675mil,2275mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-5(6675mil,2175mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-6(6675mil,2075mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-7(6675mil,1975mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-7(6675mil,1975mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-8(6978.15mil,1975mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-8(6978.15mil,1975mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad NAND1-9(6978.15mil,2075mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R1-1(7475mil,1618.504mil) on Top Layer And Text "R1'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R1-2(7475mil,1681.496mil) on Top Layer And Text "R1'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R2-1(7137.992mil,1575mil) on Top Layer And Text "R2'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R2-2(7075mil,1575mil) on Top Layer And Text "R2"
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R3-1(7100mil,1725mil) on Top Layer And Text "R3" (7075.098mil,1660.005mil)
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R3-2(7037.008mil,1725mil) on Top Layer And Text "R3' (7050.098mil,1710.005mil)

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (0.153mil < 10mil) Between Text "LED2" (7270.018mil,1435.005mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text "LED2" (7270.018mil,1435.005mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text "LED2" (7270.018mil,1435.005mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text "LED3" (7195.018mil,1560.005mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text "LED3" (7195.018mil,1560.005mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text "LED3" (7195.018mil,1560.005mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text "LED4" (7195.018mil,1710.005mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text "LED4" (7195.018mil,1710.005mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text "LED4" (7195.018mil,1710.005mil) on Top Overlay And Track

Electrical Rules Check Report

Class	Document	Message
Warning	Main.SchDoc	Off sheet J1 at -200mil,6600mil
Warning	Main.SchDoc	Off sheet J2 at -200mil,5800mil
Warning	Main.SchDoc	Off sheet J3 at -200mil,4700mil
Warning	Main.SchDoc	Off sheet J4 at -200mil,3900mil