Vocabulary terms:

glue logic- logic devices required to connect multiple chips together
opto-isolator- IC used to isolate a low-V microprocessor circuit from a high-V motor circuit
low/high active- a device that is active, or on, with a 0 or 1 respectively
LSTRB- pulse signal used in conjunction with R/W# to determine if a chip is reading/writing
cross-compiler- takes code in one language and produces instructions in another language
debugger- can start/stop executions and allow for examination of the processor state
volatile memory- memory that resets when power is lost; all RAM except NVRAM is volatile
nonvolatile memory- memory that can store values without power; PROMs, ROM, hard disk, flash, NVRAM
flash- nonvolatile memory where instructions are stored on the microprocessor
ROM- nonvolatile memory used to store tables, instructions, settings, etc
RAM- volatile memory used to store variables, stack, and cache
NVRAM- nonvolatile ram, battery powered to remove volatility
pull down/up resistor- resistors to set the natural value of a pin to 0/1 respectively (typical 4.7-10kOhm)
LC74374- latch clip used to write to I/O
LC74373- latch clip used to read to I/O
DDRn- Data Direction Register Port n, 1: output, 0: input
PTn- the I/O register
PERn- Pull Up Enable, 1: enable if input, 0: disable if input
PIEn- Interrupt Enable, 1: enable/unmask, 0: disable/mask
PPSn- Polarity Select, 1: Enable Pull Down+rising edge,0: Enable Pull Up+rising edge
RDRn- Reduced Drive Register, 1: bits given, 0: elsewhere
WOMn- wired or mode register

Chip Addressing:

1) list starting addresses
2) mark critical address lines
   - all 1's critical
   - if 0 differentiates from an other line, critical

***for gapless:** if 0 critical, all 0's to right are critical; if 0 non-critical, all 0's below it non-critical

Notes:
20 total address lines
A13-A19 varies 8k-512k
Chip 0 always starts at 0kB
Starting address for chip must be multiple of chip size

EPROM Programming:

10 attempts to program before it quits trying
tDV: wait time to ensure data is valid
tDS: wait time to ensure data is stable before latch
tAS: wait time to ensure address is stable before latch

Development Tools:

S-Record:

S	start code
1	record type
11	byte count
0038	address
DATA BITS	data contained
42	checksum

Other development tools:
Reset Switch, Com Ports, LCD Display, 7Segment, Display, LEDs, Keypad/Switches, Amplifiers/Op Amps, OptoIsolators, Relays, SCRs/Triacs, Buzzers, Potentiometers, DACs, DIP Switches, Thermometer, Breadboard, Expansion Slots/Ports/Connectors

PAL Decoding:

1) find first differing bit in start/end addresses
2) all values to the right of that are made X
3) Highest D is connected to highest A
   - i.e. if there is D0-D9, D9 is tied to A19

I/O Type	Pro	Con
Isolated	Simultaneous use of I/O	More Pins/Instructions
Memory Mapped	Many operations available	hard to detect errors
Linear Selection	Simple selection algorithms	wasteful addressing

Memory Interfacing:

20 bit addresses
starting address:
   all bits before size 0 except for A and B, which are 1
   all bits at size or after are 'X'
ending address:
   change all 'X' to 1
if LSTRB goes in the low-order chip, the system is big endian
chip size = [2^(D-C)]/1024 kB

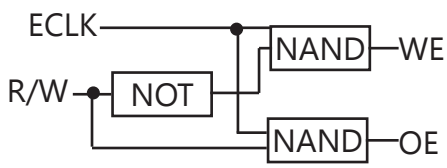
Energy Calculations:

Use dimensional analysis CAREFLULY. Pay close attention to unit cancellation.

Addressing:

ECLK = 0: Preparing / 1: Acting
table given will tell bus size

Glue Logic Diagram:



Reset Modes:

expanded wide mode:
   most significant bit: Port A
   least significant bit: Port B
ROMON = 1 » flash usable
ROMCTL = 1 » allows ROMON to be set
wide » 16-bit
narrow »8-bit

Bitmasking:

OR (set): |
   Final value will be 1
   PTH | 1
And (clear): &
   Final value will be 0
   PTH & 0
XOR (exactly one 1 sets): ^
   PTH ^ (1 or 0)

Chip Information:

MC9S12DP256B by Freescale/Motorola

Basic Information:
256 in name refers to memory (in kB)
not found on chip: electric buzzer, digital-to-analog converter, temperature sensor
interrupt vector table stored in high-order memory
registers located at low-order memory
ECLK at top of timing diagram
RW(R/W) determines read/write state

Pinout:
Pn0 is bit 0 of port n (replace n with an actual port)
Port J has only 4 bits
Enhanced capture times available on Port T
SCI channels tied to Port S
CAN ports tied to Port J and Port M
Addresses have 64kB external RAM without expanding Port K

Pinout Abbreviations:
A to D » PAD
Background debugger » BKGD
Data bus line 1 » DATA 1
expanded addresses » XADDR

HC12	HC9S12
2 8-bit accumulators	
128 kB flash max	512 kB flash max
16-bit program counter	
16-bit register	2-piece 16 bit registers
16-bit stack pointer	
8 MHz bus clock	25 MHz bus clock
	3 SPI ports

Decoder:

X chip select bits for 2^X outputs

NAND: all inputs must be 1
OR: all inputs must be 0
} for low-active select

Remember:

Gate	At least 1 X input	Output
NAND	0	1
OR	1	1
AND	0	0
NOR	1	0

DRAM	SRAM
low power at use	low power at rest
high density	simple
cheap	fast
cell construction	transistor construction
	same die as processor

Keypad:

If a for loop containing key and I, the first valid keycode pressed will be the first inputted and outputted value. If two keys (and only two keys) are pressed on the same row, their hex value won't match any value and the output will be 0 (NOT '0').
Ex if 5,9,c and F are pressed, then 5 will be the output.
If c and f are pressed, then the output will be 0,(not '0').
If the for loop contains row, then the answer for the output of this code will be in a 4 digit hex form. Take each row as a 4 digit binary code and align them like so: row 3|row 2|row 1|row 0|. Each key that is pressed on each row is denoted as a 1 in binary. Multiple keys can be pressed so multiple ones can appear in a row. Convert the 16 digit long binary number into hex. That's your answer.
Example: if 1,4,6,9 and D are pressed, the out put will be