ECE 311
LABORATORY MANUAL
VER 1.5

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Clemson University
Clemson, SC, 29634
May 1999

Version 1.5, July 2011 – J E Harriss

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Notes about the Course

Electronics I consists of a theoretical module ECE 320 and a practical module ECE 311. These courses run concurrently and the aim of the manual is to introduce students to laboratory procedure including data recording and report writing. The experiments were developed to expand on the material covered in lectures and to experimentally demonstrate the validity of principles presented in ECE 320 classes. The manual outlines 12 experiments and instructors will select the most important topics for experimental confirmation.

NOTE: Learning occurs differently for different students and no one approach is 100% effective. **Laboratory work is an effective teaching tool and it is important to realize that it stands alone. There is no plan or need to have a lecture on a subject prior to a lab.** A lab experience and a lecture should reinforce learning, but the order in which the learning takes place should not significantly affect the process.

It is this instructor's opinion that the students would better understand the fundamentals of electronics and the use of active devices in electronic circuits if the students were able to build circuits and see for themselves that the principles presented in the text are real, or pretty close to reality. It was also felt that the students would become aware of the limitations of the analytical approach to active circuit analysis by testing circuits and comparing their results with analytical solutions and circuit simulations. Most analytical approaches to circuit analysis use linear analysis techniques and these techniques are not always valid for non-linear electronics devices, or are valid only over a limited range of currents and voltages.

The component parameters presented in text books are usually nominal values, valid for most circuits. By measuring actual device parameters and comparing these values with values in the text, the students should be able to obtain a feel for the magnitudes of the device parameters used in the circuits. Experiments in the ECE 311 labs use discrete devices and some parameters (for example, diode forward current) are often much larger than the values you would measure for similar devices on an integrated circuit. The reason is that integrated circuits contain devices which are physically much smaller and hence they are unable to handle as much power as the larger discrete components.

Most of the experiments require simulation of the circuits. The simulations discussed in the experiments assume the students are familiar with B2 Spice (Beige Bag simulation program with integrated circuit emphasis). **It is important that students simulate their circuits before coming to the lab.** These simulations will be extremely important in the design of experiments: it will be impossible to complete the lab without having done the simulations and calculations based on these simulations before the lab. Most of the experiments ask that you compare the results of the simulations and the results of the analytical analysis with the measured results, to see how the three techniques compare. It is important to gain an understanding of the strengths and limitations of linear circuit analysis techniques taught in class.

It is extremely important for students to read the labs prior to coming to the laboratory. In many cases you will be asked to bring calculated component values and/or simulation results prior to starting the lab in order to guide you in selecting component values for your practical circuit. You will need this information in order to perform and complete the labs. You should also try to become familiar with standard component values, since your calculations will often

call for resistor or capacitor values which are non-standard and you will have to choose from standard components to build your circuits.

The experiments listed in the contents may not be assigned in the order presented. In particular the design experiments may be presented later in the course to let classes get ahead of the labs. The use of these labs later in the course will allow students to become more familiar with electronic circuits and devices before attempting circuit design. The design experiments are also designed as single-student exercises, to test students' individual laboratory skill development. The design experiments should be assigned as one-hour lab sessions and may be used in place of a final exam for this lab.

During the first year of introduction of this lab, the students were asked to complete an experimental evaluation sheet following each experiment. The students were invited to comment on ways to improve the experiment just completed. Students were also encouraged to propose topics they felt would benefit through experimental confirmation of principles discussed in class. Many of these ideas have been incorporated in the manual. Any suggestions from current students for ways to improve the lab learning experience are always greatly appreciated.

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In anticipation that the textbook for ECE320 may change from time to time, the lab manual attempts to remain independent of a specific textbook. Thus in many places short descriptions of principles involved are included and an attempt has been made to define the symbols used in this text. Unfortunately, nomenclature and symbols are not always standard in printed texts on electronic circuits. At the end of each experiment is a 1-page check list. The check list should be used by students to ensure they have covered the most important parts of the experiment.

Examples of lab reports and pre-lab reports have been inserted before the first experiment. These examples are provided to help students learn some of the techniques used for effective technical communication.

The author would like to thank Sally Surver for assistance in typing some of the original copies of experiments found in this lab manual. John Adjaye's help in designing, writing, and performing the experiments was invaluable. The author would also like to thank Robert Palazzo, who wrote the check lists and helped with revisions during the first year. Omer Oralkan helped with writing a lab report example. The author also acknowledges all lab instructors and undergraduates who have contributed to revisions of the manual.

D J Dumin
May 1999

Version 1.1

With the introduction of a complete set of new equipment for the lab, updating experiments and software changes, the lab manual has undergone a major revision. Whilst the general wording and theme is the same, the present author took the liberty of editing many sections and paragraphs. In the interests of keeping the volume to a minimum I have made editorial changes throughout, some paragraphs are verbatim from the first manual whilst others reflect style and

emphasis differences. It is hoped that this new version will build on the excellent foundation provided by Dr Dumin and his students. My apologies if my edits have misconstrued any ideas or concepts attributed to the original "author". As a work in progress, I expect the manual will undergo periodic revisions to keep it up to date.

My thanks to Daniel Damjanovic for suggestions and editing the original manual and to Trish Nigro who retyped the complete revised manual.

K F Poole
Jan 2004

Version 1.2

The manual has undergone a comprehensive review over the past year. Thanks to David Epting who has tracked and corrected the errors in version 1.1 and suggested many improvements throughout the manual.

Thanks to Janet Bean for preparing the 2005 version 1.2 laboratory manual.

K. F. Poole
Jan 2005

Version 1.3

The manual has been modified to accommodate new equipment – NI-ELVIS workstation and the Tektronix Type 576 Curve Tracer. Additional reformatting and corrections by Dr J. E Harriss.

E. Iyasere
May 2010

Version 1.4

The manual has undergone an extensive review and many revisions have been made to clarify and correct the lessons throughout the experiments. The manual still favors the Hameg curve tracer; a clear and balanced treatment using the Tektronix curve tracer needs to follow.

Nishant Gupta
J. E. Harriss
January 2011

Version 1.5

Correct newly identified errors. Clarify sections that students identified as troublesome. Eliminate confusing R_B references in Experiments 6 through 9.

Nishant Gupta
J. E. Harriss
July 2011

Syllabus Example

ECE 311
Electrical Engineering Lab
Syllabus

Instructor Information:
Name :
Email :
Phone :
Office :
Office Hours :

Course Coordinator:
Name : Dr. xxxxx xxxxx
Email : xxxxx@clemson.edu
Office : xxx Riggs Hall
Phone : 656-xxxx

Course Section Information:
Semester : Fall 2010
Section : 004
Time : 2:00 – 4:00 TH
Room : Riggs Hall 200C

Materials Required:
ECE 320 Text
ECE 311 Lab Manual
(download from http://www.clemson.edu/ces/departments/ece/resources/lab_manuals.html)
IEEE Lab Kit
Scientific Calculator
PC with B2 Spice circuit simulation software (B2SPICE V 5.0)
(download from http://www.beigebag.com/demos.htm#v5)
Lab Notebook

Attendance Policy:
Students are required to attend all lab sessions. A student who misses a lab will receive a grade of zero for the lab and any associated reports. No make up labs will be given. The lowest pre-lab report score and post-lab report score will be dropped in computing final averages.

Goals and Objectives:
The goal of this laboratory is to study electronics through experimentation. Upon completion of this course, students should be able to use standard laboratory equipment to analyze the behavior of basic electronic devices and to design and construct simple circuits containing these devices.

Lab Teams:
Most of the labs will consume the full two-hour lab period and will be performed by two-person lab teams. Some labs will require only one hour and will be performed by each team member sequentially and independently during half of the corresponding lab period.

Homework Policy:
Every lab requires preparation prior to performing the experiments. Most of the labs require SPICE simulations, and some of the labs require calculations of design parameters before

beginning the experiments. Students are required to perform this preparatory work prior to coming to the lab. In order to fulfill the written communication component of the course, students are required to turn in pre-lab reports written in a proposal format prior to performing the laboratory work.

Grading:
Final grades will be calculated according to the following weights:

PRE-LAB REPORT ..... 20 %
POST-LAB GRADE ..... 30 %
LAB REPORTS ..... 50 %

Pre-lab reports:
Each pre-lab report is due at the beginning of the lab period. The required report format is found in the lab manual. Each student is required to keep a copy of all pre-labs submitted. The pre-lab report should be used as the basis of the lab report, which will be written sometime after completion of the lab. In certain cases, an instructor may require the student to make corrections to simulations in the pre-lab reports, which will be due the following lab meeting. A 10-point deduction will be taken on every resubmission. Note: If you have not done your pre-lab when due, a grade of 50% will be assigned for the post lab grade as well!!!

Post-lab grades:
Upon completion of each laboratory, the instructor will verify each student's lab notebook for correctness and experimental completion. Also, an individual oral question or a short quiz will be given and a grade will be assigned.

Lab reports:
Students are required to turn in two lab reports for the semester. An opportunity to turn in a rough draft will be given with no grade assignment. An electronic copy is required for final submissions of all lab reports. Lab reports will be assigned randomly to each student. The first report will be assigned upon completion of Lab 3 and the second report will be assigned upon completion of Lab 7. The lab reports are due at the beginning of the lab period on a date determined by the instructor. The required report format is found in the manual.

Changes to the lab syllabus:
The instructor reserves the right to make changes to this syllabus during the semester. Students will be given adequate notice in the lab of any changes.

Academic Honesty: "As members of the Clemson community, we have inherited Thomas Green Clemson's vision of this institution as a 'high seminary of learning.' Fundamental to this vision is a mutual commitment to truthfulness, honor, and responsibility, without which we cannot earn the trust and respect of others. Furthermore, we recognize that academic dishonesty detracts from the value of a Clemson degree. Therefore, we shall not tolerate lying, cheating, or stealing in any form."

Lab Schedule Example

Lab Schedule (dates will be announced in each section)

Lab 0: Laboratory Introduction (Attendance mandatory);

Lab 1: Exp #1 - Semiconductor Diode Characteristics (2-person lab);

Lab 2: Exp #2 - Power Supply Operation (2-person lab);

Lab 3: Exp #4 - Diode Clippers and Clampers (2-person lab);

Lab 4: Exp #3 - Power Supply Design (one hour; 1-person lab);

Lab 5: Exp #5 - Bipolar Junction Transistor Characteristics (2-person lab);

Lab 6: Exp #6 - BJT Common Emitter Circuit Bias (2-person lab);

Lab 7: Exp #7 - BJT Common Emitter Circuit Voltage Gain (2-person lab);

Lab 8: Exp #8 - BJT Common Emitter Amplifier Design I (2-person lab);

Lab 9: Exp #9 - BJT Common Emitter Amplifier Design II (one hour; 1-person Lab)

Lab 10: Exp #11 - Field Effect Transistors (2-person lab);

Lab 11: Exp #12 – Basic Logic circuits (2-person lab);

ELECTRONICS 1
ECE 311

SAFETY

Safety is always an important topic whenever laboratory work is being considered, and it is certainly true in the case of ECE 311 labs. Safety is important.

The experiments in the laboratory use low voltages and low currents. However, the lab equipment is powered by the 110V, 60Hz, line voltage. Be careful with the line voltages. Do not touch exposed prongs on the equipment plugs when connecting the equipment to the lines.

Take care when using power supplies, which may be low voltage but can supply currents in the ampere range. Shorting such a supply can lead to a serious burn as high currents arc and can ignite flammable material. This is precisely why a car battery needs to be treated with respect. The hundreds of amps a battery can supply are sufficient to cause serious burns.

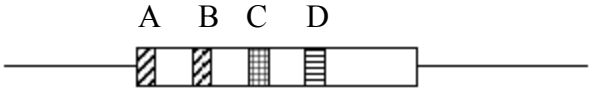
The equipment is heavy enough to be generally stable on the bench. Be sure to keep the equipment away from the edges of the benches to avoid having a piece of equipment fall off the bench. Besides endangering people who might be struck, falling equipment endangers everyone in vicinity by stressing the power cords, possibly causing a line short or live fault on the equipment, not to mention damage to the expensive lab equipment. In general electronic equipment does not survive harsh treatment.

The capacitors furnished in your lab kits are electrolytic capacitors with positive and negative terminals. Be sure to always connect the positively marked terminal to the most positive terminal in your circuit. An excess negative voltage applied to these capacitors can cause the device to overheat and explode.

The curve tracers can apply voltages as high as 200 V to a device. There is an interlock forcing the user to cover the device when applying these voltages. Do not attempt to override this safety feature when using the curve tracer.

Standard Component Values

In many of the experiments you will be asked to use standard resistor or capacitor values which are closest to those you calculated. The values were chosen to fit the tolerance and eliminate overlap. Most resistors are color coded. Figure SC-1 provides the color codes for standard resistor values to help you quickly select the values you need in your experiments. Since the capacitors used in the ECE 311 experiments are for coupling or bypass purposes, values are not as critical and hence the color coding is not included.



A = first significant figure
B = second significant figure
C = decimal multiplier
D = tolerance

Black	= 0	decimal multiplier = 10^0 = 1	
Brown	= 1	decimal multiplier = 10^1 = 10	
Red	= 2	decimal multiplier = 10^2 = 100	
Orange	= 3	decimal multiplier = 10^3 = 1000	
Yellow	= 4	decimal multiplier = 10^4 = 10000	
Green	= 5	decimal multiplier = 10^5 = 100000	
Blue	= 6	decimal multiplier = 10^6 = 1000000	
Violet	= 7	decimal multiplier = 10^7 = 10000000	
Gray	= 8	decimal multiplier = 10^8 = 100000000	
White	= 9	*	
Gold	= *	decimal multiplier = 10^{-1} = 0.1	tolerance = ±5%
Silver	= *	decimal multiplier = 10^{-2} = 0.01	tolerance = ±10%
No color	= *	decimal multiplier = *	tolerance = ±20%

Figure SC-1: Resistor color coding

The values of carbon resistors are guaranteed by the manufacturer to be within a certain tolerance, usually 5%, 10%, or 20% of the standard value. Perhaps most common is ±10%. Table SC-1 shows the standard values for the ±10% tolerance.

Standard value	Band 1	Band 2	Band 3	Band 4
10	Brown	Black	Decade multiplier	Silver
12	Brown	Red	Decade multiplier	Silver
15	Brown	Green	Decade multiplier	Silver
18	Brown	Gray	Decade multiplier	Silver
22	Red	Red	Decade multiplier	Silver
27	Red	Violet	Decade multiplier	Silver
33	Orange	Orange	Decade multiplier	Silver
39	Orange	White	Decade multiplier	Silver
47	Yellow	Violet	Decade multiplier	Silver
56	Green	Blue	Decade multiplier	Silver
68	Blue	Gray	Decade multiplier	Silver
82	Gray	Red	Decade multiplier	Silver

Table SC-1: Standard values for carbon resistors with ±10% tolerance

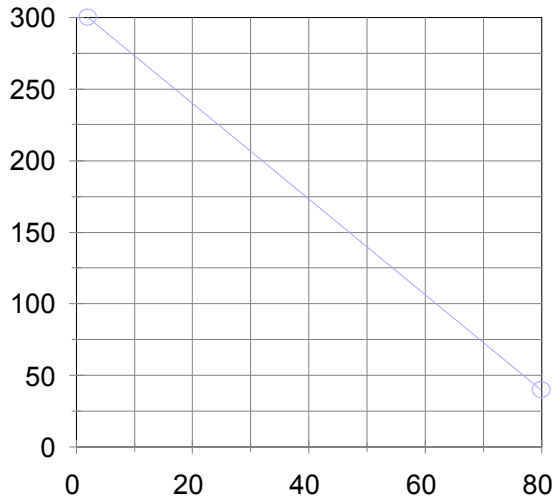
As an example of how to use this information, a 680Ω resistor with ± 10% tolerance is guaranteed to have a value between 612Ω and 748Ω. The color code is

Band 1	Band 2	Band 3	Band 4	Resistor Value	Tolerance
Blue (6)	Gray (8)	Brown ($x10^1$)	Silver (10%)	$= 68x10^1 = 680$	±68

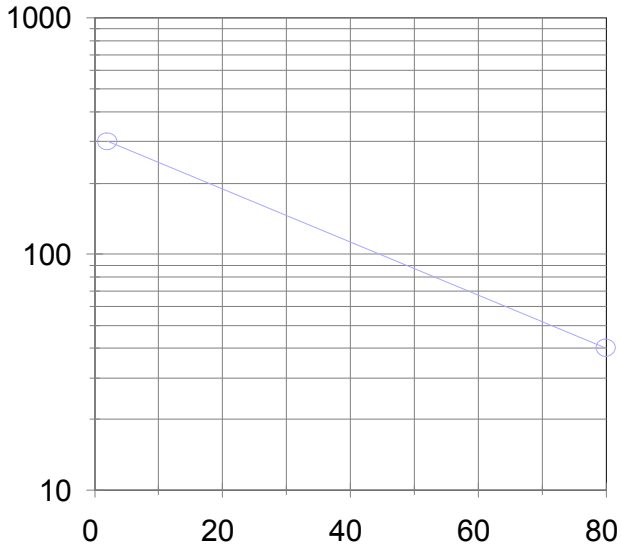
Graph Paper

Graphs of data may take many forms, whether plotted on traditional graph paper or using computer software. Three fundamental graph types to show the relationships between a dependent and an independent variable are *linear, semi-log,* and *log-log* plots.

Linear graph paper has uniform spacing along the horizontal ("X") axis and uniform spacing along the vertical ("Y") axis, although the scales along the two axes do not need to be the same.

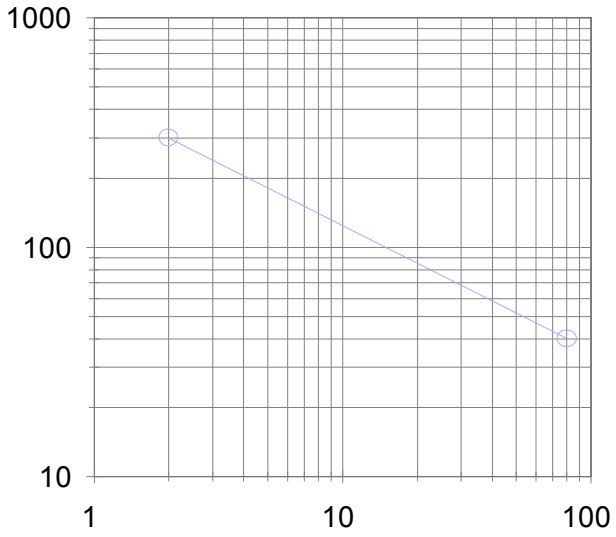


Semi-log graph paper is linear on one axis and logarithmic on the other axis:



semi-log graph paper (2-cycle)

Log-log graph paper has a logarithmic scale along both axes:



log-log graph (2-cycle by 2-cycle)

Choose the style that best reveals the relationships between the variables.

Note:

- A straight line on linear paper has the relationship y=mx+b.
  $m = (y_1-y_2) / (x_1-x_2)$
  b = y when x=0
- A straight line on semi-log paper (if x-axis is linear) has the relationship log(y)=mx+b
  $m = (\log(y_1)-\log(y_2)) / (x_1-x_2)$
  b = log(y) when x=0
- A straight line on log-log paper has the relationship $\log(y)=m\cdot\log(x)+b$
  $m = (\log(y_1)-\log(y_2)) / (\log(x_1)-\log(x_2))$
  b = log(y) when log(x)=0

LABORATORY REPORTS

Engineers are most effective if they can clearly communicate their ideas and developments to others, both other engineers and their managers. For this reason, writing and documenting are essential aspects of an engineer's job. Engineers spend over 60 percent of their time documenting their work and communicating the results to others. Many engineering students do not realize the importance of this documentation and communication process and have difficulties in their first job documenting their work. Engineers in the workplace are evaluated on their communication skills, which include both the quality and sometimes the quantity of their publications and technical reports.

In this class you are required to prepare pre-lab reports and to submit two formal lab reports for the semester. Pre-lab reports assist you in preparing for the labs by forcing you to organize your thoughts and understand the task ahead. The formal lab reports communicate the results of your work.

The lab report is as important as the work done in the lab, because unless you can communicate the results of your work, the work has little usefulness. Furthermore, the lab report reinforces the material that was learned in the lab and helps you develop effective technical communication skills. Development of both oral and written technical communication skills is one of the most important things you can learn as an undergraduate student.

Pre-Lab Reports

Almost all of the labs that are performed in ECE 311 require a pre-lab report. The pre-lab report is an important part of the lab. The pre-lab report helps you get ready for the lab and gives you some experience in writing proposals. It assures that you have, at least, given some consideration to the type of experiment that you will be performing. The pre-lab report is in the form of a proposal, a statement you would give to your supervisor, outlining what you want to do, why you want to do it, and some estimates of what results you expect to obtain.

These pre-lab reports are to be short proposals of what you intend to do in the lab. They should be limited to two typewritten pages of text and two pages of supporting documentation, usually SPICE simulations of your anticipated results. A sample pre-lab report is shown below. Feel free to modify this format if you think you could communicate more information using a different format or if you think a different format would help you prepare for the lab.

General Report Guidelines:

- No more than 2 pages of written text.
- No more than 2 pages of supporting documentation, schematics, tables, or results of SPICE simulations.

Title: The title will often be the same as the title given in the lab manual. The title is centered on the top half of the page and is written in bold type, all capitals, followed by your name, lab section, and date.

EXAMPLE:

DIODE CIRCUITS

John 0. Student, ECE 311(4), January 32, 1997

Proposal: This part should be a short and to-the-point proposal of what you expect to do and what you expect to accomplish during the lab. You can get a lot of this information from the introduction part of the experiment in your lab manual. You generally don't need to spend too much space defining all of the terms you use in the pre-lab report, since you will be referring to your lab manual.

EXAMPLE:

Proposal: It is proposed that the current-voltage (I-V) characteristics of an electronic widget be measured and compared with the theoretically predicted I-V characteristics. Both the input and output characteristics will be measured. The input characteristic is expected to have an I-V characteristic of the form

$$I_{in} = V_{in} (R_1 + R_2)^2$$

The output characteristic is expected to be of the form

$$I_{out} = K\ I_{in}$$

where K is a constant proportional to the emitter capacitance. All of the above terms are defined in the Lab Manual under Lab #4, Diode Circuits. The input and output characteristics will be measured using values of 100 $\Omega \leq R_1 \leq 200\ \Omega$, 1 $\Omega \leq R_2 \leq 1$ MΩ, and 10 pF $\leq C_E \leq$ 100 μF. SPICE simulations will be performed on the widget covering the ranges of resistance and capacitance described above and the measured characteristics will be compared with the SPICE simulations.

Experimental: This part of the pre-lab should describe how you expect to make your measurements, including what equipment will be needed. As in the proposal part, you should be able to get most of this information from your lab manual.

EXAMPLE:

Experimental: The widget input and output characteristics will be measured using a curve tracer. In this experiment, R_1 will be initially set at 100 Ω and R_2 and C_E will be independently varied in decade steps. R_1 will then be incremented in 10 Ω steps to 200 Ω, while R_2 and C_E are kept at their optimum values.

Anticipated Results: This part of the pre-lab report will contain any anticipated results, including any results of SPICE simulations.

EXAMPLE:

Anticipated Results: The input current will be plotted as a function of input voltage on log-log paper. The slope of the I-V characteristic should be a straight line with slope = 2, for all values of R_1 and R_2. The constant K will be determined from the output characteristics. The anticipated value of K is 0.01 C_E.

On the next two pages the SPICE simulations of the widget characteristics are shown. Provide SPICE output, circuit diagram, and netlist.

Formal Lab Reports

The lab report is as important as work done in the lab. The lab report reinforces the material that was learned in the lab and helps you develop effective technical communication skills. Development of both oral and written technical communication skills is one of the most important things you can learn as an undergraduate student.

Engineers are most effective if they can clearly communicate their ideas and developments to others, both other engineers and their managers. For this reason, writing and documenting are essential aspects of an engineer's job. Engineers spend over 60 percent of their time documenting their work and communicating the results to others. Many engineering students do not realize the importance of this documentation and communication process and have difficulties in their first job documenting their work. Engineers in the workplace are evaluated on their communication skills, which include both the quality and sometimes the quantity of their publications and technical reports.

The lab reports you submit in ECE 311 should conform to the guidelines given below. Each report should be a self-contained document and should be no longer than necessary to present the required information. Each report is to be typed using a word processor. Proper spelling and grammar are to be used throughout. Figures, drawings, charts, and tables should be added where they are needed and should contain understandable labels, including units for the axes. When plotting B vs. A, B is the dependent variable and is plotted on the y-axis; A is the independent variable and is plotted on the x-axis. The figure should appear in the text as soon after mention of the figure as possible, but not in the middle of a paragraph. The figure should refer to the main text and should not stand alone. Except for raw data, all figures should be computer-drawn using either a plotting program such as Cricket Graph or a spreadsheet program such as Excel. A stand-alone figure may be more confusing than no figure at all. All pages should be consecutively numbered. Sign your report on the cover page. This signature shows that you take responsibility for what is contained in the report. Reports are due at the start of the class after the lab has been performed. The details of the report are given below.

General Report Guidelines:

A technical report is expected to contain the following items or subsections:

- Title page,
- Table of contents,
- Abstract,
- Introduction,
- Theoretical discussion or background,
- Experimental procedure and methodology and experimental results,
- Discussion of results,
- Conclusion or summary,
- Acknowledgements,
- Appendices,
- References.

You may find some reports have one or more of these sections removed.

Title page: This page is the first page of the report and should act as the cover page. The title will often be the same as the title given in the lab manual. The title is centered on the top half of the page and is written in bold type, all capitals. Centered on the bottom half of the page is your name, the name of your lab partner(s), the course name, the course title, the instructor or the name of the institution for whom the report is being prepared.

EXAMPLE: The typing for this page should be larger than shown below.

DIODE CIRCUITS

John Q. Student
Lab Partner, A. Wiley Pardner
January 32, 1997
ECE 311
Electrical Engineering Laboratory III
Prepared for: Any-Old Grad. Student

Abstract: An abstract is a short and to-the-point statement of what was done, how it was done, the results, and the conclusions. The abstract gives the reader enough information to determine if the reader wants to read the full report.

EXAMPLE:

ABSTRACT

The current-voltage characteristics of an electronic widget were measured. The widget characteristics were compared with theoretical predictions. It was found that the internal resistance increased from 1 ohm to 10,000 ohm when the voltage was raised from 1 V to 1.1 V. The external resistance dropped from 1 ohm to 0.1 ohm over the same voltage range. The control factor, m, for the widget varied between 1.1 and 1.3 over the full input voltage range. The device tested in the lab was well characterized by the ideal widget equation using a form factor of 2.2.

Introduction: The introduction should explain the background of the work. It should put the experimental work into perspective and should lead the reader into the subject matter. It should have at least one sentence explaining why the work was undertaken. It should end with one or two sentences describing the general experimental approach and results.

EXAMPLE:

INTRODUCTION

A fidget can be combined with resistors and capacitors to change the wave shape of an ac signal. The position of the fidget in the circuit, with respect to the resistors and capacitors, causes the output wave shape to change. The resistor and capacitor act as a smoothing filter. Four basic fidget/resistor/capacitor circuits were studied. The resistor and capacitor values were changed over two orders of magnitude to make the RC time constant much smaller and much larger than the period of the input signal. The output wave shapes were studied as a function of resistor and capacitor values. It was found that the piecewise linear model of the fidget could adequately explain the output wave shapes.

Theoretical discussion or background: This section is used to develop the theoretical aspects of the experiment. Any relevant theory from class or from the lab manual can be used.

EXAMPLE:

BACKGROUND

When an RC network is placed across the output of a sinusoidal signal, the wave shape is filtered. The output wave shape is the input wave shape multiplied by a constant related to the RC time constant of the network and is given by

$$V_0 = V_{in}\, e^{-(t/RC)} \qquad (1)$$

where V_{in} = the input voltage, etc. (Define all terms)

(Continue with enough discussion to explain the general theoretical ideas, but don't put in so much material as to make this section overly long)

Experimental Procedure and Methodology and Experimental Results: This section is for explanation of apparatus, circuit configuration, and procedures used in this experiment. The title will probably change from experiment-to-experiment. You can put drawings and circuit diagrams into this section.

EXAMPLE:

EXPERIMENTAL PROCEDURE AND RESULTS

The circuit shown in Figure 1 was constructed. The quiescent emitter-to-ground voltage and the collector-to-ground voltage were measured as R_3 was systematically varied from 10 kΩ to 100 kΩ in 1Ω steps. The output voltage was simultaneously measured using an oscilloscope. At no time during this measurement did the output voltage wave shape become distorted. The measured values of VEO and VCO have been shown in Figure 2, along with the derived value of VCE. The collector voltage, VCE, was independent of variations in R_3 except when R_3 was

varied from 43,445Ω to 43,447Ω**.** For these variations in R_3 the collector voltage dropped by almost two orders of magnitude.

Continue to describe each of your other measurements.

Include all data here and any preliminary discussion of the results.

Discussion of experimental results: This section is probably the most important part of the report. The data should be presented in a reduced form. Usually figures are the easiest form to present data, but tables or lists can be used, where appropriate. Do not assume that the reader knows what you are talking about. Be descriptive. Include sample calculations along with your calculated data. Do not present data or graphs without explanation. Be sure to compare your measured results with those that you expected. Here is where theory meets reality. If the results agree with the theory show how. If the results do not agree with the predicted values, try to explain why you think they are different or where any errors in data-taking could have occurred. Explain any anomalous data.

EXAMPLE:

DISCUSSION OF EXPERIMENTAL RESULTS

The theory predicted that the output current could be written as

$$I_0 = I_{in}\, e^{(V_{in}/V_T)}$$

where, define terms here. By plotting the measured values of I_0 vs V_{in}, on a semi-log graph, as shown in Figure 6, it is seen that the output current is proportional to the exponential of the input voltage. Noting that the output current increases by a factor of 10 every time the term (V_{in}/V_T) increases by 2.3, it was possible to determine the value of V_T. V_T was found to be constant and equal to 4.4 V. This value of V_T is approximately 2x larger than expected. The difference was probably due to the fact that V_T is a function of voltage and we only measured V_T over a small range of voltages.

The value of V_2 was determined to be

$$V_2 = V_1^m$$

By plotting V_2 vs. V_1 on a log-log graph, the slope, m, was determined to be 2. This value of m agrees well with the expected value of 2.0.

Continue to compare all of your results with your expected results, including any comparisons with SPICE simulations. For every SPICE simulation, include a net list or circuit diagram and include the plots of the SPICE outputs, not the tables of node values.

Conclusion-Summary: This section should provide closure to your report. Conclusions should be based on the information described in the report. The conclusions may not exactly match the lab's objectives, but make sure your conclusions are supported by your data. Any advantages

and/or limitations of the information presented here should be included. You may want to include any personal observation that may not be reflected in the data, e.g., the problems encountered while using a particular instrument or when performing a particular step in the experiment.

EXAMPLE:

CONCLUSIONS

The current-voltage relationships governing operation of a super-duper-widget were measured over the range of input voltages from 0 V to 0.001 V. The output current was found to be proportional to the input voltage while the input current was exponentially proportional to the output voltage. These input-output relationships were those predicted by the text. If the input voltage had been varied over a somewhat larger range, these relationships may not have been found.

Acknowledgements: This section is used to acknowledge any technical or financial aid that was received in support of this work. You should state who your lab partner was in this section.

Appendices: This section should contain any miscellaneous calculations, any mathematical derivations or proofs, and any computer programs or SPICE simulations.

References:

This section contains all bibliographical work cited in the report. Usually you will reference your textbook and lab manual here. The format of these is

1. Author, *Title of reference,* page numbers, who published, where published, when published.

    1. B. Grob, *Basic Electronics,* pg. 43 to 435, McGraw Hill, New York, NY, 1943.

LABORATORY EXPERIMENTS

ELECTRONICS I
ECE 311

Introduction – Laboratory Demonstration

PURPOSE:

This laboratory session is intended to introduce you to the lab, B2 Spice, and some of the instruments that will be used during the semester. In this session you will learn to use a curve tracer to measure the characteristic curves of transistors in your lab kit. You will also learn to simulate those characteristic curves using B2 Spice software. You will begin to learn the terminology that will be used throughout the semester in this lab and in Electronics I.

LAB KIT:

For this lab and subsequent labs, you will need an IEEE ECE lab kit. If you do not have an IEEE ECE Lab kit, you should make arrangements to purchase one through the IEEE Student Branch as soon as possible. Some additional devices may be supplied by the lab instructor as needed. **Always bring your lab kit to class with you**.

B2 Spice:

You will use B2 Spice to simulate many of your experiments. All lab PCs are loaded with B2 Spice v5. You can obtain a personal copy from Beige Bag software. A light version is available free and a full version costs less than a textbook with special student discounts provided for bulk purchases.

You are required to have a copy of B2 Spice (v4 or v5) on your laptops and are **strongly advised to purchase the full version 5** (current student price is $60 through Beige Bag); this will be of benefit throughout your degree program. Version 5 is required for you to download and use the full database of parts. Under extenuating circumstances, e.g., laptop in for repair, you may contact your TA to gain access to ECE 311 lab computers. Lab computer usage is restricted to emergency situations.

The printer is connected to a single desktop computer in the lab. It is, thus, necessary to bring a portable drive if you want to print out any results, or need help debugging circuits.

The web address is for B2 Spice software is: http://www.beigebag.com/

Student pricing for B2Spice software is at: http://www.beigebag.com/pricing_other.htm

TERMINOLOGY:

Below are a few common terms used in this chapter. Others will be defined as we go along.

BIP	Bipolar
DUT	Device under Test
FET	Field Effect Transistor
I-V	Current-Voltage
I_b or I_B	Base current of the transistor

EQUIPMENT:

For this laboratory session you will need the following:

a. Hameg HM 6042 curve tracer or Tektronix Type 576 curve tracer
b. IEEE ECE lab kit
c. PC with B2 Spice loaded

The curve tracer automatically plots the current-voltage characteristics of two- and three-terminal devices. The curve tracer automatically applies the independent voltages or currents to the appropriate terminals and automatically measures the dependent currents and voltages that result.

Two types of curve tracers are provided for work stations in this laboratory: the Hameg HM 6042 and the Tektronix type 576. **Appendix B** includes front-panel photographs for the Tektronix curve tracer and basic setup instructions for it. **Appendix C** includes specific procedures for conducting some of the basic tests using the Tektronix type 576 curve tracer. **Appendix D** shows a copy of the Hameg curve tracer equipment manual (by permission of Hameg).

You should have read the equipment manual given to you before coming to lab. Failure to do so might result in your not being able to finish this lab session within the allotted time. **It is your responsibility to read the equipment manual and you should bring it to each lab session.** For this lab session your lab instructor will help you get started.

Outline for measuring with the curve tracer:

(In the following paragraphs, the numbers in parentheses are reference numbers on the Hameg HM6042 curve tracer manual's diagram of the unit's front panel.)

- Set up the curve tracer and select the parameters you want to measure.
- Choose the type of device under test (DUT) and connect to the correct terminals.
- Set the current, voltage, and power maximum ranges. Use V_{max} (21), I_{max} (19) and P_{max} (23) to set the X-axis, Y-axis, and power dissipation limits, respectively.
- In the BIP (bipolar) mode the rotary knob (8) enables the user to set the base current, I_B. In the FET mode the knob adjusts the gate voltage V_G.
- It is generally a good idea to start new device measurements with the minimum P_{max} setting.

Device parameters are measured and displayed on the instrument. The exact point on the curve is indicated by the cursor position. h-parameters and various DC parameters are available and are chosen by pressing the buttons marked ⬅➡(5).

PRE-LAB:

Review the portion of the curve tracer manual that accompanies your lab manual. Download a free student version of B2 Spice or purchase your own full copy (recommended) and install it on your PC.

TIPS FOR BUILDING CIRCUITS:

- Before starting to create the circuit, collect and sort out all the components (capacitors, resistors, diodes, probes, etc.) required in the lab. Doing so reduces the chance of using wrong components, especially resistors, which would produce wrong results.
- When building the circuit, try to mimic the layout of the lab manual's circuit diagram on the breadboard. It will help in finding wrong connections.
- Minimize the number of connecting wires, to reduce the chance of loose connections.
- Use standard resistors instead of the resistance box, when possible.

EXPERIMENTAL:

PART I: CURVE TRACER

1) **Transistor characteristics** (see sec 4.1, p15, Hameg Manual)
   a) Place a silicon NPN transistor 2N3904 or 2N2222 in the DUT socket. The TO-92 transistor package has the connections to E B C (Emitter, Base, Collector) from left to right with the flat portion of the case down, and looking from the top of the case.

   b) **Set the conditions** as follows: (Good starting conditions for most devices)

Type	[NPN/BIP]
V_{MAX}	[10 volts]
I_{MAX}	[20 mA]
P_{MAX}	[0.4 W]

   c) **Display the Curves:** Press the DUT switch (14) to display the curves. Notice that the curve tracer allows you to display five I-V characteristics at once. In this case, **each I-V characteristic corresponds to one particular setting of I_B.** Use the buttons marked ←→ to select I_B. Pressing the CURSOR key moves the cursor from one curve to another. Move the cursor to the maximum curve.

   d) **Measure I-V Characteristics:**

   - Using the FUNCTION key, select MAX. Rotate the knob to display the family of curves and set the maximum curve to $I_B = 45\mu A$.
   - Using the FUNCTION key, select MIN and set the minimum curve to $I_B = 5\mu A$.
   - By adjusting the MIN/MAX settings, you have set the I_B-step to $10\mu A$.
   - Using the FUNCTION key, select ◄►. Rotating the control knob with the ◄► function selected moves the cursor along a specific curve.
   - Measure some points (I_B, I_C, and V_C) on the transistor characteristics by looking at the display LCD and using the buttons marked ←→.

The importance of using the curve tracer to measure transistor characteristics will become evident when transistor circuits are discussed in ECE 320. You will need to determine experimentally the I-V characteristics of your bipolar transistors at the start of several of the experiments you will perform. Your transistor characteristic should resemble the characteristic shown in Figure 0.1**. Sketch this transistor characteristic using the values you recorded.**

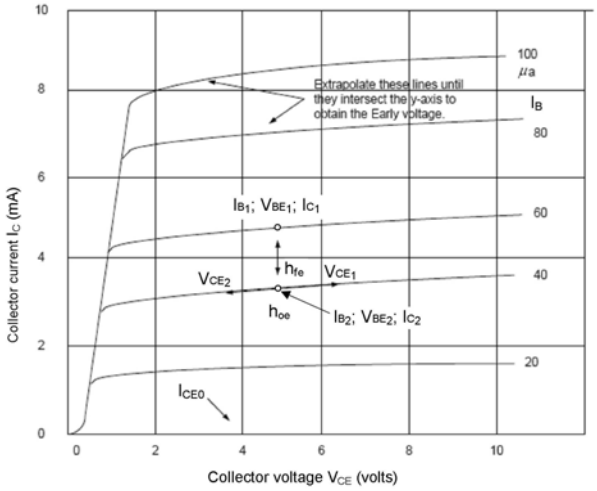


Figure 0.1: Typical I-V characteristic curves

e) **Measure Characteristics in Inverted Mode:**

- Press the DUT button to turn off power to your transistor.
- Reverse the transistor in the socket. That is, place the collector in the emitter contact and place the emitter in the collector contact. This transistor configuration is called the **inverse active mode** or **inverted mode**.
- Press the DUT button to turn on power to your transistor.
- Measure the transistor characteristics using the same settings used above. The collector current should be quite low.
- Reduce I_{MAX} to 2mA and increase maximum and minimum I_B settings by a factor of 10 using the MAX and MIN functions.
- Sketch this transistor characteristic, recording several values to note on your sketch.
- Press DUT to turn off power to the transistor.

PART 2: CIRCUIT SIMULATION

B2 Spice is a fully featured mixed-mode simulator with powerful and innovative features that make it the simulator of choice for power SPICE users. Features include a parts-chooser window, workspace editor, importing and exporting to Eagle PCB as well as other PCB programs, and animated schematics. All lab PCs are loaded with B2 Spice v5. The demo is based on B2 Spice v5 but is similar to v4.

The **schematic and output** for the circuit to obtain the transistor characteristics are given below, in Figure 0.2 and Figure 0.3.

1. Open B2 Spice v5. The Analog Schematic window opens.
2. Select ► Common Parts ►Choose Part.
3. In the **Name** box enter ► 2N3904
4. Hit the **Find** button.
5. Select **2N3904** and then click select device; this will attach a schematic symbol to the cursor. You can place it on the Schematic page by clicking on the page.
6. Continue building your circuit by repeating Step 2 through Step 5. Often the part you want may appear directly in the Common Parts list; just select it and place it on the schematic window (for example, ground, current source, voltage source)
7. Connect all parts with a wire by first selecting the "****" button.
8. Add meters to observe voltages and currents (voltmeters and ammeters).
9. SAVE your circuit.
10. Click on the **Tests** Tab.
11. Select **DC Sweep** by clicking the Setup button.
12. Select the **Sweep** Tab.
13. Select V_1 from the **Source** menu. Select "0" for the **Start Value**, "5" for the **End Value** and "100m" for the **Step Value**.
14. Click "**Set up Sweeps**". Select "I_1" from the list window. Enable "**Sweep**". Select "Linear" from **Interval Type** menu. Select "5µ" for the **Start Value**, "45µ" for the **End Value** and "10µ" for the **Step Value**. Click **Accept Changes**. Click **OK.** Enable "graph" for the 2D output.
15. Click **Run**.

NOTE: It is important that you use the actual device you want to simulate and not a GENERIC component.

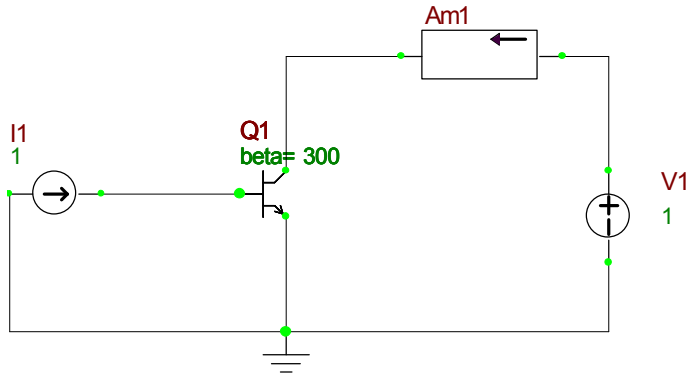


Figure 0.2: B2 Spice Circuit

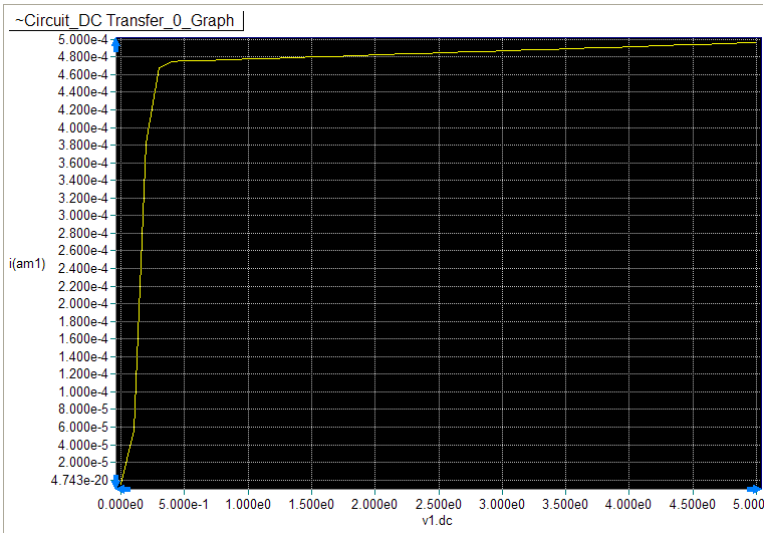


Figure 0.3: Output Information.

LAB REPORT:

There is no formal lab report required for this session. You should assure yourself that you know how to use:

i. The curve tracer to obtain the I-V characteristics of a BIP device.
ii. B2 Spice to simulate a circuit

ECE 311-EXPERIMENT 0 CHECK LIST

1) Curve Tracer

   Obtain NPN transistor characteristics.

2) SPICE

   Obtain simulation results

3) Conclusion

   Compare SPICE and curve tracer outputs.

ELECTRONICS I
ECE 311

Experiment #1 – Diode Characteristics

PURPOSE:

The purpose of this experiment is to acquaint the student with the operation of semiconductor diodes. You will use a curve tracer to obtain the current-voltage (I-V) characteristics of a silicon diode. From these characteristics, you will determine several diode parameters including the **dynamic resistance**, $r_f = r_d$; the **diode forward resistance**, $R_F = R_D$; the **cut-in voltage**, V_γ; the **forward diode ideality factor**, n; and the **breakdown voltage**, V_{BR}. All of these terms are defined below. You will find that most of these parameters depend on the current at which that parameter is measured. You will also compare the dc operation of a diode in a circuit with both the calculated and simulated operation.

PRE-LAB:

Review the INTRODUCTION section below. Simulate the diode characteristic using B2 Spice for comparison with experimentally measured results. Determine r_d, V_γ, and n for the 1N4004 diode in your diode characteristic plot. Simulate the circuit shown in Figure 1.5 for the resistor (R) values shown using a DC sweep test (sweep V_{in} and R simultaneously; see Part 2 of previous lab for help).

EQUIPMENT:

For this experiment, you will need:

a) Silicon diodes – 1N4004 or equivalant, and 1N4744. These diodes are all silicon diodes with different breakdown voltages and different power handling capabilities. The 1N4744 is a Zener Diode and has the lowest breakdown voltage. It should be used when attempting to obtain the reverse breakdown voltage. The 1N4004 diode will be used extensively in circuits in other experiments.

b) A curve tracer

c) NI ELVIS II workstation

d) IEEE ECE lab kit

e) B2 Spice simulation program

INTRODUCTION:

Diode Structure:

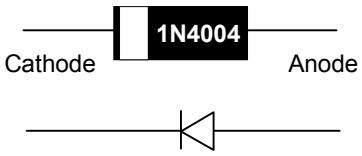


Figure 1.1

Figure 1.1 shows the physical and schematic circuit symbol of the diode. The band on the diode and the bar on the left of the circuit symbol represent the cathode (n-type material) and

must be noted. The p-type material (the anode) in the diode is located to the right. The circuit symbol of the diode is an arrow showing forward bias, when the p-side is positive with respect to the n-side, and the direction of the arrow represents the direction of large current flow.

Ideal Diode Equation:

The relationship between the diode current and voltage is given by the diode equation

$$I_D = I_S \left(e^{V_D / nV_T} - 1 \right) \tag{1.1}$$

The terms in Equation (1.1) are defined as follows:

I_D = the diode current (amperes).

V_D = the voltage across the diode (volts).

I_S = the reverse saturation current or the reverse leakage current (amperes).

I_S is a function of the diode material, the doping densities on the p-side and n-side of the diode, the geometry of the diode, the applied voltage, and temperature. I_S is usually of the order of 1μA to 1mA for a germanium diode at room temperature and of the order of 1pA = 10^{-12}A for a silicon diode at room temperature. I_S increases as the temperature rises.

V_T = kT/q = the thermal equivalent voltage = 0.0258 V at room temperature

where

q = 1.6 x 10^{-19} Coulombs = the electric charge,

k = 1.38 x 10^{-23} J/K = Boltzmann's constant,

and

T = absolute temperature (Kelvin) [room temperature = 300 K].

n = the ideality factor or the emission coefficient.

The Ideality Factor (n):

The ideality factor, n, depends on the type of semiconductor material used in the diode, the manufacturing process, the forward voltage, and the temperature. Its value generally varies between 1 and 2. For voltages less than about 0.5 V, n ~ 2; for higher voltages, n ~ 1. (Based on experimental measurements, at higher voltages, typically $1.15 \leq n \leq 1.2$.)

The ideality factor, n, can readily be found by plotting the diode forward current on a logarithmic axis vs. the diode voltage on a linear axis.

Equation (1.1) indicates that an increase in current I_D by a factor of 10 represents an increase in $exp(V_D/nV_T)$ by a factor of 10, as long as $exp(V_D/nV_T) >> 1$. If ΔV_D is the change in voltage required to produce a factor-of-10 change in the current, then

$$\Delta V_D / nV_T = \ln(10) = 2.30$$

or,

$$\Delta V_D = 2.30 \cdot n \cdot V_T = 2.30 \cdot n \cdot 0.0258 \text{ volts} = n \cdot 0.0593 \text{V} = n \cdot 59.3 \text{ mV}$$

And so,

$$n = \Delta V_D / 59.3mV \approx \Delta V_D / 60mV \qquad (1.2)$$

To find n, it is only necessary to find the amount of voltage needed to increase the diode current by a factor of 10 and use Equation (1.2).

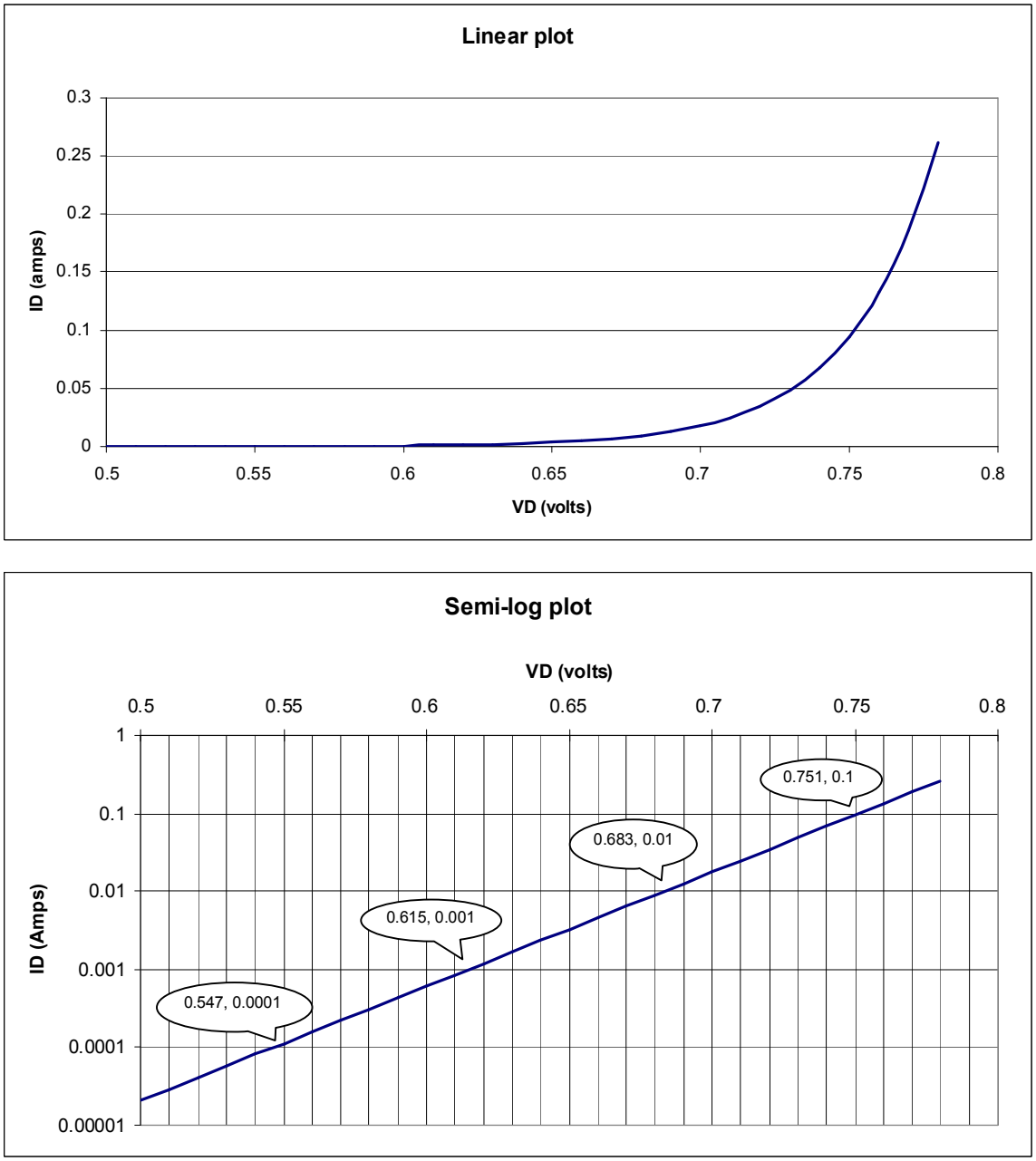


Figure 1.2: Graphs of the same forward diode current I_D vs diode voltage V_D as (a) Linear plot and (b) Semi-log plot

Figure 1.2 shows example graphs of the forward diode current I_D vs diode voltage V_D as (a) Linear plot and (b) Semi-log plot. To calculate the ideality factor n, create the semi-log plot for

the diode's data. Draw a straight line through adjacent points, then read off coordinates where the current I_D increases by powers of 10 (e.g., 0.0001, 0.001, 0.01, 0.1, …), as illustrated in Figure 1.2. Calculate ΔV_D, the amount of voltage needed to increase the diode current by a factor of 10, and then divide by 59.3mV (or 60 mV) to calculate n:

$$n = \frac{0.751 - 0.683}{0.0593} = 1.147 .$$

(*Advanced note*: The ideality factor is a measure of how close the diode matches "ideal" behavior. If the ideality factor is different from 1, it indicates either that there are unusual recombination mechanisms taking place within the diode or that the recombination is changing in magnitude. Thus, the ideality factor is a powerful tool for examining the recombination in a device.)

Cut-in Voltage V_γ:

A sketch of a diode characteristic, as it would be measured on a curve tracer, is shown in Figure 1.3. The curve tracer only measures the forward I-V or the reverse I-V characteristic in any one sweep. The characteristics shown in Figure 1.4 are the combination of the forward and reverse characteristics. Appreciable conduction occurs from around 0.4V to 0.7V for silicon and from around 0.2V to 0.4V for germanium at room temperature. The value of V_γ is a function of the current at which V_γ is measured. This point is discussed below and is one of the concepts you should master from this experiment. If the applied voltage exceeds V_γ, the diode current increases rapidly.

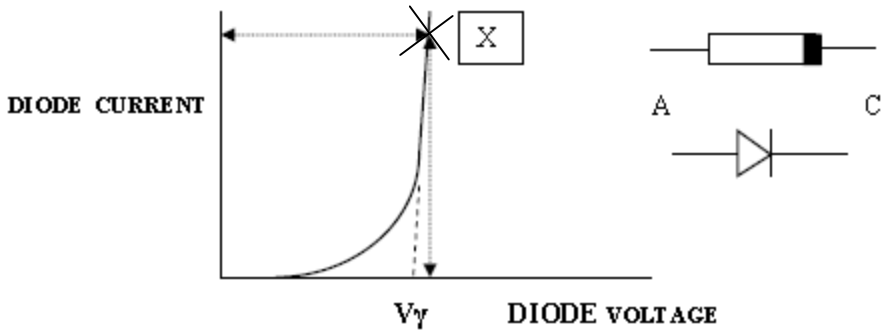


Figure 1.3: Diode forward I-V characteristic showing the definition of Vγ

The complete diode characteristic is shown in Figure 1.4, piecing together the forward-biased data and the reverse-biased data. Note that the scales of +V and –V may differ by a factor of 100, and while +I may be mA or A, –I is likely to be μA or nA.

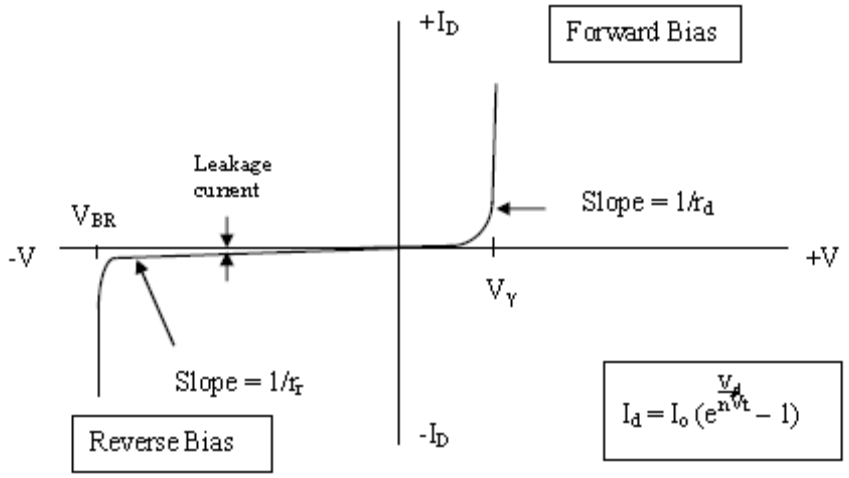


Figure 1.4: Forward and reverse diode I-V characteristics

Diode Current and Diode Saturation Current:

If the diode is operated in the forward-bias region at room temperature (27°C = 300 K), the exponential first term in the brackets in Equation (1.1) dominates and the diode current equation is given approximately by

$$I_D = I_S \, e^{V_D / nV_T} \tag{1.3}$$

The current for forward bias is an exponential function of the applied voltage, V_D.

If the diode is reverse-biased, only the small reverse current (the reverse saturation current or the reverse leakage current), $-I_s$, flows. This current flows as long as the applied reverse voltage does not exceed the diode breakdown voltage, V_{BR}. If the reverse voltage exceeds V_{BR}, a large amount of current flows and the diode may be destroyed if there is not enough series resistance to limit the diode current. In silicon diodes, I_s may be very small and V_{BR} may be very large. Both of these values may be immeasurable on the curve tracers for diodes like the 1N4004.

Diode Resistance

Three diode resistances are commonly calculated:

- DC or Static forward resistance, R_F or R_D
- AC or Dynamic forward resistance, r_f or r_d
- Reverse resistance, r_r

Another diode resistance, $\mathbf{R_S}$, is also mentioned. R_S refers to the sum of the diode's contact resistance, lead resistance, and internal diode resistance. It appears in B2 Spice simulations.

DC or Static forward resistance, R_F or R_D, is the total voltage drop across the diode divided by the current flowing through the diode, just as one would calculate using Ohm's Law. It includes contact resistance, lead resistance, material resistance, and the resistance of the p and n regions of the diode.

$$R_F = \frac{V_D}{I_D}.$$

AC or Dynamic forward resistance, r_f or r_d: In practice we don't often use the static forward resistance; more important is the dynamic or AC resistance, which is the opposition offered by the diode to *changing* current. It is calculated by the ratio [change in voltage across the diode] / [the resulting change in current through diode] at the operating voltage, V_D. That is, r_d is the *reciprocal of the slope* of diode current versus voltage at the operating point.

$$r_f \equiv r_d = \frac{1}{\Delta I_D / \Delta V_D} = \frac{\Delta V_D}{\Delta I_D} = \frac{\text{Change in voltage}}{\text{Resulting change in current}}$$

Applying the diode equation and differentiating, we find the dynamic forward resistance is given by

$$r_d = \frac{dV_D}{dI_D} = \frac{1}{dI_D / dV_D} = n\frac{V_T}{I_D} \quad . \tag{1.4}$$

Owing to the nonlinear shape of the forward characteristic, the value of AC resistance of a diode is in the range of 1 to 25 ohms. Usually it is smaller than DC resistance of the diode.

Reverse Resistance, r_r: When a diode is reverse biased, besides forward resistance, it also possesses another resistance known as reverse resistance. It can be either DC or AC depending upon whether the reverse bias is direct or alternating voltage. Ideally, the reverse resistance of the diode is infinite. However, in actual practice, the reverse resistance is never infinite, due to the existence of leakage current in a reverse-biased diode.

The **reverse resistance, r_r**, is given by the reciprocal of the slope of the reverse characteristic, prior to breakdown (see Figure 1.4).

Junction Capacitance of Diode (C_j):

The space-charge region (or depletion region) of the diode is a region that contains very few holes or electrons and lies between the n-type semiconductor and the p-type semiconductor inside of the diode. The space-charge region of the diode approximates a parallel-plate capacitor, with the value of the capacitance determined by the applied voltage. Using this approximation, the capacitance of the space-charge region is approximately given by

$$C_j = \frac{eA}{w} = C_{jo}\left(1 - \frac{V_D}{V_{bi}}\right) - \frac{1}{n} \tag{1.5}$$

where

e = permittivity of silicon (10^{-12} F/cm),

A = cross-sectional area of the diode (cm^2),

w = width of the depletion region (cm),

n = 2 for a step junction,

V_{bi} = built-in voltage, and

C_{jo} = the junction capacitance at $V_D = 0$ V.

The junction capacitance is inversely proportional to w. As the reverse-bias voltage increases, the space-charge region widens, approximately as the square root of the applied voltage, and, thus, the capacitance decreases. This variation in w causes the diode to behave as a voltage-controlled capacitor with a capacitance that varies inversely with the square root of the applied voltage. If the diode had a very large cross-sectional area, the capacitance of the space-charge region as a function of the reverse voltage could be measured on an impedance bridge. Since the diodes in your lab kits are generally relatively small, it is very difficult to measure the voltage variation of the diode capacitance. Usually only a large area diode, like the power diode in your lab kits, is large enough to be used to measure the diode capacitance using the impedance bridges in the lab. Due to the large forward diode current, it is usually possible to measure the diode capacitance only for voltages less than V_γ.

EXPERIMENT:

PART I: MEASUREMENT OF DIODE CHARACTERISTICS

A. Forward I-V Characteristic

Procedure

1. Use the curve tracer to obtain the forward characteristics of the silicon **1N4004** diode.
   - Connect diode cathode and anode terminals to terminals E and C, respectively, and set switch BIP/FET to FET).
   - Set the voltage axis to $V_{max} = 2V$.
   - Begin your measurements with $I_{max} = 2mA$.
   - Use $P_{max} = 0.4W$.
   - Press the DUT button to obtain the curve.
   - If the curve is flickering, use the function key to select ◄►, and move the control knob counter-clockwise until the flickering stops.
   - Using the cursor key, take readings from the I-V characteristic for values of current close to those in the first column of Table 1.1, to enable you to plot accurately the I-V characteristic both on linear graph paper and on logarithmic graph paper. **Increase the I_{MAX} by a factor of 10 between measurements once you cannot read a higher value on the given curve.** Tabulate your results below.

TABLE 1.1: Table of Current, voltage, forward resistance, dynamic resistance

I_D (A)	Your Value of I_D (A)	V_D (volts)	R_F (Ω) = V_D/I_D	r_d (Ω) = nV_T/I_D
30μA				
100μA				
200 μA				
400 μA				
1mA				
2mA				
6mA				
14mA				
30mA				
60mA				
100mA				
150mA				

2. Compute R_F and r_d using the values you recorded and record in the table above. See Introduction for the definitions of R_F and r_d.

B. Reverse I-V Characteristic

You should use the **1N4744** diode (Zener Diode) for this part of the experiment. If you use the 1N4004 diode, your breakdown voltage will be more negative than -100 V and diode breakdown cannot be seen on lab curve tracer. Also, the reverse leakage current will be very low for all of the silicon diodes in your lab kit, and such extremely low current cannot be measured with curve tracer.

Procedure

1. Press the DUT button to turn off the power to the diode. Reverse the voltage polarity on the diode by turning the diode around in the socket and set I_{max} to 2mA, V_{max} to 40V, and P_{max} to 0.4W. Press the DUT button to obtain the reverse characteristics.
2. Sketch the reverse I-V characteristic as accurately as possible up to the breakdown voltage, noting the breakdown voltage on your plot.

PART II: SIMPLE DIODE CIRCUITS

You should have simulated the diode-resistor circuit shown in Figure 1.5 with the values of R given below.

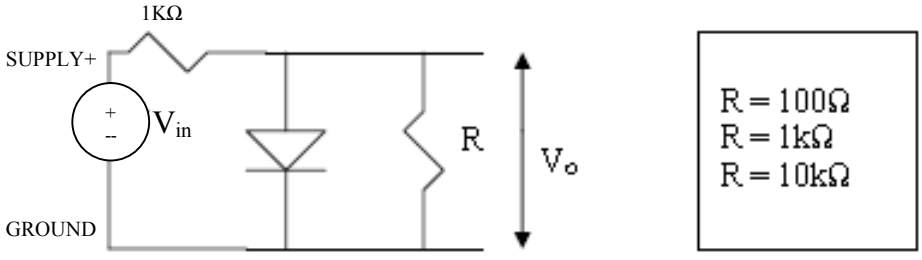


Figure 1.5: Simple Diode Circuit

Procedure

a. Build the circuit shown in Figure 1.5 on the NI-ELVIS breadboard with R = 100Ω. Use the 1N4001 or the 1N4004 diode.

b. Use the digital multimeter (DMM) DC Voltage [V⎓] function to measure the output voltage, V_o, using the VΩ and COM banana jacks.

c. Using the VPS front panel, Click "Run" and vary the voltage SUPPLY+ from 0 to 5V in increments of 0.5V and record the output voltage. If you are proficient with the ELVIS you can use the VPS sweep function with the following settings: Start 0V, Step 0.5V, Stop 5V, Interval 5000ms. In this case, Click "Sweep" instead of "Run".

d. Repeat steps a to c for the other values of R given in Figure 1.5 and complete Table 1.2, below.

Table 1.2: Measured V_o for circuit in Figure 1.5

V_{in} (volts)	V_o (volts)		
	R = 100Ω	R = 1kΩ	R = 10kΩ
0.0			
0.5			
1.0			
1.5			
2.0			
2.5			
3.0			
3.5			
4.0			
4.5			
5.0			

LAB REPORT:

PART I

1. Plot I_D vs. V_D on linear graph paper (or using software of your choice).
2. Determine V_γ directly from the plotted graph and record your result. Determine how V_γ depends on the diode current and voltage levels.
3. Determine the slope from the linear plot of the forward I-V characteristic as a function of the diode current, as shown in Figure 1.4, using the data previously taken in Table 1.1. Note that the inverse of the slope, or r_d, you measure is a function of where you choose the diode current. Obtain at least eight (8) slope data points.
4. Plot R_F and r_d from Table 1.1 as a function of diode current. How do R_F and r_d compare?
5. Create a semi-log graph of I_D (log scale) vs. V_D. Determine n from the slope. Remember that on a semi-log plot where I is plotted as a function of V_D, an exponential function is a

straight line. Use Equation (1.2) to determine n. Note that if n = 1, the current will increase by 1 decade for every 0.060V of V_D, and if n = 2, the current will increase by 1 decade for every 0.120V of V_D. Extrapolate the current to V_D = 0V and determine the value of I_S.

PART II

1. What is the effect of the diode on V_o?
2. Derive an expression for V_o as a function of V_{in} using the piecewise-linear model of the diode comprised of the values of r_d and V_γ you calculated from the linear I-V characteristic plot.
3. Compare the measured V_o with the simulated output voltage and the calculated output voltage from step II.2. Comment on any differences. Remember that the B2 Spice simulation is a simulation and is only as good as the parameters you use to describe the diode. Your experimental results are reality. You should be comparing the voltages you measured with the values you calculated using the measured diode characteristics.

ECE 311 EXPERIMENT 1 - CHECK LIST

1. **Diode Characteristics**
   a. Forward Characteristics (V_{MAX} = 2V)
      i. Obtain forward diode characteristics on curve tracer.
      ii. Record linear and log current data points using cursor.
      iii. Plot I-V characteristic (linear and semi-log).
      iv. Determine r_d as a function of diode current.
      v. Determine R_F as a function of diode current.
      vi. Determine V_γ. How does V_γ change with diode current?
   b. Reverse Characteristics
      i. Attempt to obtain reverse diode characteristics. Set V_{MAX} = 40 V.
      ii. Is the breakdown voltage greater than 100 V?
2. **Simple Diode Circuits**
   a. Build Circuit
   b. Measure output (V_o) as a function of input voltage for R = 100Ω, 1kΩ, and 10kΩ.
   c. Derive an expression for V_o and V_{in} using piecewise model.
   d. Compare measured results of V_o with simulated results and calculated output voltage.

ELECTRONICS I
ECE 311

Experiment #2 – Power Supply Operation

PURPOSE:

This laboratory session acquaints you with the operation of a diode power supply. You will study the operation of **half-wave and full-wave rectifiers, and the effect of smoothing filters**. You will also learn about DC voltage (V_{dc}), the ripple factor (RF), ripple voltage (V_r), and root mean square voltages (V_{rms} and V_r(rms)) of a power supply.

PRE-LAB:

You should simulate the circuits shown in Figures 2.3 and 2.5 with the different resistor and capacitor values that you will use in the experiment. You should be prepared to compare your simulations with your measurements after you have built your circuits.

EXPERIMENT:

(a) Diodes (1N4001 or 1N4004)

(b) Resistors

(c) Capacitors

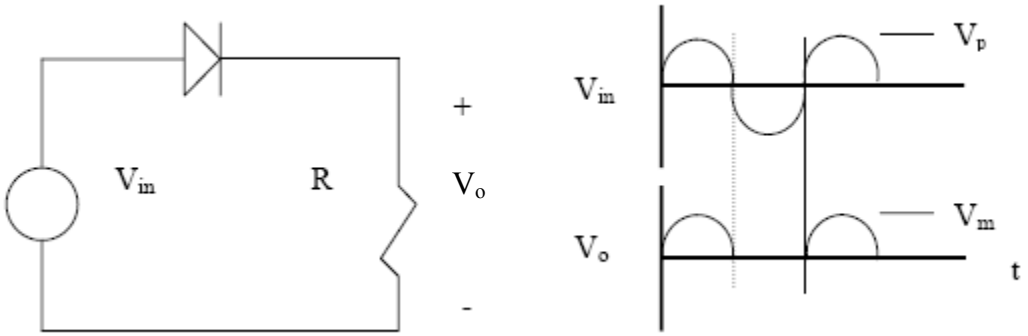
(d) NI ELVIS II Workstation

INTRODUCTION:

The diode can be used to change the wave shape of an incoming signal. When used as a rectifier, the asymmetrical properties of the diode's current-voltage characteristics can be used to convert an ac signal into a dc signal. The rectification can either be a half-wave or full-wave.

Half-Wave Rectifier

Figure 2.1(a) shows a basic half-wave diode rectifier circuit. During the positive half-cycle of the input voltage, the diode is forward-biased for all instantaneous voltages greater than the diode cut-in voltage, V_γ. Current flowing through the diode during the positive half-cycle produces approximately a half sine wave of voltages across the load resistor, as shown in the lower part of Figure 2.1(b). To simplify our discussions, we will assume that the diode is ideal and that the peak input voltage is always much larger than the V_γ of the diode. Hence, we assume that the zero of the rectified voltage coincides with the zero of the input voltage. On the negative half-cycle of the input voltage, the diode is reverse-biased. Ignoring the reverse leakage current of the diode, the load current drops to zero, resulting in zero load voltage (output voltage), as shown in Figure 2.1(b). Thus, the diode circuit has rectified the input ac voltage, converting the ac voltage to a dc voltage.



(a) (b)

Figure 2.1: A half-wave rectifier

The average or dc value of this simple half-wave rectified signal, V_{dc}, is given by

$$V_{dc} = \left(\frac{1}{T}\right)\int_0^{T/2} V_m \sin\left(\frac{(2\pi t)}{T}\right) dt = \frac{V_m}{\pi} = 0.318 V_m \tag{2.1}$$

Here V_m is the peak value of the rectified signal.

The average voltage is called the dc voltage because this voltage is what a dc voltmeter connected across the load resistor would read. Hence, if V_m = 10 V and the diode is ideal, a dc voltmeter across the load resistor would read 3.18 V.

Full-Wave Rectifier

Figure 2.2(a) shows a full-wave bridge rectifier with a load resistor R_L and an input sine wave derived from a transformer. During the positive half-cycle of the input voltage, diodes D2 and D3 are forward biased and diodes D1 and D4 are reverse biased. Therefore, terminal A is positive and terminal B is negative, as shown in Figure 2.2(b). During the negative half-cycle, illustrated in Figure 2.2(c), diodes D1 and D4 conduct, and again terminal A is positive and terminal B is negative. Thus, on either half-cycle, the load voltage has the same polarity and the load current is in the same direction, no matter which pair of diodes is conducting. The full-wave rectified signal is shown in Figure 2.2(d), with the V_o being the output voltage.

Since the area under the curve of the full-wave rectified signal is twice that of the half-wave rectified signal, the average or dc value of the full-wave rectified signal, V_{dc}, is twice that of the half-wave rectifier.

$$V_{dc} = \frac{2V_m}{\pi} = 0.636\, V_m \tag{2.2}$$

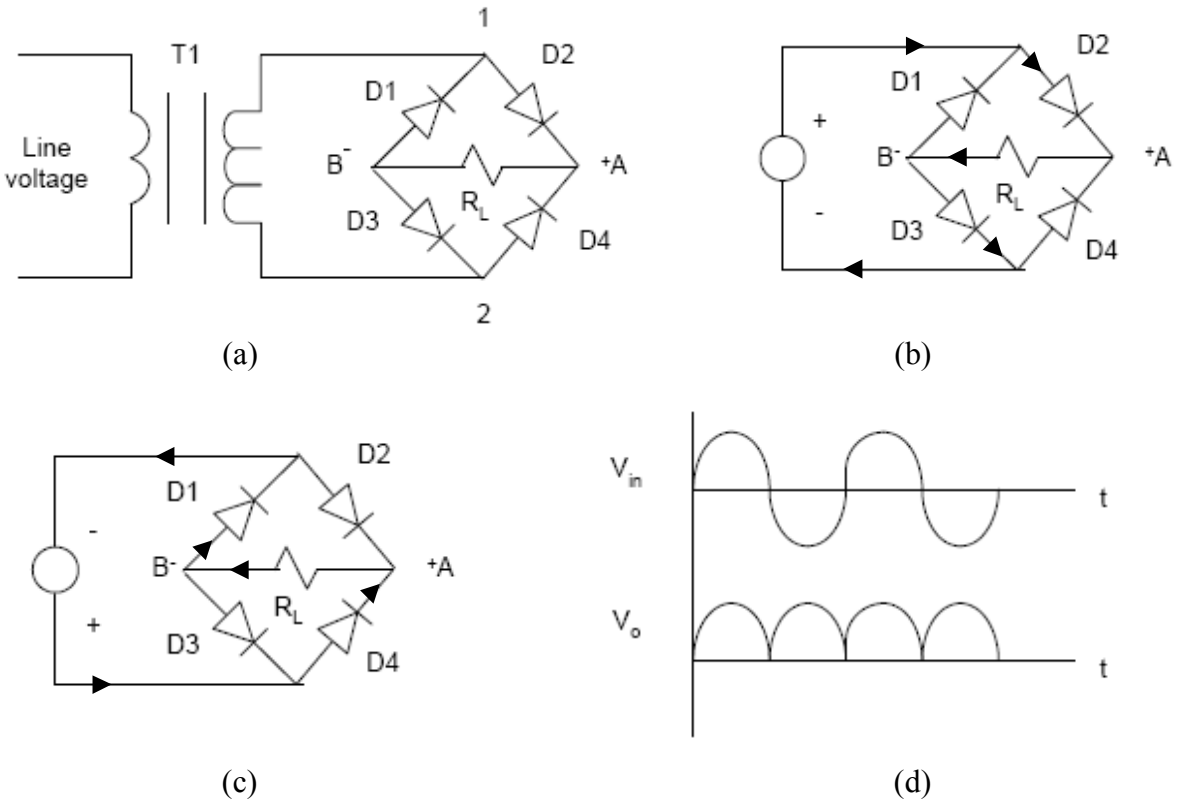


Figure 2.2: Full wave bridge rectifier circuit and waveforms

Filtering

The rectifier circuits discussed above provide a **pulsating** dc voltage at the output. **These pulsations are known as "ripple".** The uses for this kind of output are limited to charging batteries, running dc motors, and a few other applications where a constant dc voltage is not necessary. For most electronic circuits, however, a constant dc voltage similar to that from a battery is required. To convert a half-wave or full-wave rectified voltage with ripple into a more constant dc voltage, a smoothing filter must be used at the rectifier's output.

A popular smoothing filter is the capacitor-resistor filter, which consists of a single capacitor in parallel with the load resistor. Figure 2.3 shows such a filter connected to the output of a half-wave rectifier. The output wave shape of the filtered half-wave rectifier is similar to that shown in Figure 2.4, assuming that the time constant of the R_LC filter is comparable to the period of the input voltage.

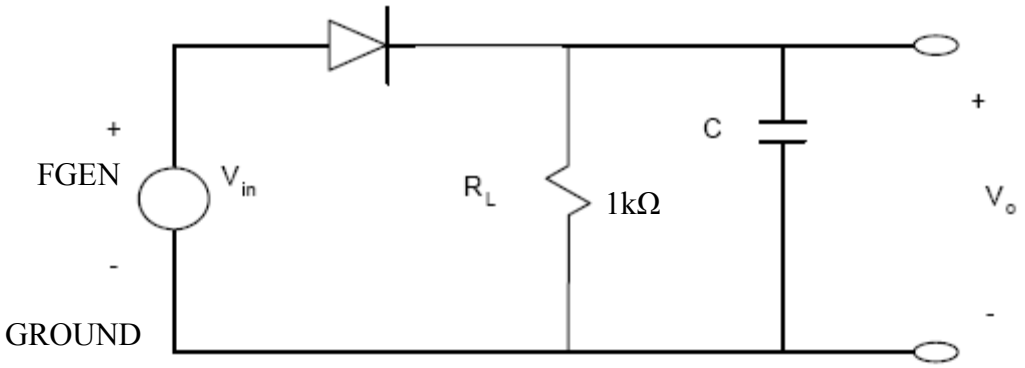


Figure 2.3: Rectifier circuit with an RC smoothing filter

Notice that the output wave shape still has ripple, but the ripple is now saw-tooth or triangular shaped, and its variation is much less than that of the unfiltered pulses. The difference between the maximum and minimum of the filtered voltage is known as the **Ripple Voltage (V_r)**. In Figure 2.4, this voltage is labeled ΔV. Thus, we have

$$V_r \equiv \Delta V = V_m - V_{min}.$$

where

V_m = peak value of the rectified signal (smaller than the V_{in}, due to V_γ and R_s),

V_{min} = the minimum of the filtered voltage. V_{min} increases as the ripple voltage decreases.

The design equation for selecting this capacitor is

$$\frac{V_r}{V_m} = \frac{T}{R_L C} = \frac{1}{f_p R_L C} \tag{2.3}$$

where

R_L = load resistance

I_L = load current

C = filter capacitance

$T = 1/f_p$ = the period of the rectified wave.

For a half-wave rectifier, f_p is the frequency of the input voltage. For a full-wave rectifier, f_p is twice the frequency of the input voltage. The output of the filtered voltage for a full-wave rectifier is shown in Figure 2.4.

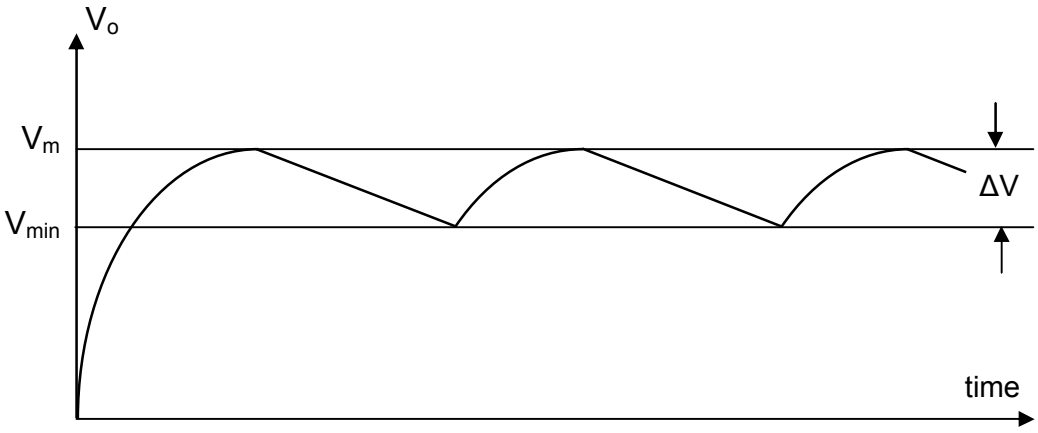


Figure 2.4: Output wave shape from a full-wave filtered rectifier.

From Figure 2.4, we see that ΔV ($=V_r$) determines the amount of ripple in the output signal. From Equation (2.3), we see that for the ripple voltage V_r to be small, the R_LC time constant must be large. In other words, the ripple can be reduced by increasing the discharging time constant R_LC. Hence, increasing either C or R_L will reduce the ripple voltage. It should be noted that the resistor R_L is usually inside a commercial power supply and any external load connected to the power supply is in parallel with R_L and acts both to lower the total load resistance and to increase the ripple. This is why an audible hum is often heard from power supplies when the external load resistance drops to a very low value.

Two figures of merit for power supplies are the **ripple voltage, V_r**, and the **ripple factor, RF**. V_r has already been defined. RF is defined as

$$RF = V_r(\text{rms}) / V_{dc}. \tag{2.4}$$

V_r(rms) is the RMS value of the ripple voltage. The value of V_r(rms) can be calculated for various input wave shapes. For a complicated wave shape, such as that shown in Figure 2.4, the value of V_r(rms) is calculated as if the filtered, rectified wave were a triangular wave, for which

$$V_r(rms) = \frac{V_m - V_{\min}}{2\sqrt{3}} = \frac{V_r}{2\sqrt{3}}. \tag{2.5}$$

It is import to note that V_r and V_r(rms) are not the same.

Earlier we talked about the average or dc voltage, V_{dc}, for unfiltered, rectified supplies. Recall that for a sinusoidal input,

$$V_{dc} = V_m/\pi = 0.318\ V_m \quad \text{for an unfiltered half-wave rectifier}$$

and

$$V_{dc} = 2V_m/\pi = 0.636\ V_m \quad \text{for an unfiltered full-wave rectifier.}$$

The average (dc) voltage will lie between V_m and V_{min}. Therefore, for the filtered, triangular wave shape shown in Figure 2.4, a better value of V_{dc} would be given by

$$V_{dc} = V_m - \frac{V_r}{2} = \frac{V_m + V_{\min}}{2} \ , \tag{2.6}$$

or equivalently,

$$V_{dc} = V_m - \frac{V_m}{2 f_p R_L C} = V_m \left(1 - \frac{1}{2 f_p R_L C} \right) = V_r \left(f_p R_L C - \frac{1}{2} \right). \tag{2.7}$$

EXPERIMENTAL:

PART 1: HALF-WAVE RECTIFIER

1. Build the circuit shown in Figure 2.3 using the NI-ELVIS function generator (FGEN) as the voltage source V_{in}. The connections are FGEN (pin #33) and GROUND (either pin 49 or 53) on the left side of the NI-ELVIS breadboard. **Leave the capacitor C out of the circuit for now**. When adding or removing components, ALWAYS "STOP" THE ELVIS INSTRUMENTS AND TURN OFF THE PROTOTYPING BOARD.
    a. Open the function generator's instrument panel. YOUR PROTOTYPING BOARD MUST BE TURNED ON FOR APPROPRIATE FUNCTION OF THE INSTRUMENT PANEL.
    b. Using the FGEN instrument panel, set the frequency of the function generator to 60 Hz.
    c. Click “Run”.
    d. Enable “Manual Mode” on the function generator.
    e. Adjust the output voltage of the function generator using the manual amplitude control knob (located at the bottom right corner of the workstation) until the voltage is $8V_{P\text{-}P}$.
    f. Verify the function generator settings by connecting the positive clip of the BNC cable to the FGEN terminal and the negative clip to GROUND terminal. Then, connect BNC connector to SCOPE CH 0 of the oscilloscope (BNC input located at upper left corner of workstation).
    g. Open SCOPE instrument panel.
        i. Set the Trigger type to “Edge” or "Immediate".
        ii. Ensure that Channel 0 is Enabled, Coupling is set to “DC”, and Source is set to “SCOPE CH 0”
        iii. Click “Run”
        iv. Adjust the function generator amplitude as needed to ensure that $V_{P\text{-}P} = 8V$
        v. Click “Stop”.

h. Connect SCOPE CH 1 of the oscilloscope across the resistor R_L. Ensure that ground leads of SCOPE CH 0 and 1 are both connected to ground.

i. Ensure that Channel 1 is Enabled, Coupling is set to "DC", and Source is set to "SCOPE CH 1"

ii. Click "Run" to measure V_{in} and V_o.

2. Make an accurate sketch of the input and output waveforms on the same graph paper, with the output waveform superimposed on the input waveform. Enable Cursors by clicking the "Cursors On" box and use the cursors to record V_m and V_{min} by switching the cursor(s) to CH1. Press STOP and adjust time/div to improve accuracy when taking cursor measurements. Record the values of V_m and V_{min} in Table 2.1.

3. Connect a 10µF capacitor in parallel with R_L. Make an accurate sketch of the new output waveform on the same graph as used in step 2, but label the new waveform. Record V_m and V_{min} using the cursors.

4. Repeat step 3 for each of the following values of capacitors: 22µF and 47µF. You can draw your output wave shapes on the same graph used in step 2, labeling each waveform. Record V_m and V_{min} for each different resistor/capacitor pair.

Table 2.1: RF at various C when R_L = 1k

R_L=1kΩ; C (µf)	V_m	V_{min}	V_r	V_r(rms)	V_{dc}	Ripple Factor
No Capacitor						
10						
22						
47						

5. Repeat steps 2-3 for R_L = 470Ω, 10 kΩ, 100 kΩ. Start a new graph for each resistor case to keep your graphs of the waveforms from becoming crowded. Record V_m and V_{min} for each case and enter values on Table 2.2.

Table 2.2: RF at various R_L when C = 10uF

C= 10µf; R_L(Ω)	V_m	V_{min}	V_r	V_r(rms)	V_{dc}	Ripple Factor
470						
10k						
100k						

6. The two extreme cases of filtering are the filter with the lowest values of R_L and C and the filter with the highest values of R_L and C. Sketch, on one graph, the output wave shapes for these two extreme cases; that is, for R_L = 470Ω, C = 10µF and R_L = 100kΩ, C = 47µF. Record V_m and V_{min} for these two cases. Enter your results in Table 2.3 Part 1.

Table 2.3: Extreme Cases of R_L and C

	Part 1: Half Wave Rectifier		Part2: Full Wave Rectifier	
	R_L = 470 Ω C = 10 μF	R_L = 100 kΩ C = 47 μF	R_L = 470 Ω C = 10 μF	R_L = 100 kΩ C = 47 μF
Vm				
Vmin				
V_r				
V_r(rms)				
V_{dc}				
Ripple Factor				

7. Determine V_{dc}, V_r, V_r(rms), and ripple factor RF for each case in steps 3, 4, and 5.
8. Use R_L = 100kΩ, C = 47μF. Note the output wave form. Put a 1 kΩ resistor in parallel with R_L and note the change in the output wave shape.

PART II: FULL-WAVE RECTIFIER & POWER SUPPLY

1. Build the circuit shown in Figure 2.5. Have your laboratory instructor inspect your circuit before turning on the function generator. Use $R_L = R_S$ = 1 kΩ.

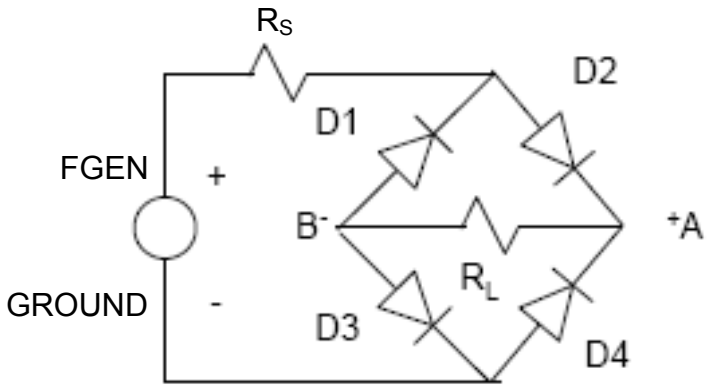


Figure 2.5: Full-wave rectifier with voltage-dropping series resistor R_S

2. Set the function generator output by connecting the function generator terminals to CH0 of the oscilloscope (BNC CH0 input located in upper left corner of workstation). Positive clip of BNC cable will be connected to FGEN and negative clip will be connected GROUND.
    a. Set the function generator's frequency to 60Hz.
    b. Click “Run”.
    c. Enable “Manual Mode” on the function generator.

   d. Adjust the output voltage of the function generator using the manual amplitude control knob (located at the bottom right corner of the workstation) until the voltage is $12V_{P\text{-}P}$.

3. Measure the voltage across R_L by connecting nodes A and B to terminals AI0+ and AI0- (located on the top left corner), respectively. **DO NOT USE BNC INPUT OF CH1.** (This is necessary to avoid oscilloscope grounding errors.)

   a. Ensure that Channel 1 is Enabled, Coupling is set to "DC", and Source is set to "AI 0".

   b. Click "Run" to measure V_{in} and V_o.

4. Make an accurate sketch of the both waveforms. Record V_m and V_{min} of the output voltage using the cursor.

5. Put a 10μF capacitor in parallel with R_L. Repeat step 4.

6. Repeat step 4 for C = 22μF and 47μF. Record V_m and V_{min} in Table 2.4 for each configuration from steps 4, 5, and 6, and compute V_r(rms), V_{dc}, and ripple factor RF.

Table 2.4: RF at various C when R_L = 1k

R_L=1kΩ; C (μf)	V_m	V_{min}	V_r	V_r(rms)	V_{dc}	Ripple Factor
No Capacitor						
10						
22						
47						

7. With C = 10μF, make an accurate sketch of the input and output waveforms for R_L = 470Ω, 10kΩ, 100kΩ. Record V_m and V_{min} in Table 2.5 and compute V_r, V_r(rms), V_{dc}, and ripple factor RF.

Table 2.5: RF at various R_L when C = 10uF

C= 10μf; R_L(Ω)	V_m	V_{min}	V_r	V_r(rms)	V_{dc}	Ripple Factor
470						
10k						
100k						

8. Sketch the waveforms for the two extreme filters, as you did for the half-wave rectifier. Record V_m and V_{min}. Enter these values in Table 2.3 Part 2 and compute V_r, V_r(rms), V_{dc}, and ripple factor RF.

LAB REPORT:

1. Discuss how the filter changed the shape of the output wave.
2. Compare measured RF with calculated RF in Equation (2.3) for each case of R_L and C.

3. Compare measured data with simulated data. How are they different?

ECE 311 EXPERIMENT 2 – CHECK LIST

1. Half-Wave Rectifier: Build circuit
    a. Vary Capacitor
        i. R_L = 1 kΩ.
        ii. Sketch input and output waveforms when capacitor is not connected and for C = 10μF, 22μF, 47μF.
        iii. Record V_m, V_{min}, V_r, V_{dc}, V_r(rms), and RF for each case.
    b. Vary Resistor
        i. C = 10μF.
        ii. Sketch input and output waveforms for R_L = 470Ω, 1kΩ, 10kΩ, 100kΩ.
        iii. Record V_m, V_{min}, V_r, V_{dc}, V_r(rms), and RF for each R_L.
    c. Sketch output waveforms for R_L=470Ω, C=10μF and for R_L=100kΩ, C=47μF.
2. Full-Wave Rectifier: Build circuit. Have instructor inspect circuit before starting function generator
    a. Vary Capacitor
        i. R_L = 1kΩ.
        ii. Sketch input and output waveforms when capacitor is not connected and for C = 10μF, 22μF, 47μF.
        iii. Record V_m, V_{min}, V_r, V_{dc}, V_r(rms), and RF for each case.
    b. Vary Resistor
        i. C = 10μF.
        ii. Sketch input and output waveforms for R_L = 470Ω, 1kΩ, 10kΩ, 100kΩ.
        iii. Record V_m, V_{min}, V_r, V_{dc}, V_r(rms), and RF for each R_L.
    c. Sketch output waveforms for R_L=470Ω, C=10μF and for R_L=100kΩ, C=47μF.

ELECTRONICS I
ECE 311

Experiment #3 – Power Supply Design

PURPOSE:

The purpose of this laboratory session is to have you use the knowledge gained in the diode experiments to design a dc power supply to meet certain specifications. **THIS LAB IS TO BE PERFORMED BY STUDENTS ACTING INDIVIDUALLY. DO YOUR DESIGN AND SIMULATIONS BEFORE THE LAB.**

PRE-LAB:

After Experiment 2, you should be familiar with the operation of DC power supplies and you should be able to apply this knowledge to the design of a power supply.

- **Design a DC power supply** that meets specifications detailed in the "Design Problem Statement". You can select either a 22μF or 47μF capacitor for your design.
- After completing your design, simulate your design using B2 Spice before coming to the lab. You should verify that your simulated power supply meets specifications.

For help with PRE-LAB calculations, a "Design Calculation" procedure is shown following the "Design Problem Statement".

EQUIPMENT:

Use components as your design requires. The 1N4004 diodes in plastic packages will conduct over 500mA before overheating. Your design will probably be less susceptible to burn-out if you use these diodes.

INTRODUCTION:

Experiment 2 introduced the fundamental aspects of rectifying a sinusoidal ac voltage to obtain a dc voltage. Experiment 2 further described the application of an RC filter to reduce ripple voltage, thereby obtaining a more nearly constant dc voltage for use in power supplies. In this experiment you will apply those concepts to design and build a dc power supply meeting specified operational requirements. This introduction summarizes many equations from Experiment 2 that will be useful for designing the power supply.

Figure 3.1 illustrates the essential nature of the dc waveform resulting from rectifying a sinusoidal ac voltage and applying an RC filter.

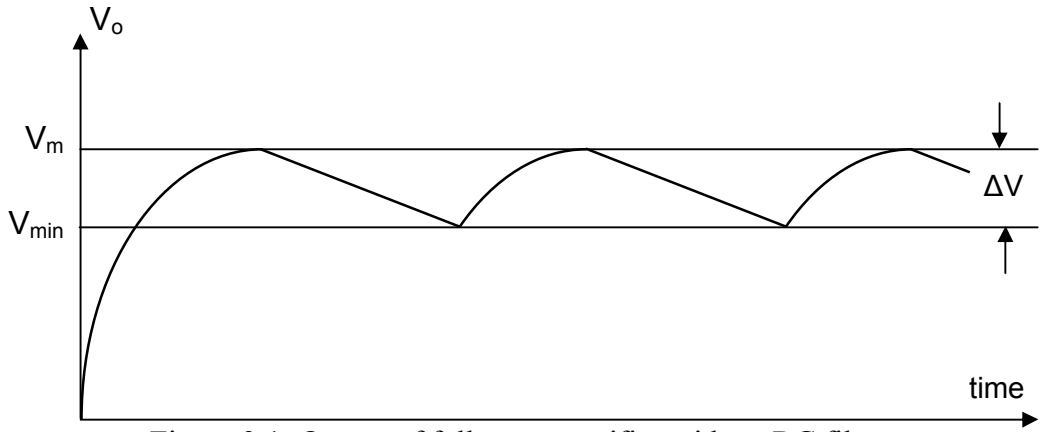


Figure 3.1: Output of full-wave rectifier with an RC filter

V_m = the maximum voltage of the rectified waveform

V_{min} = the minimum voltage of the rectified waveform

$\Delta V = V_m - V_{min}$

The cyclic variation in the waveform is called **ripple**, and we define the **ripple voltage V_r**:

$$V_r \equiv \Delta V = V_m - V_{min} \tag{3.1}$$

Recall the following from Experiment 2,

$$\frac{V_r}{V_m} = \frac{T}{R_L C} = \frac{1}{f_p R_L C} \tag{3.2}$$

from which we find

$$R_L C = \frac{V_m}{V_r f_p} \tag{3.3}$$

and

$$V_m = V_r \cdot f_p \cdot R_L \cdot C \tag{3.4}$$

where

R_L = load resistance

I_L = load current

C = filter capacitance

$T = 1/f_p$ = the period of the rectified wave.

For a half-wave rectifier, the ripple frequency f_p is the frequency of the input voltage. For a full-wave rectifier, f_p is twice the frequency of the input voltage. Thus, for a power supply using a transformer attached to the standard electrical system in the United States:

f_p = 60 Hz for a half-wave rectifier

f_p = 120 Hz for a full-wave rectifier

The root mean square (rms) ripple voltage, V_r(rms), **for a rectified sinusoid with filtered saw-tooth or triangular ripple** (such as in Figure 3.1) is given by

$$V_r(rms) = \frac{V_r}{2\sqrt{3}} = \frac{\left(V_m - V_{\min}\right)}{2\sqrt{3}} \tag{3.5}$$

Average or dc voltage $$V_{dc} = V_m - \frac{V_r}{2} = \frac{\left(V_m + V_{\min}\right)}{2} \tag{3.6}$$

Substituting Equation 3.4,

$$V_{dc} = V_r\left(f_p R_L C - \frac{1}{2}\right) = \frac{V_r}{2}\left(2 f_p R_L C - 1\right) \tag{3.6a}$$

Ripple Factor, RF $$RF = \frac{V_r(rms)}{V_{dc}} \tag{3.7}$$

NOTE: All voltages are those across the load resistor and not those at the output of the rectifier.

Substituting Equations (3.5) and (3.6a) into Equation (3.7), we find **for a rectified sinusoid with filtered saw-tooth or triangular ripple**

$$RF = \frac{1}{\sqrt{3}} \cdot \frac{1}{\left(2 f_p R_L C - 1\right)} \tag{3.7a}$$

DESIGN PROBLEM STATEMENT:

Solve Equation (3.7a) for R_L as a function of RF, f_p, and C. Show your solution and the resulting equation.

Design a bridge-type, full-wave rectified, dc power supply (as in Figure 2.5) using a filter capacitor (either 22µF or 47µF). The maximum output voltage V_m of the rectifier is to be at least $V_{in} - 2V_\gamma$, with a ripple factor, RF, less than 0.05. The voltage, V_{in}, is the voltage supplied to your rectifier circuit after the voltage drop across the resistor R_S.

Use the NI-ELVIS workstation to build and test the power supply. Use a $12V_{P\text{-}P}$, 60 Hz signal from the function generator as your input. Because of the power dissipation limits of the 1N4004 diodes, you should use a 1 kΩ resistor (R_S) in series with the function generator output to drive your rectifier circuit.

- Perform the calculations to design the circuit before simulating the circuit.
- **Simulate** and **measure** the voltage V_{in}.
- Over what range of load resistor values will your circuit meet your design specifications?

NOTE: You need to measure the function generator's output and the voltage after the 1kΩ series resistance in order to obtain the magnitude of V_{in}. Be sure to include the 1kΩ series resistor in your B2 Spice simulations. Be sure to see how the 1kΩ series resistor distorts the

input wave to the bridge rectifier circuit. **WHEN MEASURING THE OUTPUT VOLTAGE ACROSS THE LOAD RESISTOR, V_O, DO NOT USE SCOPE CH0 OR SCOPE CH1. INSTEAD, USE THE ANALOG INPUT CHANNEL, AI 0±.**

Design Calculation:

1. Solve Equation (3.7a) for R_L as a function of RF, f_p, and C.
2. Substitute into your equation the value of your capacitor (C=22μF or C=47μF), the ripple frequency f_p = 120Hz, and the Ripple Factor RF from the design statement.
3. Calculate R_L.

EXPERIMENT:

Build the power supply circuit you designed in the lab.

DO NOT BRING A POWER SUPPLY BUILT OUTSIDE OF CLASS TO THIS LAB, JUST BRING YOUR CALCULATIONS AND SIMULATIONS. YOU WILL BE WORKING INDIVIDUALLY ON THIS EXPERIMENT.

NOTE: After connecting your circuit, HAVE THE LAB INSTRUCTOR CHECK THE CIRCUIT FOR PROPER DIODE CONNECTIONS BEFORE YOU START THE FUNCTION GENERATOR. Also, REMEMBER TO MOVE BOTH THE POSITIVE AND NEGATIVE TERMINALS OF THE OSCILLOSCOPE WHEN MEASURING THE INPUT AND OUTPUT VOLTAGES.

Verify your design by measuring your circuit's input voltage, output voltage, and ripple factor. Let your lab instructor verify your results. Show your lab instructor your calculations and simulations showing the range of load resistors over which your design meets the specifications.

LAB REPORT:

You should come to the lab with your completed design calculations and B2 Spice simulations. You must show your design calculations, your simulations, and the results of your experimental circuit to the lab instructor before you leave the lab. After you have shown your circuit to your lab instructor, explain how the minimum value of R_L that satisfies your design would be affected if C were 1/2 of the value you used.

You will complete the Lab Summary in the lab. This summary will contain all of the measurements you make on your circuit, including the effects of changing the load resistor and filter capacitor.

Name:_____

ECE 311 Experiment 3- Lab Summary

TO BE TURNED-IN TO LAB INSTRUCTOR

Objective:

Design a bridge-type, full-wave rectifier, DC power supply with RF < 0.05. The supply will be driven by a function generator (FGEN) with a sinusoidal waveform of $12V_{P-P}$ at 60Hz. The maximum size for the filter capacitor is 47 μF. You must use a 1 kΩ resistor in series with the bridge to limit the current.

Get instructor to check circuit before starting the function generator.

Complete this form with data from your lab experiment — not from simulation — and turn it in along with your simulation output and all calculations.

Record the following data from the oscilloscope.

Peak input voltage (after the 1kΩ resistor), V_{in} = _____V.

Maximum output voltage, V_m = _____V.

Minimum output voltage, V_{min} = _____V.

Use the measured values above in the following calculations.

$V_r(rms) = (V_m - V_{min}) / (2\sqrt{3})$ = _____V(rms).

$V_{dc} = V_m - [(V_m - V_{min}) / 2]$ = _____V.

Ripple factor, $RF = V_r(rms) / V_{dc}$ = _____.

Answer the following two questions based on your design calculations.

What is the value of the smallest resistor R_L for which the filter will meet the design specifications? _____Ω?

If the maximum size of the filter capacitor were reduced by one-half, the smallest resistor for which the filter would meet the design specifications would be _____Ω.

ELECTRONICS I
ECE 311

Experiment #4 – Diode Clippers and Clampers

PURPOSE:

The purpose of this experiment is to study the use of diodes in wave-shaping (clipper) circuits and in level-shifting (clamper) circuits.

PRE-LAB:

The circuits to be tested and simulated are several clipper circuits and a clamper circuit. The clippers use a diode, resistor, and voltage source in 8 possible locations and orientations in a circuit. You should be familiar with the basic operation of clipper and clamper circuits as discussed in the text. You should be able to produce the output wave shapes shown for the circuits in Figures 4.1 through 4.7 below. You should simulate the circuits shown below in Figure 4.4(a), Figure 4.5(a), Figure 4.6 and Figure 4.7 using B2 Spice. (Assume R_L= 1kΩ, V_{SIN} = $8V_{P-P}$ and V_B = 2V)

You will need to compare your measured circuits with these specific circuit simulations.

EQUIPMENT:

For this experiment, you will need:

a. NI ELVIS Workstation

b. Diodes (IN4004 or equivalent)

c. Resistors and Capacitors

INTRODUCTION:

Clippers

It is frequently necessary to modify the shape of various waveforms for use in instrumentation, controls, computation, and communications. Wave shaping is often achieved by relatively simple combinations of diodes, resistors, and voltage sources. Such circuits are called clippers, limiters, amplitude selectors, or slicers. Clipper circuits are primarily used to prevent a waveform from exceeding a particular limit, either positive or negative. For example, one may need to limit a power supply's output voltage so it does not exceed +5 V. The most widely used wave shaping circuit is the rectifier, which you have previously studied.

Figure 4.1 shows a **positive clipper circuit**. As indicated, the output voltage has the entire positive half-cycles clipped off. The circuit works as follows: During the positive half-cycle of the input voltage, the diode turns on. For an ideal diode, the output voltage is zero. For an actual diode the output voltage is equal to $V\gamma$, the cut-in voltage of the diode.

During the negative half-cycle, the diode is reverse-biased and can be approximated by an open circuit. In many clippers, the load resistor, R_L, is much larger than the series resistor, R. In which case, essentially all of the negative half-cycle voltage appears at the output through

voltage-divider action. If R_L and R are comparable, then on the negative half-cycle, the output voltage would be given by

$$V_o = V_{p1} = V_p \bullet (R_L / (R_L + R)).$$

Since the first V_γ volts are used to begin conduction in the diode, the output signal is clipped near V_γ, rather than at 0V. If the diode polarity is reversed, the result is a negative clipper that removes the negative half cycle. In this case, the clipping levels occur near $-V_\gamma$.

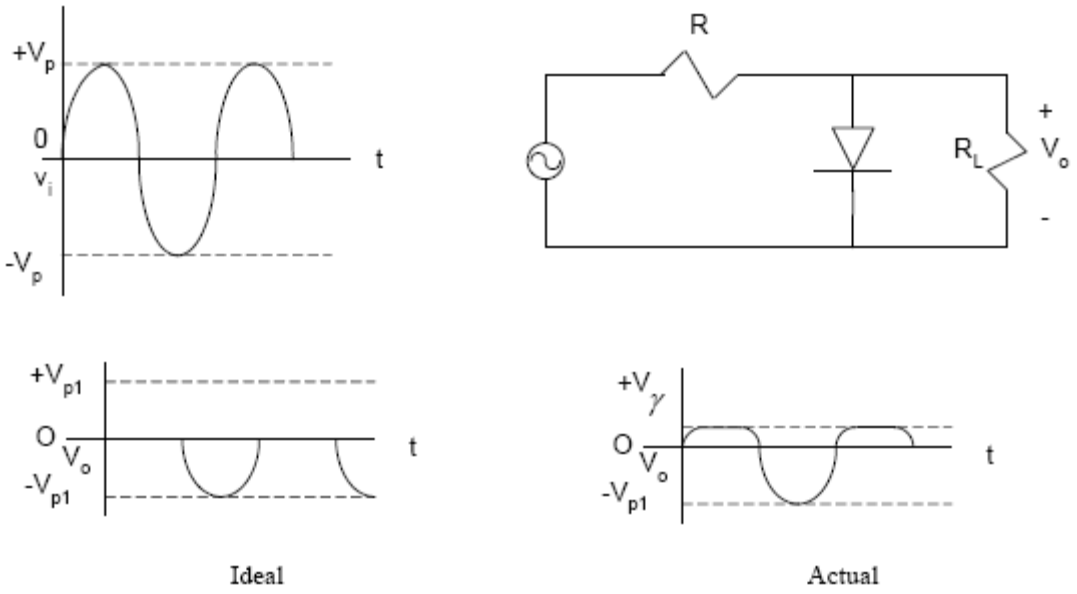
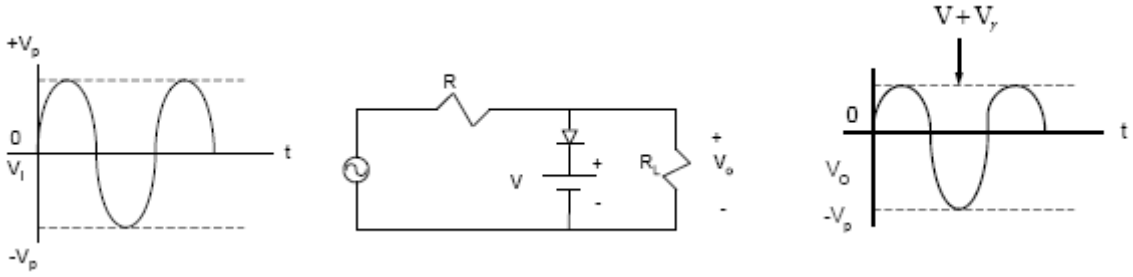


Figure 4.1: A positive clipper circuit: (a) Sinusoidal input to clipper circuit; (b) A positive clipper circuit; (c) Output of ideal positive clipper circuit; and (d) Output of actual positive clipper circuit

If a constant voltage source is placed in series with the diode shown in Figure 4.1(b), the result is a **biased positive clipper**, as shown in Figure 4.2(b). When the input voltage is greater than $V+V_\gamma$, the diode is forward biased and the output voltage is held at $(V+V_\gamma)$ volts (assuming $R_L >> R$). When the input voltage is less than $V+V_\gamma$, the diode becomes an open circuit and the circuit acts as a voltage divider. R_L is usually much greater than R, in which case, essentially all of the input voltage appears at the output. If both the diode and battery polarities are reversed, a biased negative clipper results, with the output clipped near $-(V+V_\gamma)$ volts.



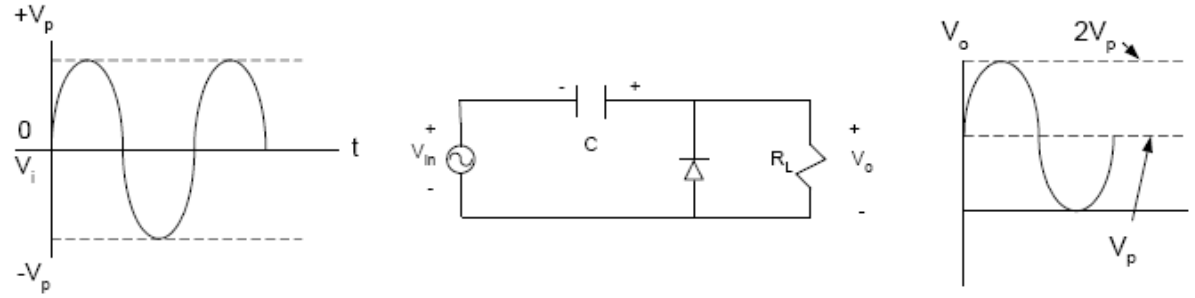
(a) (b) (c)

Figure 4.2: Biased positive clipper circuit: (a) Input to clipped circuit; (b) Biased positive clipper circuit; and (c) Output of positive clipper circuit

Clampers

In certain instances, it may be desirable to keep the output waveform essentially unchanged, but modify its dc level to some required value. This can be done by the use of diodes, resistors, capacitors, and voltage sources. Such circuits are known as clampers. For example, if the input voltage signal swings from -10V to +10V, a positive dc clamper can produce an output that keeps the signal wave shape intact but swings the voltage from 0V to +20V. TV receivers use a dc clamper to add a dc voltage to the video signal. Here the dc clamper is usually called a dc restorer.

In Figure 4.3(b) a positive dc clamper is shown. The clamper operates as follows: During the negative half-cycle of the input voltage, the diode turns on as illustrated in Figure 4.4(a). At the negative peak, the capacitor charges up to V_p with the polarity shown and the output voltage is zero. As the voltage grows beyond the negative peak, the diode shuts off as shown in Figure 4.4(b).



(a) (b) (c)

Figure 4.3: Positive dc clamper: (a) Sinusoidal input to positive dc clamper; (b) Positive dc clamper; and (c) Clamped sinusoidal output

The capacitor retains the voltage for a short time. The R_LC time constant is deliberately made much larger than the period, T, of the input signal. Hence, the capacitor remains almost fully charged during the entire off time of the diode. The capacitor thus acts like a battery of V_p volts and now only passes the ac signal, which rides on top of V_P. The output voltage signal, therefore, consists of the input signal riding on a dc voltage of $+V_p$ volts.

Since the diode drops V_γ volts when conducting, the capacitor voltage does not quite reach $+V_p$ volts. For this reason, the dc clamping is not perfect, and the negative peaks are at $-V_\gamma$ as shown in Figure 4.4(e).

When the polarity of the diode in Figure 4.3(b) is reversed, the polarity of the capacitor voltage reverses also, and the circuit becomes a negative dc clamper. Ideally, the output voltage consists of the input voltage riding on a dc voltage of $-V_p$ volts. If the diode is considered non-ideal, then the output will consist of the input signal riding on a dc voltage of $-(V_p-V_\gamma)$ volts, and the positive peaks will occur at V_γ volts.

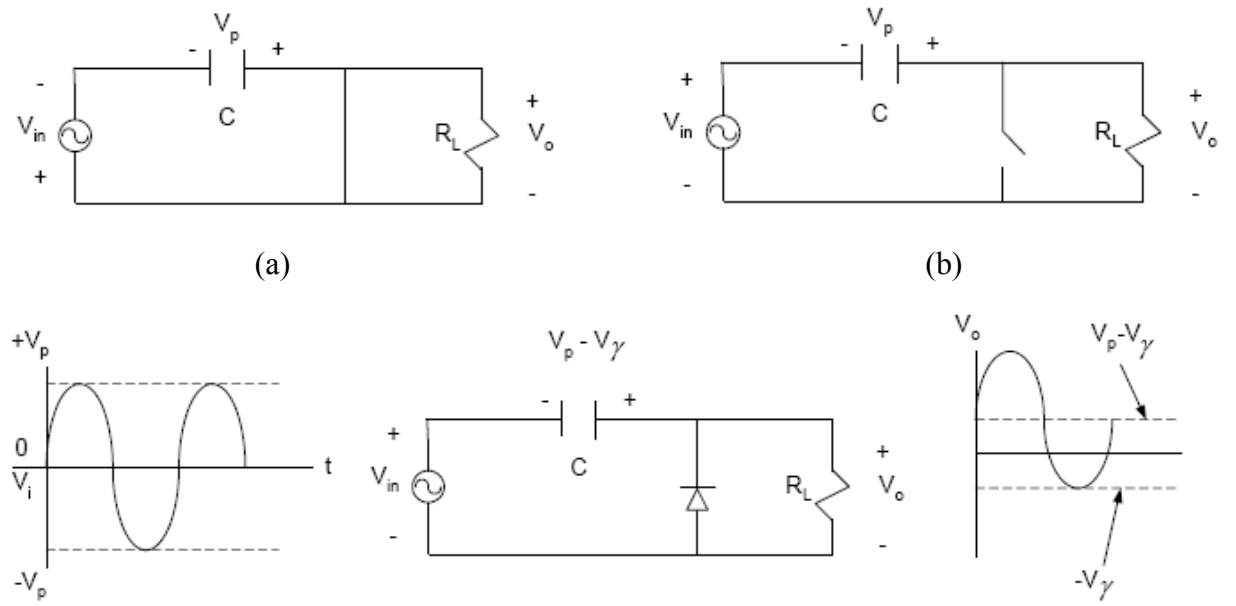


Figure 4.4: Positive clamping circuit operation

From the above discussions, it can be seen that when the diode points upward, a positive dc clamper results. When the diode points downward, the circuit is a negative dc clamper. The clamping value can be modified by putting a voltage source V_B in series with the diode, shifting the peak voltage to ($\pm V_\gamma \pm V_B$), depending on the sign of V_B and the polarity of the diode.

EXPERIMENT:

PART I: IDEAL CLIPPING CIRCUITS

NOTE: Set $V_{in} = 8V_{P\text{-}P}$ at 1kHz with 0V DC offset and R = 1kΩ for all circuits.
(FGEN setup was covered in Experiment #2, PART I: Half-Wave Rectifier, step 1.)

1. **Clipping Circuit 1**
   a. Connect the circuit shown in Figure 4.5(a) using the SUPPLY+ power supply as V_B. Set the SUPPLY+ voltage to 0V using the Variable Power Supply (VPS) front panel.
   b. Measure V_{in} and V_o using the oscilloscope. Make an accurate sketch of the input and output waveforms on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the input voltage at which clipping occurs.
   c. Set V_B (SUPPLY+) = 2V and repeat step b.

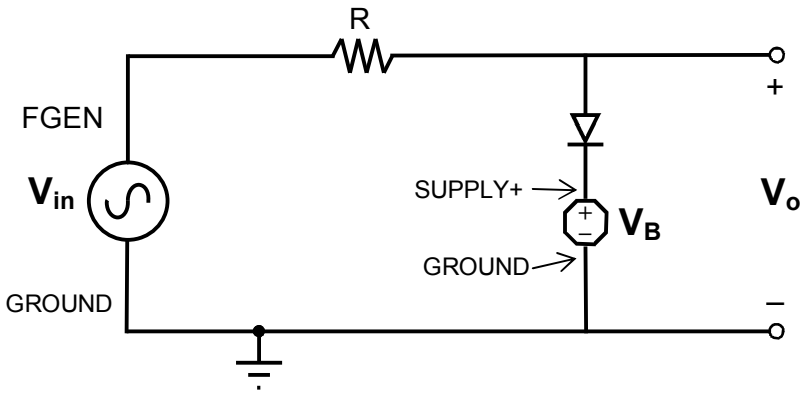


Figure 4.5(a): Clipping Circuit 1

2. Clipping Circuit 2

a. Connect the circuit shown in Figure 4.5(b) using the SUPPLY+ power supply as V_B. Set the SUPPLY+ voltage to 0V.

b. Measure V_{in} and V_o using the oscilloscope. Make an accurate sketch of the input and output waveforms on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the input voltage at which clipping occurs.

c. Set V_B (SUPPLY+) = 2V and repeat step b.

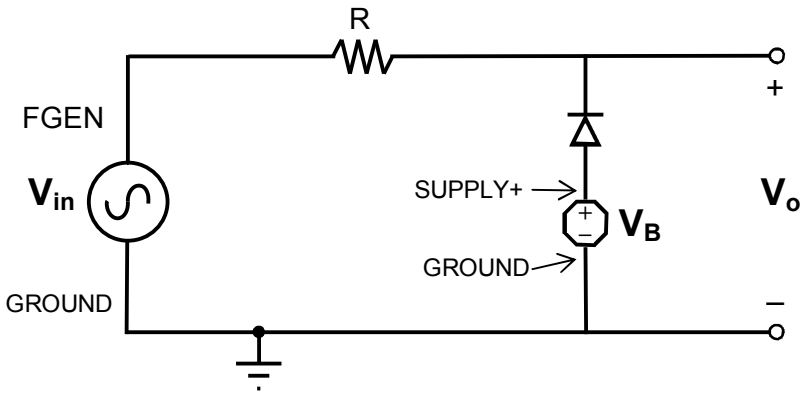


Figure 4.5(b): Clipping Circuit 2

3. Clipping Circuit 3

a. Connect the circuit shown in Figure 4.5(c) using the SUPPLY– power supply as $-V_B$. Set the SUPPLY– voltage to 0V.

b. Measure V_{in} and V_o using the oscilloscope. Make an accurate sketch of the input and output waveforms on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the input voltage at which clipping occurs.

c. Set V_B = 2V (SUPPLY– = -2V) and repeat step b.

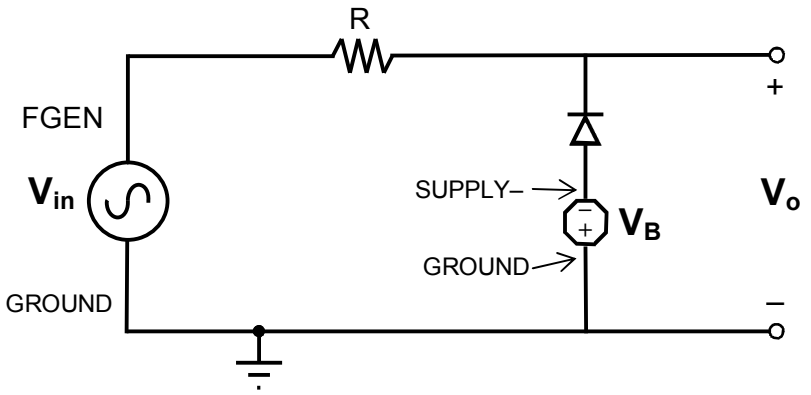


Figure 4.5(c): Clipping Circuit 3

4. Clipping Circuit 4

a. Connect the circuit shown in Figure 4.5(d) using the SUPPLY– power supply as $-V_B$. Set the SUPPLY– voltage to 0V.

b. Measure V_{in} and V_o using the oscilloscope. Make an accurate sketch of the input and output waveforms on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the input voltage at which clipping occurs.

c. Set V_B = 2V (SUPPLY– = -2V) and repeat step b.

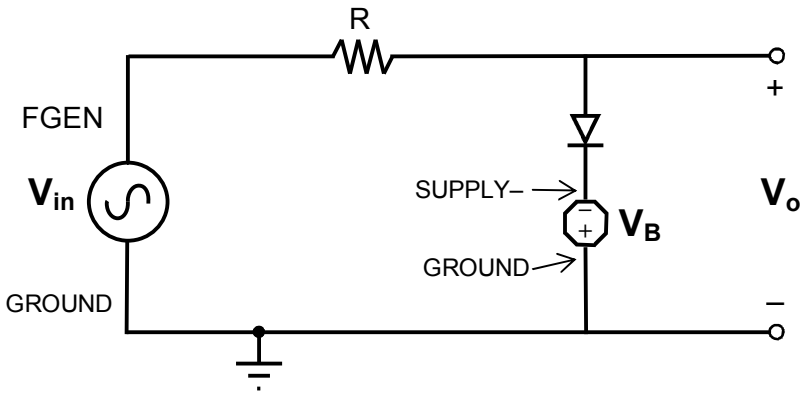


Figure 4.5(d): Clipping Circuit 4

PART II: SERIES-BIASED CLIPPING CIRCUITS

NOTE: **The Function Generator (FGEN) in the following circuits will provide both the V_{SIN} and V_B voltages. DO NOT USE SUPPLY+ OR SUPPLY– IN THE CIRCUITS**.

R = 1kΩ for all circuits.

1. Series-Biased Clipping Circuit 1

a. Connect the circuit shown in Figure 4.6(a) using the function generator to supply both V_{SIN} and V_B. Set the AMPLITUDE voltage to $8V_{P\text{-}P}$. Set the frequency to 1kHz. **Set the DC offset to 0V**.

b. Measure V_{SIN} and V_o using the oscilloscope using SCOPE CH0 and CH1, respectively. **Set the coupling on CH0 and CH1 to DC.** Click "Autoscale". Make an accurate sketch of V_{SIN} and V_o on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the value of V_{SIN} at which clipping occurs. Use the cursors as needed.

c. Set the DC offset of the function generator to 2V (**which is same as V_B=2V**) and repeat step b.

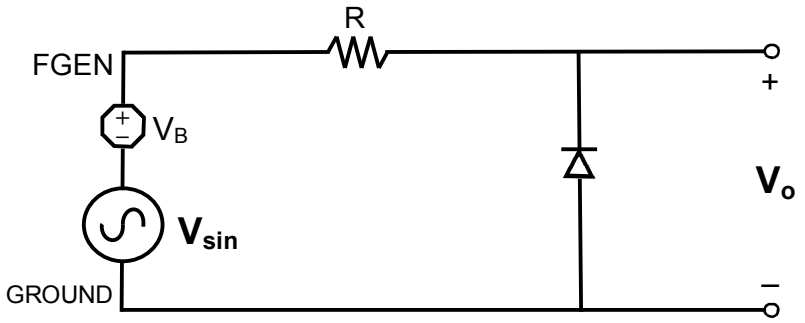


Figure 4.6(a): Series-Biased Clipping Circuit 1

2. Series-Biased Clipping Circuit 2

a. Connect the circuit shown in Figure 4.6(b) using the function generator to supply both V_{SIN} and V_B. Set the AMPLITUDE voltage to $8V_{P\text{-}P}$. Set the frequency to 1kHz. Set the DC offset to 0V.

b. Measure V_{SIN} and V_o using the oscilloscope using SCOPE CH0 and CH1, respectively. Set the coupling on CH0 and CH1 to DC. Click "Autoscale". Make an accurate sketch of V_{SIN} and V_o on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the value of V_{SIN} at which clipping occurs. Use the cursors as needed.

c. Set the DC offset of the function generator to -2V (V_B=2V) and repeat step b.

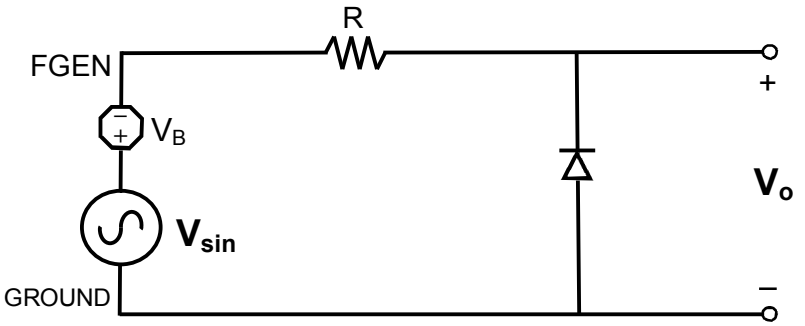


Figure 4.6(b): Series-Biased Clipping Circuit 2

3. Series-Biased Clipping Circuit 3

a. Connect the circuit shown in Figure 4.6(c) using the function generator to supply both V_{SIN} and V_B. Set the AMPLITUDE voltage to $8V_{P\text{-}P}$. Set the frequency to 1kHz. Set the DC offset to 0V.

b. Measure V_{SIN} and V_o using the oscilloscope using SCOPE CH0 and CH1, respectively. Set the coupling on CH0 and CH1 to DC. Click "Autoscale". Make an accurate sketch of V_{SIN} and V_o on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the value of V_{SIN} at which clipping occurs. Use the cursors as needed.

c. Set the DC offset of the function generator to 2V (V_B=2V)and repeat step b.

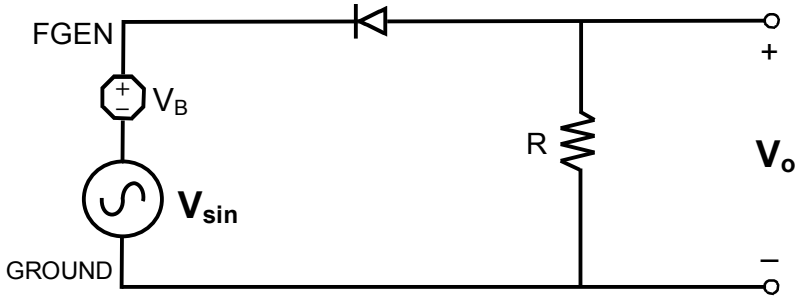


Figure 4.6(c): Series-Biased Clipping Circuit 3

4. Series-Biased Clipping Circuit 4

a. Connect the circuit shown in Figure 4.6(d) using the function generator to supply both V_{SIN} and V_B. Set the AMPLITUDE voltage to $8V_{P\text{-}P}$. Set the frequency to 1kHz. Set the DC offset to 0V.

b. Measure V_{SIN} and V_o using the oscilloscope using SCOPE CH0 and CH1, respectively. Set the coupling on CH0 and CH1 to DC. Make an accurate sketch of V_{SIN} and V_o on the same graph, making note of the peak values of V_o (minimum V_o and maximum V_o) and the value of V_{SIN} at which clipping occurs. Use the cursors as needed.

c. Set the DC offset of the function generator to -2V (V_B=2V) and repeat step b.

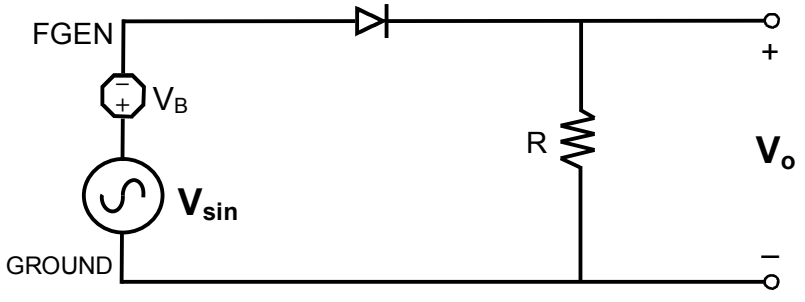


Figure 4.6(d): Series-Biased Clipping Circuit 4

PART III: PARALLEL-BIASED CLIPPER

It is possible to clip wave forms at two different voltages. The circuit shown in Figure 4.7 clips the waveform ideally at V_{B1} (SUPPLY+ = 2V) and V_{B2} (SUPPLY– = –2V). Make an accurate sketch of the input and output voltage waveforms for the circuit in Figure 4.7, noting the peaks of the output waveform and the input voltage at which clipping occurs. What would happen to the output wave shape if either V_{B1} or V_{B2} were changed continuously from 1V to 2V?

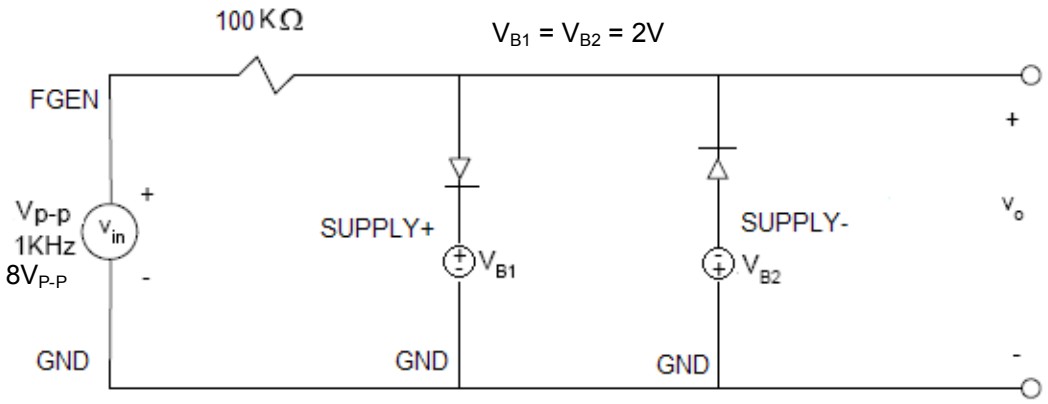


Figure 4.7: Parallel biased clipping circuit

PART IV: CLAMPERS

Build the circuit shown in Figure 4.8 and make an accurate sketch of the input and output waveforms for a $8V_{P-P}$ sine wave input voltage for each of the following conditions. **Each condition should be relative to the circuit as shown in Figure 4.8.** Be sure to record the peak values of both waveforms on your sketch. A capacitor larger than 22 µF will work in this circuit. **Set the coupling of both oscilloscope channels to DC.**

1. Circuit as shown with V_{DC} (or SUPPLY+) = 2 volt.
2. Reverse polarity of diode and of capacitor.
3. Diode as shown with the battery reversed. (**Replace SUPPLY+ with SUPPLY–**)
4. Reverse polarity of diode, of capacitor, and of battery. (**Replace SUPPLY+ with SUPPLY–**)
5. Continuously vary SUPPLY+/SUPPLY– to see how the waveform is shifted in each case.

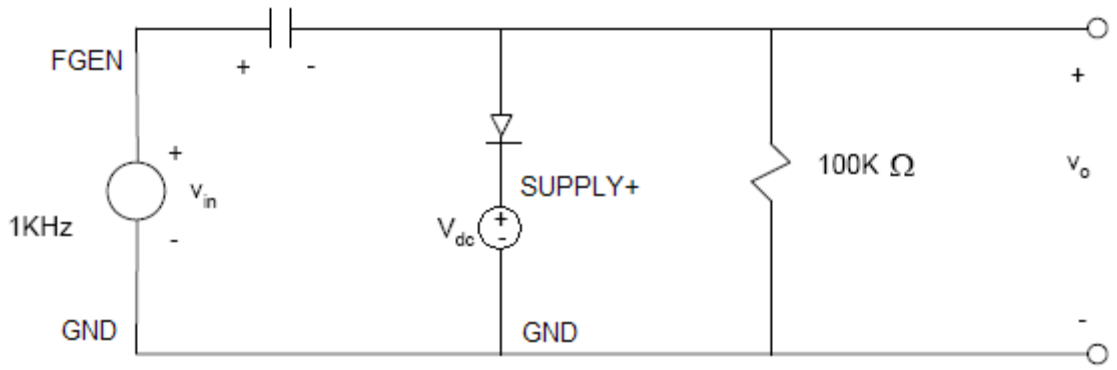


Figure 4.8: Clamping circuit

LAB REPORT:

1. Calculate the clipped voltage levels using circuit analysis for Fig. 4.5(a), 4.6(a), 4.7, and 4.8. Assume diode cut-in voltage $V_\gamma = 0.7V$ and neglect diode forward resistance r_f.
2. Make a table comparing the measured, calculated, and simulated clipped voltage levels for the circuits in Figures 4.5(a), 4.6(a), 4.7, and 4.8 (i.e. % difference).
3. Explain differences between measured, calculated, and simulated data. What are the assumptions made in calculated and simulated data? Are the assumptions valid? What are the advantages and disadvantages to three approaches?

ECE 311 EXPERIMENT 4 - CHECK LIST

PRE-LAB:

Simulate the circuits in Figures 4.5(a) ($V_B = 0$ & 2V), 4.6(a) ($V_B = 0$ & 2V), 4.7, and 4.8 (as shown).

EXPERIMENT:

1. Ideal Clipping Circuits — Build 4 circuits (Figures 4.5 a-d)
   a. **$V_{in} = 8V_{P-P}$, 1kHz, $V_B = 0$ & 2V**.
   b. Sketch the input and output waveforms.
   c. Record the voltage at which clipping occurs.
2. Series-Biased Clippers — Build 4 circuits (Figures 4.6 a-d)
   a. **$V_{sin} = 8V_{P-P}$, 1 kHz, $V_B = 0$ & 2V**.
   b. Sketch the input and output waveforms.
   c. Record the voltage at which clipping occurs.
3. Parallel-Biased Clipper — Build circuit (Figure 4.7)
   a. **$V_{in} = 8V_{P-P}$, 1kHz, V_{B1} and $V_{B2} = 2V$**.

b. Sketch the input and output waveforms.

c. Record the voltage at which clipping occurs.

4. Clamper — Build circuit (Figure 4.8)

   a. **V_{in} = 8V_{P-P}, 1kHz, V_{dc} = 2V**.

   b. Sketch the input and output waveforms.

ELECTRONICS I
ECE 311

Experiment #5 – Bipolar Junction Transistor Characteristics

PURPOSE:

This experiment is designed to introduce you to the bipolar junction transistor (BJT) characteristics that describe the common-emitter configuration of operation. Both the output and input characteristics of an npn silicon transistor will be measured.

PRE-LAB:

Read the sections in the text that describe the bipolar transistor operation and the transistor input and output characteristics. You should concentrate on understanding what is meant by a transistor input or output characteristic and the h-parameters in the small-signal transistor model.

Make sure to bring a piece of semi-log graph paper and a piece of linear graph paper (or you may plot the characteristics in Excel).

EQUIPMENT:

For the experiment you will require:

a) A silicon transistor (NPN) 2N3904 or 2N2222

b) A curve tracer

c) Semi-log graph paper

d) Linear graph paper

You will need a few sheets of notebook paper to record your readings. You should have your copy of the text with you while performing the experiment. The portion of the experiment devoted to measuring the h-parameters of the output characteristics is also covered in the portion of the Hameg manual in Appendix D.

INTRODUCTION:

A Bipolar Junction Transistor (BJT) is a three-terminal semiconductor device capable of amplifying an ac signal. The three terminals are called the emitter, the base, and the collector. The device is made up three "layers" of p-type and n-type semiconductor material. BJTs consist of a thin base layer (either P- or N-type) sandwiched between two layers of the opposite type material. Thus, BJTs are either NPN or PNP. They are somewhat like two interconnected, back-to-back diodes, with two diode junctions. The two types of BJTs are illustrated schematically in Figure 5.1.

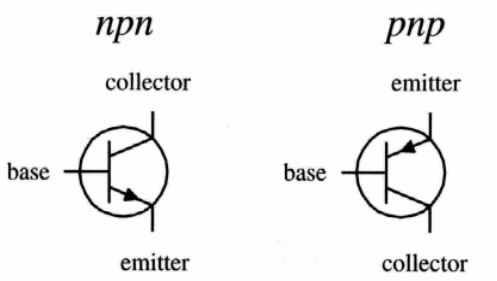


Figure 5.1 Schematic diagrams of general NPN and PNP transistors

BJTs are used to amplify current, using a small base current to control a large current between the collector and the emitter. This amplification is so important that one of the most noted parameters of transistors is the dc current gain, β, which is the ratio of collector current to base current: $I_C = \beta \cdot I_B$. In this lab you will measure several such parameters, discussed in paragraphs below.

The terminology for transistors includes a lot of subscripts. Generally, the subscripts mean:

C → Collector
E → Emitter
B → Base

So, V_{CE} is the collector-emitter voltage; V_{BE} is the base-emitter voltage; and I_B is the base current. One relationship to keep in mind is that I_C is always less than I_E. In fact, $I_E = I_C + I_B$.

Three configurations for connecting bipolar junction transistors are common-base, common-emitter, and common-collector. A large number of transistor circuits use the BJT connected in the common-emitter (CE) or grounded-emitter configuration. In the CE configuration, the input current and output voltage are the independent variables, while the input voltage and output current are the dependent variables.

In this experiment, the input and output characteristics of a transistor will be measured. **The input characteristics are plots of I_B versus V_{BE} at constant values of V_{CE}.** These characteristics will look like diode characteristics, particularly if the collector is shorted to the emitter and the emitter-base junction is forward biased. **Since the curve tracer is not able to extract the base current from the emitter current, the common-base input characteristics will be measured,** and I_E will be plotted as a function of V_{BE}. Since the characteristics will be measured under dc conditions, the dc currents and voltages will be specified.

The output characteristics, often called the collector characteristics, are plots of I_C versus V_{CE} at constant values of I_B and have 3 basic regions of transistor operation. These regions are the cutoff, the active, and the saturated regions. If a BJT transistor is to be used as an amplifier, it will usually be operated in the active region, where the relationship between the input current, I_B, and the output current, I_C, is nearly linear; that is, $I_C = \beta \cdot I_B$, where β is the gain. If the transistor is to be used in digital circuitry, it will be operated in the saturated or cutoff conditions and will only be in the active region when switching from one condition to the other.

In this experiment:

- You will measure and plot the input and output characteristics for the transistor used in the common-emitter mode and label the three regions of operation.

- You will determine the **dc current gain, h_{FE}**

  $h_{FE} = I_C/I_B = \beta_F$ (=BET on Hameg) with V_{CE} at a constant voltage (5.1)

  h_{FE} is also called $\boldsymbol{\beta_F}$, the forward dc current gain. It is often simply written as $\boldsymbol{\beta}$, and nominal values are quoted in transistor specifications. β is usually in the range of 10 to 500 (most often near 100) and is not constant, being affected by temperature and current.

- You will measure the four hybrid (h_{ij}) parameters:
  - the **small-signal current gain, h_{fe}**

    $h_{fe} = \Delta I_C/\Delta I_B \equiv \beta_o$ (=H21 on Hameg) with V_{CE} at a constant voltage (5.2)

    h_{fe} is also called $\boldsymbol{\beta_o}$, the small-signal current gain.
    Usually β_o is approximately equal β_F.

  - the **input resistance, h_{ie}**

    $h_{ie} = \Delta V_{BE}/\Delta I_B$ (=H11 on Hameg) with V_{CE} at a constant voltage (5.3)

    h_{ie} is sometimes written as $\boldsymbol{r_\pi}$

  - the **output conductance, h_{oe}**

    $h_{oe} = \Delta I_C/\Delta V_{CE}$ (=H22 on Hameg) with I_B at a constant current (5.4)

  - the **voltage feedback ratio, h_{re}**

    $h_{re} = \Delta V_{BE}/\Delta V_{CE}$ with I_B at a constant current (5.5)

These terms are defined in Figure 5.3 and Figure 5.7 as the slopes of the characteristics or the spacing between the characteristic curves.

As noted, $h_{ie} = r_\pi$. It is possible to approximate h_{ie} from the output characteristic using the relationship

$$h_{ie} = \frac{V_T}{I_{BQ}} = \frac{\beta V_T}{I_{CQ}} = \beta h_{ib} = r_\pi . \quad (5.6)$$

Here $V_T = kT/q = 26mV = 0.026V$ at room temperature, and I_{CQ} and I_{BQ} are I_C and I_B measured at the Q-point (the *quiescent point*). In most cases, the quiescent point is the operating point chosen to allow maximum symmetrical signal swing of the output waveform without clipping. When using the output characteristic to measure the value of h_{ie}, it will be necessary to decide which value of I_{CQ} or I_{BQ} is to be used.

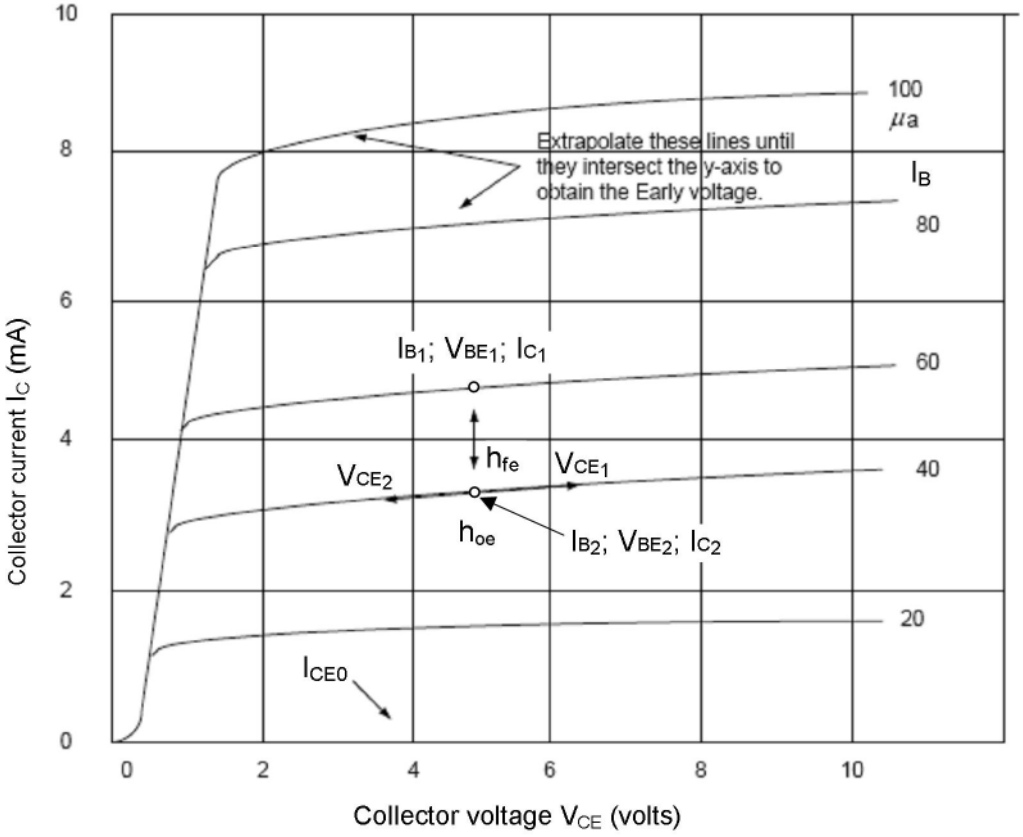


Figure 5.3: Bipolar transistor output characteristics

EXPERIMENT:

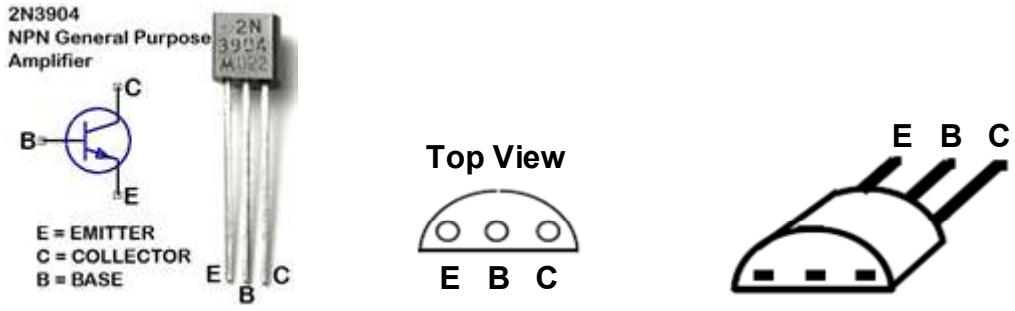


Figure 5.4: Pin digram for BJT 2N3904

PART I: OUTPUT CHARACTERISTICS

1. Linear Region

a. Figure 5.4 shows the pin configuration of the 2N3904 transistor. Use the curve tracer to obtain the output characteristics of the NPN transistor. Set menu to BIP-NPN (bipolar-NPN), V_{max} = 10 volts, I_{max} = 2mA, and P_{max} = 0.4W.

b. Adjust the curves using MIN and MAX functions until you get desired value base current I_B, as given as in Table 5.1.

c. Make a copy of the characteristic curves by hand. Your curves should be similar to those shown in Figure 5.3, which is a good representation of the output characteristics in the active region.

d. From the characteristics on the curve-tracer screen, record the values of I_{Bx}, I_{Cx} and V_{BEx} at corresponding V_{CE1} and V_{CE2}.Then, you can compute ΔI_C, ΔI_B, ΔV_C, h_{FE}, h_{fe} and h_{oe} in Table 5.1. Use the cursor control to help with your measurements. You can verify the calculated h_{xx} parameter by measuring them using the Hameg curve tracer, using the push button located below the LCD display.

NOTE: You will need to increase I_{max} and P_{max} as you increase I_B to more than 10μA (I_{max} = 20mA and P_{max} = 0.4W) and 100μA (I_{max} = 200mA and P_{max} = 4.0W).

e. Reverse the emitter and collector leads. Set V_{max} = 10 volts, I_{max} = 20mA, and P_{max} = 0.4W. Adjust MAX and MIN until five characteristics are displayed. Measure h_{FE} with the transistor operating in the inverse or inverse-active mode. Notice the decrease in the values of h_{FE}.

Table 5.1a: Measured Output Characteristics

N	I_B	Your value of I_B	V_{BE}	I_{C1} @ V_{CE}= 2.5V	I_{C2} @ V_{CE}= 5.0V	ΔI_{C2} = $I_{C2}(N)-I_{C2}(N-1)$	ΔI_B = $I_B(N)-I_B(N-1)$	ΔV_{BE} = $V_{BE}(N) - V_{BE}(N-1)$	h_{FE} @5V	h_{fe}
0	0.5μA									
1	5μA									
2	10μA									
3	50μA									
4	75μA									
5	100μA									
6	150μA									
7	200μA									

Table 5.1b: h_{oe} Calculations

N	$\Delta I_C = I_{C2} - I_{C1}$	$\Delta V_{CE} = V_{CE2} - V_{CE1}$	h_{oe}
0			
1			
2			
3			
4			
5			
6			
7			

2. Saturation Region

With V_{max} = 2V, P_{max} = 0.4W, and I_{max} = 20mA, obtain the output characteristics of the NPN transistor in *Forward Active Mode*. The value of V_{CE}(SAT) is the minimum collector voltage for which it is possible to define h_{FE} as being in the linear region of operation; which implies h_{FE} will be relatively constant for increasing V_{CE}. The minimum value of V_{CE}(SAT) is not clearly defined but is less than 0.5 V. Often this value is chosen to be 0.2 V in many texts. Notice that h_{FE} and h_{fe} are not clearly defined until the collector voltage exceeds V_{CE}(SAT). You should verify the current gain using the instrument function keys below the LCD screen.

3. Breakdown voltages and the Early voltage

The slope of the characteristic curves in the forward-active mode is due to an effect that was first analyzed by J. M. Early. The phenomenon is generally called the *Early effect.* When the curves are extrapolated to zero current, they meet at a point on the negative voltage axis, at $V_{CE} = -V_A$, as illustrated in Figure 5.5. The voltage V_A is a positive quantity called the **Early voltage**. Typical values of V_A are in the range $50 < V_A < 300V$.

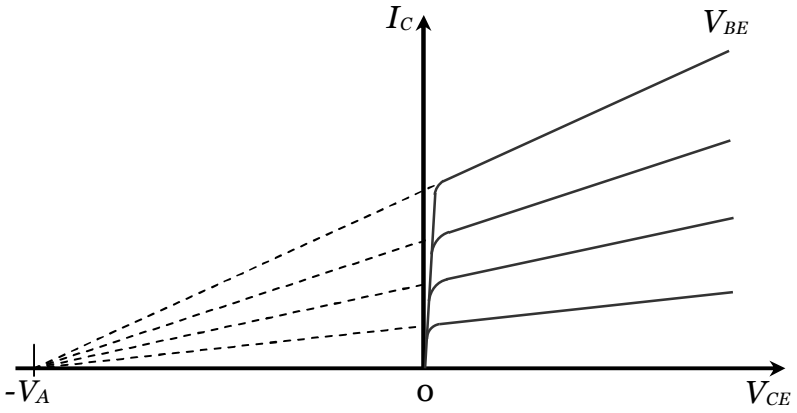


Figure 5.5: Current-Voltage characteristics for common-emitter circuit, illustrating Early voltage.

a. Set V_{max} to the highest scale, $P_{max} = 0.4W$, and $I_{max} = 2mA$. Copy this characteristic and obtain the collector breakdown voltage with the base injecting current. It may not be possible to see the breakdown voltage, depending on the maximum voltage scale capable of the curve tracer. Typical output characteristics are shown below in Figure 5.6.

b. Estimate the Early voltage by finding a linear fit ($y = mx + b$ or $I_C = mV_{CE} + b$) equation for one of the steepest output curves and solving for x when y=0 (i.e., solving for V_{CE} when I_C=0). (Early voltage for 2N3904 is often between 100V and 150V.)

Hint To Calculate Early Voltage:

- Adjust the MAX funtion until you get the top curve on the screen as almost a straight line.
- On this top curve, move the cursor far to the left on the straight-line section, and read the I_C and V_{CE} from the display; these are your I_{C1} and V_{CE1}.
- On the same curve, move the cursor far to the right on the straight-line section, and read the I_C and V_{CE} from the display; these are your I_{C2} and V_{CE2}.
- Calculate the slope m: $$m = \frac{(I_{C2} - I_{C1})}{(V_{CE2} - V_{CE1})}$$
- Solve for the I_C intercept, b: $b = I_{C1} - m \cdot V_{CE1}$
- Set $I_C = 0$ in the straight-line equation, and calculate the value of V_{CE} for the Early voltage V_A: $V_{CE}(0) = -b/m = -V_A$.

c. Insert the transistor in the inverted connection position as done in Part 1, Section 1.e. Use V_{MAX} = 10V and I_{MAX} = 2mA. Obtain the output characteristics and determine the emitter breakdown voltage. It should come aroud 6.0 to 8.0V.

d. Remove the base lead from the socket. Set the Menu to FET-NCH and measure the emitter breakdown voltage. Are the two emitter breakdown voltages the same?

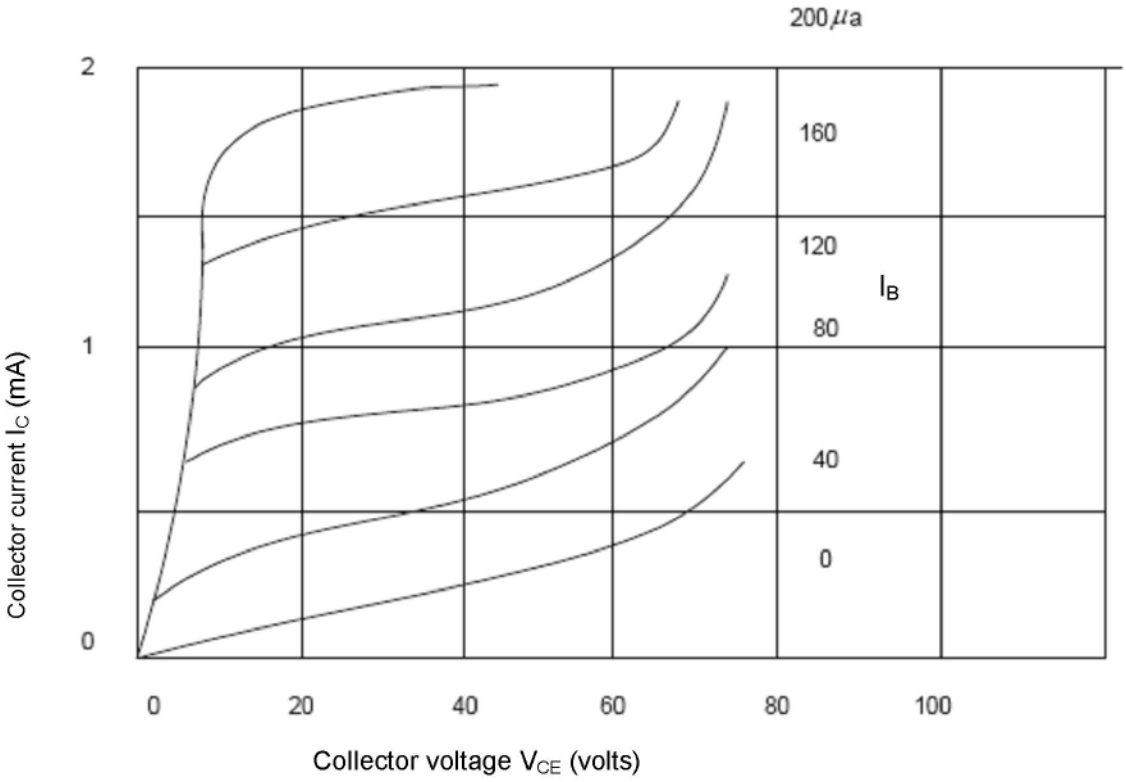


Figure 5.6: Output characteristics at high collector voltages

PART II: Input Characteristics

It is possible to use the curve tracer to obtain the input characteristics of the BJT operating in the common base (CB) configuration. You will measure the CB input characteristic and the value of h_{ib}. The value of h_{ie} can be found from

$$h_{ie} = h_{ib} \times (1 + \beta). \tag{5.7}$$

In order to make this measurement you will apply a sweep voltage to the base-emitter terminals and step the collector voltage through positive voltages.

a. Adjust the curve tracer for FET - NCH operation and reinsert the silicon NPN transistor into the test socket. Connect the base lead to the "C" terminal and the emitter lead to the "E" terminal. Use V_{MAX} = 2V and I_{MAX} = 2mA. The collector lead may be left "hanging" for the first part of this experiment. It is possible to use this configuration to measure part of the input characteristic of the emitter/base junction and to measure h_{ib}, as described in the next step (b). Then, by using the value of β found above, it is possible to calculate h_{ie}.

The type of characteristic that should appear on the screen is the one characteristic shown in Figure 5.7 and labeled as $V_{CE} = 0V$.

b. Plot the curve directly on linear graph paper and measure $h_{ib} = \Delta V_{EB} / \Delta_{IE} = h_{ie} / (\beta + 1)$. To calculate h_{ib}, choose two farthest points on the straight line region of the curve and record V_d (for V_{EB1} and V_{EB2}) and I_d (for I_{E1} and I_{E2}) from the display. In this measurement you are directly measuring I_E which is approximately equal to I_C. Use this value of h_{ib} and β (h_{fe}) (from Table 5.1) to calculate $h_{ie} = r_\pi$. In this case you will record $\Delta V_{BE} / \Delta I_E$ from your tabulated values.

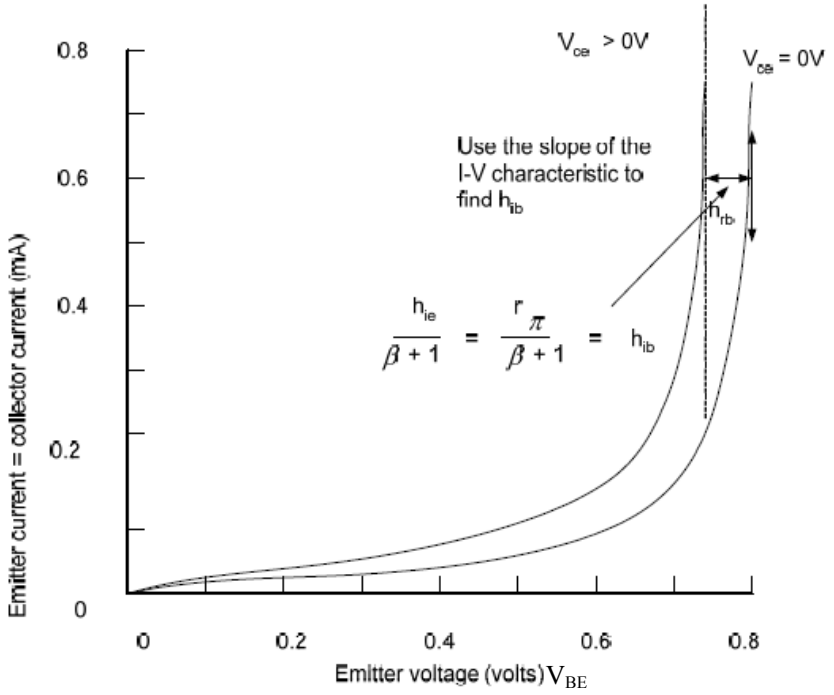


Figure 5.7: Transistor input characteristics

LAB REPORT:

Turn in a lab report containing the following:

1. An output characteristic of your transistor in the linear region of operation showing how to find h_{FE}, h_{fe}, and h_{oe}. Include relevant equations and recorded data.
2. An output characteristic of your transistor showing the saturation region and showing the range of values for $V_{CE}(SAT)$.
3. An input characteristic of your transistor showing how to find h_{ie}, h_{ib}, and h_{re}.
4. Plot h_{FE} and h_{fe} together on one graph of semi-log paper as a function of I_C.
5. Describe how h_{oe} varies with I_C.
6. Estimate the Early voltage from the high-voltage output characteristics.

ECE 311 EXPERIMENT 5 - CHECK LIST

1. Output Characteristics
    a. Measure output characteristics in the linear region.
        i. V_{MAX} = 10V, I_B/step = 0.5, 5, 50μA, adjust I_C to fit characteristics and complete Table 5.1a & b.
        ii. Copy transistor characteristics.
        iii. At V_{CE} = 2.5V and 5V record I_B, I_C, h_{FE}, h_{fe}, and h_{oe} for each I_B.
    b. Measure output characteristics in the saturation region
        i. V_{CE} = 0.5V.
        ii. Copy characteristics.
        iii. Determine V_{CE}(sat).
2. Input Characteristics
    a. Use curve tracer on DIODE. Connect base to "C" and emitter to "E". Leave collector hanging.
    b. V_{MAX} = 2V and I_{MAX} = 2mA: copy characteristic.
    c. Record several values of V_{BE} and I_E and determine the corresponding h_{ib} values.
    d. For each value of h_{ib}, determine a value for h_{ie}.

ELECTRONICS I
ECE 311

Experiment #6 – BJT Common-Emitter Circuit Bias

PURPOSE:

This experiment is intended to illustrate how a bipolar transistor circuit can be biased for the desired DC operation and how this DC condition can be kept stable if a transistor with a different $\beta = h_{fe}$ is substituted into the circuit. The biasing of the transistor establishes the Q-point of the transistor circuit. The Q-point determines the relationship between the input waveform shape and the output waveform shape. If the Q-point is not near the middle of the load line or if the input signal is too large, it is possible for the output waveform to become distorted. The CE amplifier with a bypassed emitter resistor (i.e., with a capacitor in parallel with the emitter resistor) will be used as the test circuit to show how the Q-point can be stabilized. It will be shown that moving the Q-point along the load line changes the shape of the output waveform.

PRE-LAB:

You should be familiar with the DC analysis techniques needed to find the Q-point of a common-emitter circuit. You should understand how varying the ratio of the two base resistors, R_1 and R_2, affect the base voltage and motion along the load line. Pre-Lab simulation can be divided in two parts: (i) DC sweep and (ii) Transient analysis.

(i) For the first part, you should perform DC sweep on the circuit shown in Figure 6.2 to find R_2 for the Q-point (V_{CE}=5V, I_C=1mA). Also, you should measure V_{CEQ}, I_{CQ} ($\approx I_{EQ}$) for R_2 = 1kΩ, 5kΩ, 15kΩ, and 25kΩ on the same circuit.

(ii) In the second part of the simulation, transient analyses should be performed in B2 Spice on the circuit shown in Figure 6.1 for R_2 = 1kΩ, 5kΩ, 15kΩ, and 25kΩ. Record the values of V_S and V_O. Assume $V_S = 0.02V_{P-P}$ at 1kHz, the transistor is a 2N3904, and all capacitors are greater than or equal to 10μF. For the second part, you may use source resistance R_S (=50Ω).

NOTE: Check the DEVICE IC box in transient setup. Preferred values for transient setup:

Start Time =3.00

Stop Time =3.01

Linearize Step=100u

Step Ceiling= 10u

EQUIPMENT:

- 2 NPN transistors with different β's, 2N3904, 2N2222, or equivalent. The transistors may have the same part number, as long as they have different β's.
- NI ELVIS II Workstation
- 1 Curve tracer
- 1 Decade resistance box
- Resistors and capacitors as noted in the schematic.

- Linear graph paper (or plotting software like Excel or MatLab)

INTRODUCTION:

Figure 6.1 shows a schematic diagram of a BJT common-emitter (CE) amplifier circuit. BJT transistor amplifiers are frequently used in the common-emitter configuration (CE), since this design gives both a high current gain (A_I) and a high voltage gain (A_V). This experiment explores the dc and ac characteristics of the common-emitter circuit and how changing the Q-point affects circuit performance.

- You will study the movement of the Q-point on the dc load line as R_2 is varied.
- You will see how input signals can lead to distorted output signals as the Q-point changes and/or as the magnitude of the input signal changes.
- You will learn how to create a Q-point that is almost independent of the β of the transistor that is being used.

The collector current (I_C) in a BJT circuit depends on the β of the transistor as well as the transistor's temperature and the other circuit elements. Good amplifier design requires choosing biasing resistors such that the quiescent (DC) collector current remains constant, regardless of whether a transistor with a different β is being used. Selecting the proper biasing network and resistors keeps the collector current relatively constant. A key element that stabilizes the circuit to changes in the transistor β is the emitter resistor, R_E.

Using a bias network with an emitter resistor is a good way to keep I_C relatively constant if the β or temperature changes. Any increase in I_C will cause the feedback voltage drop, V_{FB}, across R_E, to increase, thus lowering the base-emitter voltage, V_{BE}, and causing I_B to decrease. This is a negative feedback effect. Therefore, any changes in β will not cause I_C to change significantly, since I_B will scale with 1/β.

However, using an emitter resistor lowers the ac voltage gain of the circuit, since the ac component, i_c, must flow through R_E to ground. Therefore, R_E impedes i_c. The negative feedback voltage, V_{FB} across R_E "kills" the ac gain. To get around this undesired ac response and still maintain the excellent control of I_{CQ} that R_E provides, a capacitor is placed across R_E in order to short the ac current, i_c, around R_E to ground. This capacitor, $C_{E,}$ is called an emitter bypass capacitor and is generally large, 10μF or greater. This capacitor allows most of the ac current to flow around R_E directly to ground. Note that the dc current, I_{CQ}, still flows through $R_{E,}$ since the capacitor acts as an open circuit to dc, and the stabilizing effect of R_E is maintained. If R_E is physically removed from the circuit, the negative feedback effect on the gain is taken away. You will see in the next lab, Experiment #7, that without C_E, the voltage gain will be determined by the ratio of R_L and R_E, where R_L is the total ac load resistance, which the amplifier "sees". **An important principle of operation of feedback amplifiers is that the gain will be only dependent on resistor elements, not the active elements, if proper feedback is provided.**

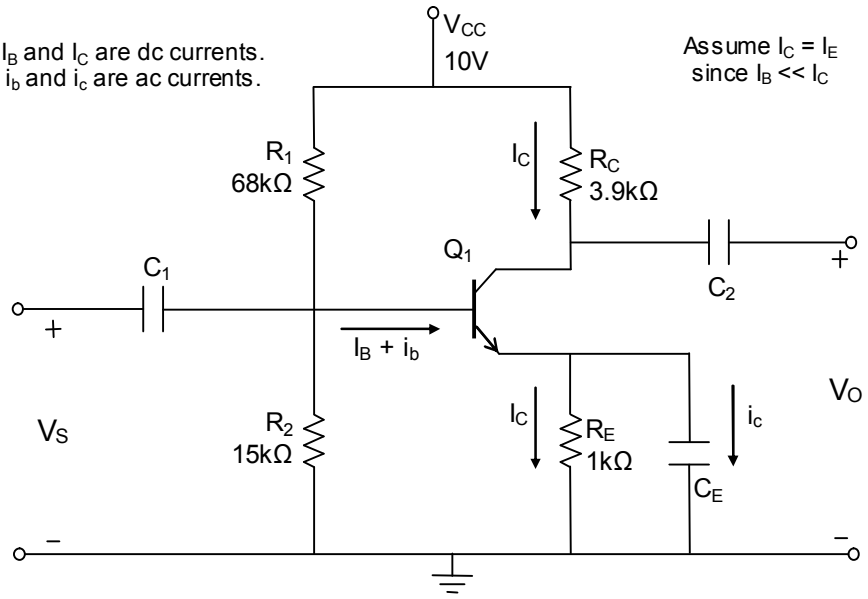


Figure 6.1: Common-emitter circuit with emitter bypass capacitor

EXPERIMENT:

PART I: Bias Measurements: The importance of the emitter resistor

1. Use the curve tracer function keys to measure the β of both transistors at a collector current of about 1.0 mA and V_{CE} of about 5 V, i.e. Q-point ≈ (5V, 1 mA). Please refer to Experiment 5, Part I step 1 for measuring β (h_{fe}) using the curve tracer. Make a hard copy of the transistor output characteristics of one of the transistors. **This is your primary transistor (use this transistor in Part II) for this experiment.** The other transistor is your secondary transistor. Each student will need at least one copy of the characteristics for the lab report. When copying the output characteristic, use scales of $I_{C,MAX} = 2$mA and $V_{CE,MAX} = 10$V. Use 5 steps of base current. Draw the DC load line on the copied output characteristics. Remember that the DC load line includes the emitter resistor. The AC load line has this resistor bypassed by the emitter capacitor.
2. Set up the circuit using the secondary transistor, as shown in Figure 6.2 without connecting the capacitors or the source voltage V_S. Use a decade box for R_2 and adjust it until V_{CE} is about 5V. R_2 will probably be close to 15 kΩ. Measure and record V_{E0}, or the emitter-to-ground voltage using the DMM. From this voltage measurement and the value of R_E, find $I_E \approx I_C$. Also measure and record V_{CE}.
3. Replace the secondary transistor with the primary transistor and measure V_{CE} and I_E. Compare your result with the secondary transistor for same R_2, you found in step 2.

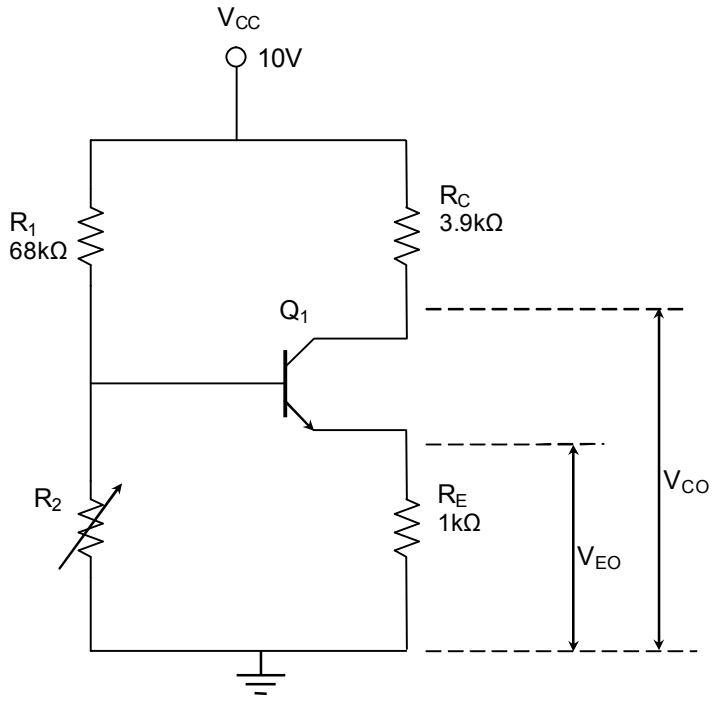


Figure 6.2: Common-emitter circuit

PART II: Q-point versus the value of the bias resistors

1. Keep the primary transistor in the circuit shown in Figure 6.2. Vary R_2 through the following values and measure and record the resulting Q-point (V_{CE} and I_C): 1kΩ, 2kΩ, 5kΩ, 8kΩ, 10kΩ, 15kΩ, 18kΩ, 20kΩ, 25kΩ, 30kΩ.

Table 6.1: Q-points measurement

R_2 (kΩ)	V_{C0}	V_{E0}	V_{CE}	I_E
1				
2				
5				
8				
15				
18				
20				
25				
30				

2. Plot the ten Q-points on your output charateristics.
3. In order to make the input signal, V_S, small enough to prevent distortion of the amplifier output, use the voltage divider circuit shown in Figure 6.3, where V_S is the voltage across

the 100Ω resistor. The voltage divider circuit shown in the Figure 6.3 divides input voltage from FGEN by 100:1.Thus, to get $V_S = 0.02V_{P\text{-}P}$, set FGEN to provide $2.0V_{P\text{-}P}$ as input to the voltage divider. **You may find, it is not possible to see the correct amplitude of V_S on the oscilloscope,** but if you are applying $2.0V_{P\text{-}P}$, 1kHz, at the input of the voltage divider shown in Figure 6.3, you can be assured that $V_S = 0.02V_{P\text{-}P}$, 1kHz.

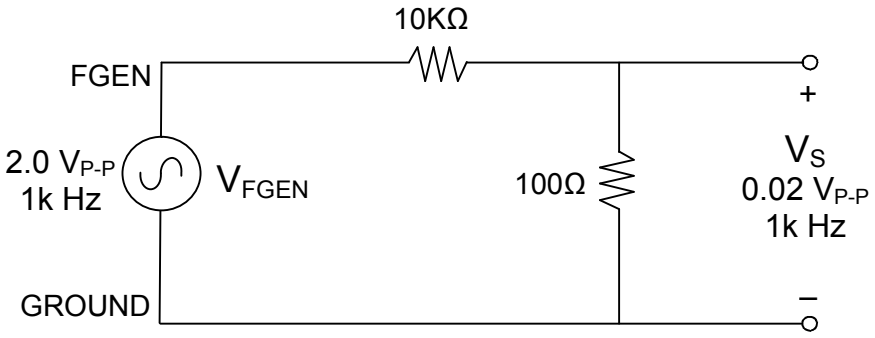


Figure 6.3: Voltage divider network to generate V_s

4. Set up the circuit in Figure 6.4 with the capacitors (use 22µF or 47µF) and voltage divider. To apply V_S to the input of the amplifier, set FGEN to $2.0V_{P\text{-}P}$, 1kHz, as input to the voltage divider, as discussed in step 3. Make sure your input is right by connecting the oscilloscope's CH0 to the function generator. **THIS IS A VERY COMMON ERROR, RESULTING IN WRONG OR UNEXPECTED OUTPUT.** If your input voltage is too large, you will clip the top and/or bottom of your output voltage. **DO NOT MAKE GAIN MEASUREMENTS ON A CLIPPED OR DISTORTED OUTPUT WAVEFORM!!!**

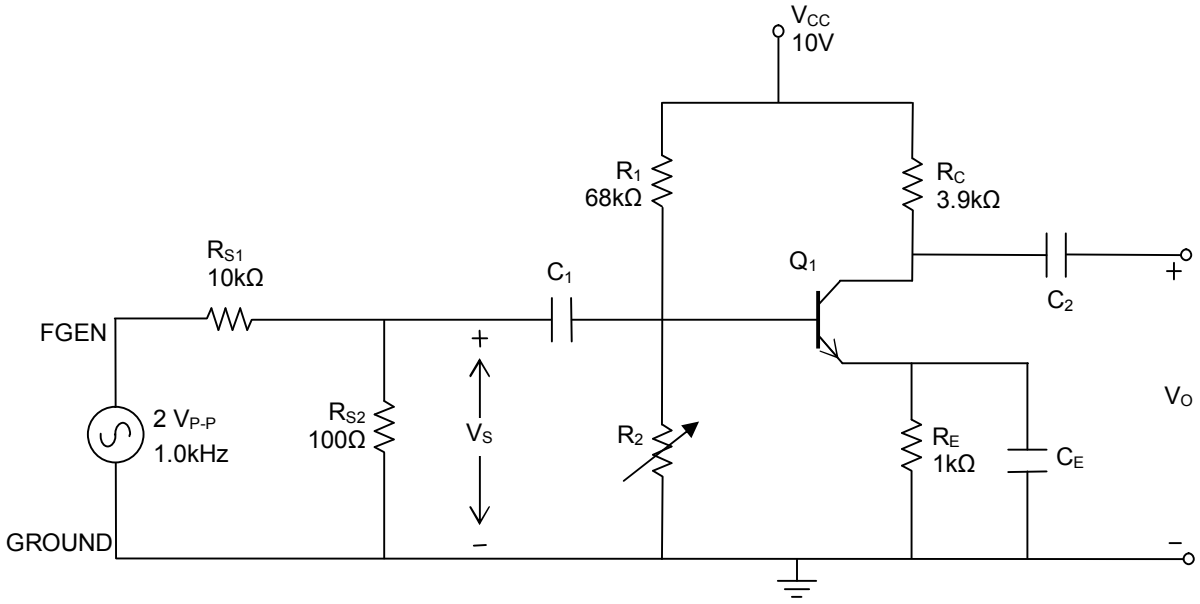


Figure 6.4: CE Amplifier with voltage divider ciruit

5. **Use SCOPE CH0 and CH1, with coupling set to "AC"**, to measure V_S and V_O. Because the voltage is small, V_S may appear too noisy to get an accurate measurement at

$0.02V_{P\text{-}P}$; that is why we rely on the voltage divider to ensure an accurate setting. Monitor the output waveform shape during all of the experiment. **Ensure that the negative leads of both channels are connected to ground during the whole experiment.**

Table 6.2: Amplified signal measurement

R_2 (kΩ)	V_O	Shape of the waveform (e.g. sinusoidal or distorted)
1		
2		
5		
8		
15		
18		
20		
25		
30		

NOTE: DO NOT MAKE GAIN MEASUREMENTS ON A CLIPPED OR DISTORTED OUTPUT WAVEFORM! YOU WILL NEED TO RECORD WHAT RESISTOR VALUES PRODUCE DISTORTED OUTPUTS.

6. Measure the input and output voltage and the shape of the output voltage as you vary R_2 from 1 kΩ to 30 kΩ, similar to step 1, and record on Table 6.2. Note all instances (values of R_2) of output waveform signal distortion. For each value of R_2, make an accurate plot of the input and output waveforms for a sinusoidal input. Note the distortion of your output signals. You will be asked to determine how variation in R_2 moved you along the load line.
7. You will now see how the amplifier responds to changes in the magnitude of the input signal. With R_2 set at 5 kΩ slowly increase the magnitude of the input voltage and note the changes in output waveform shape. Repeat this part of the experiment with R_2 = 15kΩ, 20kΩ. Determine how the output signal becomes distorted as the input signal increases for all three values of resistor R_2. Use the changes in the output waveform shapes to verify how the Q-point changes as R_2 changes. Be sure your output waveform shapes agree with your position on the load line. Remember that the CE amplifier has a 180º voltage phase reversal. That is, increases in the base current or base voltage result in increases in the collector current and decreases in the collector voltage.

LAB REPORT:

1. In Part I, compare the measured ΔI_C with the theoretical ΔI_C when you changed transistors.
2. How did the Q-point change with R_2? How did V_O change with R_2?

3. Compare measured results with B2 Spice simulation. Include B2 Spice output plots.
4. What range of R_2 drove the transistor into saturation? ... into cutoff?

ECE 311 EXPERIMENT 6 - CHECK LIST

1. **Bias Measurements**
   a. Measure and record the β of the two transistors at a Q-point = 5V, 1mA.
   b. Set-up the circuit without V_S connected.
   c. Measure and record V_{CE} and $I_E \approx I_C$
   d. Repeat 1c with the second transistor.
2. **Q-point vs. Bias Resistors**
   a. Mark the Q-point and draw the DC load line on the output characteristics of the primary transistor.
   b. Apply $V_S = 0.02V_{P\text{-}P}$ at 1 kHz.
   c. Use the oscilloscope to measure V_S (if possible) and V_O. Check for clipping of output on scope. **Note all instances of clipped voltages.**
   d. Repeat 2c, varying R_2 from 1kΩ to 30Ω.
   e. Sketch the V_S and V_O for R_2 = 2 kΩ, 5 kΩ, 10 kΩ, 15 kΩ, and 20 kΩ. Note how the output waveform becomes distorted.

ELECTRONICS I
ECE 311

Experiment #7 – BJT Common-Emitter Circuit Voltage Gain

PURPOSE:

This experiment is designed to illustrate how the voltage gain of a CE bipolar transistor circuit can be changed by changing the bias of the circuit and by changing the values of the resistors in the circuit.

- The role of the emitter bypass capacitor C_E will be illustrated.
- The base resistors determine the Q-point.
- The Q-point determines the relationship between the input wave shape and the output wave shape.
- If the Q-point is not near the middle of the load line, it is possible for the output wave shape to be distorted.
- If the magnitude of the input signal is too large, it is possible for the output wave shape to be distorted and/or clipped.

The gain of the CE amplifier is a function of the transistor used in the circuit, the values of the resistors, and the presence an emitter bypass capacitor. The CE amplifier with capacitor-by-passed emitter resistance shows good gain stability to variations in transistor β. This principle will be explored.

PRE-LAB:

- You should be familiar with the dc analysis techniques needed to find the Q-point of a common-emitter circuit.
- You should understand how varying the ratio of the two base resistors, R_1 and R_2, affect the base voltage and motion along the load line.
- You should know how R_E and R_C affect the Q-point.
- Perform B2 Spice simulations of the circuit shown in Figure 7.1, using the resistor values given and with extreme values of the resistors R_C (1kΩ & 20kΩ) and R_E (200 Ω and 10kΩ) , both with and without capacitor C_E. You should end up with ten different simulation graphs with the following resistor combinations:

  1. $R_C = 3.9k\Omega$ $R_E = 1k\Omega$ with and without C_E
  2. $R_C = 3.9k\Omega$ $R_E = 200\Omega$ with and without C_E
  3. $R_C = 3.9k\Omega$ $R_E = 10k\Omega$ with and without C_E
  4. $R_C = 1k\Omega$ $R_E = 1k\Omega$ with and without C_E
  5. $R_C = 20k\Omega$ $R_E = 1k\Omega$ with and without C_E

  Assume sinusoidal input $V_S = 0.02V_{P-P}$ at 1 kHz, the transistor is a 2N3904, and all capacitors are 22μF or greater.

NOTE: Check the DEVICE IC box in transient setup. Preferred values for transient setup:

Start Time =3.00
Stop Time =3.01
Linearize Step=100u
Step Ceiling= 10u

EQUIPMENT:

- 1 NPN transistor, either 2N3904, 2N2222, or equivalent
- 1 Curve tracer
- 1 Decade resistance box
- NI-ELVIS workstation
- Resistors and capacitors as noted in the schematic.
- Linear graph paper or graphing software (e.g., Excel or MatLab).

INTRODUCTION:

Figure 7.1 shows a schematic diagram of a BJT common-emitter (CE) amplifier circuit. BJT transistor amplifiers are frequently used in the common-emitter configuration (CE), since this design gives both a high current gain (A_I), and a high voltage gain (A_V). Experiment #6 explored the dc and ac characteristics of the common-emitter circuit and how changing the Q-point affected circuit performance. You will study how the voltage gain of the circuit is affected by changing the values of the emitter and collector resistors. You will see how input signals can lead to distorted output signals as the gain and Q-point change.

The collector current (I_C) in a BJT depends on the β of the transistor, the transistor temperature, and the circuit elements. **Good amplifier design requires choosing biasing resistors such that the quiescent (DC) collector current remains constant, regardless of transistor β or temperature.** Selecting the proper biasing network and resistors keeps the collector current and the voltage gain relatively constant. The key elements that stabilize the circuit to changes in the transistor β are the emitter resistor, R_E, and the values of the bias resistors, R_1 and R_2. To keep the high gain of the CE circuit, the emitter resistor is usually bypassed by a large capacitor. You will learn in ECE 321 that this capacitor affects the frequency response of the CE circuit, thus, the improvement in gain stability is obtained at a cost of reduced frequency response.

Using an emitter resistor lowers the ac voltage gain of the circuit, since the ac component, i_c, must flow through R_E to ground. Therefore, R_E impedes i_c; the negative feedback voltage across R_E (V_{FB}) "kills" the ac gain. To get around this undesired ac response and still maintain the excellent control of I_C that R_E provides, a capacitor is placed across R_E to short the ac current, i_c, around R_E to ground. This capacitor C_E is generally large, 10μF or greater, and allows most of the ac current through R_E to flow to ground. Note that the dc current, I_C, still flows through R_E since the capacitor acts as an open circuit to dc and the stabilizing effect of R_E is maintained. You will see in this lab that without C_E the voltage gain is determined by the ratio of R_L and R_E, where R_L is the total ac load resistance, which the amplifier "sees".

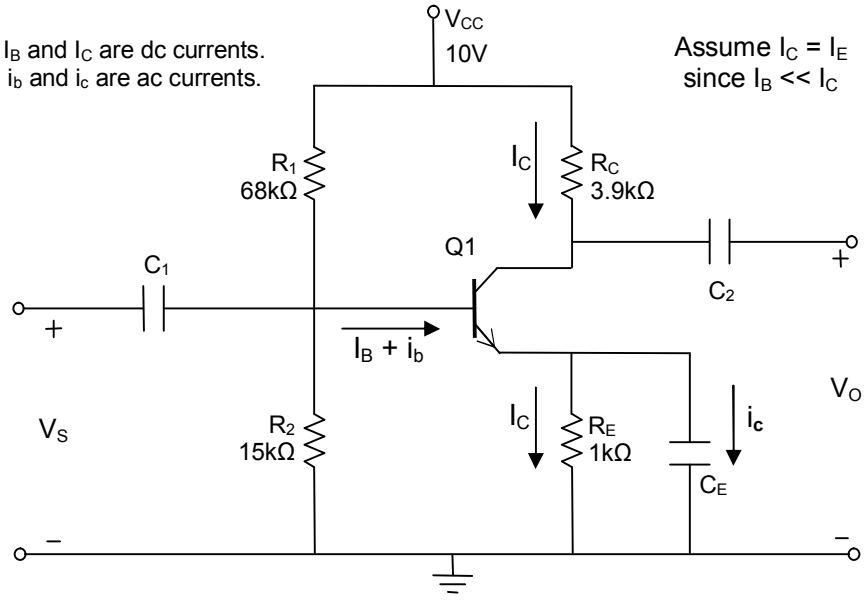


Figure 7.1: Common-emitter circuit with emitter bypass capacitor

EXPERIMENT:

PART I: Establishing the proper Q-point

1. Use the curve tracer and measure the β and V_{BE} of the transistor at a collector current of about 1.0mA and V_{CE} of about 5 V, i.e. Q-point = (5 V, 1 mA). Set I_{MAX} = 20 ma, V_{MAX} = 10V to obtain 5 steps on the curve tracer. Make a copy of the transistor characteristics. You can use either the 2N3904 or 2N2222 transistor for this part of the experiment.
2. Set up the circuit as shown in Figure 7.2 with V_{CC} = 10.0V. Use the DMM to measure V_{C0} and V_{E0}. You can calculate I_E (≈I_C) using V_{E0} and R_E. Then, obtain the Q-point (V_{CE} and I_C). Draw your load line and Q-point on your transistor characteristic.

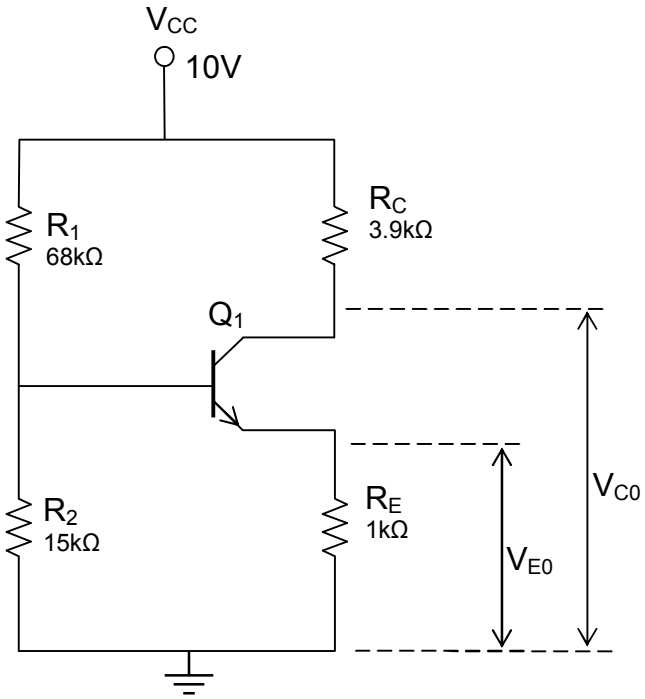


Figure 7.2: Common-emitter circuit for Q-point measurement.

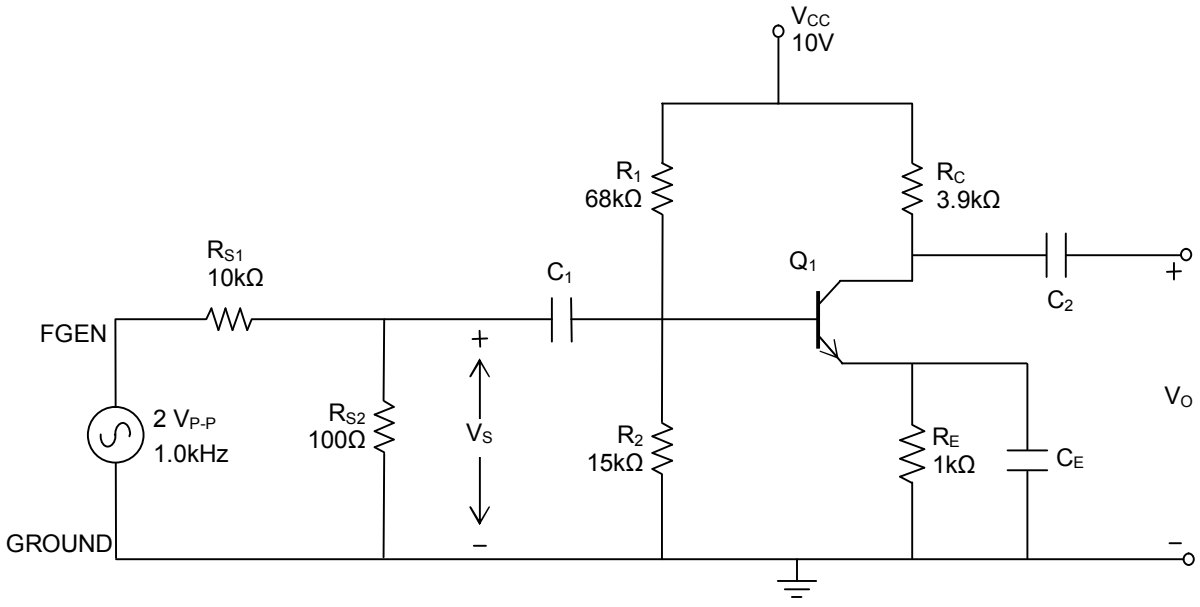


Figure 7.3: The common emitter circuit of Figure 7.2 with added capacitors and an input signal V_S provided by the function generator and the voltage divider, R_{S1} and R_{S2}.

PART II: AC Measurements

DO NOT MAKE VOLTAGE GAIN MEASUREMENTS ON A CLIPPED OR DISTORTED OUTPUT WAVEFORM!! IF YOUR OUTPUT WAVEFORM BECOMES DISTORTED, NOTE THIS CONDITION ON YOUR MEASUREMENTS AND ADJUST THE MAGNITUDE OF THE INPUT SIGNAL AND/OR RESISTORS TO OBTAIN AN UNDISTORTED OUTPUT.

1. Voltage gain versus the Collector Resistor R_C, with emitter bypass capacitor C_E

a. Build the circuit shown in Figure 7.3 for ac measurements by adding the capacitors (use 22μF or 47μF) and sinusoidal input of $2V_{P-P}$ 1kHz applied to the voltage divider circuit, R_{S1} and R_{S2}. Measure V_O and V_S with the oscilloscope. **It is possible that you will not be able to measure the exact value of V_S (i.e. 20mV) due to noise. Therefore, you should make sure that your FGEN output and R_{S1} and R_{S2} are correct as shown in Figure 7.3.** If there is no distortion in the output wave shape, continue with the experiment. If the output wave shape is distorted, either reduce the magnitude of the input signal or adjust your Q-point. **Use SCOPE CH0 and CH1, and set the coupling of both channels to "AC". Enable "Autoscale" to improve accuracy.**

b. Replace R_C with the resistance decade box and set the resistace decade box to 3.9kΩ.

c. Use the oscilloscope to measure V_O; it should have same value as in step a. Leave the oscilloscope connected to V_O throughout this experiment and monitor the output wave shape.

d. Measure V_O while R_C is varied from 1kΩ to 20kΩ using the resistance decade box. During this measurement the shape of V_O and its magnitude may change drastically for some values of R_C. Complete Table 7.1 with values of V_O. **If, at any time, your output wave shape becomes seriously distorted, note this on your table and do not take V_O measurement.** Also, sketch the output wave shapes.

e. Determine the voltage gain, $A_V = V_O/V_S$, as a function of R_C and plot your results.

Table 7.1: V_O vs R_C

R_C (Ω)	With C_E			Without C_E		
	$V_{O\text{-}PP}$	Output waveform shape	$A_V = \frac{V_{O\text{-}PP}}{V_{S\text{-}PP}}$	$V_{O\text{-}PP}$	Output waveform shape	$A_V = \frac{V_{O\text{-}PP}}{V_{S\text{-}PP}}$
1k						
3k						
6k						
9k						
15k						
20k						

2. Voltage gain versus the value of the Collector Resistor R_C, without C_E

a. Remove the emitter bypass capacitor, C_E.

b. Repeat all of Part II, section 1, and record your measurements in Table 7.1 columns for "Without C_E". If, at any time, your output wave shape becomes seriously distorted, note this on your plots and record the output wave shapes. For values of R_C that are 2kΩ less than the value that produced distortion, increase the magnitude of the input signal until distortion appears in the output signal. Note the magnitude of the input signal that causes significant distortion in the output signal.

3. Voltage gain versus the value of the Emitter Resistor with C_E in place

a. Set R_C = 3.9 kΩ using a fixed resistor instead of the resistance decade box. Connect the emitter bypass capacitor C_E as shown Figure 7.3.

b. Replace R_E with the resistance decade box and set the resistace decade box to 1kΩ.

c. With R_C = 3.9 kΩ and C_E connected, measure V_O and V_S for R_E values from 200 Ω and 10kΩ. Record your results in Table 7.2. **If at any time your output wave shape becomes seriously distorted, note this on your table and do not take V_O measurements. Sketch the waveforms.**

d. Determine the voltage gain, $A_V = V_O/V_S$, for all values of R_E and plot your results. Take extra data points when the gain is changing rapidly or when the output wave shape is becoming distorted.

e. Record the values of emitter resistor that lead to significant output waveshape distortion.

Table 7.2: V_O vs R_C

R_E (Ω)	With C_E			Without C_E		
	$V_{O\text{-}PP}$	Output waveform shape	$A_V = \frac{V_{O\text{-}PP}}{V_{S\text{-}PP}}$	$V_{O\text{-}PP}$	Output waveform shape	$A_V = \frac{V_{O\text{-}PP}}{V_{S\text{-}PP}}$
200						
500						
1k						
3k						
6k						
8k						
10k						

4. Voltage gain versus the value of the Emitter Resistor, without C_E

a. Remove the emitter bypass capacitor, C_E.

b. Repeat all of Part II, section 3, without C_E and record results in Table 7.2 columns for "Without C_E".

5. Frequency Response.

Set R_E to 1kΩ and connect C_E as shown in Figure 7.3. Vary the input signal frequency from 10 Hz to 50k Hz and use the oscilloscope to see how the magnitude of the output signal varies. Record your result in Table 7.3. You will study frequency response in ECE 321.

Table 7.3: Frequency response of $V_{O\text{-}PP}$ and voltage gain A_V

Frequency (Hz)	10	100	1k	10k	25k	50k
$\mathbf{V_{O\text{-}PP}}$						
$\mathbf{A_V}$						

6. Save this transistor. Keep this transistor safe and use its β and V_{BE} for design calculations in the pre-lab for Experiments 8 and 9. Use this transistor in Experiments 8 and 9.

LAB REPORT:

A. Make four plots of the voltage gains of your circuit as a function of the values of R_E and R_C with and without the emitter bypass capacitor.

B. Compare your experimental data with the simulations of this circuit. How accurate were the circuit simulations? How did the voltage gains change as R_E and R_C were changed.

C. Comment on the variation in voltage gain with and without the bypass capacitor in the circuit. What sacrifices are made to ensure a stable voltage gain when the capacitor was in the circuit or was out of the circuit?

D. In your lab report, you should write a conclusion to this experiment explaining how changing R_C and R_E changed the gains of your circuit, with and without the emitter bypass capacitor.

ECE 311 EXPERIMENT 7 - CHECK LIST

I. Establish Q-point.

   A. Measure β at Q-point = 5V, 1mA. Copy transistor characteristics, mark Q-point, and draw load line.

   B. Set-up circuit without V_S and with R_C = 3.9kΩ and R_E = 1kΩ. Measure and record I_C and V_{CE}.

II. Voltage Gain, A_V. Set-up circuit in Figure 7.3.

   A. A_V vs. R_C, with C_E

      i. Monitor V_O on oscilloscope.

      ii. Vary R_C from 1kΩ to 20kΩ.

      iii. Measure V_O and V_S on the oscilloscope for each R_C. Do not record A_V for distorted waves, but note which values of R_C cause distortion.

         a. Put V_O, V_S, and A_V in a table.

      iv. Plot A_V vs. R_C. Specify regions of distortion as cutoff or saturation.

B. Repeat all of Part II, A. with C_E removed.

C. A_V vs. R_E, with C_E

   i. Monitor V_O on oscilloscope.

   ii. Vary R_E from 200 Ω to 10 kΩ.

   iii. Measure V_O and V_S for each R_E. Do not record A_V for distorted waves, but note which values of R_E cause distortion.

      a. Put V_O, V_S, and A_V in a table.

   iv. Plot A_V vs. R_E. Specify regions of distortion as cutoff or saturation.

D. Repeat all of Part II, C, with C_E removed.

ELECTRONICS I
ECE 311

Experiment #8 – BJT Common-Emitter Design I

PURPOSE:

The purpose of this laboratory is to enable you to apply the knowledge you have gained in class and in the lab concerning the BJT common-emitter (CE) amplifiers to design a BJT CE amplifier to meet certain design specifications. You will determine how the voltage gain is affected by changes in the output resistance. You will learn how to measure the input and output impedances of CE circuits.

PRE-LAB:

1. You need to know how to obtain a stable Q-point for a CE amplifier. You need to know how to calculate voltage gain for a CE amplifier. **You will need to design your amplifier before coming to the lab. If you have not designed your amplifiers before coming to the lab, you will not be able to complete this experiment in the time allotted.**
2. **You will need to know the β of your transistor and the value of V_{BE} before you begin the design of your circuit. You should have measured this in Experiment 7. (TO INSTRUCTORS, ENSURE THAT THIS TASK IS ACCOMPLISHED IN THE PREVIOUS LAB).**
3. Design the CE amplifier shown in Figure 8.1 to drive a 4.7kΩ load using an npn silicon transistor and a power supply voltage of V_{CC} = 10 V and $R_L = R_C$. The voltage gain of your circuit is to be A_V = -10. You should have already used the curve tracer to determine the β and V_{BE} of the transistor you have selected. Your design should include the specification of R_1, R_2, R_C, R_E, R_O, V_{CEQ}, I_{CQ}, h_{ie}, and h_{ib}. **In this part of the experiment, C_E is not used.** You must design your amplifier for maximum symmetrical output swing. **See Design Procedure following this section for the equations needed for your design.** Assume that all coupling capacitors are large enough to pass your signal at 1kHz (i.e. 22μF or greater). Assume $R_C = R_L$ for your first design.
4. Simulate your circuit design using B2 Spice transient analysis, as in prior experiments. Note that you may need to modify some resistor values so that B2 Spice gives the correct output and gain. Measure the voltage gain. Let $V_S = 0.02V_{P\text{-}P}$.
5. Repeat the measurements of the voltage gain for $R_L = 0.1R_C$, and $R_L = 10R_C$, keeping R_C = 4.7kΩ, and tabulate your results.
6. **Remember to use standard resistor values in your final design. A table of standard resistor values is found in this lab manual.**

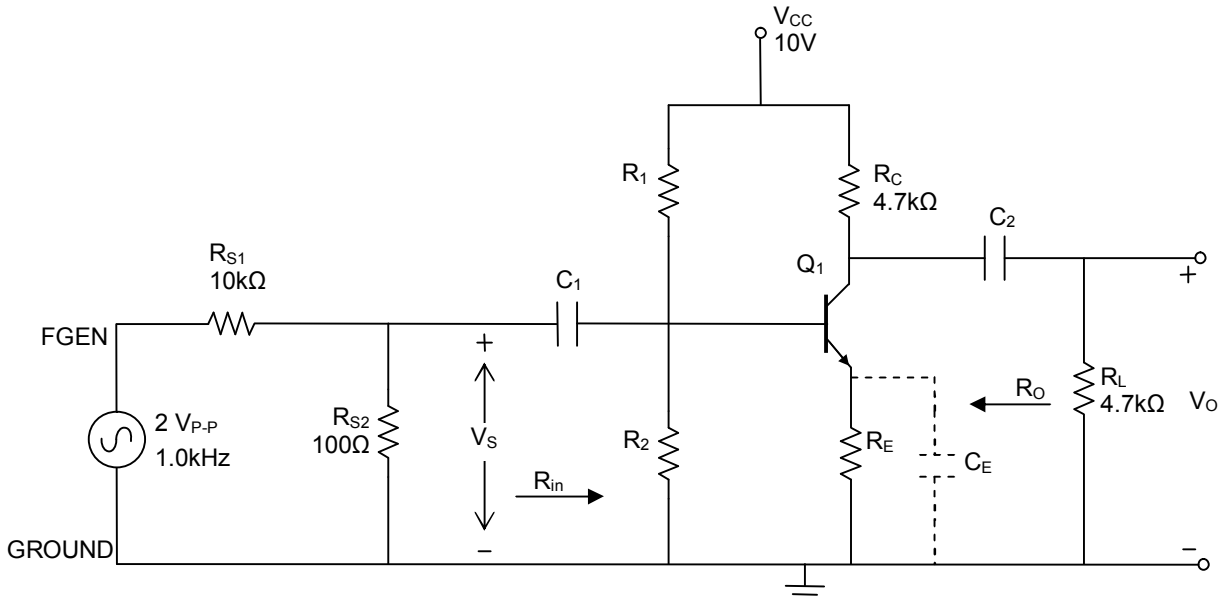


Figure 8.1: BJT amplifier design

<u>DESIGN PROCEDURE:</u> When an emitter bypass capacitor C_E is not used

- Estimate R_E from $A_V = -\left(R_L \| R_C\right) / \left(h_{ib} + R_E\right)$ for the amplifier in which emitter resistor R_E is not bypassed by a capacitor C_E.
  Recognizing that h_{ib} is usually much less than R_E, we can assume $(h_{ib} + R_E) \approx R_E$ for the non-bypassed amplifier.

- Calculate R_{ac} and R_{dc}

  $R_{ac} = \left(R_C \| R_L\right) + R_E$ if R_E is not bypassed.

  $R_{dc} = R_C + R_E$ whether R_E is bypassed or not.

- Find I_{CQ} and V_{CEQ}

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}}$$

$$V_{CEQ} = I_{CQ} \cdot R_{ac}$$

- Find h_{ie} (= r_π) and h_{ib}

$$h_{ie} = \frac{V_T}{I_{BQ}} = \beta \frac{V_T}{I_{CQ}} = \beta\, h_{ib} = r_\pi$$

where V_T (thermal voltage) = 0.026V.

- Subtract the value of h_{ib} from the value of R_E found above to obtain the actual value of R_E that is needed in the non-bypassed amplifier. Choose the nearest standard resistor to match R_E.
- Note R_{Th} and V_{Th} are the Thévenin equivalent input resistance and voltage:

$$R_{Th} = (R_1 \,||\, R_2) = \left(\frac{R_1 R_2}{R_1 + R_2} \right) \qquad \text{and} \qquad V_{Th} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC}$$

But we don't know R_1 and R_2 yet.

Note that the effective base resistance and effective base voltage are the same as the Thévenin values: $R_B = R_{Th}$ and $V_{BB} = V_{Th}$

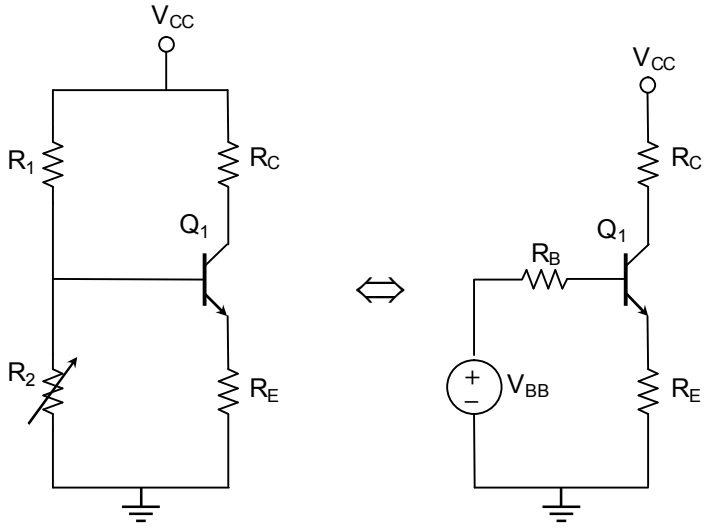


Figure 8.2: Relationship between the Thévenin-equivalent base resistance R_B and the actual circuit built with resistors R_1 and R_2. Figure is only to illustrate relationships for calculations.

- For bias stability, choose

$$R_B = R_{Th} = 0.1\,\beta\, R_E$$

and from Kirchhoff's voltage law, summing around the B–E loop, find V_{BB}:

$$V_{BB} = V_{Th} = V_{BE} + I_B R_B + I_C R_E$$

- Find R_1 and R_2 using the above resistor and voltage values:

$$R_2 = \frac{R_B}{\left(1 - \frac{V_{BB}}{V_{CC}}\right)} = \frac{R_{Th}}{\left(1 - \frac{V_{Th}}{V_{CC}}\right)}$$

$$R_1 = R_B \cdot \frac{V_{CC}}{V_{BB}} = R_{Th} \cdot \frac{V_{CC}}{V_{Th}}$$

EQUIPMENT:

Use equipment and components as required by your design and the design problem statement.

EXPERIMENT:

1. DC Measurements

a. Use the curve tracer to measure the β and V_{BE} of your transistor, if you have not already done so.

b. **Build the circuit in Figure 8.1 but without R_{S1}, R_{S2}, R_L, the capacitors, and function generator,** as was illustrated in Figure 7.2. **Use the resistance values you determined in your pre-lab and set R_C = 4.7 KΩ.** You should use the nearest standard resistance values for the resistors R_1, R_2, and R_E, even if the design values are non-standard. Attempt to build your circuit using standard values of resistors before you resort to using the decade resistance boxes.

c. Measure V_{C0} and V_{E0} of your amplifier using the DMM. Then, calculate V_{CEQ} and I_{CQ} (Q-point) using V_{C0} and V_{E0}. Compare with your design values. If V_{CEQ} is not close to calculated V_{CEQ}, please read following note. Tabulate your results and show them to the lab instructor.

NOTE: If the value of V_{CEQ} is not within 5% of your calculated value, replace R_2 with a resistance decade box and adjust the resistance value until V_{CEQ} is equal to or close to your calculated value. If you used V_{BE} = 0.7V in your calculations, you may find that your Q-point is very close to the saturation region and you will have to lower the value of R_2 to obtain a Q-point nearer the middle of the load line. If you use a decade resistance box for R_2, note how sensitive the value of V_{CEQ} is to small variations in R_2.

2. AC Analysis

a. Connect R_{S1}, R_{S2}, R_L, the capacitors, and the function generator to your circuit, as in Figure 8.1. The coupling capacitors need to be large enough to pass an ac signal of 1 KHz (22μF or greater). In Figure 8.1, the voltage divider using R_{S1} and R_{S2} is an easy way to keep the input voltage swing low enough to keep the transistor from being driven into either saturation or cut-off. After you have built the circuit, check your input and output wave shapes. Take appropriate action if your output wave shape is distorted from a sine wave.

b. Measure V_O keeping the oscilloscope coupling set to "AC". You might not be able to measure V_S (i.e., 20mV) because of noise, so you should make sure that the FGEN output is $2V_{P-P}$. From V_S and the measured value of V_O, **determine A_V** and record the result in Table 8.1. How does this value of A_V compare with the one specified in the design specification?

Table 8.1: Voltage gain measurements

R_L	$V_{O\text{-}PP}$	A_V with C_E	A_V without C_E
0.1 R_C			
R_C			
10 R_C			

c. Make an accurate sketch of the input and output waveforms.

d. Place a large value emitter-bypass capacitor across R_E and repeat steps b and c. Comment on the effect of C_E on the gain of the amplifier. Compare the new value of A_V with that given by

$$A_V = -(R_L \parallel R_C) / h_{ib} = - (\beta / r_\pi) \cdot\bullet (R_L \parallel R_C) = - (R_L \parallel R_C) / h_{ib}.$$

When R_E is not bypassed the voltage gain is given by

$$A_V = -(R_L \parallel R_C) / (R_E + h_{ib}) \approx -(R_L \parallel R_C) / R_E.$$

What does this result tell you about the effect of C_E?

e. Repeat steps 'b' through 'd' for $R_L = 0.1R_C$ and for $R_L = 10R_C$. How does the gain vary with the R_L / R_C ratio? Compare your results with the simulations.

f. Compare your amplifier designs with your B2 Spice simulations.

Extra credit portion:

It is possible to measure the output resistance. If you have time, measure the output impedance for the case where $R_L = R_C$.

Output Impedance: Remove R_L and C_E from the circuit. Measure $V_{O\text{-}PP}$. Connect a resistance decade box across the output terminals, with the resistance set at 10 kΩ. Adjust the decade box until the output voltage swing falls to half of its value before the decade box was connected across the output. The value of the resistance on the decade box will then be approximately equal to the output impedance R_O.

NOTE: CONSULT WITH YOUR INSTRUCTOR ON THE PRE-LAB FOR THE NEXT LAB BEFORE YOU LEAVE.

LAB REPORT:

1. Write a neat Engineering report for this laboratory. Your report should include all of the design calculations in your pre-lab. You should compare in a table your lab results with your design specifications and with your B2 Spice simulations.
2. Write a conclusion to this lab. Explain any differences between your calculated and measured values. Comment on the sensitivity of your design to the choice of Q-point. Comment on the effect of small variations in V_{BE} on your design and on your Q-point. Did your gains with and without C_E agree with what you expected?

ECE 311 EXPERIMENT 8 - CHECK LIST

1. Measure β and V_{BE}.
2. Build circuit in Figure 8.1 using resistors calculated in your design.

   Keep $V_{in} < 20mV_{P\text{-}P}$. All Capacitors 22μF or greater.
3. Measure V_{CE} and I_C. Compare with your design Q-point.
4. Measure V_{in} and V_o. Calculate A_v. Compare actual A_v with design spec.
5. Sketch V_{in} and V_o.
6. Insert emitter bypass capacitor. Measure V_{in} and V_o. Calculate A_v. Compare with

   $$A_V = - (R_L \,||\, R_C) / h_{ib} = - (\beta / r_\pi) \bullet (R_L \,||\, R_C)$$
7. Repeat steps 2-6 for $R_L = 0.1\ R_C$ and $10\ R_C$. How does A_v vary with R_L/R_C ratio?
8. Optional (extra credit + 50 pts.)
9. Compare design with B2 Spice simulations.

ELECTRONICS I
ECE 311

Experiment #9 – BJT Common-Emitter Amplifier Design II

PURPOSE:

The experiment is a follow-up to Experiment #6 and Experiment #7. It is intended to give the student individual experience in designing an amplifier to meet certain design specifications. You will design a BJT CE amplifier to meet a specified voltage gain, A_v, and output impedance, R_O.

THIS EXPERIMENT IS PERFORMED INDIVIDUALLY WITH A TIME LIMIT OF 1 HOUR. BUILD YOUR CIRCUIT IN THE LAB. DO NOT BRING A PREWIRED CIRCUIT TO THE LAB.

PRE-LAB:

1. Be familiar with BJT amplifier design.
2. Design a single stage, BJT CE amplifier with the specifications given below. Note that the signal source comprises the function generator and the voltage attenuator (see Figure 9.1). The output impedance (R_S) of the function generator is 50Ω. Your amplifier should also meet the following design specifications:
   a. $A_v = -100$
   b. $R_L = R_C = 4.7k\Omega$
   c. Undistorted output signal with the input signal = 0.02 V_{P-P}.

   Use $R_C = R_L$ and $V_{CC} = 10$ V. Specify R_1, R_2, R_E, R_C, and R_L. When doing your design, calculate A_v, A_i, V_{O-PP}, V_{CEQ}, I_{CQ}, h_{ib}, and h_{ie} (= r_π). You will need to use an emitter bypass capacitor to get the desired voltage gain. Assume that all coupling and bypass capacitors are large enough to be considered ac short circuits at the design frequency of 1KHz. **A general design procedure** is given following this section. Tabulate your results. Use an input signal to the base of the transistor that is around 0.02V_{P-P}.

   NOTE: You should use same β and V_{BE} for your design calculations that you used in Experiment #8.
3. Simulate the circuit you designed using B2 Spice. You may use the transient setup you used in previous BJT amplifier experiments. However, the values of resistors given in Experiment #7 or Experiment #8 will not achieve a voltage gain of -100.

EQUIPMENT:

Use equipment and components as dictated by your design.

Design Procedure: When emitter resistor R_E is bypassed by capacitor C_E.

- Calculate R_{ac}, I_{CQ} and V_{CEQ}

$$R_{ac} = (R_C \parallel R_L)$$

At room temperature $V_T = 0.026V$. When the pn-junction is turned on, the ideality factor is about 1.15-1.20, and so $nV_T \approx 0.03V$. Thus, in the special case of a common-emitter amplifier designed for maximum symmetrical signal swing and for maximum power transfer, we have $R_C = R_L$. Therefore,

$$(R_C \| R_L) = R_C/2 = R_L/2$$

$$\left|I_{CQ}\right| = \frac{nV_T\left|A_v\right|}{\left(R_C \| R_L\right)} = \frac{2nV_T\left|A_v\right|}{R_C} = \frac{2nV_T\left|A_v\right|}{R_L} = \frac{0.06V\left|A_v\right|}{R_L}$$

$$V_{CEQ} = I_{CQ}R_{ac} = \frac{I_{CQ}R_C}{2} = \frac{I_{CQ}R_L}{2}$$

- Calculate h_{ie} ($=r_\pi$) and h_{ib}

$$h_{ie} = \frac{V_T}{I_{BQ}} = \beta\frac{V_T}{I_{CQ}} = \beta\, h_{ib} = r_\pi$$

where V_T (thermal voltage) = 0.026V.

- Calculate R_{dc}

$$R_{dc} = \frac{V_{CC} - V_T\left|A_v\right|}{I_{CQ}}$$

- Calculate R_E

$$R_E = R_{dc} - R_C = R_{dc} - R_L \qquad \text{since } R_C = R_L$$

- Calculate R_B

$$R_B = 0.1\,\beta\, R_E$$

- Calculate V_{BB}

$$V_{BB} = V_{BE} + I_{BQ}R_B + I_{CQ}R_E$$

- Calculate R_1 and R_2

$$R_1 = R_B \cdot \frac{V_{CC}}{V_{BB}}$$

$$R_2 = \frac{R_B}{\left(1 - \frac{V_{BB}}{V_{CC}}\right)}$$

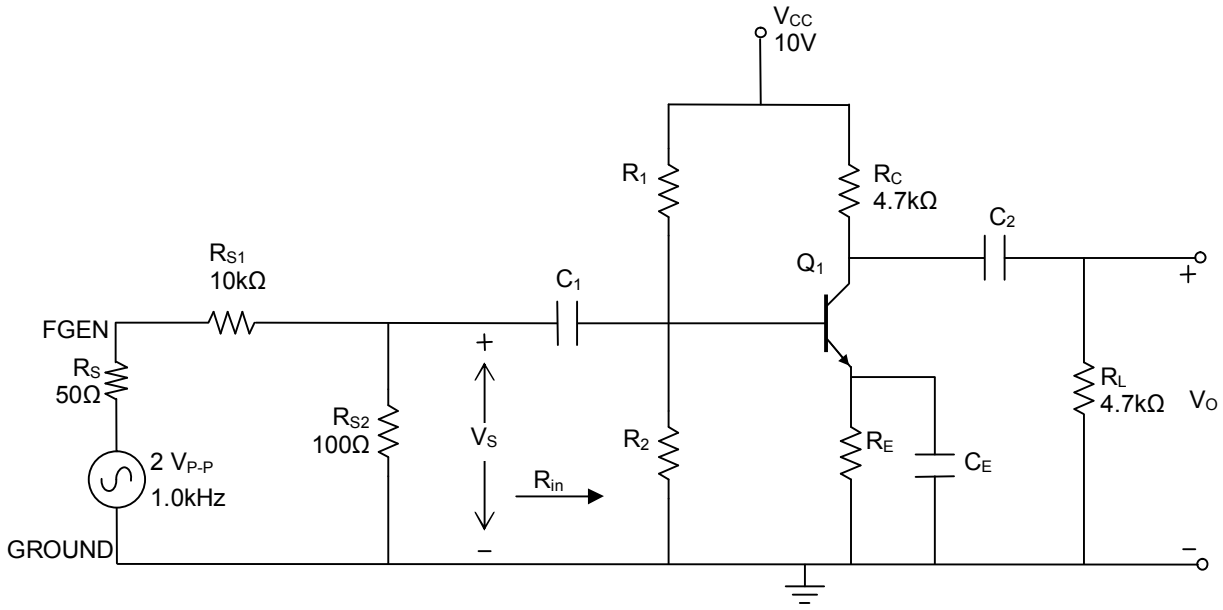


Figure 9.1: Common-emitter Amplifier

EXPERIMENTAL:

PART I: DC ANALYSIS

1. Using the resistance values you determined from your design calculations, build your amplifier, including only the core components: R_1, R_2, R_C, R_E, the transistor, and V_{CC} (similar to Figure 7.2). Use the nearest standard resistance values. You can also combine resistors in parallel and in series to obtain resistance values as close to the calculated values as possible. **However, a good design will use standard resistor values.**

2. Determine the Q-point of your circuit, as in Experiments 6, 7, and 8. If the value of V_{CEQ} is not within 5% your calculated value, replace R_1 with a resistance decade box and adjust the resistance value until V_{CEQ} is equal to or close to your calculated value. Replace the resistance value on the decade box with the closest standard resistor.

PART II: AC ANALYSIS

1. In Figure 9.1, the resistor R_S, represents the 50Ω internal impedance of the signal generator. The two resistors, R_{S1} and R_{S2}, are a voltage divider, external to the signal generator. These two resistors are chosen to keep the input signal to the amplifier low enough to insure that the output wave shape is not distorted. Use an input signal of $0.02V_{P\text{-}P}$ at the base of the transistor. To get this signal, you must use a $2V_{P\text{-}P}$ output from FGEN.

2. Complete your circuit as shown in Figure 9.1, using R_{S1}, R_{S2}, R_L, and capacitors (use 22μF or 47μF). R_S is an internal resistance already in the FGEN.

3. Apply a $0.02V_{P\text{-}P}$, 1 kHz sinusoidal input signal to your amplifier and determine the voltage gain, A_V. How does this value of A_V compare with the design specification?

Make sure the output waveform is not clipped. How does the measured value of $V_{O\text{-}PP}$ compare with the calculated value?

4. When you are demonstrating your input and output signals to the lab instructor, be sure to show that the output signal is not clipped or clamped. Show the lab instructor what happens to the output wave shape as the magnitude of the input signal increases. If the circuit you build does not meet the design specifications, explain why. Modify the biasing resistors R_1, R_2, and/or R_E to meet the design specifications.

LAB REPORT:

- You must demonstrate to the lab instructor that your amplifier meets the design specifications.
- You must demonstrate to the lab instructor how the output wave shape becomes distorted as the magnitude of the input voltage increases.
- If you have designed an amplifier with maximum output voltage swing, then the distortion in the output wave shape should be symmetrical as the input signal increases in magnitude.
- If your output wave shape distorts asymmetrically as the input voltage is increased, explain whether your design is closer to cut-off or closer to saturation on the load line.

Name: _____

ECE 311 EXPERIMENT 9

TO BE TURNED-IN TO LAB INSTRUCTOR

Objective: Design a single stage BJT CE amplifier with the following specifications:

$$A_V = -100$$

$$R_L = R_C = 4.7\ k\Omega$$

$$V_{CC} = 10V.$$

Display V_S and V_O on the oscilloscope.

Complete this form and turn it in along with your simulation output and all calculations.

β = _____ V_{BE} = _____

Calculated R_1 = _____ Standard resistor nearest calculated R_1 = _____

Calculated R_2 = _____ Standard resistor nearest calculated R_2 = _____

Calculated R_E= _____ Standard resistor nearest calculated R_E = _____

Calculated V_{CEQ}= _____ Measured value of V_{CEQ} =_____

Calculated I_{CQ} = _____ Measured value of I_{CQ} =_____

If the measured value of V_{CEQ} is not within 5% your calculated value, replace R_1 with a resistance decade box and adjust the resistance until V_{CEQ} is as close to your calculated value as possible. Replace the resistance value on the decade box with the closest standard resistor(s), and again measure V_{CEQ}. Report those final values below:

Decade Box R_1 = _____ Standard resistor nearest Decade Box R_1 =_____

Calculated V_{CEQ}= _____ Final measured value of V_{CEQ} =_____

Calculated I_{CQ} = _____ Final measured value of I_{CQ} =_____

Measured value of V_O =_____

$A_v = V_O / V_S$ = _____

Display V_S and V_O on the oscilloscope and ask your instructor to verify them.

ELECTRONICS I

ECE 311

Experiment #10 – Field Effect Transistors

PURPOSE:

The purpose of this experiment is to measure the characteristics of a field effect transistor (FET) and to compare these characteristics with the theoretically predicted characteristics.

PRE-LAB:

1. You should be familiar with the discussion of field effect transistors in your text and the parameters that are used to describe the FET. You will be measuring these parameters in the lab using the curve tracer.
2. Make sure to bring a piece of linear graph paper.

EQUIPMENT:

(a) Junction Field Effect Transistor 2N3823, 2N4416, or equivalent

(b) Curve tracer

(c) Linear graph paper, two cycle log-log graph paper

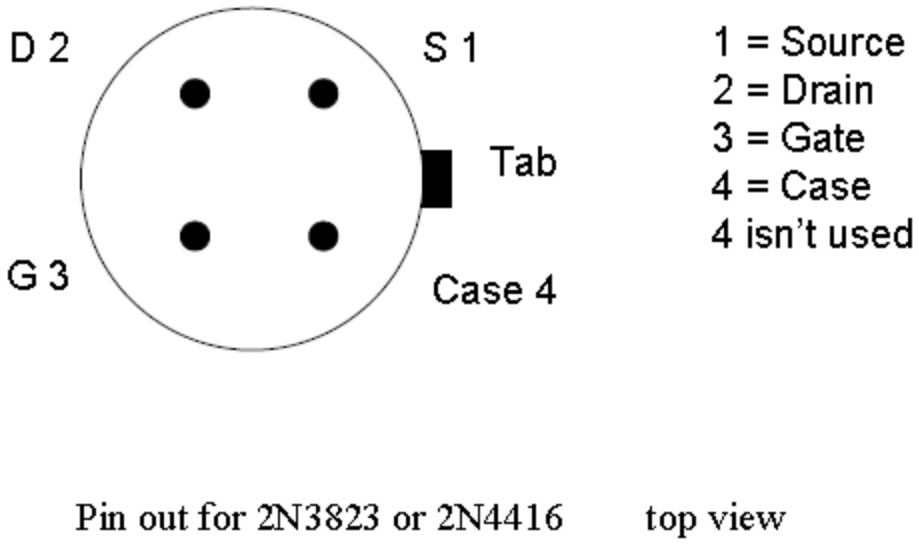


Figure 10.1: Top view of JFET pin-out

INTRODUCTION

The curve tracer will be used to display the FET characteristics. The operation of the curve tracer when measuring FET characteristics is similar to its operation when measuring bipolar transistors. In the case of the bipolar transistor (BJT), the base current is stepped to obtain the collector or output characteristics. In the case of the FET, the gate voltage is stepped to obtain the drain or output characteristics. Also, in the case of the bipolar transistor, the base must be forward biased with respect to the emitter, while in the case of the FET, the gate can be either reverse or forward biased with respect to the source, depending on whether a depletion or enhancement type of FET is being measured, respectively. In this experiment a depletion type transistor will be studied and, thus, the gate must be reverse biased with respect to the source. The curve tracers have a FET terminal connector and you will use the G-D-S terminals.

The transistor to be measured is either a 2N3823 or a 2N4416 N-channel junction field effect transistor (JFET). The top-view of the pin-out for the JFETs is shown in Figure 10.1. Both transistors are depletion transistors with negative pinch-off voltages. Both the low-level or linear-current region and the constant-current or saturation region of the JFET will be studied. Do not confuse the saturation region of a JFET output characteristic with the saturation mode of operation of a bipolar transistor.

Drain Current Equation of JFET in Linear Region

The JFET drain characteristic for an n-channel JFET can be accurately described by Equation (10.1) for values of $V_{GS}>V_P$, and $V_{DS} \leq V_{DS(SAT)} = V_{GS} - V_P$. For a p-channel JFET K_n is replaced by K_p and all currents and voltages have the opposite sign.

$$I_{DS} = K_n [2(V_{GS} - V_P) V_{DS} - V_{DS}^2], \tag{10.1}$$

where I_{DS} = drain current

K_n = the gain constant = I_{DSS}/V_P^2

V_{GS} = gate to source voltage

V_{DS} = drain to source voltage

V_P = the pinchoff voltage, defined as the value of V_{GS} at which the drain current I_{DS} goes to zero; also called the "gate-source cutoff voltage" or $V_{GS,off}$. This is equivalent to threshold voltage V_{Th} for an enhancement-mode MOSFET. (Note: for an n-channel JFET, V_P is negative.)

I_{DSS} = the saturated drain current for $V_{GS} = 0V$.

$V_{DS(SAT)} = V_{GS} - V_P$ is the drain voltage at pinchoff, beyond which the JFET is saturated and I_{DS} is nearly constant.

The Drain Resistance (r_{DS}) And Drain Conductance (g_{DS})

Equation (10.1) can be rewritten in terms of the drain resistance as

$$I_{DS} = [\ 1/r_{DS}]\ [\ 1 - (V_{GS}/V_P)^{1/2}]\ V_{DS} \tag{10.2}$$

where r_{DS} = drain resistance = $(\partial V_{DS}/\partial I_{DS}) \cong (\Delta V_{DS}/\ \Delta I_{DS})$ at a constant V_{GS}.

The drain resistance r_{DS} is related to the drain conductance, g_{DS}, by

$$r_{DS} = 1 / g_{DS}$$

where

$$g_{DS} = \partial I_{DS}/\partial V_{DS} \approx \Delta I_{DS}/\Delta V_{DS} \qquad \text{with } V_{GS} = \text{constant} \tag{10.3}$$

g_{DS} = Y22 on Hameg

Drain Current in Saturation Region

For large values of drain-to-source voltage, $V_{DS} > V_{DS\,SAT}$, the drain current tends to saturate at an approximately constant value. In this constant current region or saturation region, the drain current is approximately given by Equation (10.4).

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(\frac{V_{GS} - V_P}{-V_P}\right)^2 = I_{DSS}\left(\frac{V_{DS(SAT)}}{-V_P}\right)^2 \tag{10.4}$$

$$= K\cdot(V_{DS(SAT)})^2$$

If there is significant drain conductance, then the output current will not saturate and/or Equation (10.4) must be multiplied by

$$(1 + \lambda V_{DS}),$$

where λ is a constant greater than 0.

The linear and saturation regions of the JFET operation are shown in Figure 10.2.

Transconductance of JFET (g_m)

The transconductance, g_m, of the JFET is defined by

$$g_m = \partial i_D/\partial v_{GS} \approx \Delta i_D/\Delta v_{GS} \text{ with constant } v_{DS} \tag{10.5}$$

As shown in Equation (10.5), g_m is a measure of the change in drain current for a given change in gate-source voltage at a constant v_{DS}. The term, g_m, is analogous to β or h_{fe} for a BJT.

In this experiment the linear and saturation characteristics of a JFET will be measured. From these characteristics, V_P and I_{DSS} will be obtained. Values of r_{DS} and g_m of the transistor will be determined.

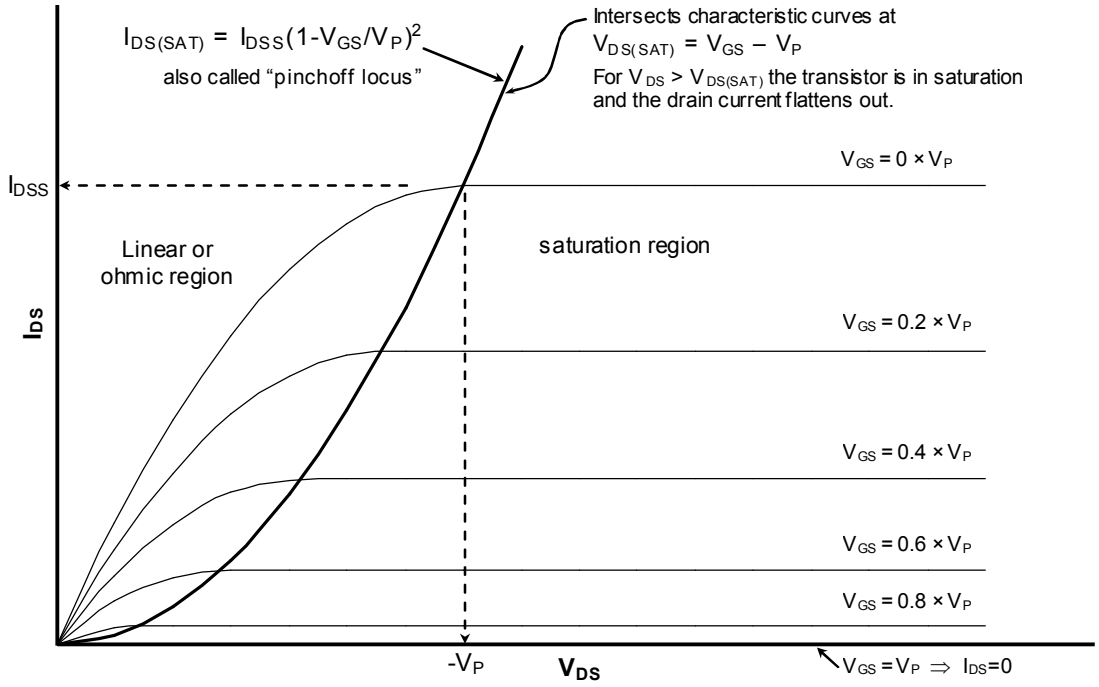


Figure 10.2: Drain characteristics or output characteristics of a JFET

EXPERIMENT:

1. Connect the JFET in the appropriate socket on the front panel of the curve tracer.
2. Obtain the low-level transistor characteristics on the curve tracer screen. To do this set the menu screen as follows:

Type:	[NCH-FET]
$V_{MAX:}$	[2V]
I_{MAX}:	[2mA]
$P_{MAX:}$	[0.4W]
V_G (MAX)	[0V]
V_G (MIN)	[-2.5V]

When you connect the FET to the socket on the Hameg, you may not see any curve on the CRT screen. You should check V_G on the LCD screen. Expect to find this value around -9.5V. To see any curve on the CRT screen, you need to set function to MAX and start turning the rotary knob clockwise to increase the maximum value of V_G for the steps. When V_G reaches around -7V, you will start seeing curves rising on the CRT screen. Move the cursor using cursor key to the top or first curve, if it is not already there. Keep increasing V_G until it reaches 0.0V. Then, move the cursor to the bottom-most or last curve and set function to MIN and again turn the rotary knob clockwise. By doing so, you are increasing minimum value of V_G for the steps. You should try to get the last (bottom) curve to be at $V_G = –2.5V$.

NOTE: The JFET you are using is an n-channel, depletion-mode JFET. A depletion transistor has a large value of drain current at a gate voltage of 0V.

Your characteristics should look approximately like those shown in Figure 10.3. Record several data points for all five characteristics. Sketch the characteristic curves.

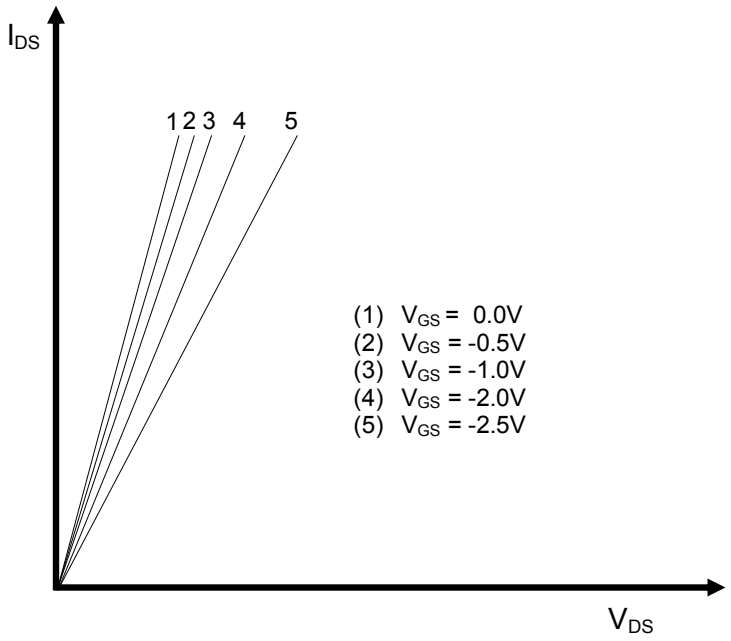


Figure 10.3: Drain characteristics for an FET operating in the linear region for small values of V_{DS}.

3. Depress the CURSOR key to move the cursors to the V_{GS} = 0 curve. Use the rotating knob to move the cursors along this curve. I_{DS} and V_{DS} should change as you do so. Determine r_{DS} for the V_{GS} = 0V characteristic and for all of the other characteristic curves displayed on the curve tracer and record your data on Table 10.1. Try to take two measurement points as distant as you can on each curve.

Table 10.1: r_{DS} Calculations

Curve	V_{GS}	V_{DS1}	I_{DS1}	V_{DS2}	I_{DS2}	ΔI_{DS}	ΔV_{DS}	r_{DS}	g_{DS}
1									
2									
3									
4									
5									

4. Determine g_m at V_{DS} = 0.05V and in increments of 0.05V. Tabulate your results in Table 10.2.

Table 10.2: Transconductance (g_m) Measurement

V_{DS} (V)	Your value of V_{DS}	I_{DS1} @ $V_{GS1} = 0.0V$	I_{DS2} @ $V_{GS2} \approx -0.5V$	$\Delta I_{DS} = I_{DS2} - I_{DS1}$	$\Delta V_{GS} = V_{GS1} - V_{GS2}$	g_m
0.05						
0.10						
0.15						
0.20						
0.25						
0.30						
0.35						

You can use the curve tracer to verify your calculations by comparing $1/Y_{22}$ ($Y_{22}=r_{DS}$) and Y_{21} (= g_m). What do your results tell you about r_{DS} and g_m as the Q-point (V_{DS}, I_{DS}) changes? Are r_{DS} and g_m constant, independent of Q-point?

5. Obtain the transistor drain characteristics in the saturated region, the following menu page setting can be used:

   V_{MAX} [40V]
   I_{MAX} [20 mA] For some transistors 2mA may be needed.
   P_{MAX} [0.4W]

   Make a couple of copies of the output characteristics. You will need one for Experiment #12. The transistor characteristics in the saturated region should resemble those shown in Figure 10.2. If there is significant drain conductance, then the currents will not be constant in the saturated region.

6. Depress the CURSOR key to move the cursors to the V_{GS} = 0 characteristic curve. Determine the values of V_P and I_{DSS} for your transistor (see Figure 10.2). Remember that I_{DSAT} occurs when $V_{GS} - V_{DS} = V_P$. Notice that I_{DS} is not saturated for values of $V_{DS} < V_{DS(SAT)} = V_{GS} - V_P$.

7. Determine the transconductance, g_m, and the drain resistance, r_{DS}, for your transistor for various Q-point values in the saturation region. You may set V_{DS} constant and vary I_{DS} by changing V_{GS}. Tabulate your results in Table 10.3. What do your results tell you about g_m, r_{DS}, and the position of the Q-point? Are these values independent of your Q-point? Remember, for the bipolar junction transistor, β was relatively independent of Q-point.

Choose values of V_{DS} = 0.25V, 0.5V, $|V_P|$, 5V, and 10V. You might need to set V_{MAX} = 10V for better accuracy.

Table 10.3: g_m Measurements for Saturation Region

V_{DS} (V)	Your value of V_{DS}	I_{DS1} @V_{GS} = 0.0V	I_{DS2} @$V_{GS} \approx -0.5V$	g_m
0.25				
0.50				
$\|V_P\|$				
5.0				
10.0				

8. Make a table of I_{DS} versus V_{GS} in both the linear region and in the saturation region for different values of V_{DS}.

9. Plot I_{DS} in the saturation region as a function of V_{GS} for V_{DS} = V_{DS}(SAT). This characteristic is the transfer characteristic, if g_{DS} = 0, and should be similar to Figure 10.4. It is possible to determine g_m directly from the transfer characteristic as the slope of the transfer characteristic. Notice that $g_m = g_m(V_{GS})$.

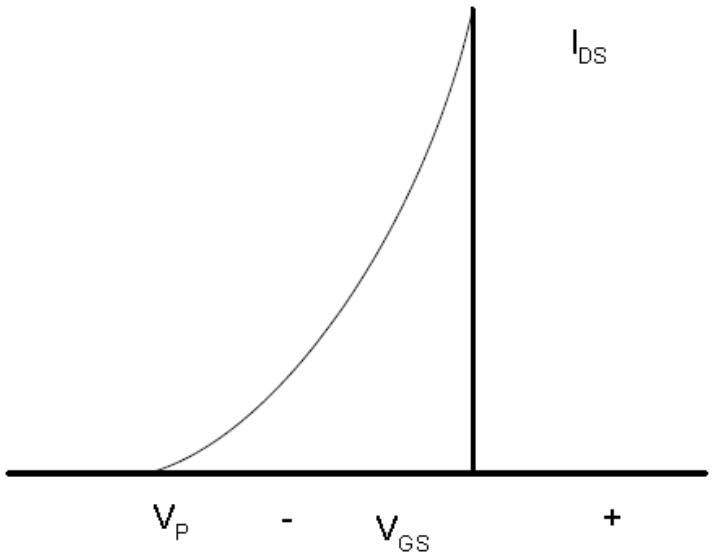


Figure 10.4: JFET Transfer Characteristic

LAB REPORT:

1. Plot the measured values of I_{DS} vs. V_{GS} in the linear region and compare with calculated values (transfer characteristics). Use Equation (10.1) for calculated values. Explain any difference.
2. Plot saturation values of I_{DS} vs. V_{GS} and compare with calculated values (transfer characteristics). Use Equation (10.4) for calculated values.
    a. How well do the saturation currents fit the expected square-law characteristic for the JFET?
    b. Explain differences.
3. Plot r_{DS} as a function of V_{DS}. Plot g_m vs. V_{GS}. Compare with expected values.

ECE 311 EXPERIMENT 10 - CHECK LIST

1. Low-level characteristics
    a. Set curve tracer Type: N-FET, $V_{MAX} = 2V$, $I_{MAX} = 2mA$
2. Record low level data
    a. Record $r_{DS} = \Delta V_{DS}/\Delta I_{DS}$ at $V_{GS} = 0V$, $g_m = \Delta I_{DS}/\Delta V_{GS}$ at V_{DS} = constant
3. Output characteristics
    a. Set curve tracer to $V_{MAX} = 10V$, $I_{MAX} = 20mA$. Print characteristics.
4. Determine V_P and I_{DSS}.
5. Record the data in saturation region. Use $V_{DS} \approx 5V$ for finding g_m.

ELECTRONICS I

ECE 311

Experiment #11 – FET Bias and Amplification

PURPOSE:

The purpose of this experiment is to study the use of the junction field effect transistor (JFET) as an amplifier, with attention given to the proper biasing of the circuit. Various methods of determining FET amplifier parameters will be studied. You need to have your circuit simulated before the lab begins; otherwise, you may have difficulty finishing the lab, if you have difficulties obtaining the proper Q-point.

PRE-LAB:

You should be familiar with biasing of the JFET using a source resistor. You should be familiar with analysis of common-source amplifiers, particularly calculation of the voltage gain. Perform a circuit simulation using B2 Spice for the circuit shown in Figure 11.6 using the values of resistors you have calculated. Use the linear characteristics from Experiment 10 to determine the closest value V_{GS} to the desired Q-point.

EQUIPMENT:

1. JFET – see Figure 11.1 for the pin-out of a 2N3823 or 2N4416
2. Curve tracer
3. NI ELVIS workstation
4. Resistors and capacitors as required

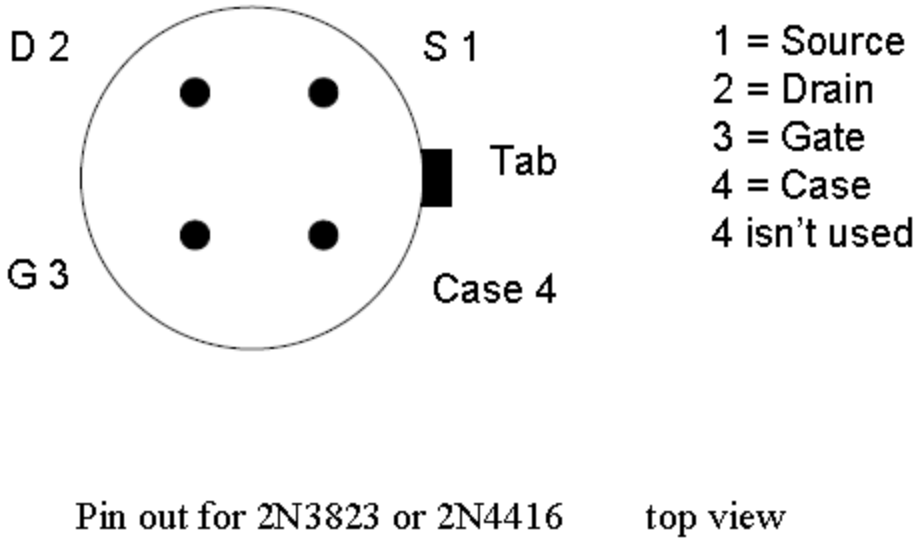


Figure 11.1: Top view of JFET pin-out

INTRODUCTION

Selection of an appropriate operating point (defined by I_{DQ}, V_{DSQ}, V_{GSQ}) for a field effect transistor (FET) amplifier stage is determined by similar considerations to those used for a BJT amplifier. These considerations include the output voltage swing and distortion, the voltage gain, and the drain current drift.

Proper biasing of field effect transistors is different from biasing BJTs. Because the gate current is zero for all practical purposes, thermal runaway is not normally a problem. The gate-to-source bias voltage is of the opposite sign as the power supply voltage. The output current is proportional to the square of the input voltage and not linearly proportional to the input current, as is the case with a BJT. Thus, design for maximum voltage swing is not usually desired, since maximum voltage swing will lead to distortion of the output signal. Proper biasing of a FET amplifier is necessary for correct circuit operation.

As with BJTs, there are different configurations for low frequency FET amplifiers. The different FET configurations are the common-source (CS) and common-drain (CD) amplifiers, shown in Figure 11.2 and Figure 11.3, respectively. The CS FET amplifier is analogous to the common collector (CC) BJT amplifier.

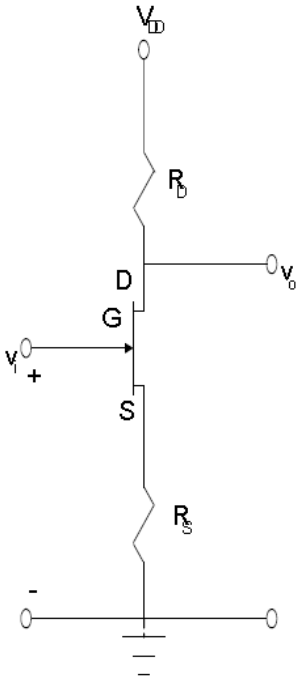


Figure 11.2: Common-Drain Amplifier

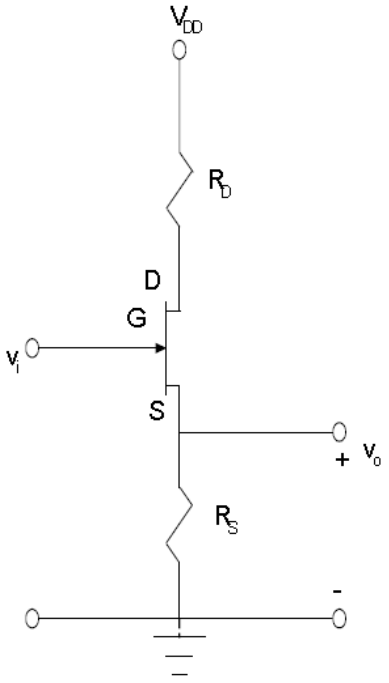


Figure 11.3: Common-Source Amplifier

Determining the voltage gain for a FET amplifier is similar to determining the voltage gain of a BJT amplifier. First, replace the circuit with its equivalent small-signal model and determine the input–output relationship for the amplifier using the small-signal model. Remember that a power supply is considered to be an ac ground. In a FET amplifier the input will be a voltage and the output will be a current. The low-frequency, small-signal model is shown in Figure 11.4.

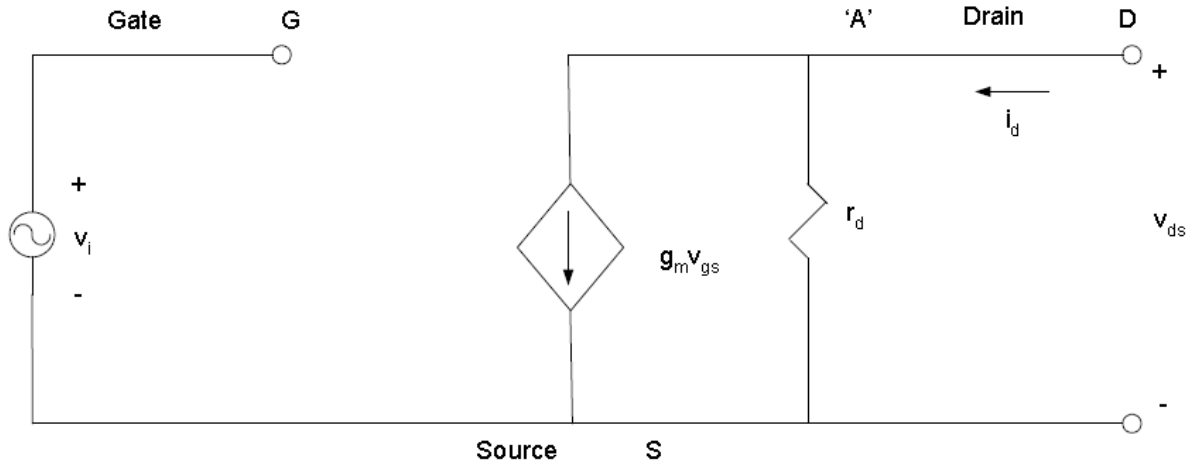


Figure 11.4: Small-signal, low-frequency model of a JFET

Applying KCL to the output node A, we fine the small-signal variation in i_d to be,

$$i_d = g_m v_{gs} + (1/r_d)\, v_{ds} \tag{11.1}$$

where

$$g_m = i_d/v_{gs} \text{ at } v_{ds} = \text{a constant.} \tag{11.2}$$

In Equation (11.2), the currents and voltages are considered to be instantaneous values, or ac values. In terms of changes in I_D and V_{GS},

$$g_m = dI_D / dV_{GS} = \Delta I_D/\Delta V_{GS} \text{ at a constant } V_{DS} \text{ is the transconductance.}$$

The parameter, r_d, is called the drain resistance or output resistance and is given by

$$r_d = v_{ds}/i_d \qquad \text{at } v_{gs} = \text{a constant}$$

or

$$r_d = dV_{DS}/dI_D \text{ at constant } V_{GS}. \tag{11.3}$$

An amplification factor, μ, can then be defined as:

$$\mu = r_d\, g_m. \tag{11.4}$$

Using the small-signal model, the voltage gain of a FET amplifier can be determined. For example, consider a common source amplifier. The CS amplifier with the JFET small-signal model is shown in Figure 11.5.

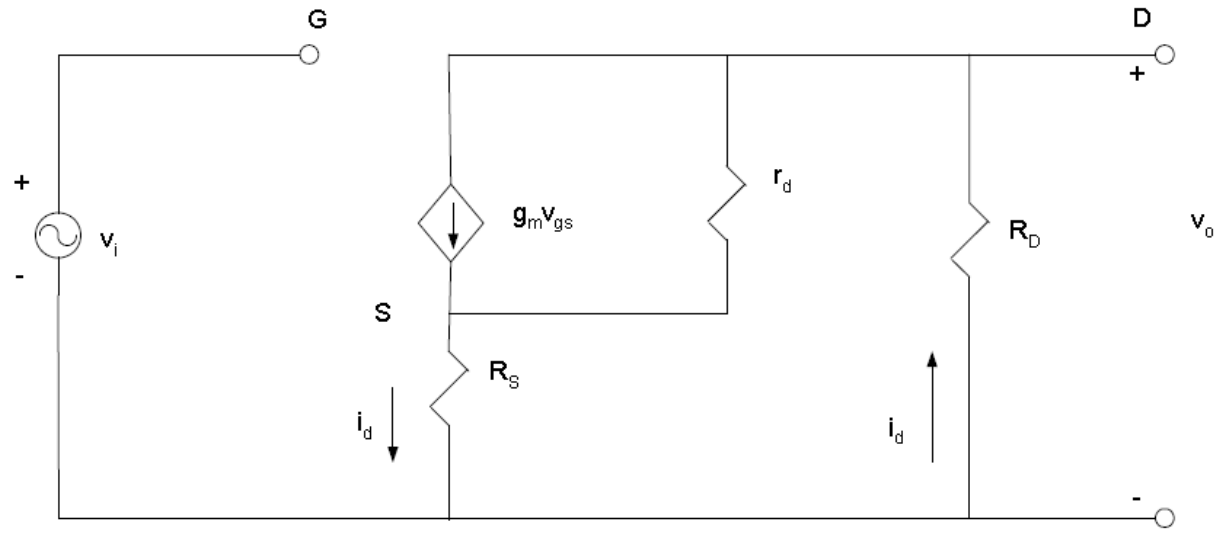


Figure 11.5: Common-Source JFET amplifier with small-signal model

Applying KVL to the output circuit, we find:

$$i_d R_D + (i_d - g_m v_{gs})\, r_d + i_d R_S = 0 \tag{11.5}$$

and

$$v_{gs} = v_i - i_d R_S. \tag{11.6}$$

Combining (11.5) and (11.6) results in

$$i_d = \mu\, v_i / [r_d + R_D + (\mu + 1)\, R_S] \tag{11.7}$$

since $\mu = r_d\, g_m$.

From the circuit in Figure 11.4 or 11.5, the output voltage is given by

$$v_o = -i_d R_D. \tag{11.8}$$

Therefore, we have

$$v_o = -\mu\, v_i R_D / [r_d + R_D + (\mu + 1)\, R_S] \tag{11.9}$$

If $R_S = 0$, or is bypassed by a capacitor, the voltage gain is

$$A_v = v_o/v_i = -\mu\, R_D / (r_d + R_D) = g_m R_D\, r_d/(r_d + R_D) = g_m R_{D1} \tag{11.10}$$

$$R_{D1} = r_d \,||\, R_D. \tag{11.11}$$

In this lab, a FET common-source amplifier, with self bias, as shown in Figure 11.6, will be studied. For a specified drain current, I_D, the corresponding gate to source voltage, V_{GS}, can be determined from plotted transfer characteristics. Since the gate current, I_G, is negligible, the source resistance, R_S, is given by

$$R_S = -V_{GS}/I_D. \tag{11.12}$$

Using either the drain characteristics or the transfer characteristics of the JFET used in this experiment, determine an operating point specified in the lab and calculate the proper R_S needed in the circuit using the output or transfer characteristics. Knowing R_S and I_D and given V_{DS}, the proper value of R_D will be calculated for use in the FET circuit. After determining the proper resistance values, the dc voltages will be measured and the ac voltage gains will be measured and recorded.

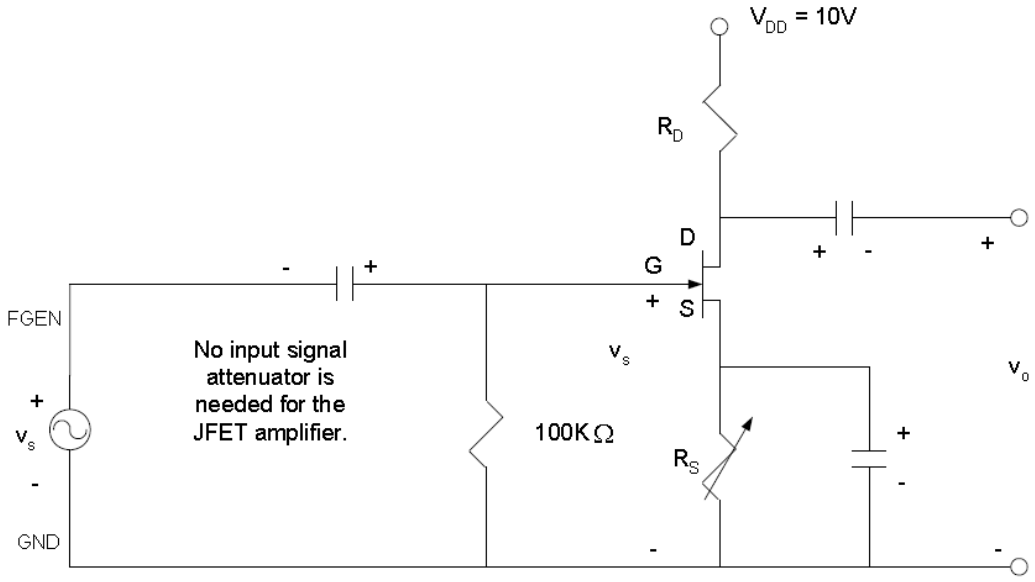


Figure 11.6: Common source amplifier. All C's ≥ 10μF at 25 volts

EXPERIMENT:

PART I: Bias Circuitry

1. Measure the common source characteristics of the JFET on the curve tracer. You can use the extra set of drain characteristics you measured in Experiment #10. Record the JFET type and number for your report. Note that the steps of gate voltage are used, instead of base current as was done for the BJT. Consult the equipment manual for JFET characteristics measurements as necessary. Use these characteristics to calculate g_m, once you have determined your Q-point.

   Print these characteristic curves on linear graph paper with the appropriate numerical values recorded. Find and record the best approximate values of I_{DSS} and V_P. Pick a quiescent Q-point close to V_{DS} = 5V and $I_D = 1/2(I_{DSS})$. At this Q-point, determine and record V_{GS} and g_m for use in determining R_D and R_S in part 2.

   Note that $g_m = \Delta I_D/\Delta V_{GS}$. Have your instructor verify your Q-point.

2. DC Measurements

   a. From your Q-point calculated in part 1, determine and record the values of R_D and R_S shown in the circuit in Figure 11.6 from the following equations:

$$V_{GS} = -I_D R_S \tag{11.13}$$

$$V_{DD} = V_{DS} + I_D (R_S + R_D) \quad (11.14)$$

Use the closest value of V_{GS} to your Q-point, with $I_D = ½(I_{DSS})$.

Let your instructor confirm your calculations. Use standard value resistors in your lab kit which are close in value to the resistance values you have calculated. Be sure to show your calculations in your report as well as what resistor values were actually used in the lab.

b. Construct the circuit shown in Figure 11.6. Use the values of R_D and R_S you have determined.

c. Measure and record the dc voltages, V_{DS}, V_{GS} and V_D. V_D is measured with respect to the ground. Calculate I_D and include the calculations in your report. Are these values close to expected values? Why or why not?

d. Determine g_m from the following equation:

$$g_m = 2\ \{[I_{DSS} I_{DQ}]^{1/2}\}/|V_p|$$

where $I_{DQ} = I_{DSS}/2$ for your Q-point. Compare the value that you calculate with the value measured on the curve tracer.

PART II: AC Measurements

Note: Accurate measurements of R_D, R_S and all required voltages are essential for correct calculations.

1. Apply a small sinusoidal (e.g. $0.2V_{P-P}$) 1 kHz signal at v_s in the above circuit and measure the voltage amplification $A_v = v_o/v_s$ using the oscilloscope. Be sure no appreciable distortion is present at the output; i.e. the output voltage should be close to a sine wave! There should be no need for a signal attenuator as used in the bipolar transistor amplifiers. Placing a large resistor (>100kΩ) across v_o may improve your results.
2. Increase the magnitude of v_s until significant distortion occurs. Does the output waveform shape agree with the square law characteristics of the transistor? Is your Q-point near the middle of the transistor drain characteristics?
3. When you have established a maximum output signal without significant distortion, vary the input frequency from 3Hz to 30kHz and measure v_o. Plot either v_o or A_v as a function of frequency on semi-log graph paper. Is the gain independent of frequency?

LAB REPORT:

1. Compare the two values of g_m you found. How well do they agree?
2. Compare the experimental voltage gain with the simulated voltage gain. Explain differences.
3. How and why does the output wave shape change as the magnitude change?

ECE 311 EXPERIMENT 11 - CHECK LIST

1. Biasing
    a. Print JFET characteristics from the curve tracer. Choose a Q-point (V_{ds} = 5V, $I_{dss}/2$).
    b. Measure g_m, V_{gs} at the Q-point.
    c. DC Measurements
        i. Calculate R_D and R_S using Eq. 11.1 and 11.2.
        ii. Build the circuit in Figure 11.6.
        iii. Measure and record DC voltages V_{DO}, V_{DS}, and V_{GS}. Calculate I_{DS}. Are these values close to expected values?
        iv. Determine g_m using $g_m = (2\sqrt{(I_{DSS}\, I_{DQ})}) / |V_p|$, where $I_{DQ} = I_{DSS}/2$.
2. Amplification
    a. Apply a small sinusoidal signal. Measure A_v using oscilloscope. Check for output distortion.
    b. Increase the magnitude of the input signal until significant distortion occurs. Sketch the output wave shape. Does the output wave shape agree with the transistor square law characteristics?

ELECTRONICS I

ECE 311

Experiment #12 – Basic Logic Circuits

PURPOSE:

This experiment is intended to introduce the student to the characteristics of logic circuits and specifically the operation of a CMOS INVERTER and a 2-input CMOS NAND gate. CMOS is short for Complementary Metal Oxide Semiconductor.

NOTE: A Diode–Transistor Logic (DTL) NAND gate is the logic-equivalent of a Transistor–Transistor Logic (TTL) NAND gate. The inputs to the DTL circuit are through diodes, while the inputs to the TTL circuits are through multiple-emitter bipolar transistors.

Historically, the DTL circuits were used before it became possible to manufacture multiple-emitter bipolar transistors and prior to MOS (Metal Oxide Semiconductor) technology rising to dominance.

PRE-LAB:

Read the sections of the book devoted to MOS logic circuits. The TTL circuit shown in Figure 12.1(a) is for reference only. You should understand how the circuits shown in Figure 12.1 act as inverters and compare their complexity. In CMOS technology, the number of components is dramatically reduced and only transistors are used. This change facilitates manufacture as integrated circuits and reduces power consumption, which is why CMOS dominates standard logic circuits today. You should understand the meaning of CMOS technology and the operation of the CMOS gates.

You should have completed the simulation of a CMOS inverter and 2-input CMOS NAND gate so that you can compare your test results with the simulation. Understand the concepts of rise time (t_r), fall time (t_f) and delay time (t_{pLH}, t_{pHL}). Provide a sketch showing these definitions.

For the Pre-Lab simulation, you need to complete followings simulation B2 Spice.

- You should complete the simulation of a CMOS inverter (Figure 12.3) and 2-input CMOS NAND gate (Figure 12.4), so that you can compare your experiment results with the simulation.
- Understand the concepts of rise time (t_r), fall time (t_f) and delay time (t_{pLH}, t_{pHL}). Provide a sketch showing these definitions on your simulation plots from your Inverter circuit. For more details on these concepts, please refer to your textbook.
- Vary the input frequency to your inverter. Record and compare the inverter's effect at 10kHz, 25kHz, and 50kHz. Determine the maximum frequency of operation with no load.
- Load the output of the inverter with a 0.1µF capacitor and test again by varying the frequency of the input signal generator. Record and compare the inverter's effect at 10kHz, 25kHz, and 50kHz. Determine the frequency at which the device fails to operate.

EQUIPMENT:

1. 2 N-Channel CMOS transistor (ZVN4424A or equivalent)

2. 2 P-Channel CMOS transistor (ZVP4424A or equivalent)
3. 0.1uF capacitor
4. NI ELVIS II workstation

INTRODUCTION

Figure 12.1(a) shows a diagram of the basic TTL INVERTER. Fig 12.1(b) shows the CMOS equivalent.

What is CMOS?

Complementary metal oxide semiconductor (CMOS) technology uses a pair of FET transistors — one n-channel and one p-channel — to form logic gates.

How CMOS works:

A CMOS inverter is shown in Figure 12.1(b). If the input is high logic level (5V), the n-channel device (connected to ground *Gnd*) is "on" and the p-channel device (connected to supply) is "off". Since the lower device is on and connected to ground, the output is also shorted to ground. The 5V supply is dropped across the upper device. Hence, a high on the input yields a low on the output.

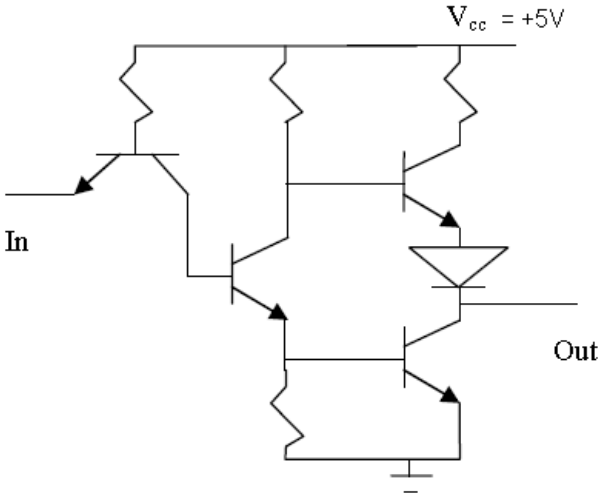


Figure 12.1(a): TTL Inverter

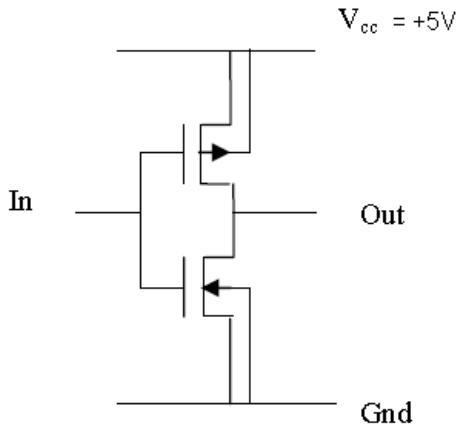


Figure 12.1(b): CMOS Inverter

Note that these devices are either hard "on" or hard "off" in the steady state. Another description is that they are either "cut-off" or "saturated". This makes design simpler, as the devices act as switches, and current values are less important for the operation. Power consumption is important, thus, the lowest values of operational current are desirable. The major design activity is sizing the devices to optimize factors such as speed of operation, power consumed, and ability to drive a load or fan-out.

Fan-out is the term used to describe the number similar of gates the inverter can drive and still operate at a reasonable speed.

Rise Time and Fall Time

Rise time for a pulse wave is the time required for the leading edge of the signal to rise from 10% to 90% of the final high value.

Fall time is the time interval required for the signal to fall from 90% of the high value to 10% of high value along the trailing edge, as illustrated in Figure 12.2.

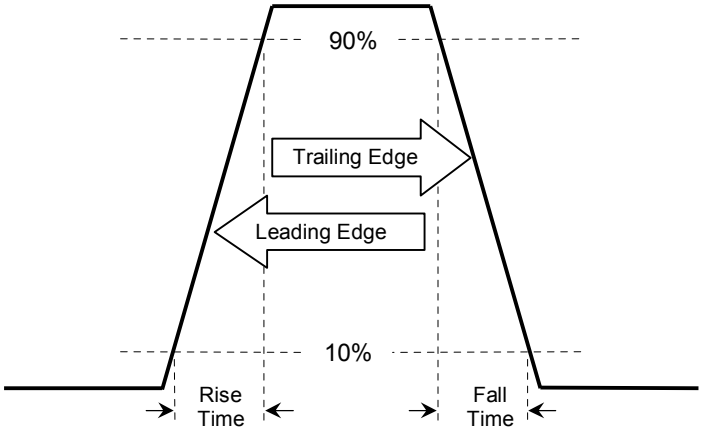


Figure 12.2: Rise time and Fall time

EXPERIMENT:

Pin diagram for ZVN4424A (nMOS) and ZVP4424A (pMOS) is shown in Figure 12.3.

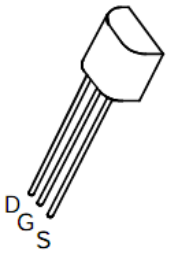


Figure 12.3: Pin diagrams for ZVN4424A (nMOS) and ZVP4424A (pMOS)

1. Build the circuit shown in Figure 12.4. Use the +5V terminal (located on the bottom left corner of the ELVIS workstation) as the power supply and the function generator for the input signal. Connect the scope CH0 and CH1 to the input and output respectively to observe the operation. **Set SCOPE coupling to DC for both CH0 and CH1.**

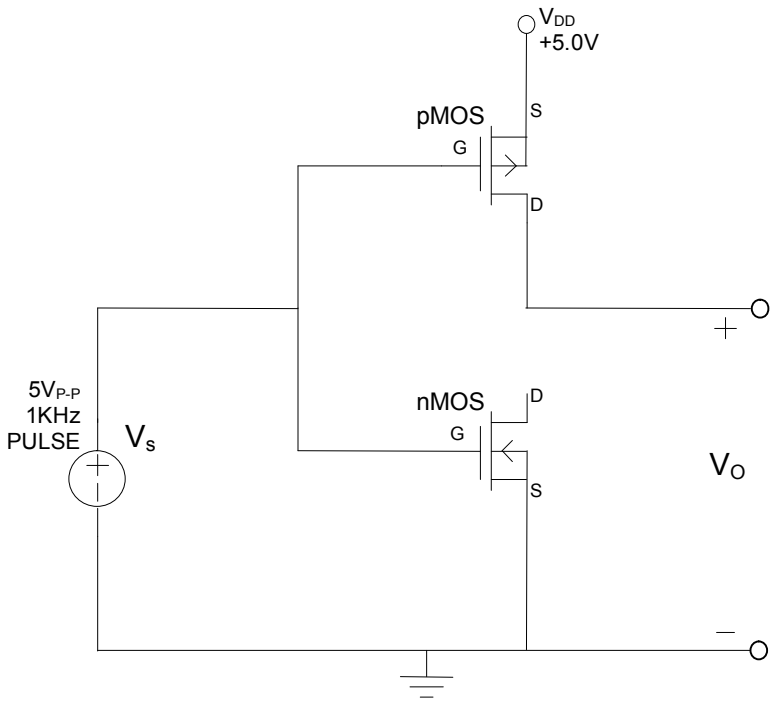


Figure 12.4: CMOS Inverter

2. Set the function generator as follows:
   a. Square wave
   b. Amplitude = $5V_{P-P}$
   c. DC offset = +2.5V
   d. Frequency = 1kHz
3. Connect the SYNC signal (PIN 34 on the left side of the workstation) to the TRIG BNC input (located at the top left corner of the workstation). Set the Trigger type on the scope to DIGITAL. Click Run on the scope and function generator.
4. Vary the input frequency to your inverter. Record and compare the inverter's effect at 10kHz, 25kHz, and 50kHz.
5. Load the output of the inverter with a 0.1µF capacitor and test again by varying the frequency of the input signal generator. Record and compare the inverter's effect at 10kHz, 25kHz, and 50kHz.
6. Disconnect the 0.1µF capacitor, FGEN, and the scope from the inverter circuit. Use SUPPLY+ as input and connect DMM at the output of the Inverter. Increase input voltage in steps of 0.5V and record output voltage on Table 12.1. Show that the circuit performs the INVERTER operation by plotting the output voltage as a function of the input voltage. Also, let your lab instructor verify your results.

Table 12.1: Input voltage vs output voltage for Inverter

Input Voltage (V)	Output Voltage (V)
0.0	
0.5	
1.0	
1.5	
2.0	
2.5	
3.0	
3.5	
4.0	
4.5	
5.0	

7. Connect the circuit for a 2-input CMOS NAND gate shown in Figure 12.5. Verify the correct operation; Use DIO 0 and 1 as the inputs (located on the right side of the workstation). Connect the output signal to LED 0 (located on the right side of the workstation).

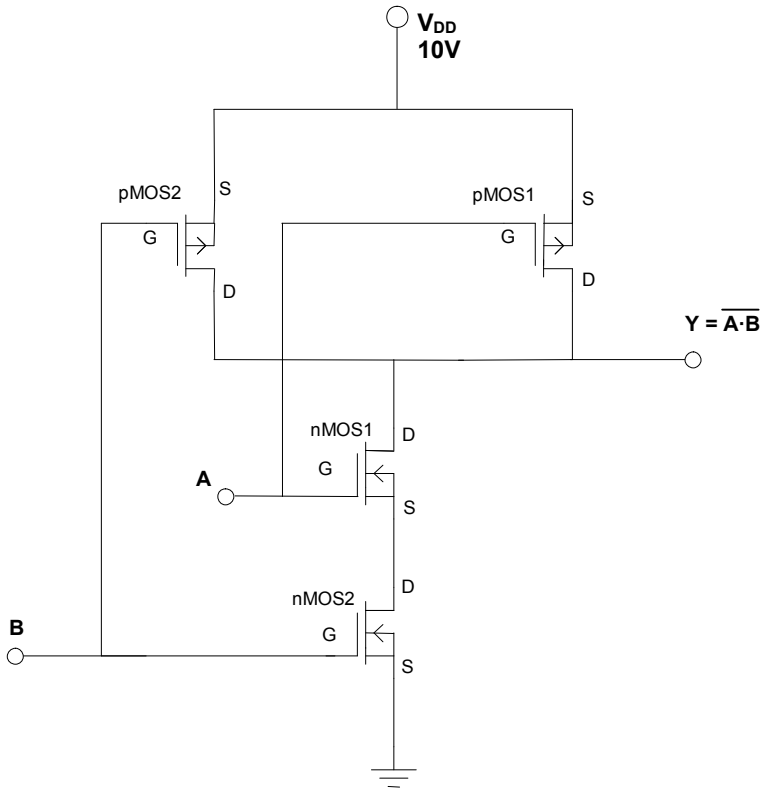


Figure 12.5: CMOS NAND Gate

8. Manually change the logic level of both inputs using the DigOut Digital writer. Observe the LED output signal and develop the truth table for the NAND gate as shown in Table 12.2.

Table 12.2: Truth Table for NAND Gate

Input A	Input B	Output Y
0	0	
0	1	
1	0	
1	1	

LAB REPORT:

Your report should include the following:

1. A discussion of your results in steps 4, 5, and 6, including truth tables, maximum operating frequency, and the effect of load on the operating frequency.
2. Compare the behavior of your circuit to the results of your simulation. Determine the rise, fall, and delay times.
3. A truth table of the NAND gate you built in step 7.
4. Your conclusions.

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Appendix A:
Summary on Report Writing

The report structure given in the Introduction to this manual is very detailed. This attempts to point out the essentials of a properly composed report. Many students do not seem to grasp how an engineering report needs to be structured in a systematic manner. The sections that should be included in a report may be outlined as follows:

1. Introduction:

   In this section the theoretical background to the experiment should be described briefly at least one page in length.

2. Experimental setup:

   In this section the experimental setup must be described, detailing the instrumentation used and what purpose each piece of equipment serves in the overall experiment. This information should be presented in a brief and concise manner.

3. Predicted results:

   The expected results can be outlined here. Typically these would be simulations obtained from SPICE. Each result needs to be explained briefly. This section, as well as sections 1 and 2, in effect constitutes the pre-lab report as well as the introductory sections of the overall final report for the experiment.

4. Discussion of results:

   This should be a very detailed section on the results obtained. In other words the experimental steps taken need to be presented one after another. The results should not just be listed. One should simply follow through all the steps completed in the experiment and for each step list the results obtained in a table or in the form of a figure. Each experimental step needs to be outlined in words, stating exactly what was done, followed by the corresponding results.

5. Results:

   In the Conclusion the results obtained need to be explained. Basically what one has to do here is explain how the results measured and listed in the "Discussion" compared to the predicted results, and hence whether or not the experimental results corroborated the theory presented in the "Introduction". It is common practice to mention by how much the measured results differed from the predicted results. Typically, if the deviations are less than 5%-10% one can say that the predicted results corresponded to the measured results within a reasonable margin of error i.e. the theory has been verified. Therefore the conclusion is what should be concentrated on the most. The information presented in this section should be detailed. This section should be typically 1 to 1.5 pages long, and will carry the greatest amount of weight in the overall grade awarded.

Appendix B:
Tektronix Type 576 Curve Tracer Introduction

Figure B.1: Overview of Tektronix type 576 curve tracer

Figure B.2: Oscilloscope Controls

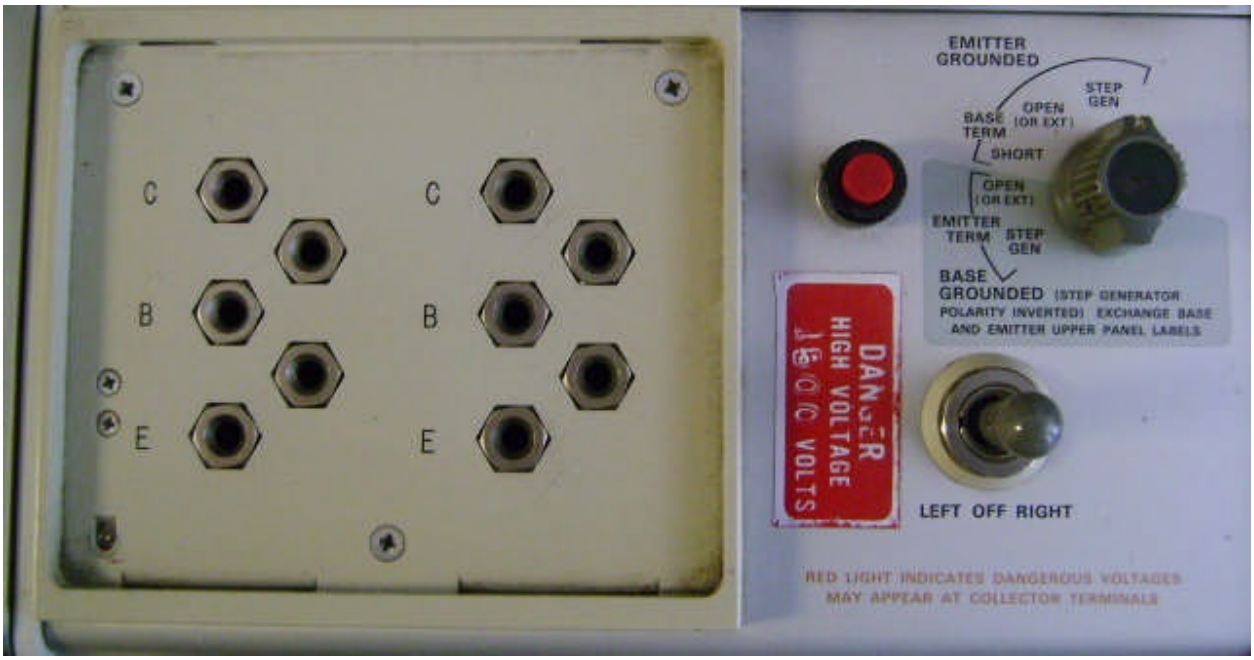


Figure B.3: Test Fixture and Terminal Selector Switch

Figure B.4: Step-Generator Controls

Figure B.5: Collector Supply

The following procedure allows the operator to become familiar with the front panel controls and their functions, as well as how they may be used to display transistor or diode characteristics. This procedure may also be used as a general check of the instrument's performance.

1. Apply power to the Type 576 Curve Tracer.
2. Allow the instrument to warm up for a few minutes. Instrument should operate within specified tolerances 5 minutes after it has been turned on.
3. Set the Type 576 and Standard Test Fixture front panel controls as follows:

READOUT ILLUM	Fully counterclockwise
GRATICULE ILLUM	Fully counterclockwise
INTENSITY	Fully counterclockwise
FOCUS	Centered
VERTICAL	1mA
DISPLAY OFFSET	NORM (OFF)
CENTERLINE VALUE	0
HORIZONTAL	1V COLLECTOR
Vertical POSITION	Centered
Vertical FINE POSITION	Centered
Horizontal POSITION	Centered
Horizontal FINE POSITION	Centered
ZERO	Released
CAL	Released
DISPLAY INVERT	Released
MAX PEAK VOLTS	15
MAX PEAK POWER WATTS	0.1 (Pull and turn)
VARIABLE COLLECTOR SUPPLY	Fully Counterclockwise
POLARITY	AC
MODE	NORM
NUMBER OF STEPS	1
CURRENT LIMIT	20 mA
AMPLITUDE	0.05 µA
OFFSET	ZERO (Pressed)
STEPS	Pressed

PULSED STEPS	Released
STEP FAMILY	REP ON
RATE	NORM
POLARITY INVERT	Released
STEP MULT .1 X	Released
Terminal Selector	BASE TERM STEP GEN (EMITTER GROUNDED)
LEFT-OFF-RIGHT	OFF

4. Turn the GRATICULE ILLUM control throughout its range. Note that the graticule lines become illuminated as the control is turned clockwise. Set the control for desired illumination.
5. Turn the READOUT ILLUM control throughout its range. Note that the fiber-optic readouts and the readout titles become illuminated as the control is turned clockwise. Set the control for the desired readout illumination. The readout should read for these initial control settings; 1 mA per vertical division, 1 V per horizontal division, 50 nA per step and 20k β or g_m per division.
6. Turn the INTENSITY control clockwise until a spot appears at the center of the CRT graticule. To avoid burning the CRT phosphor, adjust the INTENSITY control until the spot is easily visible, but not overly bright.
7. Turn the FOCUS control throughout its range. Adjust the FOCUS control for a sharp, well-defined spot.
8. Turn the vertical FINE POSITION control throughout its range. Note that the control has a range of at least ±2.5 divisions about the center horizontal line. Set the control so that the spot is centered vertically on the CRT graticule.
9. Repeat step 8 using the horizontal FINE POSITION control.
10. Turn the vertical coarse POSITION switch. Note that the spot moves 5 divisions vertically each time the switch is moved one position. (The extreme positions of the switch represent 10 divisions of deflection, which in this case causes the spot to be off the CRT graticule.) Set the POSITION switch to the center position.
11. Repeat step 10 using the horizontal coarse POSITION switch.
12. Set the POLARITY switch to - (PNP). Note that the spot moves to the upper right corner of the CRT graticule.
13. Set the POLARITY switch to + (NPN). Note that the spot moves to the lower left corner of the CRT graticule.
14. Connect a 100kΩ resistor to the C and E right sides terminals of standard test fixture.
15. Set the LEFT-OFF-RIGHT switch to RIGHT and turn the VARIABLE COLLECTOR SUPPLY control until a trace appears diagonally across the CRT.
16. Turn the VERTICAL switch clockwise and note that as the vertical deflection factor decreases the slope of the line increases. Turn the VERTICAL switch counterclockwise from the 1mA position and note that the slope decreases. Also note that the PER VERT DIV readout changes in accordance with the position of the VERTICAL switch. Reset the VERTICAL switch to 1 mA.

17. Repeat step 17 using the HORIZONTAL switch **within the COLLECTOR range of the switch**. The change in slope of the trace will be the inverse of what it was for the VERTICAL switch. Reset the HORIZONTAL switch to 1V COLLECTOR.
18. Press the ZERO button. Note that the diagonal trace reduces to a spot in the lower left corner of the CRT graticule. This spot denotes the point of zero deflection of the vertical and horizontal amplifiers. Release the ZERO button.
19. Press the CAL button. Note that the diagonal trace reduces to a spot in the upper right corner of the CRT graticule. The position of this spot indicates 10 divisions of deflection both vertically and horizontally. Release the CAL button.
20. Press the DISPLAY INVERT button and turn the VARIABLE COLLECTOR SUPPLY control counterclockwise. Note that the display has been inverted and is now originating from the upper right corner of the CRT graticule. Release the DISPLAY INVERT button.
21. Turn the MAX PEAK VOLTS switch to 75V. Note that the yellow light comes on.
22. While the yellow light is on, turn the VARIABLE COLLECTOR SUPPLY control fully clockwise. Note that the diagonal line obtained in step 15 does not appear. When the yellow light is on, the Collector Supply is disabled.
23. Set the following Type 576 controls:

MAX PEAK VOLTS	75
VARIABLE COLLECTOR SUPPLY	Fully counterclockwise
LEFT-OFF-RIGHT	OFF

24. Install the protective box on the Standard Test Fixture.
25. Close the lid of the protective box and set the LEFT-OFF-RIG HT switch to RIGHT. Note that the yellow light turns off and the red light turns on.

WARNING

The red light indicates that dangerous voltages may appear at the collector terminals of the Standard Test Fixture.

26. Turn the VARIABLE COLLECTOR SUPPLY control slowly clockwise until there is a noticeable trace (DO NOT ADJUST TO FULL 100%). Note that the diagonal trace appears indicating that the Collector Supply has been enabled.
27. Set the following Type 576 controls to:

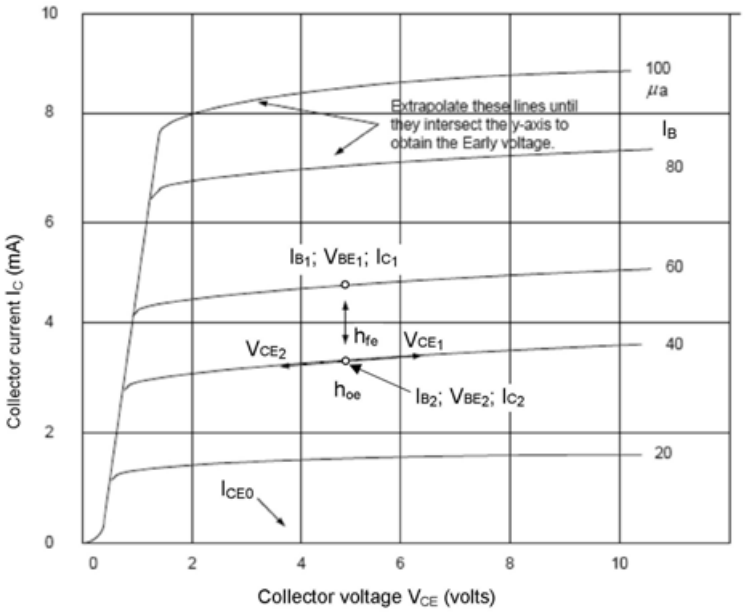
MAX PEAK VOLTS	15
VARIABLE COLLECTOR SUPPLY	Fully Counterclockwise

    (The protective box may be removed if desired.)
28. Turn the VARIABLE COLLECTOR SUPPLY control to about 20% reaches the center of the CRT graticule. Pull out on the PEAK POWER WATTS switch and set it to 0.5W. Note that the diagonal trace lengthens as the switch is turned through its range. Also note that the SER I ES RESISTORS decrease as the maximum peak power is increased.
29. Set the following Type 576 controls to :

LEFT-OFF-RIGHT	OFF
VARIABLE COLLECTOR SUPPLY	Fully Counterclockwise
HORIZONTAL	2V COLLECTOR

DISPLAY OFFSET	NORM (OFF)
CENTERLINE VALUE	0
Vertical POSITION	Switch Centered
POLARITY	+ (NPN)
MAX PEAK POWER WATTS	0.5W

30. Disconnect the resistor and connect the E, B and C terminals of the right side terminal of the standard text fixture to the E, B, and C terminals of a silicon NPN transistor 2N3904 or 2N222.
31. Set the LEFT-OFF-RIGHT switch to RIGHT and turn the VARIABLE COLLECTOR SUPPLY clockwise until the peak collector-emitter voltage is about 10 volts.
32. Turn the AMPLITUDE switch to 10µA.
33. Turn the NUMBER OF STEPS switch clockwise to 5.
34. Record some points (I_b, I_C and V_C) on the transistor characteristics. The importance of using the curve tracer to measure transistor characteristics will become evident when transistor circuits are discussed in ECE 320. You will need to experimentally determine the I-V characteristics of your bipolar transistors at the start of several of the experiments you will perform. Your transistor characteristic should resemble the characteristic shown below. Sketch this transistor characteristic using the values you recorded. Note than I_b= {0, 10, 20, 30, 40, 50µA}.



Typical I-V characteristic curves

Appendix C:
Tektronix Type 576 Curve Tracer Operating Manual

This section includes steps for acquiring the following measurements:

- *Diode forward I-V characteristics*
- *Diode forward and reverse I-V characteristics at the same time*
- *IC vs. VCE characteristics for a BJT*
- *ID vs. VDS characteristics for a FET*

Steps for acquiring diode forward I-V characteristics

1. Connect anode and cathode of diode to collector and emitter terminals of the right hand side terminal of standard text fixture.
2. Apply power to the Type 576.
3. Allow the instrument to warm up for a few minutes. Instrument should operate within specified tolerances 5 minutes after it has been turned on.
4. Set the Type 576 and Standard Test Fixture front panel controls as follows:

LEFT-OFF-RIGHT	OFF
VARIABLE COLLECTOR SUPPLY	Fully Counterclockwise
VERTICAL	0.1mA
DISPLAY OFFSET	NORM (OFF)
CENTERLINE VALUE	0
HORIZONTAL	0.2V COLLECTOR
Vertical POSITION	Centered
Vertical FINE POSITION	Centered
Horizontal POSITION	Centered
Horizontal FINE POSITION	Centered
ZERO	Released
CAL	Released
DISPLAY INVERT	Released
MAX PEAK VOLTS	15
MAX PEAK POWER WATTS	0.5

POLARITY	+NPN
MODE	NORM
NUMBER OF STEPS	1
CURRENT LIMIT	20 mA
AMPLITUDE	0.5 µA
OFFSET	ZERO (Pressed)
STEPS	Pressed
PULSED STEPS	Released
STEP FAMILY	REP ON (Pressed)
RATE	NORM
POLARITY INVERT	Released
STEP MULT .1 X	Released
Terminal Selector	BASE TERM STEP GEN (EMITTER GROUNDED)

5. Set the LEFT-OFF-RIGHT switch to RIGHT and turn the VARIABLE COLLECTOR SUPPLY control clockwise until you can determine the turn-on voltage (or the upper current limit). Note the display of the forward voltage characteristic of the diode. Adjust VERTICAL and HORIZONTAL settings as necessary.

Steps for acquiring diode forward and reverse I-V characteristics at the same time (e.g. for Zener diodes)

1. Connect anode and cathode of diode to collector and emitter terminals of the right hand side terminal of standard text fixture.
2. Apply power to the Type 576.
3. Allow the instrument to warm up for a few minutes. Instrument should operate within specified tolerances 5 minutes after it has been turned on.
4. Set the Type 576 and Standard Test Fixture front panel controls as follows:

LEFT-OFF-RIGHT	OFF
VARIABLE COLLECTOR SUPPLY	Fully Counterclockwise
VERTICAL	2mA
DISPLAY OFFSET	NORM (OFF)
CENTERLINE VALUE	0
HORIZONTAL	5V COLLECTOR

Vertical POSITION	Centered
Vertical FINE POSITION	Centered
Horizontal POSITION	Centered
Horizontal FINE POSITION	Centered
ZERO	Released
CAL	Released
DISPLAY INVERT	Released
MAX PEAK VOLTS	15 (Choose based on assumed reverse or Zener breakdown voltage. You might need protective box.)
MAX PEAK POWER WATTS	0.5
POLARITY	AC
MODE	NORM
NUMBER OF STEPS	1
CURRENT LIMIT	20 mA
AMPLITUDE	0.5 µA
OFFSET	ZERO
STEPS	Pressed
PULSED STEPS	Released
STEP FAMILY	REP ON
R ATE	NORM
POLARITY INVERT	Released
STEP MULT .1 X	Released
Terminal Selector	BASE TERM STEP GEN

5. Set the LEFT-OFF-RIGHT switch to RIGHT and turn the VARIABLE COLLECTOR SUPPLY control clockwise until the Zener breakdown voltage is visible. Note the display of the forward and reverse voltage characteristics of the diode. Adjust VERTICAL and HORIZONTAL settings as necessary.

Steps for acquiring I_C vs. V_{CE} characteristics for a BJT

1. Connect the terminals of the BJT to the appropriate terminals on the right hand side terminal of standard text fixture.
2. Apply power to the Type 576.
3. Allow the instrument to warm up for a few minutes. Instrument should operate within specified tolerances 5 minutes after it has been turned on.
4. Set the Type 576 and Standard Test Fixture front panel controls as follows:

VERTICAL	1mA
DISPLAY OFFSET	NORM (OFF)
CENTERLINE VALUE	0
HORIZONTAL	2V COLLECTOR
Vertical POSITION	Centered
Vertical FINE POSITION	Centered
Horizontal POSITION	Centered
Horizontal FINE POSITION	Centered
ZERO	Released
CAL	Released
DISPLAY INVERT	Released
MAX PEAK VOLTS	15
PEAK POWER WATTS	0.5
VARIABLE COLLECTOR SUPPLY	Fully Counterclockwise
POLARITY	+NPN
MODE	NORM
NUMBER OF STEPS	5
CURRENT LIMIT	20 mA
AMPLITUDE (IB/Step)	10 µA
OFFSET	ZERO
STEPS	Pressed
PULSED STEPS	Released
STEP FAMILY	REP ON

RATE	NORM
POLARITY INVERT	Released
STEP MULT .1 X	Released
Terminal Selector	BASE TERM STEP GEN (EMITTER GROUNDED)
LEFT-OFF-RIGHT	OFF

5. Set the LEFT-OFF-RIGHT switch to RIGHT and turn the VARIABLE COLLECTOR SUPPLY control clockwise until the peak collector voltage is 10V. Note the display of collector current vs. collector-emitter voltage for ten different values of base current. Adjust NUMBER OF STEPS, AMPLITUDE (IB/STEP), VERTICAL and HORIZONTAL settings as necessary.

Steps for acquiring I_D vs. V_{DS} characteristics for a FET

1. Install the universal FET adapter (Tektronix Part No. 013-009x-02) on the Standard Test Fixture and place an N-channel junction FET into the right test socket of the adapter.
2. Apply power to the Type 576.
3. Allow the instrument to warm up for a few minutes. Instrument should operate within specified tolerances 5 minutes after it has been turned on.
4. Set the Type 576 and Standard Test Fixture front panel controls as follows:

LEFT-OFF-RIGHT	OFF
VARIABLE COLLECTOR SUPPLY	Fully Counterclockwise
VERTICAL	1mA
DISPLAY OFFSET	NORM (OFF)
CENTERLINE VALUE	0
HORIZONTAL	1V COLLECTOR
Vertical POSITION	Centered
Vertical FINE POSITION	Centered
Horizontal POSITION	Centered
Horizontal FINE POSITION	Centered
ZERO	Released
CAL	Released
DISPLAY INVERT	Released
MAX PEAK VOLTS	15

MAX PEAK POWER WATTS	0.5
POLARITY	+NPN
MODE	NORM
NUMBER OF STEPS	5
CURRENT LIMIT	20 mA
AMPLITUDE (VGS/Step)	0.5V
OFFSET	ZERO
STEPS	Pressed
PULSED STEPS	Released
STEP FAMILY	REP ON
RATE	NORM
POLARITY INVERT	Pressed
STEP MULT .1 X	Released
Terminal Selector	BASE TERM STEP GEN

5. Set the LEFT-OFF-RIGHT switch to RIGHT and turn the VARIABLE COLLECTOR SUPPLY control slowly clockwise until the peak collector voltage is about 10V. Note the display of drain current vs. drain voltage for different values of gate voltage. Adjust POLARITY INVERT, NUMBER OF STEPS, AMPLITUDE (VG/STEP), VERTICAL and HORIZONTAL settings as necessary. **NOTE: Pressing the POLARITY INVERT button varies the gate voltage from 0V to -∞ in the negative direction. If the POLARITY INVERT button is released the gate voltage varies from 0V to ∞ in the positive direction.**

Cautions

1. At really low current settings, stray capacitance is a bigger issue and the curves become loops. You can use the LOOP COMPENSATION knob to adjust the curves when this occurs or assume an approximate best fit line.
2. When changing components always set LEFT-OFF-RIGHT to OFF and VARIABLE COLLECTOR SUPPLY to fully counterclockwise.
3. The small-signal short-circuit forward current transfer ratio (emitter grounded), h_{fe}, is $\Delta IC/\Delta IB$. To determine h_{fe} at various points in a family of curves, multiply the vertical separation of two adjacent curves by the β OR g_m PER DIV readout.

Appendix D:
Hameg HM6042 Curve Tracer Manual

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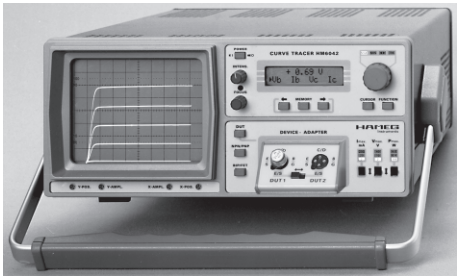
Curve Tracer HM6042

- **Ease of Operation**
- **Characterisation and Test of Semiconductor Devices**
- **Accurate Cursor Measurements**
- **Quick and easy Comparison of Semiconductors**
- **Reference Data Memory**
- **On-Screen Display of 5 Curves**
- **Low Power Consumption**



The **HM6042 Curve Tracer** is used to accurately display the characteristics of two and three terminal semiconductor devices. The instrument combines ease of operation and versatile features at an affordable price. Unlike its counterpart, the HM8042 plug-in unit, it uses a built-in **CRT** and an **LCD** to display the characteristics of the device under test.

The **HM6042** displays a set of 5 curves at a time. All numeric values and parametric data can be read out on a 2x16 digit **LCD**. Device type and all relevant parameters are selected and modified by a simple front-panel keypad entry. Collector voltage and current parameters are easily changed. A 3-step power limiter avoids damage of the **D**evice **U**nder **T**est by excessive power.

One set of parameters can be stored in memory for comparison of one device to another or a reference device. This feature gives substantial enhancements in productivity when matching semiconductors. Two cursors can be moved along the displayed curves. X and Y position of the cursor will be displayed on the screen. Basic accuracy is 2% of the measurement value. Measured parameters are: base voltage, base current, collector current, collector voltage and Beta. The dynamic parameters h11, h21, and h22 are **calculated** by the **internal processor**.

A device adapter socket with side-by-side terminals for two devices for the comparison of two semiconductors is supplied with the instrument.

The **HM6042** is remarkably easy to operate. This makes the instrument also ideally suited for educational use.

Specifications
(Reference Temperature 23°C ± 1°C)

Measurement Ranges
3 Voltage Ranges:
Collector/Drain Voltages ≤ 2V, 10V, 40V ±5%
3 Current ranges:
Collector/Drain Currents ≤ 2mA, 20mA, 200mA ±5%
3 Power Ranges:
Output Power ≤ 0.04W, 0.4W, 4W ±10%

Base-/Gate-Voltages and Currents:
I_b 1µA to 10mA V_b to 2V ±5% V_g to 10V ±5%

Accuracy
Accuracy of Static Values:
$V_{c/d}$ ± (2% o.v.[1] + 3 Dig.) $I_{c/d}$ ± (2% o.v. + 3 Dig.)
I_b ± (2% o.v. + 3 Dig.) V_b ± (2% o.v. + 3 Dig.)
V_g ± (3% o.v. + 3 Dig.)
β to 1000: ± (5 % o.v. + 3 Dig.)
to 100000: ± [(6 + 0.001 x β) % o.v. + 3 Dig.]

Accuracy of Dynamic Values:
h11 ≤ 1000Ω ± (12% o.v. + 3 Dig.)
≥ 1000Ω
± [(12 + 0.001 meas. value) % o.v.+ 3 Dig.]
h21 ≤ 1000 ± (12% o.v. + 3 Dig.)
≥ 1000
± [(12 + 0.001 meas. value) % o.v.+ 3 Dig.]
y21 ≤ 1000mS ± (12% o.v.. + 3 Dig.)
h/y22 ≤ 1000mS ± (12% o.v.. + 3 Dig.)

Miscellaneous
Reference measurement values can be stored for component selection.

Cursor Measurements:
Single mode: The Cursor marks the position from which the measurement value is calculated.

Tracking mode: Two Cursors mark the positions, from hich the h/y-Parameter measurement values are calculated.

Evaluation of curves from
Diodes, Zener Diodes, NPN/PNP-Transistors, FET/MOS-FET (N/P-Channel), Thyristors

Display: 2x16-Digit, LCD
Presentation of measurement values from a set of 5 curves on CRT.

General Information
CRT: D14-364GY/123 or ER151-GH/-, 6" rectangular screen (8x10cm) internal graticule
Acceleration voltage: approx. 2000V
Trace rotation: adjustable on front panel
Line voltage: 100-240V AC ±10%, 50/60Hz
Power consumption: approx. 36 Watt at 50Hz.
Min./Max. ambient temperature: 0°C...+40°C
Protective system: Safety class I (IEC 1010-1)
Weight: approx. 5.6kg, color: techno-brown
Cabinet: **W** 285, **H** 125, **D** 380 mm
1) o.v. = of value

1. General Information

The Curve Tracer **HM6042** is easy to operate. The logical arrangement of the controls allows anyone to quickly become familiar with the operation of the instrument. However, experienced users are also advised to read through these instructions so that all functions are understood. Immediately after unpacking, the instrument should be checked for mechanical damage and loose parts in the interior. If there is transport damage, the supplier must be informed immediately. The instrument must then not be put into operation.

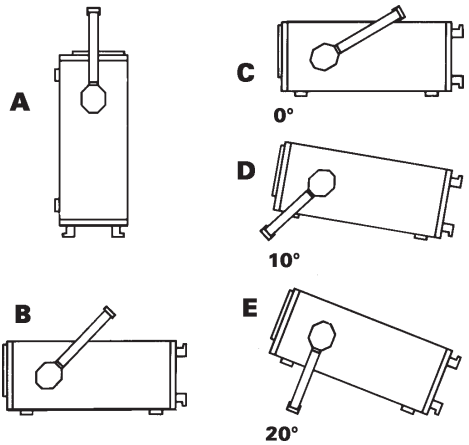
1. 1. Symbols used for the instrument


ATTENTION - refer to manual


Danger - High voltage


Protective ground (earth) terminal

1. 2. Tilt handle



To view the CRT screen from the best angle, there are three different positions (C, D, and E) for setting up the instrument. If the instrument is set down on the floor after being carried, the handle automatically remains in the upright carrying position (A). In order to place the instrument onto a horizontal surface, the handle should be turned to the upper side of the Curve Tracer (C). For the D position (10° inclination), the handle should be turned to the opposite direction of the carrying position until it locks in place automatically underneath the instrument. For the E position (20° inclination), the handle should be pulled to release it from the D position and swing backwards until it locks once more. The handle may also be set to a position for horizontal carrying by turning it to the upper side to lock in the B position. At the same time, the instrument must be lifted, because otherwise the handle will jump back.

1. 3. Safety hints

This instrument has been designed and tested in accordance with IEC Publication 1010-1, Safety requirements for electrical equipment for measurement, control, and laboratory use. The CENELEC regulations EN

61010-1 correspond to this standard. It has left the factory in a safe condition. This operating manual contains important information and warnings that have to be followed by the user to ensure safe operation and to retain the Curve Tracer in a safe condition. The case, chassis and all measuring terminals are connected to the protective earth contact of the appliance inlet. The instrument operates according to **Safety Class I** (three-conductor power cord with protective ground conductor and a plug with ground contact). The mains/line plug shall only be inserted in a socket outlet provided with a protective ground contact. The protective action must not be negated by the use of an extension cord without a protective conductor.

The grounded accessible metal parts (case, sockets, and jacks) and the mains/line supply contacts (line/live, neutral) of the instrument have been tested against insulation breakdown with 2200V DC. Under certain conditions, 50Hz or 60Hz hum voltages can occur in the measuring circuit due to the interconnection with other mains/line-powered equipment or instruments. This can be avoided by using an isolation transformer (Safety Class II) between the mains/line outlet and the power plug of the device being investigated.

Cathode-ray tubes normally emit X-rays. However, the dose equivalent rate falls far below the maximum permissible value of 36 pA/kg (0.5mR/h). Whenever it is likely that protection has been impaired, the instrument shall be made inoperative and be secured against any unintended operation. The protection is likely to be impaired if, for example, the instrument

- shows visible damage,
- fails to perform the intended measurements,
- has been subjected to prolonged storage under unfavorable conditions (e.g. in the open or in moist environments),
- has been subject to severe transport stress (e.g. in poor packaging).

1. 4. Operating Conditions

The instrument has been designed for indoor use. The permissible ambient temperature range during operation is +10°C (+50°F) ... +40°C (+104°F). It may occasionally be subjected to temperatures between +10°C (+50°F) and -10°C (+14°F) without degrading its safety. The permissible ambient temperature range for storage or transportation is -40°C (+14°F) ... +70°C (+158°F).

The maximum operating altitude is up to 2200 m; the maximum relative humidity is up to 80%. If condensed water exists in the instrument it should be acclimatized before switching on. In some cases (e.g. instrument extremely cold) two hours should be allowed before the instrument is put into operation. The instrument should be kept in a clean and dry room and must not be operated in explosive, corrosive, dusty, or moist environments. The Curve Tracer can be operated in any position, but the convection cooling must not be impaired. For continuous operation the instrument should be used in the horizontal position, preferably tilted upwards, resting on the tilt handle.

The specifications stating tolerances are only valid if the instrument has warmed up for 60 minutes at an ambient temperature between +15°C (+59°F) and +30°C (+86°F). Values without tolerances are typical for an average instrument.

1. 5. Warranty

HAMEG warrants to its customers that the products it manufactures and sells will be free from defects in materials and workmanship for a period of two years. This warranty shall not apply to any defect, failure or damage caused by improper use or inadequate maintenance and care. **HAMEG** shall not be obliged to provide service under this warranty to repair damage resulting from attempts by personnel other than **HAMEG** representatives to install, repair, service, or modify these products.

In order to obtain service under this warranty, customers have to contact and notify their distributor.

Each instrument is subjected to a quality test with ten-hour burn-in before leaving the factory. Practically all early failures are detected by this method. In the case of shipments by post, rail, or carrier it is recommended to preserve the original packing carefully. Transport damages and damage due to gross negligence is not covered by warranty.

In the case of a complaint, a label should be attached to the housing of the instrument that describes briefly the faults observed. If at the same time the name and telephone number (dialing code and telephone or direct number or department designation) is stated for possible queries, this helps towards speeding up the processing of warranty claims.

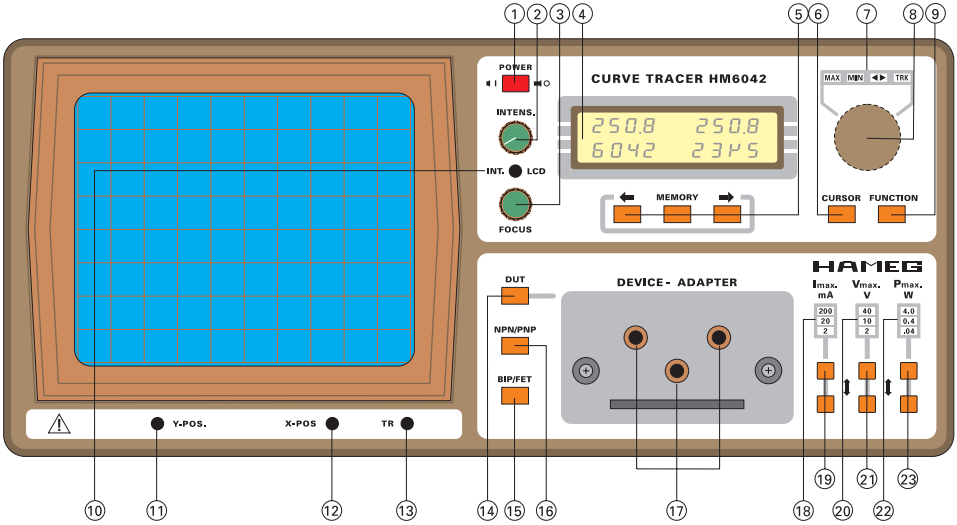
1. 6. Maintenance

Various important properties of the instrument should be checked carefully in certain intervals to ensure that all signals and measurement results are displayed with the accuracy on which the technical data are based.

The exterior of the instrument should be cleaned regularly with a dusting brush. Dirt that is difficult to remove on the casing and handle, the plastic and alloy parts, can be removed with a moistened cloth (99% water +1% mild detergent). Spirit or washing benzene (petroleum ether) can be used to remove greasy dirt.

The screen may be cleaned with water or washing benzene (but not with spirit (alcohol) or solvents), it must then be wiped with a dry clean lint-free cloth. Under no circumstances may the cleaning fluid get into the instrument. The use of other cleaning agents can attack the plastic and paint surfaces.

Front panel / Control elements HM6042



(1) POWER
Power switch (mains).

(2) INTENS
Adjust the beam intensity.

(3) FOCUS
Adjust the beam sharpness.

(4) DISPLAY (LCD)
Indicates measurement results and parameters.

(5) ← → (push buttons)
Select the parameters to be measured

(5) MEMORY (push button)
Store measured values and enable compare function

(6) CURSOR (push button)
Move cursor from curve to curve.

(7) TRK/ ◀▶ /MIN/MAX (LED bar)
Indicates the selected cursor function.

(8) Tune test voltages and currents.

(9) ↕ FUNCTION (push button)
Select one of the cursor functions.

(10) INT. LCD
Adjust the contrast of the LCD.

(11/12) Y-POS X-POS
Adjust the trace in vertical and horizontal position.

(13) TR
Adjust the trace rotation.

(14) DUT (push button)
Start/stop test, connect/disconnect the Device Under Test

(15) BIP/FET (switch)
Select between bipolar and field effect transistor/diode.

(16) NPN/PNP (switch)
Select between NPN and PNP transistors.

(17) E/S; C/D; B/G (jacks)
Mechanical and electrical connection for the DEVICE ADAPTER.

(18) 200mA, 20A, 2 mA (LED bar)
Indicates selected max. test current

(19) Imax. (push buttons)
Select max. test current.

(20) 40V, 10V, 2V (LED bar)
Indicates selected max. test voltage

(21) Vmax. (push buttons)
Select max. test voltage.

(22) 4W, 0.4W, 0.04W (LED bar)
Indicates selected max. test power.

(23) Pmax. (push buttons)
Select max. test power.

2. Set-up of the instrument

2. 1. Safety advice

Due to its measuring technique voltages up to 50 V are present at the 4 mm banana jacks, marked as E/S, C/D, and B/G. Therefore, it is assumed that the **HM6042** will only be operated by qualified personnel which is acquainted with the danger involved.

2. 2. General

The **HM6042** provides DC parameter characterization of 2- and 3-lead semiconductor devices like transistors, diodes and MOSFETs. Five characteristic curves displayed on the CRT's screen and digitized to be used for the calculation and indication of ten different parameters. Depending on the parameter to be measured one or two cursors enable the user to precisely select the point of measurement on one of the curves. The microprocessor-operated instrument is extremely versatile, yet remarkably easy to operate. Most of the instrument set-ups are done automatically by the instrument according to the selected measuring function.

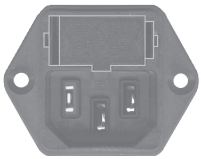
To use the **HM6042** no special expertise is required. The instrument is easy to set-up and operation is straightforward. Nevertheless, a few basic guidelines should be followed in order to ensure problem-free operation of the curve tracer.

2. 3. Selecting the line voltage

The instrument is able to operate with mains/line voltages of 115V AC and 230V AC. The voltage selection switch is located on the rear side of the instrument and indicates the voltage as set. The desired voltage can be selected using a small screwdriver.

Remove the power cable from the wall outlet prior to making any changes to the voltage setting. Fuses have to be replaced by fuses with an appropriate value (see table below) prior to connecting the power cable. Both fuses are accessible by removing the fuse cover located above the 3-pole power connector. The fuse holder can be released by pressing its plastic retainers with the aid of a small screwdriver. The retainers are located on the right and left side of the holder and must be pressed towards the center. The fuse(s) then can be replaced by pressing it/them in until locked on both sides. The use of patched fuses or a short-circuited fuse holder is not permissible; **HAMEG** assumes no liability for any damage caused as a result of incorrect fuse usage; all warranty claims become null and void.

Fuse type:
Size 5 x 20 mm; 250 V AC;
Must meet IEC specification 127,
Sheet III (or DIN 41 662 or DIN 41 571, sheet 3).
Time characteristic: time lag
Line voltage 115 V~ ±10 %: Fuse rating: T 315 mA
Line voltage 230 V~ ±10 %: Fuse rating: T 160 mA



2. 4. Screen settings

2. 4. 1. Adjusting the trace rotation

Due to influences of the magnetic earth field it may be necessary to compensate an angular misalignment of the trace. To adjust the trace into its horizontal position (in parallel to the bottom grid line) turn the TR potentiometer **(13)** located below the CRT screen with a small screwdriver. The DUT function may not be activated during this procedure.

2. 4. 2. Adjusting Y-POS./X-POS.

Normally the readjustment of the X and Y position of the trace is not necessary. However, if the left end of the trace is not aligned to the lower left corner of the grid you should adjust it to start at this point. To perform this procedure use the Y-POS. and the X-POS. screws, which are located below the CRT screen at the front panel of the instrument.

3. Performing device tests

As soon as the **HM6042** is switched on, a baseline is visible at the CTR screen as long as no DUT (Device Under Test) is inserted. A bright spot on the line indicates the current cursor position.

The standard device adapter, as supplied with each **HM6042**, is to be mounted to the instrument using the banana jack combination **(17)** at the front panel of the instrument. The terminals are designated as E/S (Emitter/Source), C/D (Collector/Drain), and B/G (Base/Gate).

This adapter is able to carry two DUTs; with the help of the instrument's memory function (see chapter 4. 3) and the device adapter's toggle switch device selections and component matching tests can be performed easily.

On request other device adapters are available from **HAMEG** to be used on the **HM6042** instrument.

If the standard device adapter is not suitable for special test purposes a DUT can be connected to the terminals using ordinary test cables. Their maximum length is limited to 25 cm each. The measurement accuracy of the instrument however can be degraded due to hum and noise on the cables. The use of shielded cables is not recommended because of their relatively high stray capacitance.

When using single wire connections extreme care has to be taken for safety purposes.

For testing diodes please use terminal E and C **(17)** and set the BIP/FET switch **(15)** to position FET (locked).

To start a test the push button DUT **(14)** has to be pressed. Immediately, the value of the selected parameter appears on the LCD.

The instrument can be toggled from its active to its inactive state by pressing the DUT key repeatedly; simultaneously the DUT will be disconnected from the internal test circuitry. The inactive state is indicated on the LCD by the message -off-.

3. 1. Choosing the DUT type

The **HM6042** has to be set-up according to the type of DUT (Device Under Test) to be proved.

To test NPN bipolar transistors switch BIP/FET **(15)** and switch NPN/PNP **(16)** has to be in released position. When working with PNP transistors switch NPN/PNP **(16)** has to be set into the locked position. As usual, the measurement is performed using the common-emitter circuit.

To test FETs set switch BIP/FET **(15)** into the locked position.

Diodes are tested with the same set-up as FETs using terminals E and C.

3. 2. Setting the test ranges

Through its range settings the instrument is enabled to limit the test voltage (U_{CE}, U_{DS}) and the test current (IC, ID) to predefined values. The ranges for current, voltage, and power can be selected by use of the push buttons for:

Imax **(19)**	200 mA	20 mA	2 mA
Vmax **(21)**	40 V	10 V	2 V
Pmax **(23)**	4.0 W	0.4 W	.04 W

The corresponding LEDs **(18)**, **(20)**, and **(22)** indicate the maximum value of the range as set. In test mode BIP the rotary knob enables the user to adjust the base current in incremental steps according to the selected range as defined below:

Range	Current (I_B)	No. of steps	Current / step
1	0.3 µA ... 100 µA	127	0.8 µA ± 10 %
2	3 µA ... 1 mA	127	8 µA ± 10 %
3	30 µA ... 10 mA	127	80 µA ± 10 %

The base current at the indicated cursor position is displayed on the LCD with IB/IG selected by the push buttons (← →, 5).

When FETs are under test the rotary knob **(8)** allows adjusting the gate voltage U_G between -10V to +10V in 256 incremental steps. This means 80mV/ step approximately.

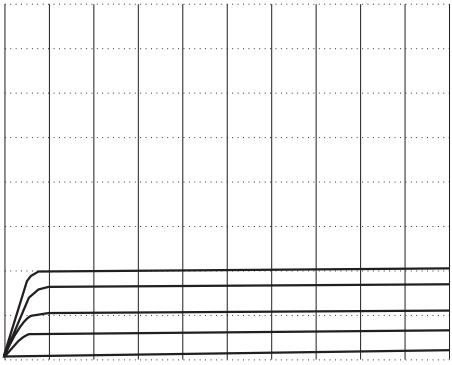


Figure 1

Five curves ($I_C = f(U_{CE})$, $ID = f(U_G)$) normally are displayed on the screen to represent the characteristic behavior of a transistor under test. After selecting the **MIN** or **MAX** setting with the push button called **FUNCTION (9)** the rotary knob can be used to modify the minimum/maximum base current/gate voltage in a sense that the five curves fit for the operating range to be evaluated. Please consider not exceeding the current and voltage settings beyond the DUTs power dissipation limits.

3. 3. Displaying curves

The Imax and Vmax settings determine the operating range for the test and define how the curves are going to be displaying on the CRT screen.

As shown in Figure 1, the upper edge of the grid represents the maximum value of the test current (I_C, I_D) according to the selected range (Imax = 200mA/ 20mA/ 2mA).

The right edge of the 8 x 10 screen grid represents the maximum value of the selected voltage range (Vmax = 40V/ 10V/ 2V).

The display is linear along both axes.

For example, if Vmax is set to 40V and Imax is set to 20mA the horizontal resolution will be 4V/DIV and a vertical resolution will be 2.5mA / DIV.

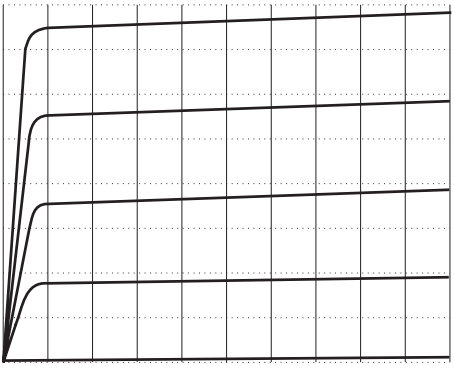


Figure 2

Using the **MIN** or **MAX** function **(9)** and then turning the rotary knob **(8)** allows you to position five characteristic curves on the screen and get the desired diagnostic results. Care has to be taken not to supersede the safe operating area of the device. Use the Vmax setup **(22)** to automatically limit the power applied to the device.

Please ensure that the DUT function has been activated for enabling the measurement.

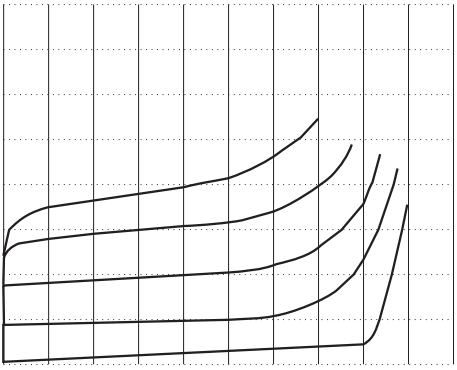


Figure 3

3. 4. Measuring device parameters

Generally, the behavior of transistors is determined by their static and dynamic parameters. To display the different parameter values on the display press one of the two bush buttons ← → **(5)** which are located below the LCD.

The screen cursor (highlighted dot) indicates exactly the point on the curve where the actual measurement happens to be done.

Please ensure that the DUT function has been activated to perform the measurement.

The following parameters can be measured and displayed by the instrument:

Static Parameters

V_B/V_G Base/Gate Voltage
I_B/I_G Base/Gate Current
I_C/I_D Collector/Drain Current
V_C/V_D Collector/Drain Voltage
β Current Gain

Dynamic Parameters

h11 Short-circuit input impedance
h21 Short-circuit forward-current transfer ratio
h22 Open-circuit output conductance
y21 Short-circuit forward admittance
y22 Short-circuit output admittance

3. 5. Using the cursor functions

The cursor (highlighted dot) indicates the point on a characteristic curve where the actual value is going to be digitized by the instrument. After the **HM6042** has been powered on, the cursor will appear on the third of the five characteristic curves.
The cursor can be repositioned by using the **CURSOR** switch **(6)** or the rotary knob **(8)**. With the **CURSOR** key **(6)** the cursor can be moved from one curve to the next. To move the cursor horizontally along a curve please select ◄ ►on the LED function bar **(FUNCTION 9, 7)** and turn the rotary knob **(8)** to reposition it in the desired direction.

The numerical value for the selected static parameter **(5)** will be displayed on the LCD in accordance to the actual cursor position.

When choosing the option to display one of the dynamic parameters h11, h21, or y21, a second cursor appears on the curve below. Turning the rotary knob, now moves both cursors horizontally along their respective curves. The **HM6042** digitizes the values as required at the highlighted positions and displays the calculated result on the LCD.

If you selected to test one of the dynamic parameters h22 or y22, the second cursor appears on the same curve beside the original cursor. Turning

the rotary knob **(8)** while function ◄ ►is activated **(9, 7)** will change the position of the second cursor.
After selecting function **TRK (9, 7)** and turning the rotary knob, now both cursors will be moved along the curve in their tracking mode. The **HM6042** digitizes the values at the highlighted positions and displays the calculated result for h22 or y22 on the LCD as requested.

The second cursor is only visible in the measuring mode for the dynamic parameters and will be switched on and off by the instrument automatically.

3. 6. Memory function, component matching

To support the easy selection of transistors (component matching), the **HM6042** provides a very helpful memory function. When pressing the **MEMORY** push button **(5)** the instrument stores the measured parameter internally and allows comparing the parameters of a second transistor with the value stored in memory. The second device under test should be mounted on the second test socket of the adapter. So, the selection of devices related to a reference component can be simply achieved by switching between the left and right socket of the adapter.

Thus the selection of components with respect to the displayed parameter (i.e. I_C/I_D, β, h11, h22, y21, or y22) is a rather easy and time saving task.

To quit the memory function or to use another transistor as reference component press the memory button **(5)** repeatedly.

4. Application examples

4. 1. Characteristic curves of a bipolar transistor

1. Connect the device to be tested to the appropriate input.
2. Ensure the BIP/FET switch **(15)** is set to the BIP position.
3. Select NPN or PNP as appropriate with the NPN/PNP switch **(16)**.
4. Select the appropriate range for the maximum current **(Imax) (19)**, maximum voltage **(Vmax) (21)**, and maximum power **Pmax (23)**.
5. Press the DUT switch **(14)**. Five curves (see Figure 1 or 2) now will be visible on the screen.

   Components under test can have higher temperatures. Please be careful when handling components having been connected to the test instrument.

6. The vertical position of the curves $I_C = f(U_{CE})$ is determined by the base current IB as parameter and can be adjusted stepwise by turning the rotary knob **(8)** while **FUNCTION (9, 7)** is set to **MAX** or **MIN**. With **MAX** selected base current for the top curve will be set, with **MIN** selected that for the bottom curve. The three curves between these two are going to be displayed in equal distances.

   After the **HM6042** is powered on, the base current is set to its minimum value.

7. Use the cursor functions **(FUNCTION (9), CURSOR (8))** and choose the parameter to be calculated by the instrument and displayed on the **LCD (← →, 5)** by pressing the appropriate keys.

4. 2. Characteristic curves of a field effect transistor

Testing a FET is similar to that for a bipolar transistor with respect of the following exceptions:

The BIP/FET switch has to be set to the FET position.

The vertical position of the curves $I_D = f(V_{DS})$ is determined by the gate voltage (U_G) parameter and can be adjusted stepwise by turning the rotary knob **(8)** with **FUNCTION (9)** set to **MAX** or **MIN**. With **MAX** selected the gate voltage for the top curve will be set, with **MIN** selected that for the bottom curve. The three curves between these two are displayed in equal distances.Choose the parameter to be calculated and displayed **(← →, 5)** on the LCD by pressing the appropriate key until you get the expected result.

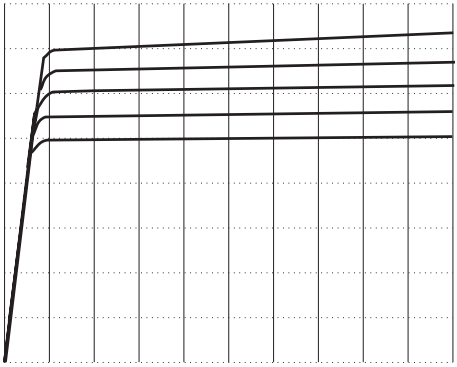


Figure 4

Security hint

Voltages up to 50V DC can be present at the device under test when using the following max. test voltages: V_D = 40V and V_G= -10V. Anyone using the test equipment needs to be advised of the possible danger and the proper precautions to be taken when working with voltages of this level.

4. 3. Component matching

1. Measure the desired parameter of the reference transistor (← →, 5), the DUT key **(14)** is activated.
2. Press the MEMORY push button **(5)** to store the parameters of the reference transistor and to enable the compare function. The character ? appears on the LCD, and - 0 - is displayed as the value.
3. Press the DUT push button once more and insert the transistor to be tested into the second socket of the adapter. Now toggle the adapter's switch to connect the second component to the instrument.
4. Press the DUT button again. Now, the numerical difference between the reference and the actually measured value of the selected parameter will be displayed on the LCD.
   Repeat steps 3. and 4. to test other components for matching.
5. Press the MEMORY push button again to return the test set to normal operation.