CPSC 3220 – Quiz #9 April 11, 2018 Name: __**Answer Key**__

1. Most modern computer systems choose a page size of 4 KB.

a) (2 points) Give one reason why doubling the page size might increase performance.

(any one is valid)
1. If the program exhibits spatial locality (at the new page granularity), then both page n and page n+1 are needed at the same time, reducing page faults.
2. Likewise, page n and page n+1 can be evicted at the same time.
3. Increasing the page size increases the range of addresses that can be translated by a fixed number of entries in the TLB.
4. Fewer pages implies fewer use/modified bits to keep track of.
5. Fewer pages implies less space taken up by page tables, leaving more room for useful pages, decreasing page faults.

b) (2 points) Give one reason why doubling the page size might decrease performance.

(any one is valid)
1. If the program exhibits no spatial locality (at the new page granularity), there will be less room for useful pages, increasing page faults.
2. Likewise, whenever any part of i is referenced, both subpages are marked as recently used, even if the other half is not being used.
3. Internal fragmentation if application memory regions are small com- pared to the new page size.
4. Disk access time is increased slightly, as both pages need to be writ- ten/read from disk, even when only one is needed.

2. For each of the following statements, indicate whether the statement is true or false, and explain why.

a) (2 points) A direct mapped cache can sometimes have a higher hit rate than a fully associative cache (on the same reference pattern).

True, FIFO scan with a working set larger than then the cache size
A direct mapped cache limits the flexibility of the cache replacement algorithm. In each slot, only the most recently referenced cache block can be saved. With a fully associative cache, the cache replacement algorithm is free to evict any cache block, even one that is about to be used.
A FIFO scan that is slightly larger than the cache size, a direct mapped cache will have cache hits on most references, missing only where two blocks from the scan map to the same cache entry.
By contrast, if the fully associative cache uses a least recently used policy, it will cause a cache miss on every reference to a new cache block.

Continued on Back

b) (2 points) Adding a cache never hurts performance.

False, a scan pattern that is purely random.
If the reference pattern is purely random, with no locality, or if the replacement policy is a poor fit for the reference pattern, then the cache will not help performance. Instead, it will add useless overhead for consulting the cache that could be avoided.

3. Suppose an application is assigned 4 pages of physical memory and the memory is initially empty. It then references pages in the following sequence: ACBD BAED FBCF AEFA

a) (2 points) Show how the system would fault pages into the four frames of physical memory, using the FIFO replacement policy.

	A	C	B	D	B	A	E	D	F	B	C	F	A	E	F	A
1	A					+	E							+		
2		C							F			+			+	
3			B		+					+	C					
4				D				+					A			+

b) (2 points) Show how the system would fault pages into the four frames of physical memory, using the LRU replacement policy.

	A	C	B	D	B	A	E	D	F	B	C	F	A	E	F	A
1	**A**					**+**				**B**				**E**		
2		**C**					**E**				**C**					
3			**B**		**+**				**F**			**+**			**+**	
4				**D**				**+**					**A**			**+**