- ON SCRATCH PAPER WRITE BINARY 0 to F!

 An embedded system is an electronic system controlled by one or more computers/microprocessors that are internal to the system. That is, the system is not thought of as a computer, but something else. An example of a system that needs to be a "realtime" system and what
- the functionality of it is in real time: Air traffic control system the current location.

 - A microcontroller is a "computer on a chip"
- Who makes the processor discussed in this class? There are two answers: Microchip Founded 1987.
- A real-time system must insure that a task is completed within a
- certain time span.

 Name five things discussed in class, which must be considered when designing an embedded System. Real-Time Execution; Physical Size and Environment; Power Consumption; User Interface; Multirate Operation; Cost; Memory Needs; Hardware versus Software

Operation; Cost; Memory Needs -Old chip was: Mips32 M4K Core -In a time span: real-time system -Diagnostic PIC32: JTAG

-Diagnostic PIC32: J1AG
-Functions: CTMU, Timer, PWM, ADC, UART, SPI, RTCC, Compare -CTMU External Input Pins : 11

- The HC12 has two 8bit accumulators, A and B, which can be ganged

together
- The HC12 has two 8-bit accumulators, which can be ganged together.
- The HC12 has at most 128-kB of flash on board.

*What is the size of the registers in (in bits) of the HC12 processor? - What size are the standard addresses (in bits) of the HC12 processor?) ie. "The HC12 is a __-bit machine." 16
- The HC12 is a __-bit machine." 16
- The HC12 has a maximum 8 MHz bus clock.
- The HC12 has a 16-bit stack pointer.

The program counter in the HC12 is 16 bits The HC9S12 was an improvement on the HC12 and has a maximum 25-MHz Clock

The HC9S12 has at most 512-kB of flash on board The HC12 has two [a]-bit registers, X and Y. 16

How is SRAM generally used in a system? Lvl1 cache, Lvl 2 cache,

NVRAM

What type of Memory is used to store variables in a(n) (embedded) system? RAM, Volatile, SRAM, DRAM

- *What is the advantage of using DRAM over SRAM? Lower power at use, Higher Density, Less expensive. - *What type of memory is made out of transistors? (What type of RAM is

made out of transistors?) SRAM
- Which of the following is volatile? SRAM, DRAM, SDRAM

What type of memory is used to store the Stack in an embedded system? RAM, Volatile, SRAM, DRAM -Which type of memory is generally used to store system states in an embedded system? ROM, NonVolatile, PROM, EPROM, EEPROM

 What type of memory is generally used to store Program Instructions in an embedded system? ROM, NonVolatile, PROM, EPROM, EEPROM embedded system? ROM, NonVolatile, PROM, EPROM, EEFRO - What is the advantage of using SRAM over DRAM? Lower power consumption (at rest), Simpler to implement, Faster, Can be placed on

consumption (at rest), simpler to implement, rasker, Can be place same die as processor logic

- What type of memory is generally used to store User Settings in an embedded system? ROM or NonVolatile or PROM or EPROM or EPROM or

Which of the following are nony EEPROM. EPROM. NVRAM. OTP ROM.

Flash, Masked ROM, PROM.

- Which type of RAM stores its data using small capacitors? DRAM





Flowchart, how many times does the programmer try to program a difficult cell before it quits? 10

cell before it quits? 10

- Timing diagram, how long must programmer wait to insure the DATA is valid after the EPROM is told to output the cell data written to it? tDV

- Flow chart, how does the programmer program the EPROM? Programs all the cells, then checks each one for validity

use crus, user CRECKS each one for validity
-Timing diagram, at what point in time does the EPROM programmer read
the DATA to be verified from the bus? The second rising edge of CE#
-Timing diagram, how long must the DATA be stable before the EPROM
latches the data into memory? (D8) Timing diagram, how long must the ADDRESS be stable before the EPROM

latches data into memory? tAS what signal tells the EPROM to output the cell data which Timing diagram, what was written to it? CE#

was written to it? CE#

- Timing diagram, at what point in time does the EPROM read the DATA it is to program into its cell? The first rising edge of CE#

Timing diagram, how long must the programmer leave the ADDRESS on the bus after they have read the data to be verified? tAH

Timing diagram, what signal determines when the EPROM reads the data to e programmed into the cell? CE#

New Section Name four different things that you generally find on a microcontroller project board. Reset Switch; Com Ports; LCD Display; 7Segment Display; LEDs; Keypad/Switches; Amplifiers/Op Amps; OptoIsolators; Relays; SCRs/Triacs; Buzzers; Potentiometers; DACs; Dip

- What's the name of an electromechanical device that is used to switch higher

=Start Code, 1=Record Type, 11=Byte Count, 0038=Address, [42]=Data

What is circuitry that is used to interface two different chips together called?

- what is circuity that is used to interface two different emps together cancer.
Glue logic

- What kind of IC is used to isolate a low voltage microprocessor circuit from a higher voltage motor circuit? Opto-isolator

- What is the name for a program which takes C code written on a computer

- What is the name on a plogatin which alsees Code within the order of the and creates code for a microprocontroller? That is, it creates for a processor other than the one it runs on. Cross Compiler

- What is the name for software and/or hardware which allows you to start and stop execution and examine the state of the processor while it is executing

your code? **Debugger**- What is the name for the file generated by a compiler to run on a

- What is the name to the nie generated or y a compiler to run on a Motorolal Freescale processor? \$1978-record with fire freescale processor? \$1978-record a volume control in audio devices. Act as a variable resistor - What is a relay used for in a circuit? Relays can control current flow without having hardware/physical device and can degrade of time without having hardware/physical device and degrade of time

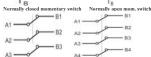
- What are dip switches used for in an embedded system? For setting up various configuration options

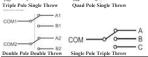
How is a "momentary switch" different than a regular "on/off" switch? - How is a "momentary switch" different than a regular "on our switch? Momentary is like a push button, on/off switch is like light switch.
- What do you call a switch that is normally off, and must be held down (depressed) to be on? That is, once it is released it is off again. Push Button Switch! Momentary Switch.

What does SPST on a relay stand for? Single Pole Single Throw

- What does DPDT on a relay stand for? **Double Pole Double Throw**- What does SPDT on a relay stand for? **Single Pole Double Throw** B Single Pole Double Throw

COM1 COM2-Double Pole Single Throw





- The "256" in the part number MC9S12DP256B refers to the amount of

- The term glue logic refers to the added circuitry necessary to interface two or more chips together.

The flash memory in the chip is used to hold code instructions for the chip.

What signal from the MC9S112 is used in conjunction with the R/W# line to

what signal norm are NC-95112 is used in conjunction with the re-war interference of the first size being read? LSTRB
 Which of the following is/are not found on the MC9S12? Pieze Electric Buzzer, Digital to Analog Converter, Temperature Sensor
 What type of data/information is stored at the upper end of the MC9S12

memory map? Interrupt Vector Table - The [a] memory in the chip is used to hold code instructions for the chip.

- The [a] memory in the chip is used to hold code instructions for the chip. Flish
- What is a compiler called which generates code for a process other than the one it is running on? Cross Compiler
- What signal from the MCOS12 is used to determine whether or not a memory chip is being read from or written to? RVW#

emp is being read from or written to? ICW##

- What type of memory is located at the very beginning (lowest addresses) of
the MC9S12 Memory Map by default? Registers

- What type of memory in the 9S12 would you use to store program setting in?

What signal from the MC9S12 is used for memory reads when external - What signal norm the WO-312 is used in finding the data when the memory is used, but is not used in single chip mode? LSTRB
-What signal is shown at the top of the timing diagram? (As indicated by a '?')

- N - K - K 8 - X - X - X

Clear PTH: PTH = PTH & 0x52; Analog: ANSELxSET = 0xA000 Digital: ANSELxCLR = 0xA000: Change Notice Interrupt Disable: CNENxCLR = hex Enable: CNENxSET = hex; Internal Pull Down Enable: CNPDxSET = hex: Disable: CNPDxCLR = hex

Internal Pull Up Enable: CNPUxSET = hex; Dishale: CNPUxCLR = hex: PORTx = read (value of pins) n = PORTx & 0xA234: I ATv = write Zeros: I ATyCI R = hey-

Outputs Open Drain: ODCxSET = hex; Outnuts Pull Push: ODCxCLR = hex;

Port[0] is right most port



Battery*(AmpHour/24*30*months or 24*365*year) = Avg Draw Need(x) ± Don't Need(1-x) = Avg Draw

What is the purpose/function of a pull-down resistor? Pulls an input down to a zero by latching it to ground

to a zero by latering it to ground

- Give an advantage and disadvantage of using isolated(port-based I/O. Pro

- Simultaneous memory and I/O. Cons- Additional pins needed for address,
data, controls; additional instructions needed to access the I/O bus What latch chip was used in class to write to I/O devices? 74374

(What does the following line of C instruct the compiler to do? What does it allow the programmer to do? (What does unsigned char do?) (What does

volatile mean?) #define PTH *(volatile unsigned char *\0x260

Variable can be changed from outside the program (external device can drive high/low)

- Give an advantage and disadvantage of using memory-mapped I/O. Pro many operations, no addition pins or instructions necessary: Con- I/O many operations, no addition pins or instructions necessary; Con-I/O error on a memory map cannot be caught and results in program crashing, less memory can be addressed.

- Give an advantage and disadvantage of using "linear select addressing of

I/O. Pro - Simple selection logic and one port per address-line; Con -Wasteful Addressing
- Why is a latch needed to store the address from the 9S12 when

- Why is a latch again with an I/O device? Bus is multiplexed so address must stored while data is put on the bus
- Why is the 373 Latch's G input connected to 5 volts? The latche's G input

is not-ed so it has to connect to 5 volts to make it a zero.
-What is the difference between the 74-373 and the 74-374? 74373 uses an enable, 74374 latches values on the rising edge of a clock What latch chip was used in class to read from I/O devices? 74373 -*What is a typical size/value of a pull-up/ pull-down resistor? 4.7KOhm -

10KOhm

IOKOhm

The ISA does not support serial I/O directly. Why? Because everything starts out as parallel within the CPU
Everything does in the CPU is done in parallel (not serial). Why? This is done because there are plenty of jobs that compute has to do and most all of them are performed individually. Therefore, parallelism makes everything WAY faster and other programs do not have to wait for another to complete before it executes.

- Why is it necessary to have the Latch on the left (light blue)?



It uses the clock pulse to latch the values from the address bus to the decoder. Prevents all values from being latched at once.

- An open drain output allows for "wired-Oring" or pins. True - An open dram output antwas for wired-fring or pins. Frue
- This register can be used to detect overloads or shorts at port pins. PTIn
- This register can be used to internally connect a resistor to form a port pin to
either Vcc or Vdd if the corresponding pin is set to input. PERn
- In order to know which pin an interrupt has occurred on, this register must be

read. PIFn A [a] resistor is generally used to make an input pin's default value 1. Pull

This register can determine whether the pull resistor is "pull-up" or "pull-

down". PPSn

This register can determine whether the interrupt is detected on either the rising edge or falling edge of a signal. PPSn

Which register is written to in order to change the values of a certain port's nice? PTS.

• What Port only has 4 pins instead of 8? J - Which register needs to be configured before ever outputting a value to a

- Which register needs to be configured before ever outputting a value to certain port pin? DDRn
- This register determines whether or not a transition on a port pin will produce an interrupt. PIEn

produce an interrupt. PIE.B -The ISA level directly supports serial instructions. False -Which register determines if port pins will be used as input or output? DDRn

- Which register determines if port pins will act as an OR gate when its pins are tied together, or not? WOMn

ster reads the state of the register buffer if reading a pin is set to - This register tells whether or not an interrupt has occurred a specific pin of a

port, PIFn

port. PIFn

- This register can be used to limit the amount of current supplied to a circuit connected to the corresponding port. RDRn

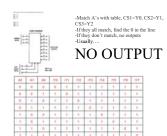
- This Register ignores data written to it if its pins are set up for input. PTn

The first address of an 6-K memory only is 144 K in a system with 20-bit addresses.

and every valid address for this chip has the form

- Everything beyond address line is an X

 Using values below, add up to get address number, place 1 where number is used (All values are in K(thousands)) used (All values are in K(tho 19=512,18=256,17=128,16=64,15=32,14=16,13=8,12=4,11=2,10=1





Fill in appropriate 1's or 0's to get correct output on each line
- If line is excluded, put an x => x can be 1 or 0
- Convert A19-A0 to hex



h EG and KI =>D0 to D7 is low order chin (E = D0, G = D7 -> low)

b. FG and KL=>D0 to D7 is low order chip (F = D0, G = D7 > low)

c. A19-A0=>Put 1 where A and B are, D's otherwise, convert to HEX

d. A19-A0=>Put 1 at A and B, at D put 1's onward, otherwise 0's

c. Big endian if LSTRB goes into low-order chip (high -> little endian)

Chip 0

Chip 0

Chip 1

Chip 2

Chip 2

Chip 3

Chip 3

Chip 4

Chip 5

Chip 5

Chip 5

Chip 1

- C and H are A1
- D and I=> take ending address, covert to binary, where bit's are all 1's, that

- D and E⇒ take ending address, covert to binary, where bit's are all 1's, 1 starting position is D and 1
 - E and J⇒7f big endian LSTRB goes into Low order chip, Little endian LSTRB goes into high order chip, A0 goes into opposite chip
 - FG and KL⇒Low order chip is D0-D7, other is D8-D15

-Chip 0 = 2\(^(D-10))

The upper address lines of a 25-bit address are to be connected to the inputs of a 10-input PAL to decode memory-mapped VC addresses in a system. The PAL is to generate a low signal when an achieve in the range 9x84800 - 0x84FFF

Convert both to binary=>Write starting address on top of ending - Put x where they start to differ and onward

DOBH = [a] PERH = [b] PIEH = [c] PPEH = [d] PDEH = [d]

DDRH=Either output or inverted input bits PERH=Pull Device Enabled Bits

PIEH=Interrupt Enabled Bits
PPSH=Rising Edge Triggered Interrupt bits and pull down bits

Hose would you set the following pins of Fort. It without affecting any other pins

Set bit(s) 2 3 4

Convert to Binary - If set, OR with PTH - If clear, AND with PTH

PTH | Ox Something

Clear bit(s) 1 4 6

- Convert to Binary=>Invert the binary number=>Convert to hex



Convert Port B to Binary => the rightmost bit is value of ADDR
- Match up other columns => ECLK=0, preparing ECLK=1, performing

PTJ = 0;

while ((PTH & 0x20) == 0);

- If while loop = 0=> Every bit that is a 1, put Port[x]=1

If while loop = 1=> No possible solutions

What is the value of ChangedSw (in hex) after this code is run? unsigned char OldSw = 0xD1; unsigned char NewSw = 0x1E; unsgined char ChangedSw;

ChangedSw = (OldSw ^ -NewSw) & -OldSw; Convert all to binary
 When raising binary to binary => bits are same, 0; bits are different, 1

Look where

unsigned char OldSw, NewSw, ChangedSw while (OldSw -- NewSw) NewSw - PTH; ChangedSw = (NewSw ^ OldSw) & -NewSw;

OldSw - NewSw - Use 1010 for Old->Use 1001 for new->Follow code, see what changed

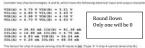
Rewrite Keypad as Circle keys pressed->0's if pressed->1's otherwise (in form of keypad)

For bitshifting-convert across to binary (Nott if needed)

Otherwise look at keypad and determine where button was pressed

Single button in row, it's that one; Two single buttons in two differ rows, it's the top button; Two buttons in same row or none pushed, it's 0

Switch on bottom ν_{cc} Το κΩ ξ PORT H[0] SW i = GND

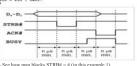


First look at II's->A to B make sure Max A>Min B if not A = 0
Repeat for B to A-> Max B>Min A if not B = 0

Repeat steps for IO's -If pass both test: A to B get minimum of IOH(A)/IIH(B) and IOL(A)/IIL(B) Whichever is min, that is = A -> Switch A and B's for B

whale ((FTS & 0x03) 1=0); PTS - PTS & -0801

MOP! PTJ - PTJ | 0=01;

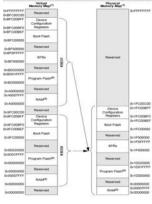


((#*N*(# of Mhz))/(clock ticks))-1 (don't use x10^-3 or any multiplier)

ADDRESS DECODING

-round up





Chip 0: 128 F3 Chip 1: 128 F3 Chip 2: 226 F3 Chip 3: 32 F3 Chip 4: 6 F3 Chip 4: 6 F3

Make a table

28 OFN

Pin#	Full Pin Name	Pin#	Full Pin Name
1	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	16	Vss
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	17	VCAP
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	18	PGED2/RPB10/D+/CTED11/RB10
5	Vss	19	PGEC2/RPB11/D-/RB11
6	OSC1/CLKI/RPA2/RA2	20	Vusasva
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13
8	SOSCI/RPB4/RB4	22	CVREFOUT/AN10/C3INB/RPB14/VBuson/SCK1/CTED5/RB14
9	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	Voo	24	AVss
11	TMS/RPB5/USBID/RB5	25	AVDD
12	Vaus	26	MCLR
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1

36 VTLA

Pin#	Full Pin Name	Pin #	Full Pin Name
1	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	19	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	20	RPC9/CTED7/RC9
3	PGED4 ⁽⁴⁾ /AN6/RPC0/RC0	21	Vss
4	PGEC4 ⁽⁴⁾ /AN7/RPC1/RC1	22	VCAP
5	VDD	23	Voo
6	Vss	24	PGED2/RPB10/D+/CTED11/RB10
7	OSC1/CLKI/RPA2/RA2	25	PGEC2/RPB11/D-/RB11
8	OSC2/CLKO/RPA3/PMA0/RA3	26	Vusasvs
9	SOSCI/RPB4/RB4	27	AN11/RPB13/CTPLS/PMRD/RB13
10	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	28	CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14
11	AN12/RPC3/RC3	29	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
12	Vss	30	AVss
13	VDD	31	AVoo
14	VDD	32	MCLR
15	TMS/RPB5/USBID/RB5	33	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0
16	Vaus	34	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1
17	TDI/RPB7/CTED3/PMD5/INT0/RB7	35	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0
18	TCK/RPB8/SCL1/CTED10/PMD4/RB8	36	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1

Pin#	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	ANB/RPC2/PMA2/RC2
6	Vss	28	Voo
7	VCAP	29	Vss
8	PGED2/RPB10/D+/CTED11/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/D-/RB11	31	OSC2/CLKO/RPA3/RA3
10	Vusesvs	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4/TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4/TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/VBuson/SCK1/CTED5/RB14	36	AN12/RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVDD	39	Vss
18	MCLR	40	Voo
19	PGED3//REF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	41	RPB5/USBID/RB5
20	PGEC3//REF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	42	Vaus
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

28 QFN

1 MCLR 2 POEDAN 4 POEDIA 5 POECIA 6 ANACIN 6 ANACIN 8 VACCIN 8 VACCIN 9 OPERICIA	Full Pin Name ICCTR OCCUPAGE - ACNEE - AND CLIN CEDEPAGE CED IFFE POECUNAL - ACNEE - AND READ CLIN CEDEPAGE CED IN PROCESS IN PRO	Pin # 15 15 15 15 15 15 15 15 15 15 15 15 15	Fell Pa Num Year TOKING BESCLICTED TOKING III TOKING BESCLICTED TOKING III VIS VIS
	PRE-ACHER-ANDCHACREDIFFER PRE-ACHER-ANDCHED SPRINGRANGE AND SPRINGRANGE SPRING		PB7/CTED3/PMICS/INTORIS PPB/S/CL1/CTED4/PMICS/R RPB/S/CTED4/PMICS/R
	PRE-VCNEF-JANDCSANCRPADICTED IPPI PRE-VCNEF-JAND RPA LICTED SPRINGRAL NAZCHADICZHBICZHAD RPED PAMORBI NAZCHADICZHAD REFECTED ZZEMA I REI		TORRESTCTEOMACSANTORBI COCKREBOOCLACTEODORACHAIII TORRESESSOATOTEOARMONRIII Visa
	/NEX-JCVREY-JAN1/RPA1/CTED2/PMD6/RA. NA2/C1/ND/C2N/B/C3/ND/RPB0/PMD0/RB/CANA/C1/ND/C2N/B/RP1/CTED2/PMD1/RB/RA/C1/ND/C2N/A/RPR1/CTED2/PMD1/RB/RA/C1/ND/C2N/A/RPR1/CTED2/PMD1/RB/RA/C1/ND/C2N/A/RPR1/CTED2/PMD1/RB/RA/C1/ND/C2N/A/RPR1/CTED2/PMD1/RB/RA/C1/ND/C2N/A/RPR1/CTED2/PMD1/RB/RA/C1/ND		TCKRPBSSCLICTED4PACMR TDORPSSSDAIKTED4PADSR VSS
	N2/C1INDIC2INB/C3IND/RPB0/PMD0/RBI		TDORPESINDANCTED4PMD3Rilli V5s
	ANSICTINC/CSINA/RPB1/CTED13/PMD1/RI		
		20	
	ANAICTINB/C2ND/RPB2/SDA2/CTED13/PMD2/RBC		
	ANS/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	21	PGED2/RPB10/D+/CTED11/RB10
Г		22	PGEC2/RPB11/D-/RB11
1	OSC1/CLK/IRPA2/RA2	R	Votesva
10 OSC2/CU	OSC2/CLKO/RPA3/PMAB/RA3	*	AN11/RPB13/CTPLS/PMRD/RB13
11 SOSCURPB4/RB4		×	CNEFOUTIAN10C3INB/RPB14Nb
12 SOSCOR	SOSCORPA4/T1CK/CTED9/PMA1/RA4	8	ANNICSINA/RPB15/SCK2/CTED6/FIII::::::::::::::::::::::::::::::::::
13 VDD		27	Wis
14 TMS/RPB	TMS/RPB5/USBID/RB5	25	AVEO

TABLE 4-1: SFR MEMORY MAP

9.90 9.000 An	Virtual Address					
Peripheral	Base	Offset Start				
Watchdog Timer		0x0000				
RTCC		0x0200				
Timer1-5		0x0600				
Input Capture 1-5		0x2000				
Output Compare 1-5		0x3000				
IC1 and IC2		0x5000				
SPI1 and SPI2		0x5800				
UART1 and UART2		0x6000				
PMP		0x7000				
ADC	0xBF80	0x9000				
CVREF		0x9800				
Comparator		0xA000				
СТМИ		0xA200				
Oscillator		0xF000				
Device and Revision ID		0xF220				
Peripheral Module Disable		0xF240				
Flash Controller		0xF400				
Reset		0xF600				
PPS		0xFA04				
Interrupts		0x1000				
Bus Matrix		0x2000				
DMA	0xBF88	0x3000				
USB		0x5050				
PORTA-PORTC		0x6000				
Configuration	0xBFC0	0x0BF0				

TABLE 26-2: PERIPHERAL MODULE DISABLE REGISTER MAP

988		Bits																	
(BF80_#) (BF80_#) Register Name(1)	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets	
E0.40	PMD1	31:16			_	-	-	-	_	-	-	_	_	-	_	-	-	-	0000
F240	PMDT	15:0	_	_	_	CVRMD	_	_	_	CTMUMD	_	_	_	-	_	_	_	AD1MD	0000
F250	PMD2	31:16	_		_	-	-	-	_	-	_	_	-	-	_	_		_	0000
F250	FWD2	15:0	-	-	-	_	-	_	-	_	_	_	_	_	_	CMP3MD	CMP2MD	CMP1MD	0000
F260	PMD3	31:16	_	_	_	_	-	_	_	_	_	_	_	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
F200	FINIDS	15:0	_	×-×	-	_	-	-	_	_	_	_	_	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
F270	PMD4	31:16	_	_	_		-	_	_	_	_	_	_	_		_	_	_	0000
F270	PMD4	15:0			-	-	-	-	_	_	_		-	T5MD	T4MD	T3MD	T2MD	T1MD	0000
F200	PMD5	31:16	_	-	-	_	_	-	-	USB1MD	_	_	_	_	_	-	I2C1MD	I2C1MD	0000
F280	PINIDS	15:0		_	-	-	-	_	SPI2MD	SPI1MD	-	_	_	_	_	-	U2MD	U1MD	0000
F200	PMD6	31:16	_		-	-	-	-	_	-	_	· · · · · ·	_		_	-	-	PMPMD	0000
F290	-MD6	15:0	-	_	_		-	_	_	_		·	_	_	_	_	REFOMD	RTCCMD	0000

Legend: x = unknown value on Reset, — = unimplemented, read as °C'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 °CLR, SET and INV Registers" for more information.