Hardware exceptions: user or processor, external interrupts or internal timers.
Software exceptions: Illegal instructions, divide by 0, traps i.e. *(int*) (0x0000000)
Exception Handling: Resets – power on reset, external resets, watchdog, and clock monitor reset.
Watchdog: counts down to 0x0 and then resets processor, can't turn off after turning on (except reset).
Clock Monitor: resets when system clock frequency drops below prescribed value.
Brown-out: supply voltage goes below threshold.

- Power-on Reset (POR)
- Master Clear Reset pin (MCLR)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

Asynchronous Interrupt: I/O - communication, Errors
Synchronous Interrupts: I/O – update periodically, Processes – switch between tasks, Timing- measure elapsed time.
Maskable Interrupt: enabled and disabled in software
Non-Maskable: enabled by software, only disabled by hardware.

RCON:

bit 31-10 **Unimplemented:** Read as '0'
bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = Configuration mismatch Reset has occurred
0 = Configuration mismatch Reset has not occurred
bit 8 **VREGS:** Voltage Regulator Standby Enable bit
1 = Regulator is enabled and is on during Sleep mode
0 = Regulator is disabled and is off during Sleep mode
bit 7 **EXTR:** External Reset (MCLR) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred
bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset as not executed
bit 5 **Unimplemented:** Read as '0'
bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT Time-out has occurred
0 = WDT Time-out has not occurred
bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode
bit 2 **IDLE:** Wake From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode
bit 1 **BOR:** Brown-out Reset Flag bit[1]
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred
bit 0 **POR:** Power-on Reset Flag bit[1]
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

IP, IS: bits 7:0 – IP00, IS00. bits 15:8 – IP01, IS01. bits 23:16 – IP02, IS02. Bits 31:24 – IP03, IS03.
External interrupts: INTCONbits.INTxEP – sets edge polarity (0 falling, 1 rising).
- void __ISR(_EXTERNAL_0_VECTOR, ipl2) Int0_IRQ(void);
- void __attribute__((interrupt(ipl2), vector(_EXTERNAL_0_VECTOR))) Int0_IRQ (void);
-

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION

Interrupt Source[1]	IRQ #	Vector #	Flag	Enable	Priority	Sub-priority	Persistent Interrupt
Highest Natural Order Priority							
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
INT0 – External Interrupt	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
IC1E – Input Capture 1 Error	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
IC1 – Input Capture 1	6	5	IFS0<6>	IEC0<6>	IPC1<12:10>	IPC1<9:8>	Yes
OC1 – Output Compare 1	7	6	IFS0<7>	IEC0<7>	IPC1<20:18>	IPC1<17:16>	No
INT1 – External Interrupt 1	8	7	IFS0<8>	IEC0<8>	IPC1<28:26>	IPC1<25:24>	No
T2 – Timer2	9	8	IFS0<9>	IEC0<9>	IPC2<4:2>	IPC2<1:0>	No
IC2E – Input Capture 2	10	9	IFS0<10>	IEC0<10>	IPC2<12:10>	IPC2<9:8>	Yes
IC2 – Input Capture 2	11	9	IFS0<11>	IEC0<11>	IPC2<12:10>	IPC2<9:8>	Yes
OC2 – Output Compare 2	12	10	IFS0<12>	IEC0<12>	IPC2<20:18>	IPC2<17:16>	No
INT2 – External Interrupt 2	13	11	IFS0<13>	IEC0<13>	IPC2<28:26>	IPC2<25:24>	No
T3 – Timer3	14	12	IFS0<14>	IEC0<14>	IPC3<4:2>	IPC3<1:0>	No
IC3E – Input Capture 3	15	13	IFS0<15>	IEC0<15>	IPC3<12:10>	IPC3<9:8>	Yes
IC3 – Input Capture 3	16	13	IFS0<16>	IEC0<16>	IPC3<12:10>	IPC3<9:8>	Yes
OC3 – Output Compare 3	17	14	IFS0<17>	IEC0<17>	IPC3<20:18>	IPC3<17:16>	No
INT3 – External Interrupt 3	18	15	IFS0<18>	IEC0<18>	IPC3<28:26>	IPC3<25:24>	No
T4 – Timer4	19	16	IFS0<19>	IEC0<19>	IPC4<4:2>	IPC4<1:0>	No
IC4E – Input Capture 4 Error	20	17	IFS0<20>	IEC0<20>	IPC4<12:10>	IPC4<9:8>	Yes
IC4 – Input Capture 4	21	17	IFS0<21>	IEC0<21>	IPC4<12:10>	IPC4<9:8>	Yes
OC4 – Output Compare 4	22	18	IFS0<22>	IEC0<22>	IPC4<20:18>	IPC4<17:16>	No
INT4 – External Interrupt 4	23	19	IFS0<23>	IEC0<23>	IPC4<28:26>	IPC4<25:24>	No
T5 – Timer5	24	20	IFS0<24>	IEC0<24>	IPC5<4:2>	IPC5<1:0>	No
IC5E – Input Capture 5 Error	25	21	IFS0<25>	IEC0<25>	IPC5<12:10>	IPC5<9:8>	Yes
IC5 – Input Capture 5	26	21	IFS0<26>	IEC0<26>	IPC5<12:10>	IPC5<9:8>	Yes
OC5 – Output Compare 5	27	22	IFS0<27>	IEC0<27>	IPC5<20:18>	IPC5<17:16>	No
AD1 – ADC1 Convert done	28	23	IFS0<28>	IEC0<28>	IPC5<28:26>	IPC5<25:24>	Yes
FSCM – Fail-Safe Clock Monitor	29	24	IFS0<29>	IEC0<29>	IPC6<4:2>	IPC6<1:0>	No
RTCC – Real-Time Clock and Calendar	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>	No
FCE – Flash Control Event	31	26	IFS0<31>	IEC0<31>	IPC6<20:18>	IPC6<17:16>	No
CMP1 – Comparator Interrupt	32	27	IFS1<0>	IEC1<0>	IPC6<28:26>	IPC6<25:24>	No
CMP2 – Comparator Interrupt	33	28	IFS1<1>	IEC1<1>	IPC7<4:2>	IPC7<1:0>	No
CMP3 – Comparator Interrupt	34	29	IFS1<2>	IEC1<2>	IPC7<12:10>	IPC7<9:8>	No
USB – USB Interrupts	35	30	IFS1<3>	IEC1<3>	IPC7<20:18>	IPC7<17:16>	Yes
SPI1E – SPI1 Fault	36	31	IFS1<4>	IEC1<4>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1RX – SPI1 Receive Done	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>	Yes
SPI1TX – SPI1 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>	Yes

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source[1]	IRQ #	Vector #	Flag	Enable	Priority	Sub-priority	Persistent Interrupt
U1E – UART1 Fault	39	32	IFS1<7>	IEC1<7>	IPC8<4:2>	IPC8<1:0>	Yes
U1RX – UART1 Receive Done	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>	Yes
U1TX – UART1 Transfer Done	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>	Yes
I2C1B – I2C1 Bus Collision Event	42	33	IFS1<10>	IEC1<10>	IPC8<12:10>	IPC8<9:8>	Yes
I2C1S – I2C1 Slave Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>	Yes
I2C1M – I2C1 Master Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>	Yes
CNA – PORTA Input Change Interrupt	45	34	IFS1<13>	IEC1<13>	IPC8<20:18>	IPC8<17:16>	Yes
CNB – PORTB Input Change Interrupt	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>	Yes
CNC – PORTC Input Change Interrupt	47	34	IFS1<15>	IEC1<15>	IPC8<20:18>	IPC8<17:16>	Yes
PMP – Parallel Master Port	48	35	IFS1<16>	IEC1<16>	IPC8<28:26>	IPC8<25:24>	Yes
PMPE – Parallel Master Port Error	49	35	IFS1<17>	IEC1<17>	IPC8<28:26>	IPC8<25:24>	Yes
SPI2E – SPI2 Fault	50	36	IFS1<18>	IEC1<18>	IPC9<4:2>	IPC9<1:0>	Yes
SPI2RX – SPI2 Receive Done	51	36	IFS1<19>	IEC1<19>	IPC9<4:2>	IPC9<1:0>	Yes
SPI2TX – SPI2 Transfer Done	52	36	IFS1<20>	IEC1<20>	IPC9<4:2>	IPC9<1:0>	Yes
U2E – UART2 Error	53	37	IFS1<21>	IEC1<21>	IPC9<12:10>	IPC9<9:8>	Yes
U2RX – UART2 Receiver	54	37	IFS1<22>	IEC1<22>	IPC9<12:10>	IPC9<9:8>	Yes
U2TX – UART2 Transmitter	55	37	IFS1<23>	IEC1<23>	IPC9<12:10>	IPC9<9:8>	Yes
I2C2B – I2C2 Bus Collision Event	56	38	IFS1<24>	IEC1<24>	IPC9<20:18>	IPC9<17:16>	Yes
I2C2S – I2C2 Slave Event	57	38	IFS1<25>	IEC1<25>	IPC9<20:18>	IPC9<17:16>	Yes
I2C2M – I2C2 Master Event	58	38	IFS1<26>	IEC1<26>	IPC9<20:18>	IPC9<17:16>	Yes
CTMU – CTMU Event	59	39	IFS1<27>	IEC1<27>	IPC9<28:26>	IPC9<25:24>	Yes
DMA0 – DMA Channel 0	60	40	IFS1<28>	IEC1<28>	IPC10<4:2>	IPC10<1:0>	No
DMA1 – DMA Channel 1	61	41	IFS1<29>	IEC1<29>	IPC10<12:10>	IPC10<9:8>	No
DMA2 – DMA Channel 2	62	42	IFS1<30>	IEC1<30>	IPC10<20:18>	IPC10<17:16>	No
DMA3 – DMA Channel 3	63	43	IFS1<31>	IEC1<31>	IPC10<28:26>	IPC10<25:24>	No
Lowest Natural Order Priority							

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features" and TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features" for the lists of available peripherals.

- **Input capture:** counts pulses until rising/falling edge to determine duty factors, measure Pulse width etc.
- **Output compare:** like alarm clock, create signal after predefined time has elapsed. Make PWM
- **OSCCON -** oscillator function
  - bit 21 – PBDIVRDY and 20/19 PBDIV
- PBDIV divides SYSCLK by 1, 2, 4, 8 (default) for 00, 01, 10, 11
-

- **Core timer –** uses COUNT and COMPARE registers can be used to generate interrupt when COMPARE = COUNT. Interrupt 0.
- COUNT has ½ frequency of SYSCLK.

$$f_{CT} = \frac{f_{SYSCLK}}{2X(COMPARE)} \qquad T_{CT} = \frac{2X(COMPARE)}{f_{SYSCLK}}$$

- CP0_GET_COUNT(), CPO_SET_COUNT(value), CP0_GET_COMPARE(), CP0_SET_COMPARE(val).
- **Timers:** PIC32 has TMR1-TMR5.
- **Type A Timer:** TMR1 sync/async 16-bit
- **Type B Timers**: TMR2- TMR5 syn 16-bit but can be Combined, 2/3 & 4/5 to use as 32-bit

Type A: T1CON

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **ON:** Timer On bit[1]
1 = Timer is enabled
0 = Timer is disabled
bit 14 **Unimplemented:** Read as '0'
bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode
bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
1 = Writes to Timer1 are ignored until pending write operation completes
0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)
bit 11 **TWIP:** Asynchronous Timer Write in Progress bit
In Asynchronous Timer mode:
1 = Asynchronous write to the Timer1 register in progress
0 = Asynchronous write to Timer1 register is complete
In Synchronous Timer mode:
This bit is read as '0'.
bit 10-8 **Unimplemented:** Read as '0'
bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled
bit 6 **Unimplemented:** Read as '0'
bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)
bit 3 **Unimplemented:** Read as '0'
bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit
When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized
When TCS = 0:
This bit is ignored.
bit 1 **TCS:** Timer Clock Source Select bit
1 = External clock from TxCKI pin
0 = Internal peripheral clock
bit 0 **Unimplemented:** Read as '0'

- **Input Capture:** PIC32 has 5

ADD 1 TO PRy

Type B: TxCON, x = [2,5]

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **ON:** Timer On bit[1,3]
1 = Module is enabled
0 = Module is disabled
bit 14 **Unimplemented:** Read as '0'
bit 13 **SIDL:** Stop in Idle Mode bit[4]
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode
bit 12-8 **Unimplemented:** Read as '0'
bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit[3]
When TCS = 1:
This bit is ignored and is read as '0'.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled
bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits[3]
111 = 1:256 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

REGISTER 13-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)
bit 3 **T32:** 32-Bit Timer Mode Select bit[2]
1 = Odd numbered and even numbered timers form a 32-bit timer
0 = Odd numbered and even numbered timers form a separate 16-bit timer
bit 2 **Unimplemented:** Read as '0'
bit 1 **TCS:** Timer Clock Source Select bit[3]
1 = External clock from TxCK pin
0 = Internal peripheral clock
bit 0 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2: This bit is available only on even numbered timers (Timer2 and Timer4).
3: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.
4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

Input Capture: ICxCON, x = [1,5]

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **ON:** Input Capture Module Enable bit[1]
1 = Module is enabled
0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications
bit 14 **Unimplemented:** Read as '0'
bit 13 **SIDL:** Stop in Idle Control bit
1 = Halt in Idle mode
0 = Continue to operate in Idle mode
bit 12-10 **Unimplemented:** Read as '0'
bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
1 = Capture rising edge first
0 = Capture falling edge first
bit 8 **C32:** 32-bit Capture Select bit
1 = 32-bit timer resource capture
0 = 16-bit timer resource capture
bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
0 = Timer3 is the counter source for capture
1 = Timer2 is the counter source for capture
bit 6-5 **ICI<1:0>:** Interrupt Control bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event
bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
1 = Input capture overflow has occurred
0 = No input capture overflow has occurred
bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
1 = Input capture buffer is not empty; at least one more capture value can be read
0 = Input capture buffer is empty

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)
bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
101 = Prescaled Capture Event mode – every sixteenth rising edge
100 = Prescaled Capture Event mode – every fourth rising edge
011 = Simple Capture Event mode – every rising edge
010 = Simple Capture Event mode – every falling edge
001 = Edge Detect mode – every edge (rising and falling)
000 = Input Capture module is disabled

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Output compare – OCxCON, x = [1,5]

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **ON:** Output Compare Peripheral On bit[1]
1 = Output Compare peripheral is enabled
0 = Output Compare peripheral is disabled
bit 14 **Unimplemented:** Read as '0'
bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode
bit 12-6 **Unimplemented:** Read as '0'
bit 5 **OC32:** 32-bit Compare Mode bit
1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source
0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source
bit 4 **OCFLT:** PWM Fault Condition Status bit[2]
1 = PWM Fault condition has occurred (cleared in hardware only)
0 = No PWM Fault condition has occurred
bit 3 **OCTSEL:** Output Compare Timer Select bit
1 = Timer3 is the clock source for this Output Compare module
0 = Timer2 is the clock source for this Output Compare module
bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
111 = PWM mode on OCx; Fault pin enabled
110 = PWM mode on OCx; Fault pin disabled
101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
100 = Initialize OCx pin low; generate single output pulse on OCx pin
011 = Compare event toggles OCx pin
010 = Initialize OCx pin high; compare event forces OCx pin low
001 = Initialize OCx pin low; compare event forces OCx pin high
000 = Output compare peripheral is disabled but continues to draw current

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2: This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

- **Square Wave Calcs:** final frequency / 2 - half period on.
- **RPM:** Let N = number of "equally spaced events"
  f_tmr = timer frequency
  ticks = TMRx(new) – TMRx(old)
  RPM = 60 / (N * (ticks/f_tmr))
- **Watchdog timer – STWD100**

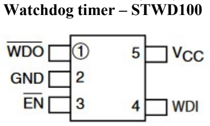


Table 9-3: WDT Time-out Period vs. Postscaler Settings[1, 2]

FWDTPS<4:0>	Postscaler Ratio	Time-out Period
00000	1:1	1 ms
00001	1:2	2 ms
00010	1:4	4 ms
00011	1:8	8 ms
00100	1:16	16 ms
00101	1:32	32 ms
00110	1:64	64 ms
00111	1:128	128 ms
01000	1:256	256 ms
01001	1:512	512 ms
01010	1:1024	1.024 s
01011	1:2048	2.048 s
01100	1:4096	4.096 s
01101	1:8192	8.192 s
01110	1:16384	16.384 s
01111	1:32768	32.768 s
10000	1:65536	65.536 s
10001	1:131072	131.072 s
10010	1:262144	262.144 s
10011	1:524288	524.288 s
10100	1:1045876	1048.576 s

Note 1: All other combinations will result in operation as if the prescaler was set to 10100.
2: The periods listed are based on a 32 kHz (nominal) input clock.

DEVCGF1 – FWDTEN 1 = on

bit 31-10 **Unimplemented:** Read as '0'
bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = Configuration mismatch Reset has occurred
0 = Configuration mismatch Reset has not occurred
bit 8 **VREGS:** Voltage Regulator Standby Enable bit
1 = Regulator is enabled and is on during Sleep mode
0 = Regulator is disabled and is off during Sleep mode
bit 7 **EXTR:** External Reset (MCLR) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred
bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset as not executed
bit 5 **Unimplemented:** Read as '0'
bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT Time-out has occurred
0 = WDT Time-out has not occurred
bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode
bit 2 **IDLE:** Wake From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode
bit 1 **BOR:** Brown-out Reset Flag bit[1]
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred
bit 0 **POR:** Power-on Reset Flag bit[1]
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

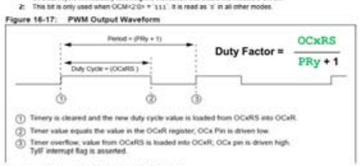
Note 1: User software must clear this bit to view next detection.

RCON --^ ------ PWM ------v

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **ON:** Output Compare Peripheral On bit[1]
1 = Output Compare peripheral is enabled
0 = Output Compare peripheral is disabled
bit 14 **Unimplemented:** Read as '0'
bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode
bit 12-6 **Unimplemented:** Read as '0'
bit 5 **OC32:** 32-bit Compare Mode bit
1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source
0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source
bit 4 **OCFLT:** PWM Fault Condition Status bit[2]
1 = PWM Fault condition has occurred (cleared in hardware only)
0 = No PWM Fault condition has occurred
bit 3 **OCTSEL:** Output Compare Timer Select bit
1 = Timer3 is the clock source for this Output Compare module
0 = Timer2 is the clock source for this Output Compare module
bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
111 = PWM mode on OCx; Fault pin enabled
110 = PWM mode on OCx; Fault pin disabled
101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
100 = Initialize OCx pin low; generate single output pulse on OCx pin
011 = Compare event toggles OCx pin
010 = Initialize OCx pin high; compare event forces OCx pin low
001 = Initialize OCx pin low; compare event forces OCx pin high
000 = Output compare peripheral is disabled but continues to draw current

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2: This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

Figure 16-17: PWM Output Waveform



① Timer is cleared and the new duty cycle value is loaded from OCxRS into OCxR.
② Timer value equals the value in the OCxR register; OCx Pin is driven low.
③ Timer overflow; value from OCxRS is loaded into OCxR; OCx pin is driven high. TyIF interrupt flag is asserted.

Equation 16-1: Calculating the PWM Period

PWM Period = [(PR + 1) * TPB * (TMR Prescale Value)]
PWM Frequency = 1/[PWM Period]

Equation 16-2: Calculation for Maximum PWM Resolution

$$\text{Maximum PWM Resolution (bits)} = \frac{\log_{10}\left(\frac{F_{PB}}{F_{PWM} \cdot TMR_y \cdot \text{Prescaler bits}}\right)}{\log_{10}(2)}$$

Max RES^^ DON'T ROUND/TRUNCATE

Serial Peripheral Interface (SPI) - Full Duplex
Inter Integrated Circuits (I^2C) - Half Duplex
MOSI – Master Out Slave In (Data out)
MISO – Master In Slave Out (Data in)
SCK – Serial clock
SS# - Slave Select
PIC32 has **2 SPI** peripherals available

REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	MCLKSEL[2]	—	—	—	—	—	SPIFE	ENHBUF[2]
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON[1]	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE[3]
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEN	CKP[4]	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>	

Legend:
R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'
-n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled (SSx pin used as FSYNC input/output)
0 = Framed SPI support is disabled
bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on SSx pin bit (Framed SPI mode only)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)
bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
1 = Frame pulse is active-high
0 = Frame pulse is active-low
bit 28 **MSSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support enabled. The SS pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.
bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide
bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in FRAMED_SYNC mode.
111 = Reserved; do not use
110 = Reserved; do not use
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character
bit 23 **MCLKSEL:** Master Clock Enable bit[2]
1 = REFCLK is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator
bit 22-18 **Unimplemented:** Read as '0'

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2: This bit can only be written when the ON bit = 0.
3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock
bit 16 **ENHBUF:** Enhanced Buffer Enable bit[2]
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled
bit 15 **ON:** SPI Peripheral On bit[1]
1 = SPI Peripheral is enabled
0 = SPI Peripheral is disabled
bit 14 **Unimplemented:** Read as '0'
bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode
bit 12 **DISSDO:** Disable SDOx pin bit
1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
0 = SDOx pin is controlled by the module
bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits
When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
1	0	32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
0	1	16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame
0	0	16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

bit 9 **SMP:** SPI Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.
To write a '1' to this bit, the MSTEN value = 1 must first be written.

bit 8 **CKE:** SPI Clock Edge Select bit[3]
1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)
bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = SSx pin used for Slave mode
0 = SSx pin not used for Slave mode, pin controlled by port function.
bit 6 **CKP:** Clock Polarity Select bit[4]
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2: This bit can only be written when the ON bit = 0.
3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode
bit 4 **DISSDI:** Disable SDI bit
1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
0 = SDI pin is controlled by the SPI module
bit 3-2 **STXISEL<1:0>:** SPI Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete
bit 1-0 **SRXISEL<1:0>:** SPI Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2: This bit can only be written when the ON bit = 0.
3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

REGISTER 17-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	AUDEN[1]	—	—	—	AUDMONO[1,2]	—	AUDMOD<1:0>[1,2]	

Legend:
R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'
-n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit
1 = Data from RX FIFO is sign extended
0 = Data from RX FIFO is not sign extended
bit 14-13 **Unimplemented:** Read as '0'
bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
1 = Frame Error overflow generates error events
0 = Frame Error does not generate error events
bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
1 = Receive overflow generates error events
0 = Receive overflow does not generate error events
bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
1 = Transmit underrun generates error events
0 = Transmit underrun does not generate error events
bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)
1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
0 = A ROV is a critical error that stops SPI operation
bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
0 = A TUR is a critical error that stops SPI operation
bit 7 **AUDEN:** Enable Audio CODEC Support bit[1]
1 = Audio protocol enabled
0 = Audio protocol disabled
bit 6-5 **Unimplemented:** Read as '0'
bit 3 **AUDMONO:** Transmit Audio Data Format bit[1,2]
1 = Audio data is mono (Each data word is transmitted on both left and right channels)
0 = Audio data is stereo
bit 2 **Unimplemented:** Read as '0'
bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit[1,2]
11 = PCM/DSP mode
10 = Right-Justified mode
01 = Left-Justified mode
00 = I²S mode

Note 1: This bit can only be written when the ON bit = 0.
2: This bit is only valid for AUDEN = 1.

Equation 23-1:

$$F_{SCK} = \frac{F_{PB}}{2 \cdot (SPIxBRG + 1)}$$

- **SPIxBRG<0:8>** - Baud rate register

REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend: C = Clearable bit; HS = Set in hardware; R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'; -n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'
bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)
bit 23-21 **Unimplemented:** Read as '0'
bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)
bit 15-13 **Unimplemented:** Read as '0'
bit 12 **FRMERR:** SPI Frame Error status bit
1 = Frame error detected
0 = No Frame error detected
This bit is only valid when FRMEN = 1.
bit 11 **SPIBUSY:** SPI Activity Status bit
1 = SPI peripheral is currently busy with some transactions
0 = SPI peripheral is currently idle
bit 10-9 **Unimplemented:** Read as '0'
bit 8 **SPITUR:** Transmit Under Run bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or writing a '0' to SPITUR.
bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
1 = When SPI module shift register is empty
0 = When SPI module shift register is not empty
bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred
This bit is set in hardware; can bit only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or by writing a '0' to SPIROV.
bit 5 **SPIRBE:** RX FIFO Empty bit (valid only when ENHBUF = 1)
1 = RX FIFO is empty (CRPTR = SWPTR)
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)
bit 4 **Unimplemented:** Read as '0'
bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB is empty
0 = Transmit buffer, SPIxTXB is not empty
Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.
Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.
bit 2 **Unimplemented:** Read as '0'
bit 1 **SPITBF:** SPI Transmit Buffer Full Status bit
1 = Transmit not yet started, SPITXB is full
0 = Transmit buffer is not full
Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB.
Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR.
Enhanced Buffer Mode:
Set when CWPTR + 1 = SRPTR; cleared otherwise
bit 0 **SPIRBF:** SPI Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB is full
0 = Receive buffer, SPIxRXB is not full
Standard Buffer Mode:
Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB.
Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer Mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise

PIC32 has 3 comparators
CVRCON

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **ON:** Comparator Voltage Reference On bit[1]
1 = Module is enabled
Setting this bit does not affect other bits in the register.
0 = Module is disabled and does not consume current.
Clearing this bit does not affect the other bits in the register.
bit 14-7 **Unimplemented:** Read as '0'
bit 6 **CVROE:** CVREFOUT Enable bit
1 = Voltage level is output on CVREFOUT pin
0 = Voltage level is disconnected from CVREFOUT pin
bit 5 **CVRR:** CVREF Range Selection bit
1 = 0 to 0.67 CVRSRC, with CVRSRC/24 step size
0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size
bit 4 **CVRSS:** CVREF Source Selection bit
1 = Comparator voltage reference source, CVRSRC = (VREF+) – (VREF-)
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS
bit 3-0 **CVR<3:0>:** CVREF Value Selection 0 ≤ CVR<3:0> ≤ 15 bits
When CVRR = 1:
CVREF = (CVR<3:0>/24) • (CVRSRC)
When CVRR = 0:
CVREF = 1/4 • (CVRSRC) + (CVR<3:0>/32) • (CVRSRC)

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 23-1: CMXCON: COMPARATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON[1]	COE	CPOL[2]	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend: R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'; -n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **ON:** Comparator ON bit[1]
1 = Module is enabled. Setting this bit does not affect the other bits in this register
0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register
bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is driven on the output CxOUT pin
0 = Comparator output is not driven on the output CxOUT pin
bit 13 **CPOL:** Comparator Output Inversion bit[2]
1 = Output is inverted
0 = Output is not inverted
bit 12-9 **Unimplemented:** Read as '0'
bit 8 **COUT:** Comparator Output bit
1 = Output of the Comparator is a '1'
0 = Output of the Comparator is a '0'
bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
00 = Comparator interrupt generation is disabled
bit 5 **Unimplemented:** Read as '0'
bit 4 **CREF:** Comparator Positive Input Configure bit
1 = Comparator non-inverting input is connected to the internal CVREF
0 = Comparator non-inverting input is connected to the CxINA pin
bit 3-2 **Unimplemented:** Read as '0'
bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator
11 = Comparator inverting input is connected to the IVREF
10 = Comparator inverting input is connected to the CxIND pin
01 = Comparator inverting input is connected to the CxINC pin
00 = Comparator inverting input is connected to the CxINB pin

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

D to A:

$$\textbf{Output} = K\,V_{REF}\frac{\textbf{Code}}{2^N}\ \textbf{Volts}$$

$$\textbf{Resolution} = \Delta = K\,V_{REF}\frac{1}{2^N}$$

$$\textbf{Maximum Output Voltage} = K\,V_{REF}\frac{2^N-1}{2^N} = K\,V_{REF} - \Delta$$

Zero Error – error when input = 0
Full-Scale Error - error when input is the maximum
Relative Accuracy Error – error between actual and the line from output_max and output_min.
Monotonicity - output always increasing as input increases
Settling Time - The required for the output to reach with a D/2 of the stable output when the input changes from 0 to 2^N-1, or 2^N-1 to 0.
A-to-D:
Offset Error - Error of analog transition point nearest 0 Volts.
Full Scale (Gain) Error - Error of analog transition point farthest from 0 Volts.
Differential Nonlinearity Error - The maximum difference between a step D and the constant ideal D.
DNLE = Maximum $|D_k - D|$

A *Successive Approximation Register* **(SAR)** is an ADC where each output bit is determined sequentially, starting with the most significant bit (MSB) working down to the least significant bit (LSB) in a binary search algorithm.
Dual-Ramp ADCs use an RC Operational Amplifier Circuit coupled with a timer to measure the value of an input.
- Slower but more precise because it needs to charge and discharge a capacitor.

PIC32 A-to-D:
- 10 bit, up to 16 analog inputs, internal VREF, multiple channel scan, 16-word buffer, 8 conversion formats and can run during idle/sleep mode.

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON[1]	—	SIDL	—	—	FORM<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
	SSRC<2:0>			CLRASAM	—	ASAM	SAMP[2]	DONE[3]

Legend: R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'; -n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **ON:** ADC Operating Mode bit[1]
1 = ADC module is operating
0 = ADC module is not operating
bit 14 **Unimplemented:** Read as '0'
bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation when the device enters Idle mode
bit 12-11 **Unimplemented:** Read as '0'
bit 10-8 **FORM<2:0>:** Data Output Format bits
111 = Signed Fractional 32-bit (DOUT = sddd dddd d000 0000 0000 0000 0000 0000)
110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss ssss sddd dddd)
100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits
111 = Internal counter ends sampling and starts conversion (auto convert)
110 = Reserved
101 = Reserved
100 = Reserved
011 = CTMU ends sampling and starts conversion
010 = Timer 3 period match ends sampling and starts conversion
001 = Active transition on INT0 pin ends sampling and starts conversion
000 = Clearing SAMP bit ends sampling and starts conversion

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)
bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)
1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
0 = Normal operation, buffer contents will be overwritten by the next conversion sequence
bit 3 **Unimplemented:** Read as '0'
bit 2 **ASAM:** ADC Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.
0 = Sampling begins when SAMP bit is set
bit 1 **SAMP:** ADC Sample Enable bit[2]
1 = The ADC sample and hold amplifier is sampling
0 = The ADC sample/hold amplifier is holding
When ASAM = 0, writing '1' to this bit starts sampling.
When SSRC = 000, writing '0' to this bit will end sampling and start conversion.
bit 0 **DONE:** Analog-to-Digital Conversion Status bit[3]
1 = Analog-to-digital conversion is done
0 = Analog-to-digital conversion is not done or has not started
Clearing this bit will not affect any operation in progress.

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.
3: This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

- Signed voltages: Vad = (# / 1024) * VREF+
  - o (VREF+ - VREF-) / 2 + Vad
  - o For fractions add 1 if POSITIVE

REGISTER 22-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	—	CSCNA	—	—
7:0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFS	—	SMPI<3:0>				BUFM	ALTS

Legend: R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'; -n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	VREFH	VREFL
000	AVDD	AVSS
001	External VREF+ pin	AVSS
010	AVDD	External VREF- pin
011	External VREF+ pin	External VREF- pin
1xx	AVDD	AVSS

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit
1 = Enable Offset Calibration mode
Positive and negative inputs of the sample and hold amplifier are connected to VREFL
0 = Disable Offset Calibration mode
The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL
bit 11 **Unimplemented:** Read as '0'
bit 10 **CSCNA:** Input Scan Select bit
1 = Scan inputs
0 = Do not scan inputs
bit 9-8 **Unimplemented:** Read as '0'
bit 7 **BUFS:** Buffer Fill Status bit
Only valid when BUFM = 1.
1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7
0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF
bit 6 **Unimplemented:** Read as '0'
bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence
bit 1 **BUFM:** ADC Result Buffer Mode Select bit
1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8
0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0
bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples
0 = Always use Sample A input multiplexer settings

REGISTER 22-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADRC	—	—	SAMC<4:0>[1]				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
	ADCS<7:0>[2]							

Legend: R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'; -n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **ADRC:** ADC Conversion Clock Source bit
1 = Clock derived from FRC
0 = Clock derived from Peripheral Bus Clock (PBCLK)
bit 14-13 **Unimplemented:** Read as '0'
bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits[1]
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)
bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits[2]
11111111 = TPB • 2 • (ADCS<7:0> + 1) = 512 • TPB = TAD
•
•
•
00000001 = TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD
00000000 = TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD

Note 1: This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
2: This bit is not used if the ADRC (AD1CON3<15>) bit = 1.

REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NB	—	—	—	CH0SB<3:0>			
23:16	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NA	—	—	—	CH0SA<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend: R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'; -n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31 **CH0NB:** Negative Input Select bit for Sample B
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL
bit 30-28 **Unimplemented:** Read as '0'
bit 27-24 **CH0SB<3:0>:** Positive Input Select bits for Sample B
1111 = Channel 0 positive input is Open[1]
1110 = Channel 0 positive input is IVREF[2]
1101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)[3]
1100 = Channel 0 positive input is AN12[4]
•
•
•
0001 = Channel 0 positive input is AN1
0000 = Channel 0 positive input is AN0
bit 23 **CH0NA:** Negative Input Select bit for Sample A Multiplexer Setting[2]
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL
bit 22-20 **Unimplemented:** Read as '0'
bit 19-16 **CH0SA<3:0>:** Positive Input Select bits for Sample A Multiplexer Setting
1111 = Channel 0 positive input is Open[1]
1110 = Channel 0 positive input is IVREF[2]
1101 = Channel 0 positive input is CTMU temperature (CTMUT)[3]
1100 = Channel 0 positive input is AN12[4]
•
•
•
0001 = Channel 0 positive input is AN1
0000 = Channel 0 positive input is AN0
bit 15-0 **Unimplemented:** Read as '0'

Note 1: This selection is only used with CTMU capacitive and time measurement.
2: See **Section 24.0 "Comparator Voltage Reference (CVREF)"** for more information.
3: See **Section 25.0 "Charge Time Measurement Unit (CTMU)"** for more information.
4: AN12 is only available on 44-pin devices. AN6-AN8 are not available on 28-pin devices.

REGISTER 22-6: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

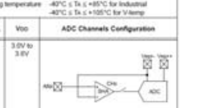
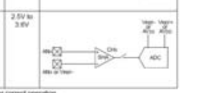
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0

Legend: R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'; -n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
bit 15-0 **CSSL<15:0>:** ADC Input Pin Scan Selection bits[1,2]
1 = Select ANx for input scan
0 = Skip ANx for input scan

Note 1: CSSL = ANx, where 'x' = 0-12; CSSL13 selects CTMU input for scan; CSSL14 selects IVREF for scan; CSSL15 selects VSS for scan.
2: On devices with less than 13 analog inputs, all CSSLx bits can be selected, however, inputs selected for scan without a corresponding input on the device will convert to VREFL.

TABLE 30-35: 10-BIT CONVERSION RATE PARAMETERS

AC CHARACTERISTICS[2]					Standard Operating Conditions (see Note 3): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial, -40°C ≤ TA ≤ +105°C for V-temp
ADC Speed	TAD Min.	Sampling Time Min.	Rs Max.	VDD	ADC Channels Configuration
1 Msps to 400 ksps[1]	65 ns	132 ns	500Ω	3.0V to 3.6V	
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	

Note 1: External VREF- and VREF+ pins must be used for correct operation.
2: These parameters are characterized, but not tested in manufacturing.
3: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 30-36: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS							Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial, -40°C ≤ TA ≤ +105°C for V-temp
Param. No.	Symbol	Characteristics	Min.	Typical[1]	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period[2]	65	—	—	ns	See Table 30-35
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed)	—	—	1000	ksps	AVDD = 3.0V to 3.6V
			—	—	400	ksps	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	1 TAD	—	—	—	TSAMP must be ≥ 132 ns
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger[3]	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1)[3]	—	0.5 TAD	—	—	—
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On[3]	—	—	2	µs	—

Note 1: These parameters are characterized, but not tested in manufacturing.
2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.
3: Characterized by design but not tested.
4: The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

Equation 17-1: ADC Conversion Clock Period

$$T_{AD} = 2 \bullet (T_{PB} \bullet (ADCS + 1))$$

$$ADCS = \left(\frac{T_{AD}}{2 \bullet T_{PB}}\right) - 1$$

Equation 17-2: Available Sampling Time, Sequential Sampling

$$T_{SMP} = TriggerPulseInterval(T_{SEQ}) - ConversionTime(T_{CONV})$$

$$T_{SMP} = T_{SEQ} - T_{CONV}$$

Note: TSEQ is the trigger pulse interval time.

UARTS:
Overrun Error – A new character has arrived before previous character has been read.
Underrun Condition – The UART's transmit buffer is empty while communication has been taking place.
Framing Error – Start and/or stop bits are in error. That is, the line is not low where a start bit should be, or it is not high where the stop bit(s) should be located.
Parity Error – The parity bit (if present) is not the value should be for the transmitted data bits.
Break Condition – A certain number of consecutive 0's (generally more than a complete character) have been received. Can be sent intentionally to tell the receiver communication is finished.
Baud Rate: Symbols per second

REGISTER 19-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON[1]	—	SIDL	IREN	RTSMD	—	UEN<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend: R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'; -n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
bit 15 **ON:** UARTx Enable bit[1]
1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits
0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal
bit 14 **Unimplemented:** Read as '0'
bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when device enters Idle mode
0 = Continue operation in Idle mode
bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit
1 = IrDA is enabled
0 = IrDA is disabled
bit 11 **RTSMD:** Mode Selection for UxRTS Pin bit[2]
1 = UxRTS pin is in Simplex mode
0 = UxRTS pin is in Flow Control mode
bit 10 **Unimplemented:** Read as '0'
bit 9-8 **UEN<1:0>:** UARTx Enable bits[2]
11 = UxTX, UxRX and UxBCLK pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used
01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/UxBCLK pins are controlled by corresponding bits in the PORTx register
bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
1 = Wake-up enabled
0 = Wake-up disabled
bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Loopback mode is enabled
0 = Loopback mode is disabled

Note 1: When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2: These bits are not available in some UART modules. Refer to the "UART" chapter in the specific device data sheet for more information on availability of these bits in different UART modules.

Register 21-1: UxMODE: UARTx Mode Register (Continued)
bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement disabled or completed
bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'
bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock enabled
0 = Standard Speed mode – 16x baud clock enabled
bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity
bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ADM_EN
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-1
	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
7:0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0	R-0
	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA

Legend: R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'; -n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31-25 **Unimplemented:** Read as '0'
bit 24 **ADM_EN:** Automatic Address Detect Mode Enable bit
1 = Automatic Address Detect mode is enabled
0 = Automatic Address Detect mode is disabled
bit 23-16 **ADDR<7:0>:** Automatic Address Mask bits
When the ADM_EN bit is '1', this value defines the address character to use for automatic address detection.
bit 15-14 **UTXISEL<1:0>:** TX Interrupt Mode Selection bits
11 = Reserved, do not use
10 = Interrupt is generated and asserted while the transmit buffer is empty
01 = Interrupt is generated and asserted when all characters have been transmitted
00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space
bit 13 **UTXINV:** Transmit Polarity Inversion bit
If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):
1 = UxTX Idle state is '0'
0 = UxTX Idle state is '1'
If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):
1 = IrDA encoded UxTX Idle state is '1'
0 = IrDA encoded UxTX Idle state is '0'
bit 12 **URXEN:** Receiver Enable bit
1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON = 1)
0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module. UxRX pin is controlled by port.
bit 11 **UTXBRK:** Transmit Break bit
1 = Send Break on next transmission. Start bit followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
0 = Break transmission is disabled or completed
bit 10 **UTXEN:** Transmit Enable bit
1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)
0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset. UxTX pin is controlled by port.
bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
1 = Transmit buffer is full
0 = Transmit buffer is not full, at least one more character can be written
bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)
bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved; do not use
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters)
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters)
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)
bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect.
0 = Address Detect mode is disabled
bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received
bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected
bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected
bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed
bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Register 21-5: UxBRG: UARTx Baud Rate Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BRG<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BRG<7:0>							

Legend: R = Readable bit; W = Writable bit; U = Unimplemented bit, read as '0'; -n = Value at POR; '1' = Bit is set; '0' = Bit is cleared; x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
bit 15-0 **BRG<15:0>:** Baud Rate Divisor bits

Equation 21-1: UART Baud Rate with BRGH = 0

$$Baud\ Rate = \frac{F_{PB}}{16 \cdot (UxBRG + 1)}$$

$$UxBRG = \frac{F_{PB}}{16 \cdot Baud\ Rate} - 1$$

Note: F_{PB} denotes the PBCLK frequency.

If BRGH = 1 then replace 16 with 4 ^.

Stepper Motors:
- Unlike many motors, they have full torque at stand-still and have excellent response to starting, stopping, and reversing.
- They don't need brushes for commutation, so they have a longer motor life depending primarily on bearing and coil life.
- They can achieve very low speeds and only require open-loop control
- Furthermore, their speed is determined by the period of these pulses, not by their voltage.
- **Disadvantages:**
Resonance can be a problem if not controlled.
Do not perform as well for high-speed applications.
Stepping Modes:
Wave Drive Mode: one by one A – B – A' – B'
Full Step Drive: 2 at a time AB – BA' – A'B' – B'A
Half Step Drive: combo of above two AB-A-BA'-A'-A'B'-B'-B'A-A
Micro Stepping: smaller step sizes
Stator – Stationary (generally) part of the motor held in place by the outer casing of the motor.
Rotor – Inner part that rotates in response to changes in the activation pattern. It is supported at each end by bearings and includes a projecting shaft for the connection of the load.
Stator Teeth – Radial projections on the stator which provide a more precise path for the magnetic flux to flow between the stator and the rotor and produce the motor's movement.
Rotor Teeth – Radial projections on the rotor which are also used to provide a path for the magnetic field that produces the motor's movement.
Multi-Stack Variable Reluctance: rotor teeth lose to (not equal) stator is multiple of phases.

$$\text{Step Size} = \frac{360^\circ}{\Phi t} \quad \text{where} \quad \Phi = \text{Number of Phases}, \; t = \text{Number of Rotor Teeth}$$

$$\text{Tooth Pitch} = {}^{360^\circ}/_{12} = 30^\circ$$

12 = rotor teeth
Hybrid: Rotor teeth > Stator Teeth (still multiple of poles)

$$\text{Step size} = \frac{360^\circ\,(RT-ST)}{(RT \times ST)}$$