**BJT Common-Emitter Circuit Voltage Gain**

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**Proposal**

The purpose of this experiment is to visually experience and observe the effects of the BJT Common-Emitter Circuit and how the voltage output is affected by the circuit when the circuit has different values of the collector and emitter resistors, as well as the roles of the emitter bypass capacitor. As is known, the base resistors of the biasing section of the circuit determine the Q-point, which in turn determines the relationship between the input and output waveforms, along with possible distortion of the output waveform if the Q-point is not near the center of the load line or if the input signal is too large. The voltage gain of the common-emitter amplifier will be observed throughout this experiment as a result of the differences in circuit design that will be utilized.

**Experimental**

In this experiment, the curve tracer will be used to record values for and of the chosen transistor at a collector current value of 1mA and voltage across the transistor of 5V. Then the circuit in Figure 7.2 of the lab manual will be constructed and the DMM will be used to measure and as well as the Q-point will be obtained from calculations, and the load line will be drawn on our transistor characteristic. Next the circuit in Figure 7.3 of the lab manual will be constructed and Vo and Vs will be measured using the oscilloscope. If there is distortion, reduce the magnitude of the input signal or adjust the Q-point, and then continue. Using the previously stated procedure, Table 7.1 of the lab manual will be filled out according to the measurements taken for the circuit in Figure 7.3 of the lab manual with Rc modified to step through the values in Table 7.1 including the section that says to repeat all measurements without the emitter bypass capacitor. The same basic procedure will the be repeated to fill out Table 7.2 of the lab manual, except that the emitter resistor will be modified to step through the values in Table 7.2 and the collector resistor will remain constant at 3.9 kiloOhms. Then the emitter resistor will be set to 1 kiloOhm, and the emitter bypass capacitor will be reconnected to the circuit, and the input signal frequency will be modified to step through the values of 10 Hz to 50 kHz, and the output voltages and voltage gain will be recorded in Table 7.3 of the lab manual. Lastly, the transistor we use will be saved and its values of for and will be utilized for design calculations in the pre-lab for Labs 8 and 9, and the transistor itself will be used for Labs 8 and 9.

**Simulations for Expected Results**

**\***Vs is assumed to be 0.02 Volts Peak to Peak with 1kHz frequency for all simulations\*

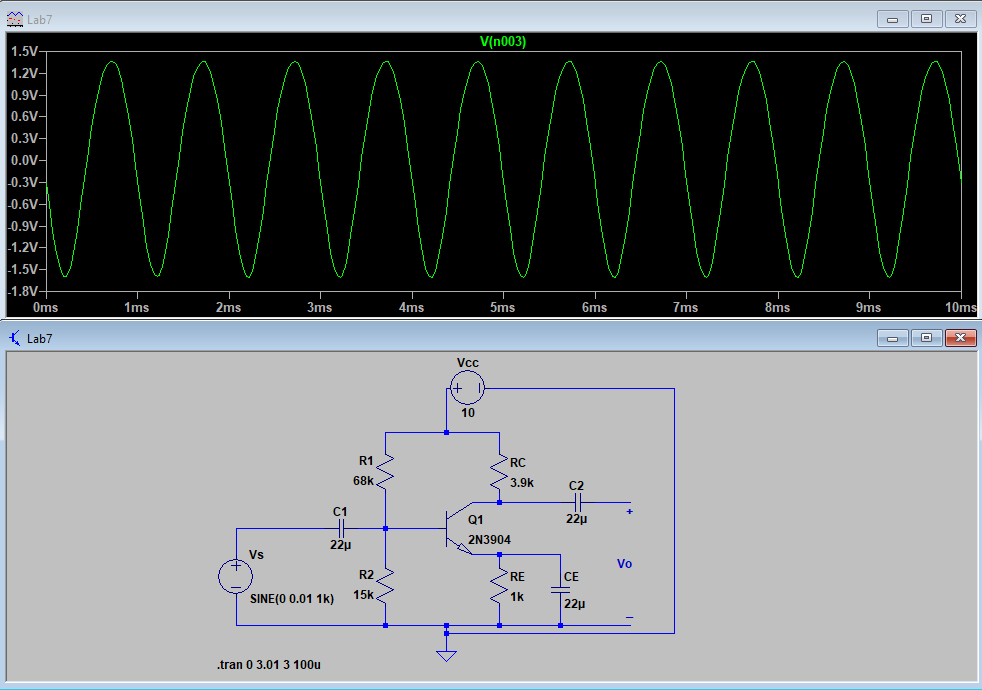


Figure 1: Figure 7.1 Simulation of Vo w/

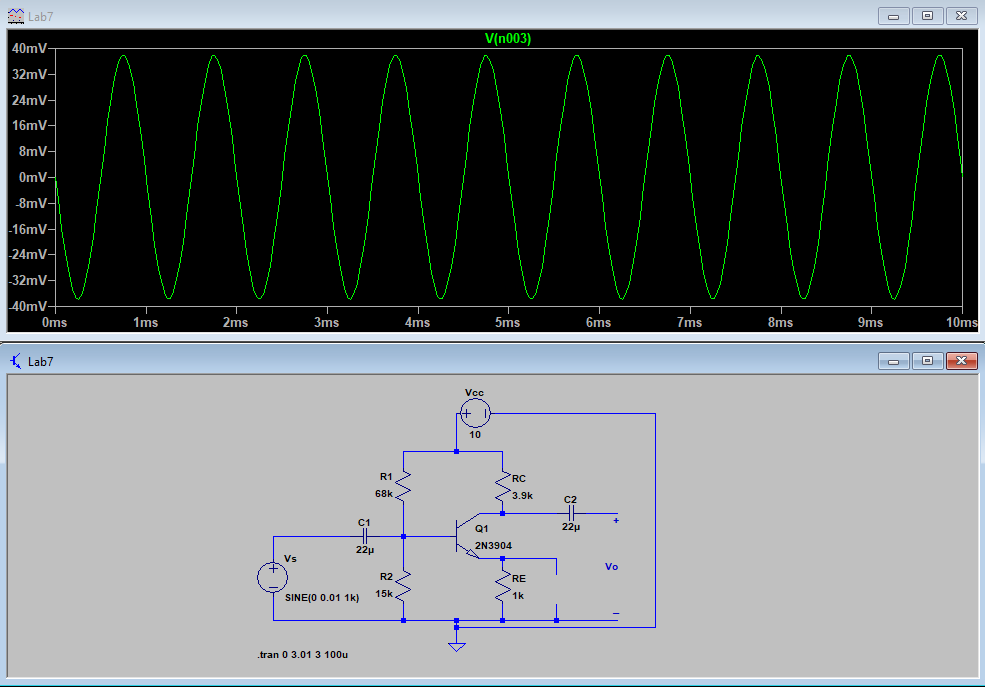


Figure 2: Figure 7.1 Simulation of Vo w/

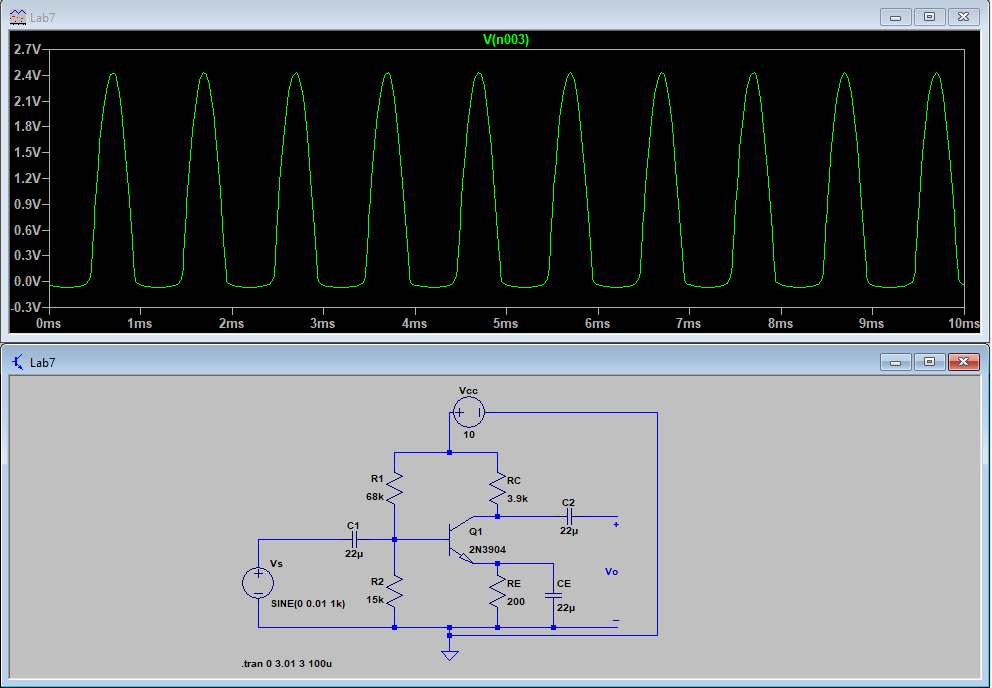


Figure 3: Figure 7.1 Simulation of Vo w/

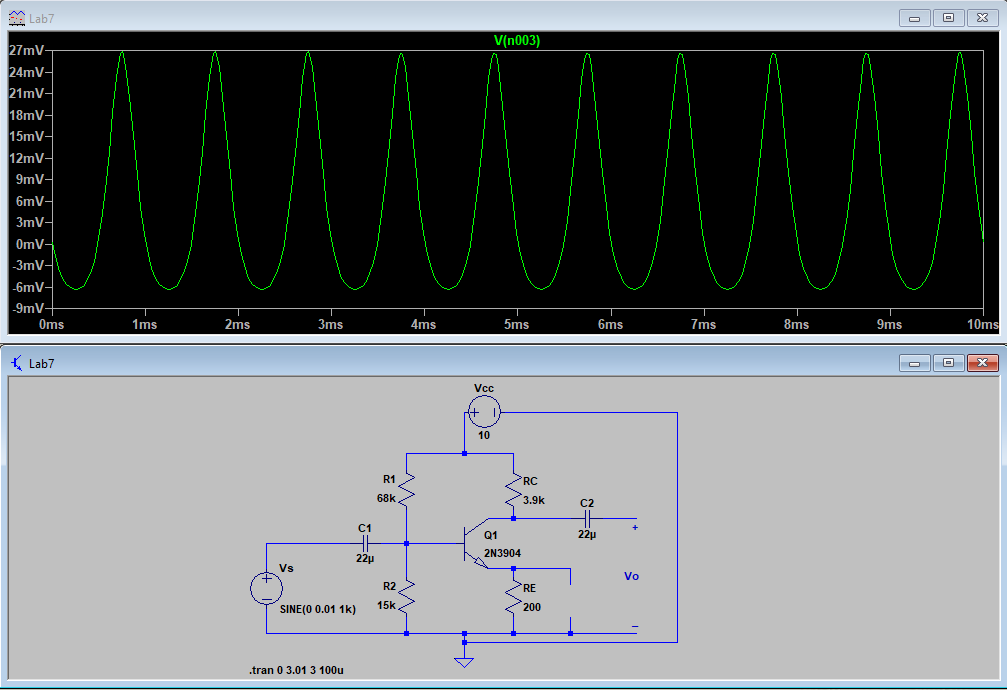


Figure 4: Figure 7.1 Simulation of Vo w/

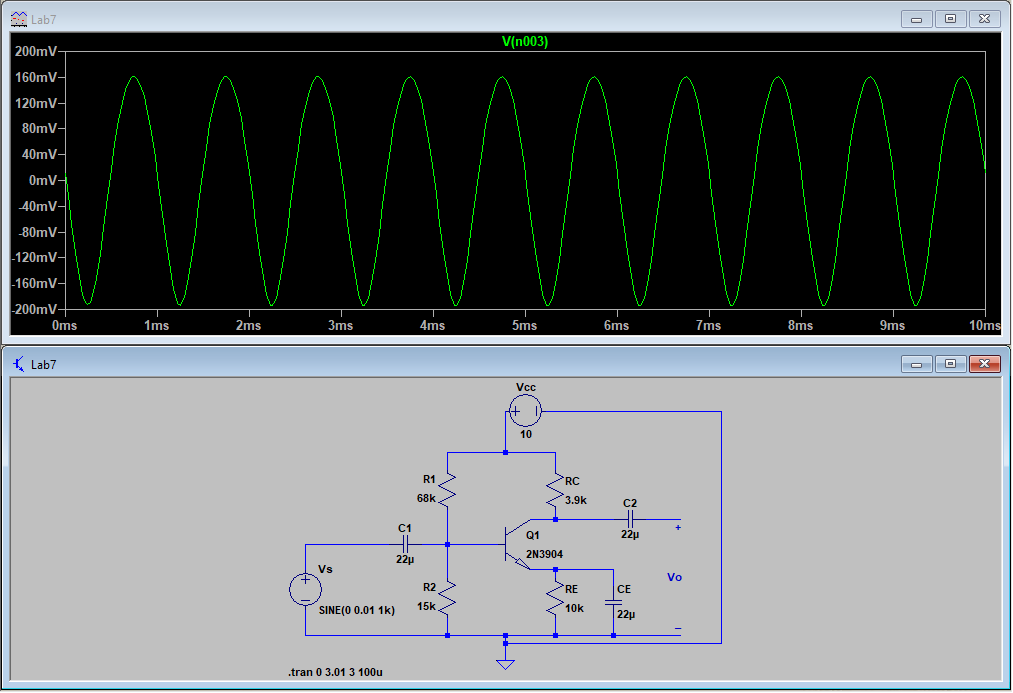


Figure 5: Figure 7.1 Simulation of Vo w/

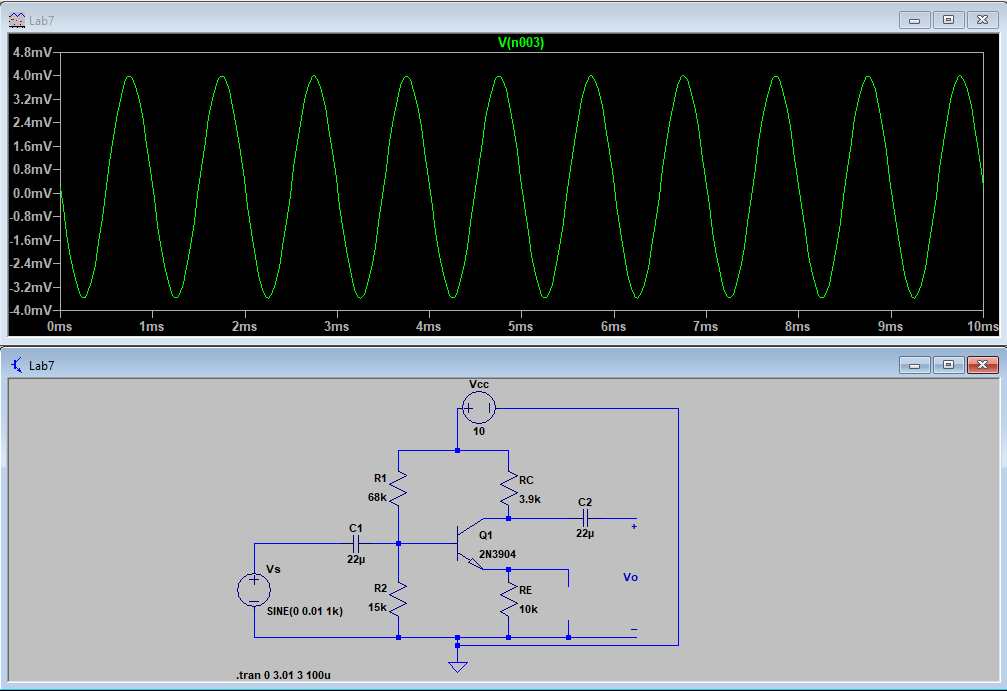


Figure 6: Figure 7.1 Simulation of Vo w/

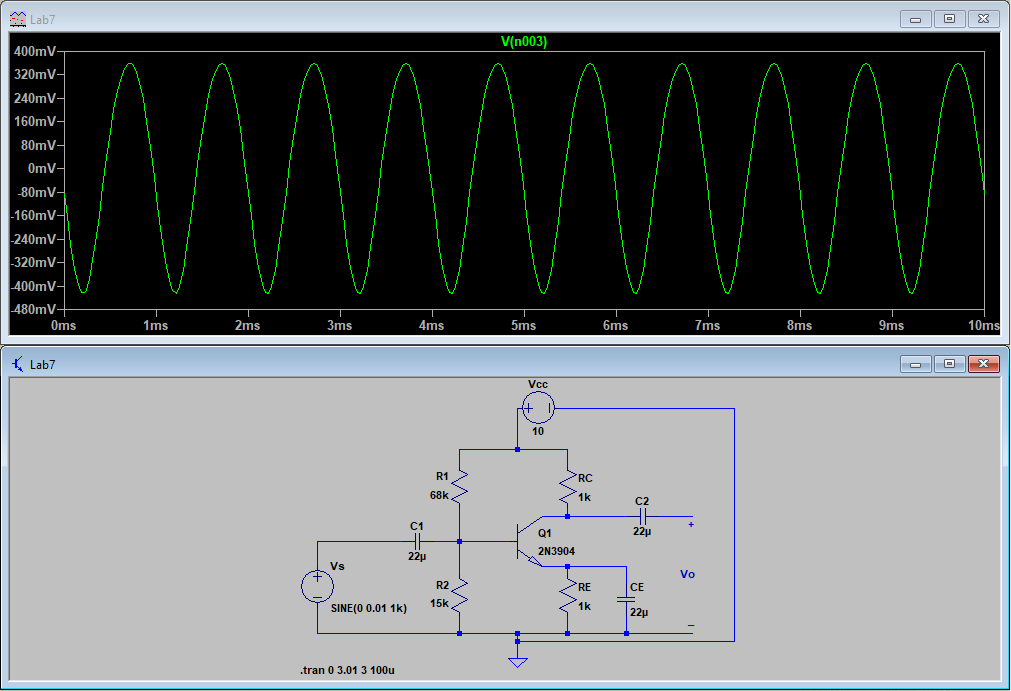


Figure 7: Figure 7.1 Simulation of Vo w/

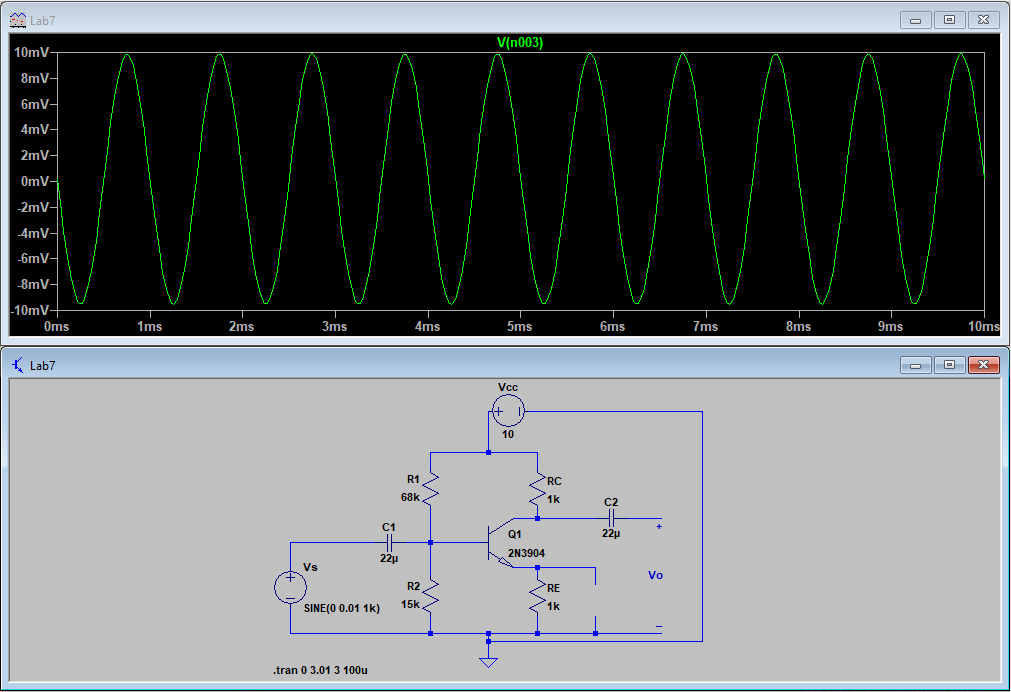


Figure 8: Figure 7.1 Simulation of Vo w/

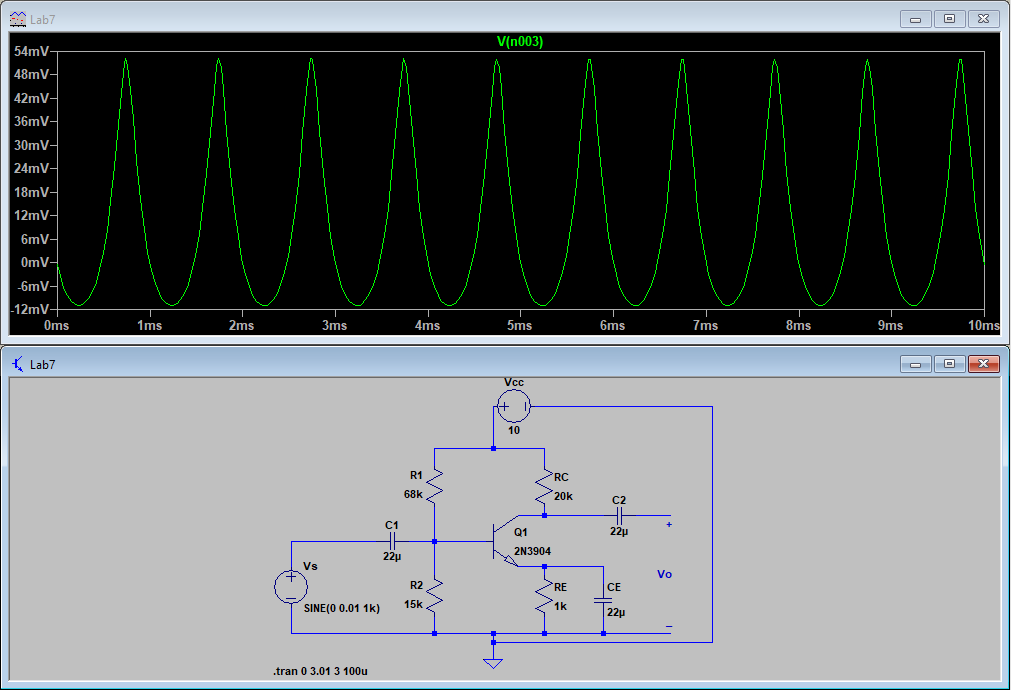


Figure 9: Figure 7.1 Simulation of Vo w/

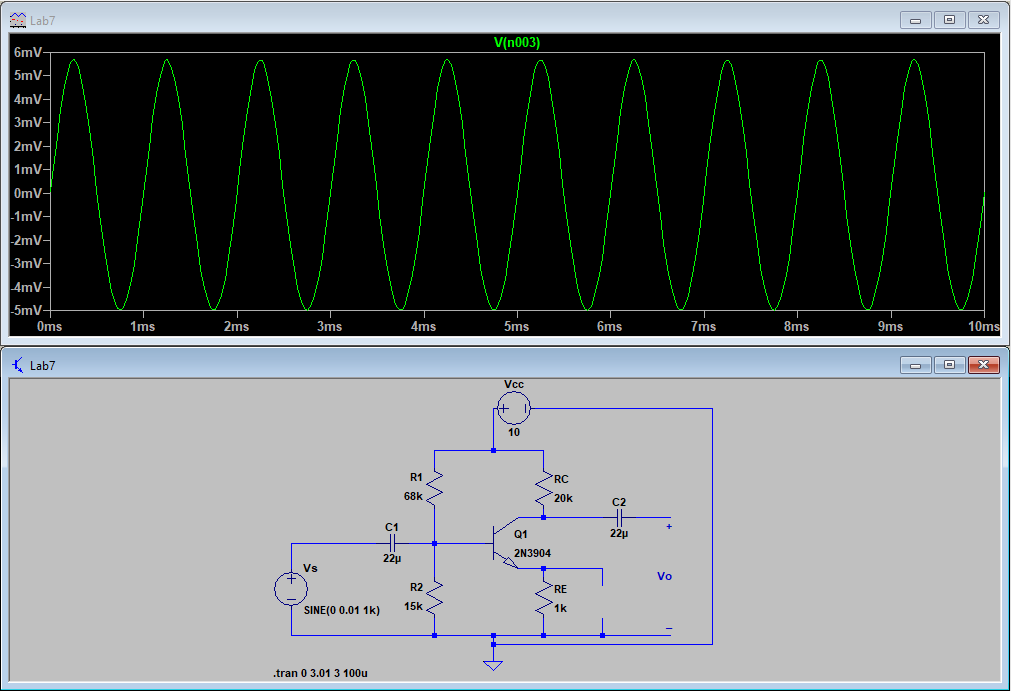


Figure 10: Figure 7.1 Simulation of Vo w/