EEL 5764 HW #2

1. Impact on cache hierarchy, power, and overall application energy for an L2 cache with:

a) Small block size - small block size increases the miss rate for compulsory misses, but decreases the miss rate for conflict misses or capacity misses in comparison to a larger block size. Which in turn would reduce miss penalty, which lowers power consumption overall for programs with high locality of instructions and data with fewer cache misses. Therefore application energy is slightly lowered with a smaller overall miss penalty.

b) Small cache size - smaller cache size increases capacity misses and decreases hit time. However it can also reduce overall power consumption as less energy is needed to search the cache, however if there are no other optimizations, only power consumption will decrease slightly.

HW #2 (cont.)

1c) High associativity - the higher the associativity of a cache the more hardware is necessary to determine a hit, therefore hit times are increased although conflict misses are decreased as well as capacity misses. However all that extra hardware needs to be powered so the higher a caches associativity, the higher the power consumption and energy needs.

2 (5.13)

VP accessed	TLB (hit or miss)	Page Table (hit or fault)
1	miss	fault
5	hit	X
9	miss	fault
14	miss	fault
10	hit	X
6	miss	hit
15	hit	X
12	miss	hit
7	miss	hit
2	miss	fault

→

HW #2 (cont.)

3 A.1)

	loads	stores	branches	jumps	ALU
astar	28%	6%	18%	2%	46%
gcc	17%	23%	20%	4%	56%
average	22.5%	14.5%	19%	3%	41%

$$CPI_{eff} = (1 \cdot 0.41) + (5 \cdot 0.225) + (3 \cdot 0.145) + ([5+3)/2] \cdot 0.19) + (3 \cdot 0.03)$$

(ALU, LOADS, STORES, BRANCHES, JUMPS)

$$\Rightarrow \boxed{CPI_{eff} = 2.82 \text{ clock cycles}}$$

5 taken
3 not taken
> avg of 4