EEL 5764 Computer Architecture
Fall 2018
Midterm 1

Name: _____ **UFID:** _____

Notes:
- Exam is 75 minutes long.
- Exam is closed book and closed notes.
- Other than scientific calculators, all electronics must be turned off.
- Please write legibly. Otherwise your grades may be negatively affected.
- You must show your work for all problems.
- Use the back of the exam paper as necessary. Indicate clearly, which problems the answers on the back correspond to.

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1. **(8x2 pts)** Decide whether the following statements are true or false. Add brief (1-2 sentence) explanations to justify your answers.

   a. Segmentation and paging can both result in wasted space for virtual memory.

   b. Larger block size always results in less cache misses.

   c. For a page residing in main memory, you can always find its virtual address to physical address translation in TLB.

   d. You do not need to pay attention to Amdahl's Law because it is not applicable any more.

   e. In Tomasulo's algorithm, floating point instructions issued for execution wait for availability of functional unit in the Reorder Buffer.

   f. Non-aligned memory access decreases performance.

   g. In following instruction sequence:

   ```
   Load R2, #60(R3)
   Subtract R9, R2, #30
   ```

   data hazard can be fully eliminated by forwarding.

h. Instructions pass the "Issue" stage out-of-order with dynamic scheduling.

2. **(10 pts)** For a given processor with a five-stage pipeline, branch instructions constitute 25% of the total instructions, and branches are taken 70% of the time. Assume that branches are always predicted as non-taken, taken branches stall the pipeline for 3 cycles, and non-taken branches do not cause any stall. How much faster would the processor be without the branch hazards?

3. **(10 pts)** You're designing a system which has a requirement average memory access time of 3ns. You are using a direct mapped cache that has access time of 0.5ns and miss penalty of 20 cycles. Assume cycle time is 0.5ns. What is the maximum miss rate your cache must maintain to keep the average memory access time to 3ns?

4. **(8 pts)** Assume that a processor has the following properties: 2ns cycle time, 2 cycle ALU, 2 cycle branches, and 10 cycle memory access. Assume ALU instructions are 40%, branch instructions are 10%, and memory instructions are 50%, of the program. What is the average execution time of this processor?

5. **(8 pts)** A program consisting of 1000 instructions is executed on a 5-stage processor. How many cycles would be required to complete the program, (i) without pipelining, (ii) with pipelining? Assume ideal overlap in case of pipelining.

6. **(10 pts)** Consider the following information regarding cache design.
   - Average memory access per instruction is 1.5
   - Ideal CPI = 1 cycle
   - Clock rate = 1 GHz
   - Main memory access time = 100ns
   - Hit time for L2 cache = 20 cycles
   - Local miss rates for L1 and L2 cache are 2% and 40% respectively.

   Compute the effective CPIs *with* and *without* L2 cache.

7. **(4x2 pts)** For each of the questions below, you will need to select one or more of the choices. Add a 1-sentence explanation for your choice(s).
   a. Moore's law states that

i. transistor density will double every year
ii. transistor density will double every 18 months
iii. transistor density will double every 36 months
iv. transistor scaling will stop eventually

b. Instruction `Add R4,100(R1)` is an example of:
   i. Immediate addressing
   ii. Displacement addressing
   iii. Scaled addressing
   iv. Memory indirect addressing

c. ISA affects the following performance related metrics:
   i. Instruction count
   ii. Clock frequency
   iii. CPI
   iv. NONE

d. In a write-back scheme, a block is copied to main memory during block replacement if
   i. Valid bit = 1
   ii. Dirty bit = 1
   iii. Valid bit =1 and Dirty bit = 1
   iv. None