1. (30 pts) You are designing a PMD that is optimized for low power. Qualitatively explain the impact on cache hierarchy (L2 and memory) power and overall application energy if you design an L2 cache with:

a.Small block size

Small block size is related to miss rate. If there is a lot of miss, then power consumption may increase if accessing main memory takes more power than the L2 Cache access.

b.Small cache size

There will be less static power consumption due to less area.
If there is a lot of miss, then power consumption may go up if main memory access takes more power than accessing the L2 Cache.

c.High associativity

There will be extra hardware requirement to implement higher associativity which will lead to extra power consumption. However, the amount of misses may be reduced which will in turn reduce the number of main memory access. If accessing main memory causes more power consumption than the L2 Cache access then it may attribute to a slight reduction in power consumption. But in the end, it is hard to tell if the overall power consumption will be go down or not. It has a huge dependency on the data access pattern.

2.

Virtual Page Accessed	TBL (hit or miss)	Page Table (Hit or Fault)
1	Miss	Fault
5	Miss	Hit
9	Miss	Fault
14	Miss	Fault
10	Miss	Hit
6	Miss	Hit
15	Miss	Hit
12	Miss	Hit
7	Miss	Hit
2	Miss	Fault

3.

Average fraction of Loads (between astar and gcc): 0.225
Average fraction of Stores (between astar and gcc): 0.145
Average fraction of Branches (between astar and gcc): 0.19
Average fraction of Jumps (between astar and gcc): 0.03
Average fraction of ALU OP (between astar and gcc): 0.41

Average CC for Branches = (5+3)/2 = 4

Assuming 50% branches are taken and the other 50% not taken.

Effective CPI for an embedded system executing astar and gcc is:
(0.225*5) + (0.145*3) + (0.19*4) + (0.03*3) +(0.41 * 1) = **2.82**