EEL 5764 HW #4

11/25/19

1 5.4(a)) 1) C0: R, AC00
2) C0: W, AC00 <--40

	MSI	MESI
1) Read miss, in mem, no sharers	S	E
2) Write to cache, no sharers	invalidate	M (no invalidate signal)

Goes to mem once + invalidates for MSI ⇒ 115 stall cycles
Goes to mem once for MESI ⇒ 100 stall cycles

5.4(b)) 1) C0: R, AC20
2) C0: W, AC20 <-60

	MSI	MESI
1) Read miss, in mem, sharers	S	S
2) Write to cache, invalidate sharers	invalidate	invalidate

Both go to memory once & both invalidate once
∴ 115 stall cycles for both MSI & MESI

5.4(c)) 1) C0: R, AC00
2) C0: R, AC20

	MSI	MESI
1) Read miss, in mem, no sharers	S	E
2) Read miss, in mem, sharers	S	S

Both reach mem twice and no other stalls
⇒ 200 stall cycles for both MSI & MESI

HW #4 (cont.)

Mem Access		State P1	State P2	State P3	Bus Action	Cycles
P1 Reads	MSI	S	n/a	n/a	BusRd	120
	MESI	E	n/a	n/a	BusRd	120
	MOESI	E	n/a	n/a	BusRd	120
P1 Writes	MSI	M	I	I	BusInv	120
	MESI	M	n/a	n/a	n/a	1
	MOESI	M	n/a	n/a	n/a	1
P2 Reads	MSI	S	S	I	BusRd	120
	MESI	S	S	n/a	BusRd	120
	MOESI	O	S	n/a	n/a	1
P3 Reads	MSI	S	S	S	BusRd	120
	MESI	S	S	S	BusRd	120
	MOESI	O	S	S	n/a	1
P2 Writes	MSI	I	M	I	BusInv	120
	MESI	I	M	I	BusInv	120
	MOESI	I	M	I	BusInv	120
P1 Reads	MSI	S	S	I	BusRd	120
	MESI	S	S	I	BusRd	120
	MOESI	S	O	I	n/a	1
P3 Writes	MSI	I	I	M	BusRdX	120
	MESI	I	I	M	BusRdX	120
	MOESI	I	I	M	BusRdX	120
P1 Writes	MSI	M	I	I	BusRdX	120
	MESI	M	I	I	BusRdX	120
	MOESI	M	I	I	BusRdX	120
P1 Reads	MSI	M	I	I	n/a	1
	MESI	M	I	I	n/a	1
	MOESI	M	I	I	n/a	1