EEL 5764 Computer Architecture
Fall 2019
Homework 4

Note: Discussion is allowed, but your submission must be your own work.

Q1) [10,10,10] Complete the following problems at the end of Chapter 5 of the textbook(Hennessey Patterson 6th Edition): **5.4(a), 5.4(b), 5.4(c).**

Q2) [20] Draw state table for MSI, MESI & MOESI for the following set of instructions for a 3 processor configuration. Consider that every bus transaction takes 120 cycles and 1 cycle for a hit. Your state table should have the following structure:

Mem. Access	State P1	State P2	State P3	Bus Action	Cycles

Sequence:
Processor 1reads
Processor 1 writes
Processor 2 reads
Processor 3 reads
Processor 2 writes
Processor 1 reads
Processor 3 writes
Processor 1 writes
Processor 1 reads