1 (a) True

(b) False, reduce compulsory increase capacity and conflict

(c) False

(d) False

(e) False, wait at reservation station

(f) True, more reads than necessary

(g) False, one cycle stall still necessary

(h) False, in-order

2] Branch (misprediction) frequency = (.25)(.7) = .175

Speedup with hazards = (pipeline depth) / (1 + branch freq * branch penalty) = 5 / (1 + 0.175 * 3) = 3.28

Overall speedup without hazards / Speedup with hazards = 5/3.25 = 1.59

3] 3ns = AMAT = hit time + miss rate * miss penalty = 0.5ns + (miss rate) * (20 * 0.5 ns)

Miss rate = (3 – 0.5) / (20 * 0.5) = 0.25

4] (2 * 2ns) * (.4) + (2 * 2ns) * (.1) + (10 * 2ns) (.5) = 1.6 + .4 + 10 = 12 ns

5] Without pipelining: 5 * 1000 cycles

With pipelining: 5 + 999 cycles = 1004 cycles

6] [Note: memory references come from Instruction fetch (every instruction) and memory operations for load/store. That is why there are more than 1 memory references per instruction on average.]

Clock rate = 1 GHz. 1 cycle = 1 ns. Memory access time = 100 ns. Thus, main memory access time = 100 cycles

Time to process an instruction = (memory references per instruction) * (memory access time)

[Assuming that rest of the instruction processing time is negligible.]

Avg. memory access time without L2 = 0.02 * (100) = 2 cycles

Avg memory access time with L2 = 0.02 *[20 + 0.4 *100] = 1.2 cycles

Processing time per instruction without L2 = 1.5 * 2 = 3 cycles = 3ns

Processing time per instruction with L2 = 1.5 * 1.2 = 1.8 cycles = 1.8 ns

7] (a : ii), (b : ii), (c : i & iii), (d : iii)