EEL 5764 Computer Architecture

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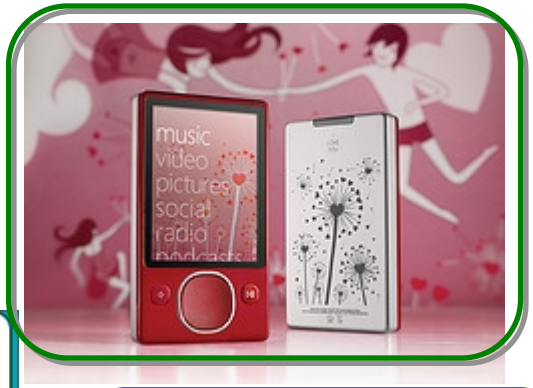
Lecture 3:
System Design Parameters

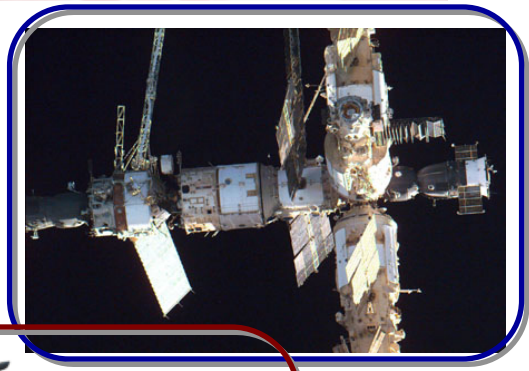
Announcements

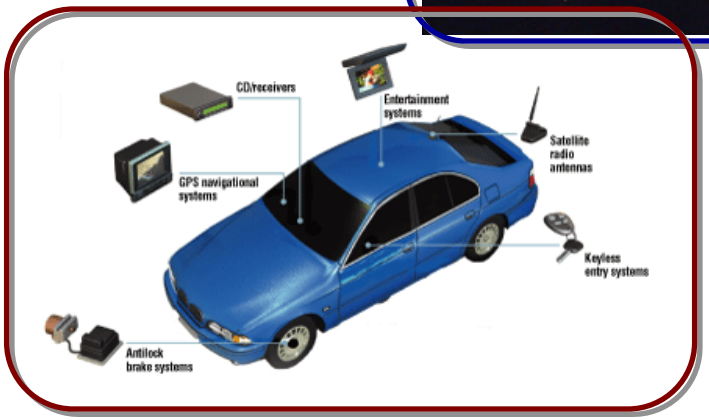
- **TA office hours posted on Canvas**
- TA office hours will be held in NEB 288*
- My (Instructor) office hours will be in BEN 323
- We will post an overall schedule for the course by next week
  - →Will include HW assignment schedule and mid-terms

System Design Parameters

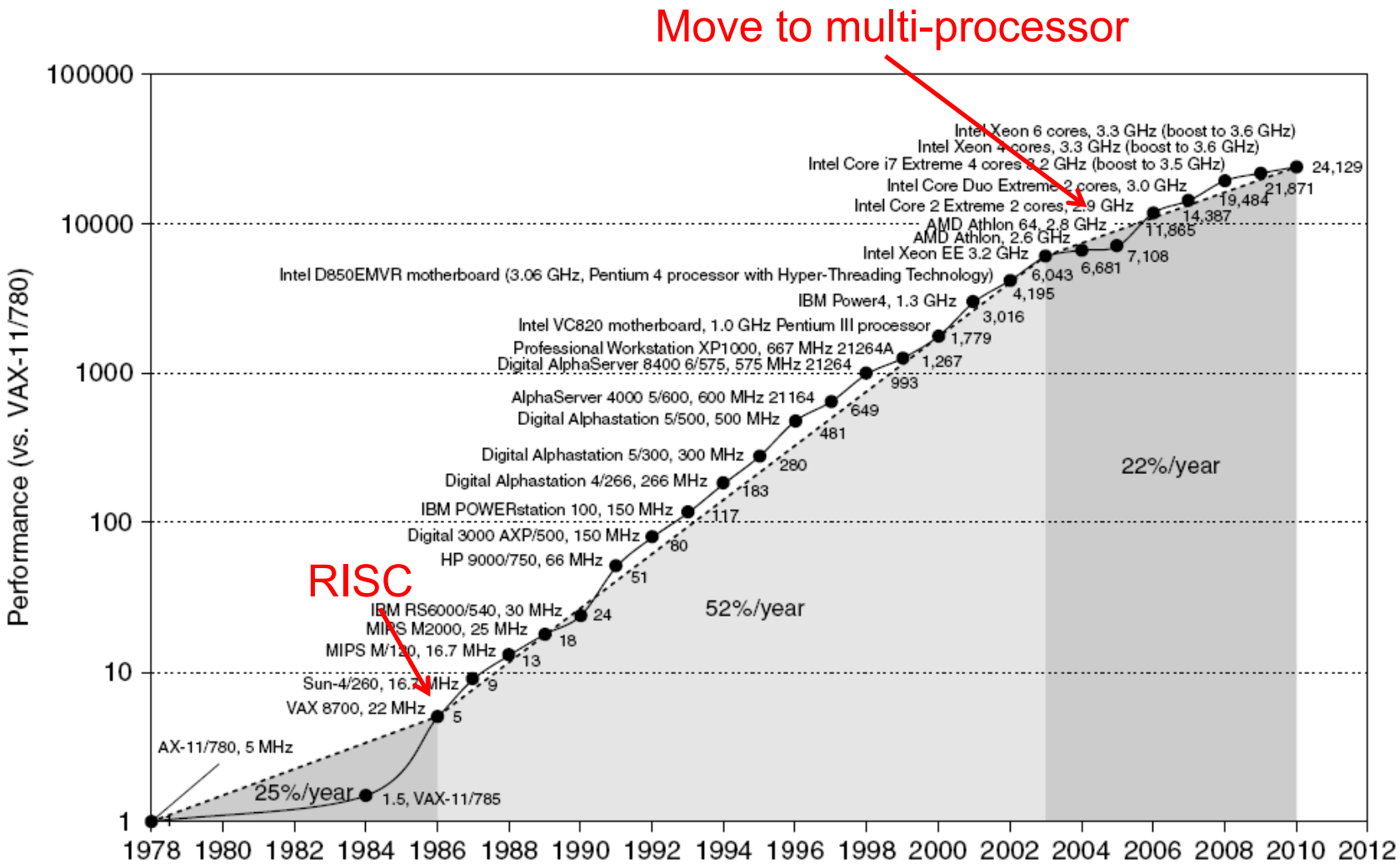
- Performance (Speed)
- Cost
- Power (static + dynamic)
  - →Peak power
  - →Average power
- Robustness
  - →Noise-tolerance
  - →Radiation-hardness
- Testability
- Reconfigurability
- Time-to-market etc.







Single Processor Performance



Computer Technology Driving Forces

- **Improvements in semiconductor technology**
  - →Feature size, clock speed, cost
- **Improvements in computer architectures**
  - →Enabled by high-level language compilers, UNIX
  - →Lead to RISC architectures

- **Together have enabled:**
  - →More powerful and efficient computers.
  - →New classes of computers, i.e. mobile devices, etc.
  - →Penetration of GP CPUs into many applications.
  - →Tradeoff between performance and productivity in SW development.

Current Trends in Architecture

- Power Wall
- Memory Wall
- Lack of Instruction-Level parallelism (ILP) to exploit
  → Single processor performance improvement ended in 2003

- New models for performance:
  → Data-level parallelism (DLP)
  → Thread-level parallelism (TLP)
  → Request-level parallelism (RLP)

- These require explicit restructuring of the application
  →Applications must expose parallelism explicitly.

Classes of Parallelism

- Exploitation of parallelism -> performance

- Classes of parallelism in applications:
  - → *Data-Level Parallelism* (DLP)
  - → *Task-Level Parallelism* (TLP)

- Classes of architectural parallelism:
  - → *Instruction-Level Parallelism* (ILP)
  - → *Vector architectures/Graphic Processor Units* (GPUs)
  - → *Thread-Level Parallelism (TLP)*
  - → *Request-Level Parallelism (RLP)*

Flynn's Taxonomy

- *Single instruction stream, single data stream (SISD)*
  - → Exploit ILP and TLP in some degree
- *Single instruction stream, multiple data streams (SIMD)*
  - → Targets DLP
  - → Vector architectures
  - → Multimedia extensions
  - → Graphics processor units
- *Multiple instruction streams, single data stream (MISD)*
  - → No commercial implementation
- *Multiple instruction streams, multiple data streams (MIMD)*
  - → Targets TLP and RLP
  - → Tightly-coupled MIMD - TLP
  - → Loosely-coupled MIMD - RLP

Computer Architecture – Past and Now

- "Old" view of computer architecture:
  - → Instruction Set Architecture (ISA) design
  - → i.e. decisions regarding:
    - ➤ registers, memory addressing, addressing modes, instruction operands, available operations, control flow instructions, instruction encoding

- "Real" computer architecture:
  - → ISA design is less of a focus
  - → Specific requirements of the target machine
  - → Design to find a best tradeoff among performance, cost, power, and availability, etc, optimized for target applications
  - → Includes ISA, microarchitecture, logic/circuit design, implementation, etc.

Impacts from requirements of applications and technology