EEL 5764 Computer Architecture, Fall 2019
Homework 3
Due: 11/12/2019, 4:00 am

Note: While discussions in the general topic area are allowed, your submission must be your own work.

Q1] (20 pts) Complete the following problems at the end of Chapter 3 of textbook: **3.11**

Q2] (20 pts) A 5-stage pipelined RISC processor running at 3.4GHz uses a static branch predictor with always-not-taken prediction. A program is executed on the processor. Assume that **20%** of the dynamic instructions in the program are branch instructions and **80% of all the branches are Taken. Also assume that branch mispredictions are the only source of pipeline stalls in the processor**. Calculate the instruction throughput (*Instructions completed per second*) under following scenarios:
(a) The computation of branch outcome is done in the "EX" stage.
(b) The computation of branch outcome is done in the "ID" stage.

Q3] (10 pts) Assume the following MIPS code:

```
        ADD R2, R1, R1
Loop:   BNEZ R2, If2
        ADDI R2, R1, #2
If2:    ADDI R2, R1, #-1
        JUMP Loop
Done:
```

Using a two-bit predictor, what will be the prediction accuracy? **Assume that the predictor is initialized to Not-Taken.**