Computer Architecture Project Proposal

Project Name: Implementing and Comparing Memory Performance with and without Translation Lookaside Buffers

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Team Name = TLB: Team Lets Ball

Translation lookaside buffers are an important part of modern CPUs to improve memory access time. Throughout modern computing history, computer architects have formulated several methods of optimizing the average memory access time, complexity, and hardware footprint of caches and memory. We plan on investigating the effect of different TLB configurations on memory performance. Specifically, we plan on implementing a control version with no instruction TLB or data TLB, a version with no instruction TLB and a small data TLB, a version with a small instruction TLB and no data TLB, and one last version with a large instruction TLB and a large data TLB. Each of these variations will be compared using multiple different metrics. Specifically, the attributes we plan on measuring will be the AMAT (average memory access time), the utilization of each TLB when implemented, and the average CPI with and without the different TLB implementations.

We intend to investigate these memory address translation methods via a utilization of the SimpleScalar hardware modeling and software analysis tool. There will be three experimental variables tested in this investigation when it comes to the TLBs: the presence of an instruction or data TLB, the presence of a TLB for both instruction and data memory, and the size of each TLB. The goal of changing all these variables is to characterize the best TLB profile that has been tested and what characteristics identify the best TLB profile.