Universidad De Buenos Aires

Facultad De Ingeniería

66.17 Sistemas digitales

Voltímetro digital con salida VGA

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Índice

1. Objetivos

El objetivo del presente Trabajo Práctico consiste en especificar, diseñar, describir una arquitectura, simular, sintetizar e implementar en FPGA un sistema digital para un voltímetro digital con salida VGA.

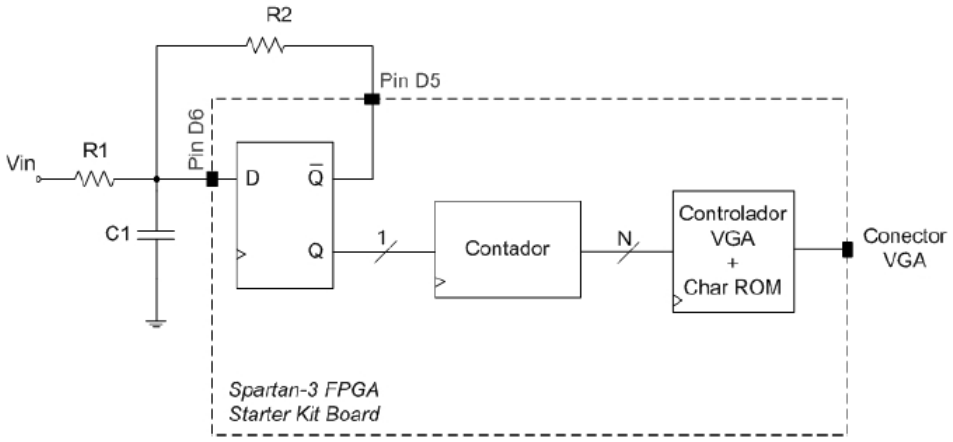

Figura 1: Diagrama en bloques de la arquitectura propuesta.

2. Modulos

2.1. Registro

Se realizo una implementación simple de un registro usando un process que seteaba la salida a partir de las entradas.

```
entity registro is
     generic(N: integer:= 4); -- valor genérico
     port(
          D: in std_logic_vector(N-1 downto 0); -- entrada del registro
          clk: in std_logic; -- señal de reloj
          rst: in std_logic; -- señal de reset
          ena: in std_logic; -- señal de habilitación
          Q: out std_logic_vector(N-1 downto 0) -- salida del registro
     );
end;


architecture pp of registro is
begin
     process(clk, rst, ena)
     begin
          if rst = '1' then
               Q <= (others => '0');
          elsif clk = '1' and clk'event then
               if ena = '1' then
                    Q <= D;
               end if;
```

```
          end if;
     end process;
end;
```

2.2. Char ROM

Para la memoria ROM se declaro un array de 255x8 donde se guarda la configuración de los números, ya que solo necesitamos los numeros del 0 al 9, el punto y la V, este array fue seteado en 0 desde la posicion 96 a la 255.

2.3. Controlador VGA

A través del controlador VGA ubicamos cada digito segun la fila y columna donde debia aparecer, obteniamos el digito correspondiente del contador de decadas y segun que numero era haciamos referencia a la dirección de la ROM donde se encontraba dicha representación.

2.4. Contador

Para el diseño del contador se uso un process que se encargaba de ir sumando hasta cierto valor, en el que reseteaba y volvia a empezar.

2.5. Conclusión

Con la realización del presente trabajo se logro aprender a hacer una aplicación para FPGA con salida VGA, esto nos permite tener una representación grafica mucho más flexible que la limitada por hardward como pueden ser los leds o displays de 7 segmentos.

2.6. Output sintetización

Xilinx Design Summary

Board_Top Project Status (10/22/2013 - 13:31:34)			
Project File:	testXilinx.xise	**Parser Errors:**	No Errors
Module Name:	aplicVGA	**Implementation State:**	Placed and Routed
Target Device:	xc3s500e-4fg320	• **Errors:**	No Errors
Product Version:	ISE 14.2	• **Warnings:**	68 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	104	9,312	1%	
Number used as Flip Flops	85			
Number used as Latches	19			
Number of 4 input LUTs	228	9,312	2%	
Number of occupied Slices	166	4,656	3%	
Number of Slices containing only related logic	166	166	100%	
Number of Slices containing unrelated logic	0	166	0%	
Total Number of 4 input LUTs	284	9,312	3%	
Number used as logic	228			
Number used as a route-thru	56			
Number of bonded IOBs	12	232	5%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.21			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Oct 23	0	52 Warnings (0	6 Infos (0 new)

		15:45:12 2013		new)	
Translation Report	Current	Fri Oct 23 15:45:16 2013	0	0	0
Map Report	Current	Fri Oct 23 15:45:19 2013	0	3 Warnings (0 new)	4 Infos (0 new)
Place and Route Report	Current	Fri Oct 23 15:45:40 2013	0	2 Warning (0 new)	2 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Fri Oct 23 15:45:42 2013	0	0	6 Infos (0 new)
Bitgen Report	Out of Date	Fri Oct 23 15:45:52 2013	0	3 Warnings (0 new)	0

Secondary Reports		[-]
Report Name	**Status**	**Generated**
WebTalk Report	Out of Date	Fri Oct 23 15:45:23 2013
WebTalk Log File	Out of Date	Fri Oct 23 15:45:45 2013

Date Generated: 10/23/2013 - 15:45:55

Board_Top Project Status (09/21/2013 - 11:13:33)			
Project File:	testXilinx.xise	**Parser Errors:**	No Errors
Module Name:	Board_Top	**Implementation State:**	Placed and Routed
Target Device:	xc3s500e-4fg320	• **Errors:**	No Errors
Product Version:	ISE 14.2	• **Warnings:**	16 Warnings (16 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	84	9,312	1%	
Number of 4 input LUTs	68	9,312	1%	
Number of occupied Slices	79	4,656	1%	
Number of Slices containing only related logic	79	79	100%	
Number of Slices containing unrelated logic	0	79	0%	
Total Number of 4 input LUTs	130	9,312	1%	
Number used as logic	68			
Number used as a route-thru	62			
Number of bonded IOBs	17	232	7%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.71			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun Sep 22 15:12:32 2013	0	5 Warnings (5 new)	0
Translation Report	Current	Sun Sep 22 15:12:38	0	0	0

		2013			
Map Report	Current	Sun Sep 22 15:12:42 2013	0	3 Warnings (3 new)	4 Infos (4 new)
Place and Route Report	Current	Sun Sep 22 15:12:55 2013	0	5 Warnings (5 new)	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	Sun Sep 22 15:12:59 2013	0	0	6 Infos (6 new)
Bitgen Report					

Secondary Reports		[-]
Report Name	**Status**	**Generated**

Date Generated: 09/22/2013 - 15:13:01