Board_Top Project Status (10/22/2013 - 13:31:34)			
Project File:	testXilinx.xise	**Parser Errors:**	No Errors
Module Name:	aplicVGA	**Implementation State:**	Placed and Routed
Target Device:	xc3s500e-4fg320	• **Errors:**	No Errors
Product Version:	ISE 14.2	• **Warnings:**	50 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	104	9,312	1%	
Number used as Flip Flops	85			
Number used as Latches	19			
Number of 4 input LUTs	228	9,312	2%	
Number of occupied Slices	166	4,656	3%	
Number of Slices containing only related logic	166	166	100%	
Number of Slices containing unrelated logic	0	166	0%	
Total Number of 4 input LUTs	284	9,312	3%	
Number used as logic	228			
Number used as a route-thru	56			
Number of bonded IOBs	12	232	5%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.21			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Tue Oct 22	0	46 Warnings (0	6 Infos (0 new)

		13:31:09 2013		new)	
Translation Report	Current	Tue Oct 22 13:31:13 2013	0	0	0
Map Report	Current	Tue Oct 22 13:31:16 2013	0	3 Warnings (0 new)	4 Infos (0 new)
Place and Route Report	Current	Tue Oct 22 13:31:30 2013	0	1 Warning (0 new)	2 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Tue Oct 22 13:31:32 2013	0	0	6 Infos (0 new)
Bitgen Report	Out of Date	Tue Oct 22 13:21:20 2013	0	3 Warnings (0 new)	0

Secondary Reports		**[-]**
Report Name	**Status**	**Generated**
WebTalk Report	Out of Date	Tue Oct 22 13:21:20 2013
WebTalk Log File	Out of Date	Tue Oct 22 13:21:41 2013

Date Generated: 10/22/2013 - 13:31:34