Board_Top Project Status (09/21/2013 - 11:13:33)			
Project File:	testXilinx.xise	**Parser Errors:**	No Errors
Module Name:	Board_Top	**Implementation State:**	Placed and Routed
Target Device:	xc3s500e-4fg320	• **Errors:**	No Errors
Product Version:	ISE 14.2	• **Warnings:**	16 Warnings (16 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	84	9,312	1%	
Number of 4 input LUTs	68	9,312	1%	
Number of occupied Slices	79	4,656	1%	
Number of Slices containing only related logic	79	79	100%	
Number of Slices containing unrelated logic	0	79	0%	
Total Number of 4 input LUTs	130	9,312	1%	
Number used as logic	68			
Number used as a route-thru	62			
Number of bonded IOBs	17	232	7%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.71			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun Sep 22 15:12:32 2013	0	5 Warnings (5 new)	0
Translation Report	Current	Sun Sep 22 15:12:38	0	0	0

		2013			
Map Report	Current	Sun Sep 22 15:12:42 2013	0	3 Warnings (3 new)	4 Infos (4 new)
Place and Route Report	Current	Sun Sep 22 15:12:55 2013	0	5 Warnings (5 new)	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	Sun Sep 22 15:12:59 2013	0	0	6 Infos (6 new)
Bitgen Report					

Secondary Reports		[-]
Report Name	**Status**	**Generated**

Date Generated: 09/22/2013 - 15:13:01