| Board_Top Project Status (10/22/2013 - 13:31:34) | | | |
|---|---|---|---|
| **Project File:** | testXilinx.xise | **Parser Errors:** | No Errors |
| **Module Name:** | aplicVGA | **Implementation State:** | Placed and Routed |
| **Target Device:** | xc3s500e-4fg320 | • **Errors:** | No Errors |
| **Product Version:** | ISE 14.2 | • **Warnings:** | 68 Warnings (0 new) |
| **Design Goal:** | Balanced | • **Routing Results:** | All Signals Completely Routed |
| **Design Strategy:** | Xilinx Default (unlocked) | • **Timing Constraints:** | All Constraints Met |
| **Environment:** | System Settings | • **Final Timing Score:** | 0 (Timing Report) |

| Device Utilization Summary | | | | [-] |
|---|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** |
| Total Number Slice Registers | 104 | 9,312 | 1% | |
| Number used as Flip Flops | 85 | | | |
| Number used as Latches | 19 | | | |
| Number of 4 input LUTs | 228 | 9,312 | 2% | |
| Number of occupied Slices | 166 | 4,656 | 3% | |
| Number of Slices containing only related logic | 166 | 166 | 100% | |
| Number of Slices containing unrelated logic | 0 | 166 | 0% | |
| Total Number of 4 input LUTs | 284 | 9,312 | 3% | |
| Number used as logic | 228 | | | |
| Number used as a route-thru | 56 | | | |
| Number of bonded IOBs | 12 | 232 | 5% | |
| Number of BUFGMUXs | 1 | 24 | 4% | |
| Average Fanout of Non-Clock Nets | 3.21 | | | |

| Performance Summary | | | [-] |
|---|---|---|---|
| **Final Timing Score:** | 0 (Setup: 0, Hold: 0) | **Pinout Data:** | Pinout Report |
| **Routing Results:** | All Signals Completely Routed | **Clock Data:** | Clock Report |
| **Timing Constraints:** | All Constraints Met | | |

| Detailed Reports | | | | | [-] |
|---|---|---|---|---|---|
| **Report Name** | **Status** | **Generated** | **Errors** | **Warnings** | **Infos** |
| Synthesis Report | Current | Fri Oct 23 | 0 | 52 Warnings (0 | 6 Infos (0 new) |

| | | | | | |
|---|---|---|---|---|---|
| | | 15:45:12 2013 | | new) | |
| Translation Report | Current | Fri Oct 23 15:45:16 2013 | 0 | 0 | 0 |
| Map Report | Current | Fri Oct 23 15:45:19 2013 | 0 | 3 Warnings (0 new) | 4 Infos (0 new) |
| Place and Route Report | Current | Fri Oct 23 15:45:40 2013 | 0 | 2 Warning (0 new) | 2 Infos (0 new) |
| Power Report | | | | | |
| Post-PAR Static Timing Report | Current | Fri Oct 23 15:45:42 2013 | 0 | 0 | 6 Infos (0 new) |
| Bitgen Report | Out of Date | Fri Oct 23 15:45:52 2013 | 0 | 3 Warnings (0 new) | 0 |

| **Secondary Reports** | | [-] |
|---|---|---|
| **Report Name** | **Status** | **Generated** |
| WebTalk Report | Out of Date | Fri Oct 23 15:45:23 2013 |
| WebTalk Log File | Out of Date | Fri Oct 23 15:45:45 2013 |

**Date Generated:** 10/23/2013 - 15:45:55