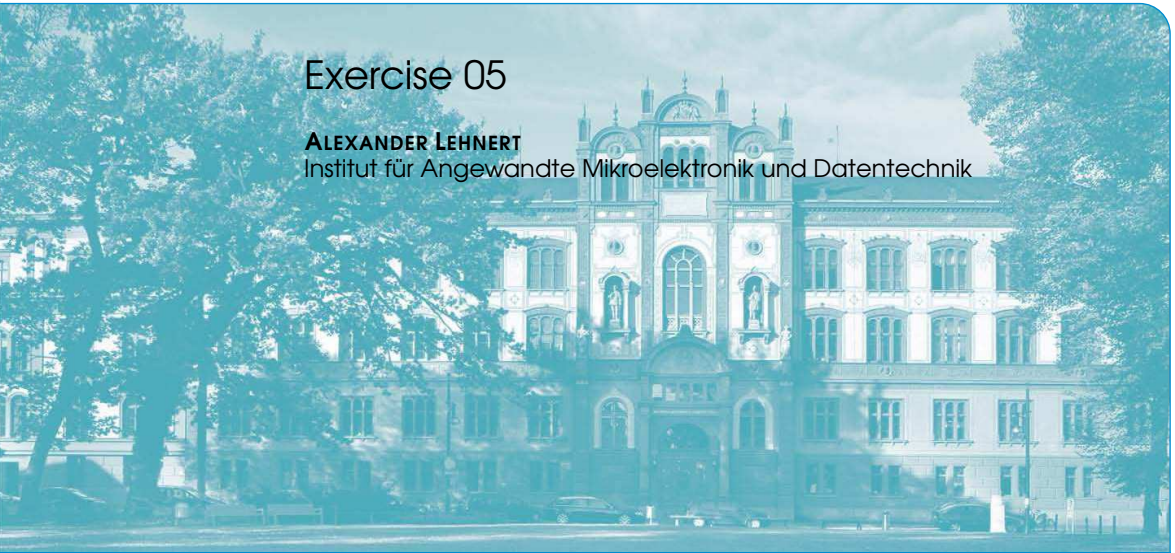

Exercise 05

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Overview

1. Program Counter
2. ALU
3. Register File
4. Instruction Memory
5. Data Memory
6. Control Logic

The Memory Block: Block Diagram

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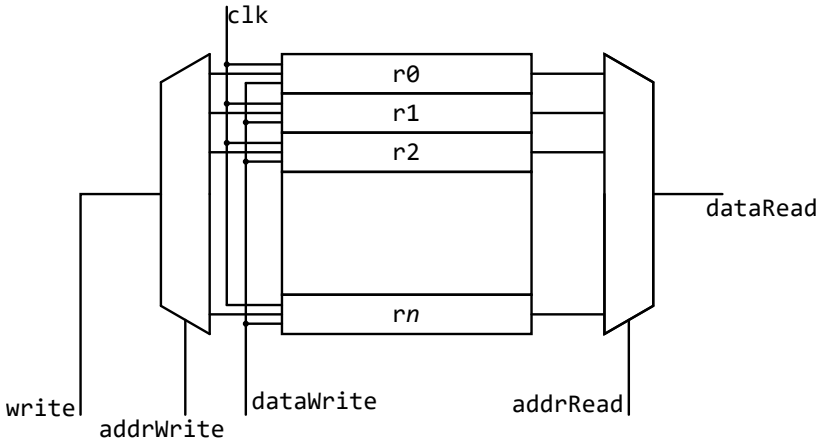

Mapping

- For now: Mapping to LUTs
- Are there more components?

Mapping

- For now: Mapping to LUTs
- Are there more components?
- Better: Mapping to BRAM
- How to map to BRAM?

Evaluation: Timing

- Required: Implementation
- Yields Timing Report
- We can control timing: Clock Delay Constraint
- WNS: Worst negative slack
- Data paths can be explored in detail
- How to find the operating frequency?

Evaluation: Power

- What causes power dissipation?

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- Static power, is determined by the components utilized
- Dynamic power, depends on the switching activity

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Evaluation: Power

- What causes power dissipation?
- Static power, is determined by the components utilized
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- How to get a switching activity?
- Option 1: Statistical assumptions
- Option 2: Record switching activity during simulation

→ Post-Implementation Simulation

Tasks

1. Implement memory entity
2. Simulation: Verify your implementation functionally
3. Synthesis and implementation: Evaluate your design
4. Explore other mappings