GPC v1 Instruction Table

OP Code	ASM Rep.	PARM A	PARM B	Clock cycles	Length	DESCRIPTION
00	NOP			3	1	Only Advances Program Counter by 1
01	LDA	source		9	3	Loads value at {source} memory address into A-Register
02	LDA	value		5	2	Loads Immediate value into A-Register
03	LDB	source		9	3	Loads value at {source} memory address into B-Register
04	LDB	value		5	2	Loads Immediate value into B-Register
05	STA	target		8	3	Stores value at A register to {target} memory address
06	STB	target		8	3	Stores value at B register to {target} memory address
07	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
08	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
09	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
0A	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
0B	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
0C	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
0D	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
0E	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
0F	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
10	ADD			3	1	Adds A and B register together and stores to A-Register
11	ADD	target		9	3	Adds A and B register together and stores to {target} memory address
12	ADC			3	1	Adds A and B register together and stores to A-Register + sets carry flag if A+B>0xFF
13	ADC	target		9	3	Adds A and B register together and stores to {target} memory address + sets carry flag if A+B>0xFF
14	OR			3	1	ORs A and B register and stores to A-Register
15	OR	target		9	3	ORs A and B register and stores to {target} memory address
16	AND			3	1	ANDs A and B register and stores to A-Register
17	AND	target		9	3	ANDs A and B register and stores to {target} memory address
18	NOT			3	1	Inverts value of A-Register and stores result in A-Register
19	NOT	target		9	3	Inverts value of A-Register and stores result at {target} memory address
1A	XOR			3	1	XORs A and B register and stores to A-Register
1B	XOR	target		9	3	XORs A and B register and stores to {target} memory address
1C	SL			3	1	Shifts bits in A-Register 1 left and stores result in A-Register
1D	SL	target		9	3	Shifts bits in A-Register 1 left and stores result at {target} memory address
1E	SR			3	1	Shifts bits in A-Register 1 right and stores result in A-Register
1F	SR	target		9	3	Shifts bits in A-Register 1 right and stores result at {target} memory address
20	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
21	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
22	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
23	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
24	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
25	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
26	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
27	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
28	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
29	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
2A	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
2B	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
2C	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
2D	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
2E	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
2F	resevered					Resevered for future revision of Instruction set do not use on GPCv1 chip
30	JMP	target		7	3	Jumps to {target} memory address
31	JZE	target		3-7	3	Jumps to {target} memory address if zero flag is set
32	JCA	target		3-7	3	Jumps to {target} memory address if carry flag is set
33	JEQ	target		3-7	3	Jumps to {target} memory address if EQ flag is set
34	JNE	target		3-7	3	Jumps to {target} memory address if EQ flag is not set
35	JSR	target		11	3	Jumps to {target} memory address and puts current memory address on stack to return to
36	RSR			9	1	Returns from subroutine to memory address on stack