Universidade de Aveiro

Mestrado em Engenharia de Computadores e Telemática

Arquitecturas de Alto Desempenho

Introduction to VHDL Simulation

Academic year 2023/2024

1. The `flipFlopD.vhd` file (available at the course elearning site) contains the VHDL description of an asynchronous digital circuit which represents a 1 bit storage device and is to be simulated using the Quartus Prime Lite Edition software package.
   1.1. Open the file with a text editor, read it carefully, draw a schematics that depicts its internal organization and explain what it does.
   1.2. Create a Quartus project and simulate its operation.

2. The `lRot_8bit.vhd` file (available at the course elearning site) contains the VHDL description of a combinatorial digital circuit which is to be simulated using the Quartus Prime Lite Edition software package.
   2.1. Open the file with a text editor, read it carefully, draw a schematics that depicts its internal organization and explain what it does.
   2.2. Create a Quartus project and simulate its operation.
   2.3. The circuit as it is described has a privileged direction of operation. Modify the design so that it can operate equally well in both directions. Start by specifying its interface, draw a schematics of its internal organization and only then write the VHDL code that describes it. Create a new Quartus project and simulate its operation.