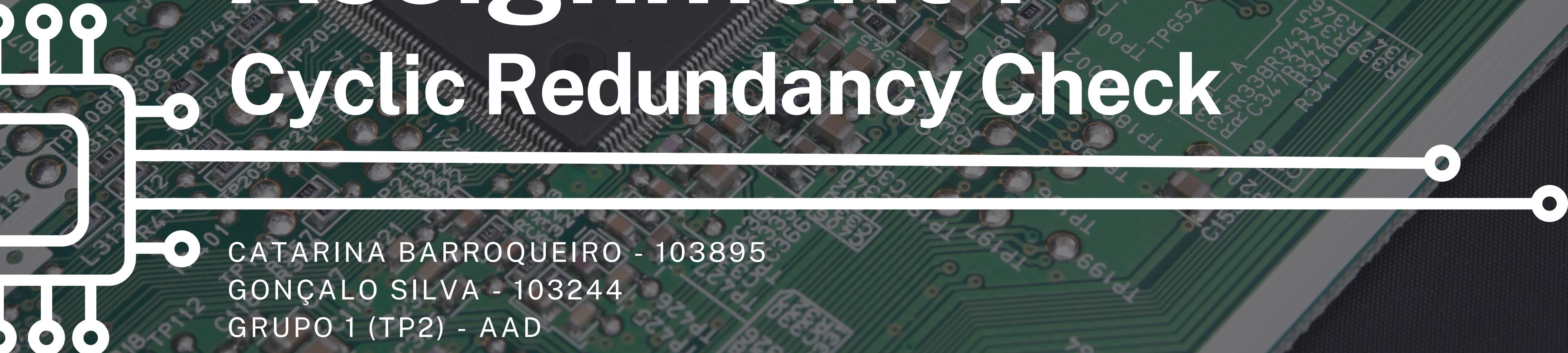


Assignment 1

Cyclic Redundancy Check



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GRUPO 1 (TP2) - AAD

ENCODER PARALLEL IMPLEMENTATION

APPROACH

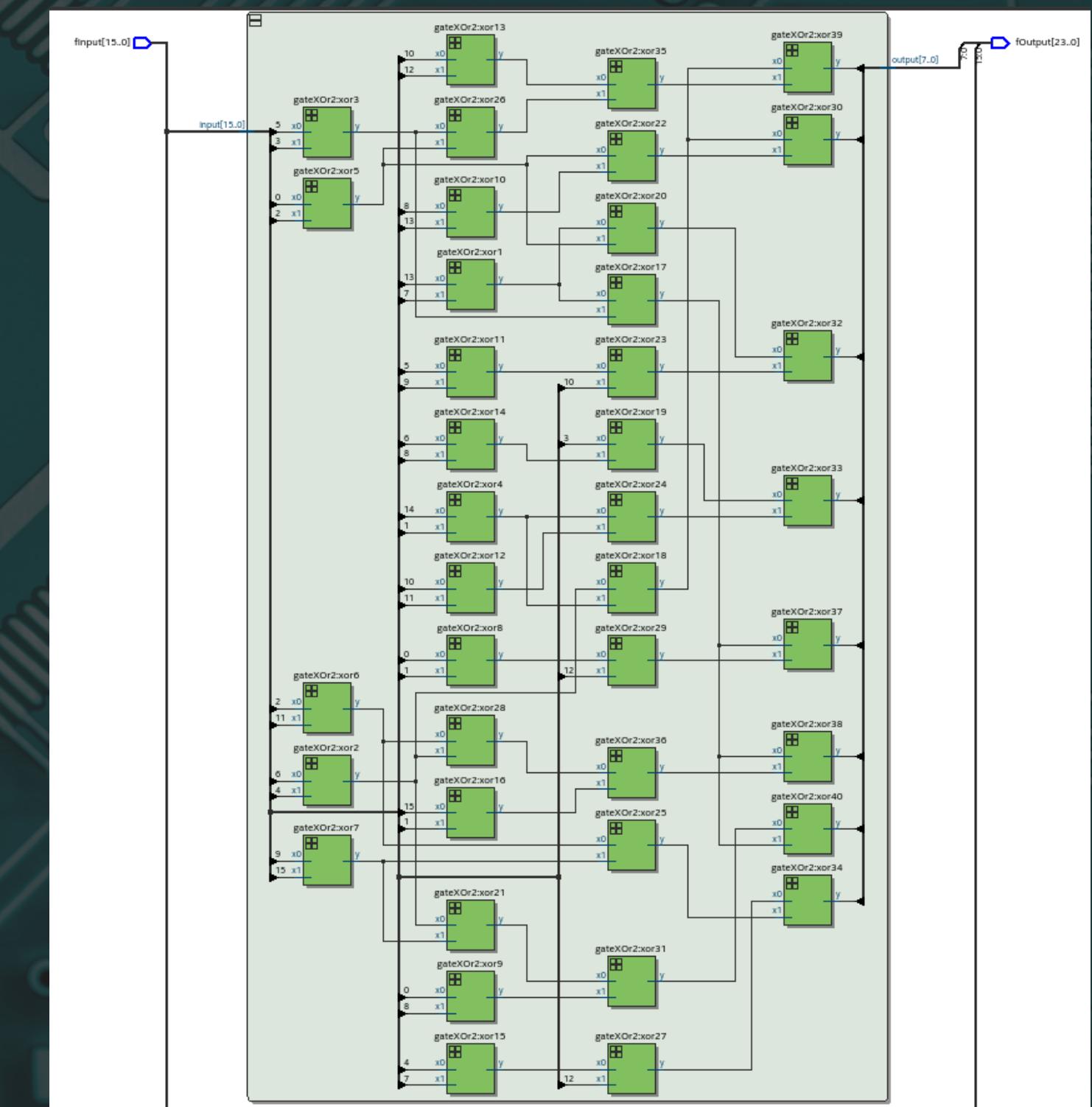
- Implemented using the Properties of the remainder
- The original equations were reduced using a script as well as an excel sheet

BENCHMARK

- 4 Levels
 - 40 X-Ors
 - 4 x-or propagation time delays

	Level 1							
	R7	R6	R5	R4	R3	R2	R1	R0
a0	X			X			X	
a1	X	X	X		X			X
a2		X	X	X		X		X
a3	X	X	X		X		X	
a4		X	X	X			X	X
a5	X	X	X			X	X	
a6		X	X	X		X		X
a7	X	X		X		X	X	
a8					X		X	X
a9				X		X	X	
a10					X	X		
a11		X		X	X			
a12	X		X	X				
a13	X	X		X		X	X	X
a14			X	X			X	X
a15	X		X	X				

Gates	Operands	
XOR1	a13,a7	X
XOR2	a6,a4	X
XOR3	a5,a3	X
XOR4	a2,a1	X
XOR5	a15,a11	X
XOR6	a0,a12	X
XOR7	a10,a14	X
XOR8	a0,a9	X
XOR9	a13,a14	X
XOR10	a0,a8	X
XOR11	a15,a8	X
XOR12	a9,a12	X
XOR13	a8,a11	X
XOR14	a5,a10	X
XOR15	a6,a3	X
XOR16	a4,a7	X





ENCODER RESULTS

Example

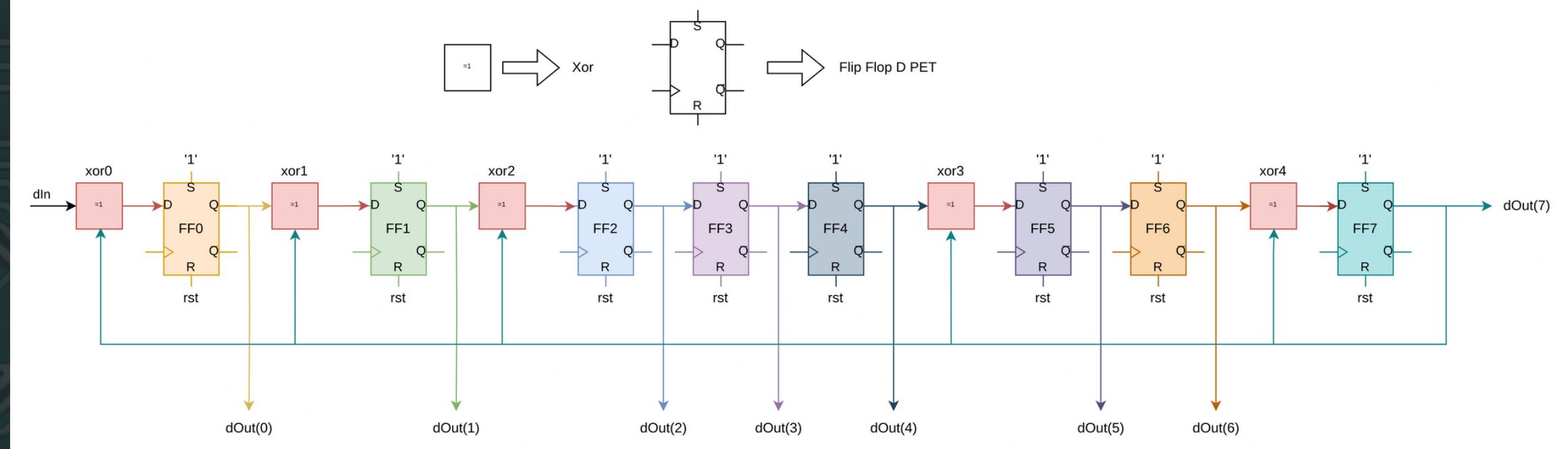
- **Message** = 1010101010101010
- **Output** = 1010101010101011101000 -> CRC

Name	Value at 0 ps	0 ps	80.0 ns	160.0 ns	240.0 ns	320.0 ns	400.0 ns	480.0 ns	560.0 ns	640.0 ns	720.0 ns	800.0 ns	880.0 ns	960.0 ns
finput	B 1010101010101010							1010101010101010						
fOutput	B 1010101010101011101000							1010101010101011101000						

CHECKER BIT-SERIAL IMPLEMENTATION

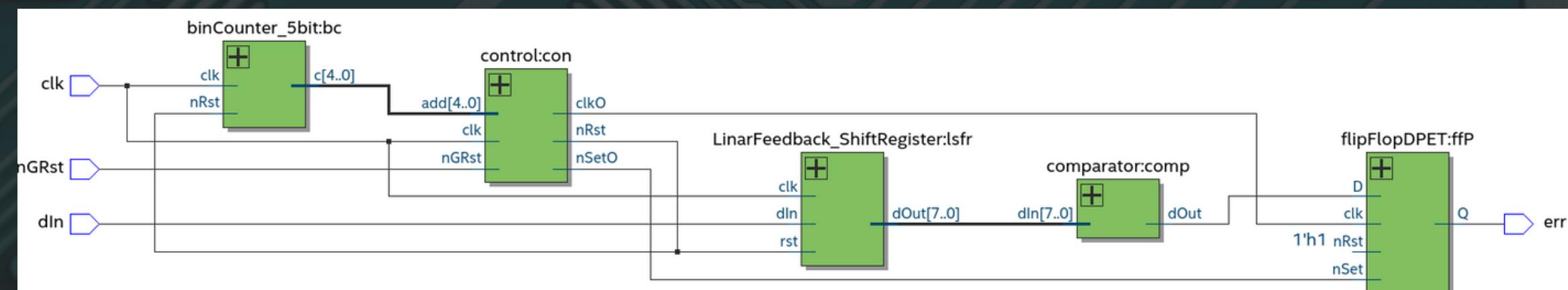
APPROACH

- Implemented using the division algorithm
- 1 - Linear Feedback Shift Register
 - 5 - Xor's
 - 8 - Flip-Flop D PET
- 1 - Comparator to 0
 - 8 - OR's



BENCHMARK

- 25 clock cycles
 - 24 for number insertion
 - 1 for the error bit to be inserted into the Flip Flop D PET



CHECKER RESULTS

Example with 3 values

- Example with 3 values:
 - **Message1** = 101010101010101011101000 -> No error
 - **Message2** = 101010101010101011101000 -> No error
 - **Message3** = 101010101010101011101000 -> **Error**

