University of Washington

BEE331 Lab 2.1

2301991 *Jason Truong*

2130474 *Henry Haight*

supervised by
Prof. Joseph Decuir

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Characterising MOSFET; I-V Curve

Design Objective

In this lab, we introduce ourselves to the MOSFET, we characterise its function V_{DS} and I_D curve; related to Triode, Threshold, and Saturation.

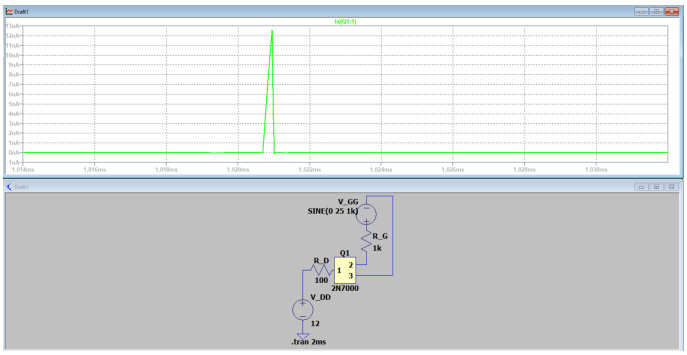
Circuit Design Outline

With an NMOS (2N7000) Transistor in series from Voltage Input $V_{DD} = 12V$ to a resistor ($R_D = 100\Omega$), the voltage drop in $V_{DS} = V_D - V_S$, to ground. In the Gate V_G over the capacitor of the MOSFET; in series with a resistor ($R_G = 1k\Omega$), being supplied with it's own voltage source; V_{GG}.

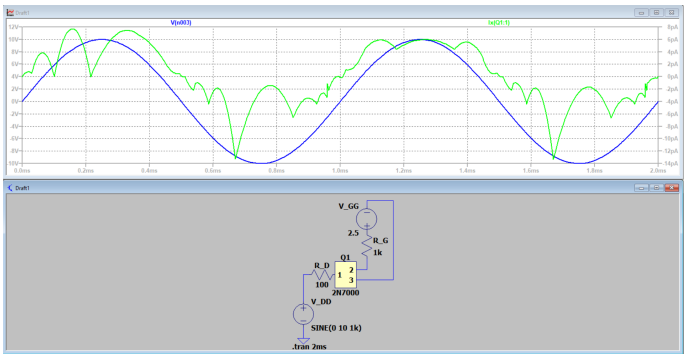
The demonstrated circuits below use a sinusoidal sweep with V_{DD} and V_{GG} respectively to demonstrate the I_D relation over a voltage-change.

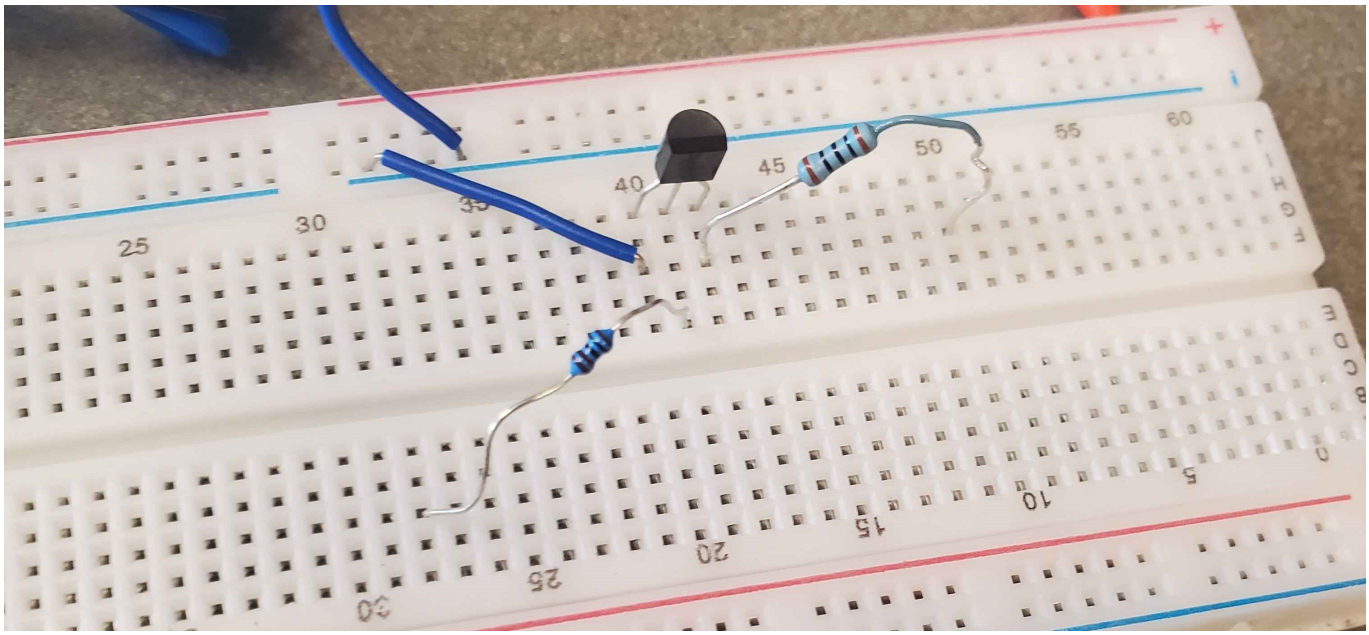
Figure 1: 2N7000 NMOS

(a) LTSpice + Rudimentary Schematic I_D vs V_{GS} Sweep



(b) LTSpice + Rudimentary Schematic I_D vs V_{DS} Sweep





(c) 2N7000 NMOS Transistor MOSFET Circuit

Descriptions of Measurements & Calculations

Analysis

- **i. Use your plot (or data) to find the value of V_{GS} which just starts to produce a non-zero drain current. This is the threshold voltage V_t of the MOSFET under test.**

  See below for tables and graphs of [I_D vs V_{GS}], and [I_D vs V_{GS}].

- **ii. How close are the measured and calculated values of V_{DS} at the boundary of triode and saturation regions of the MOSFET?**

  V_{GS} *vs* I_D: From when the current has a measurable rating ($1.8V$), saturates at a $0.6V$ difference ($2.4V$).

  V_{DS} *vs* I_D: From when the current plateaus at its greatest amount ($1V$ to $1.5V$), saturates at a $.5V$ difference (@$1.5V$). Then proceeds to break the component's specifications by breaching current at around $5V$

- **What model parameters of the MOSFET would you adjust (and how) to match the experimental results?**

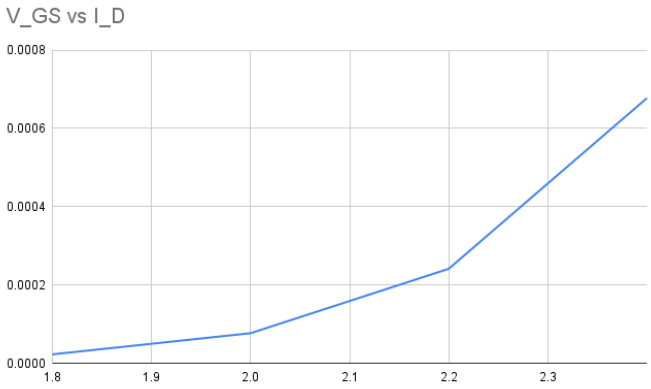
  To simulate the I_D change over a voltage change for [Saturation] and [To $10V$] respectively, we AC-swept over a region. Aside from the simulation-method, here is the Github link to the .lib model we used to simulate the 2N7000 component.

- **Do the values of k_n obtained from measurements agree with k_n obtained from the model?**

  Simply, yes; given $k_n = (\frac{I_D * 2}{V_{RD} - 1.6})^2$

Figure 1: NMOS Circuits

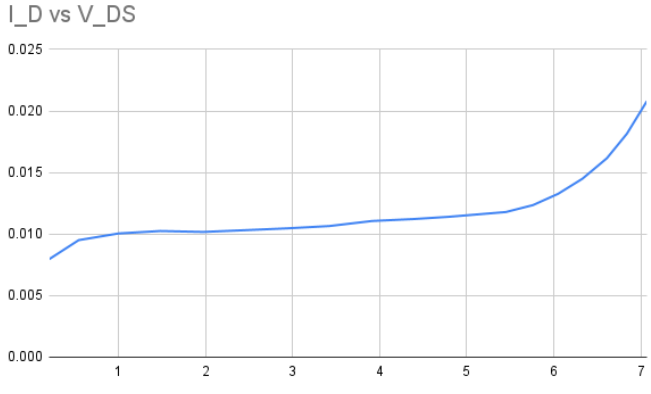
(a) V_{GS} vs I_D Graph



(b) Lab 2 2-2A-I Table

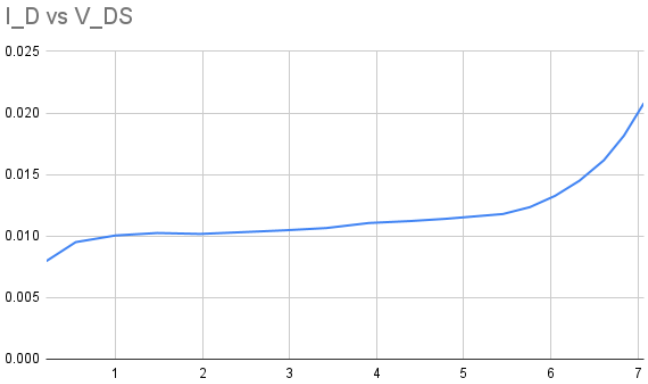
VGS	V(RD)	ID	kn
0.2	0		
0.4	0		
0.6	0		
0.8	0		
1	0		
1.2	0		
1.4	0		
1.6	0.0002	0.000002	#DIV/0!
1.8	0.00228	0.0000228	0.00114
2	0.00768	0.0000768	0.00096
2.2	0.024139	0.00024139	0.001341055556
2.4	0.06775	0.0006775	0.0021171875

(c) I_D vs V_DS



(d) Lab 2 2-2A-I Table

VDD	V(RD)	ID	VDS
1	0.7955	0.007955	0.2
1.5	0.9507	0.009507	0.54
2	1.005	0.01005	1
2.5	1.0248	0.010248	1.48
3	1.0172	0.010172	1.97
3.5	1.0314	0.010314	2.45
4	1.0465	0.010465	2.94
4.5	1.065	0.01065	3.42
5	1.106	0.01106	3.91
5.5	1.122	0.01122	4.39
6	1.14	0.0114	4.79
6.5	1.16	0.0116	5.13
7	1.179	0.01179	5.45
7.5	1.235	0.01235	5.76
8	1.327	0.01327	6.05
8.5	1.45	0.0145	6.33
9	1.616	0.01616	6.61
9.5	1.815	0.01815	6.84
10	2.08	0.0208	7.07



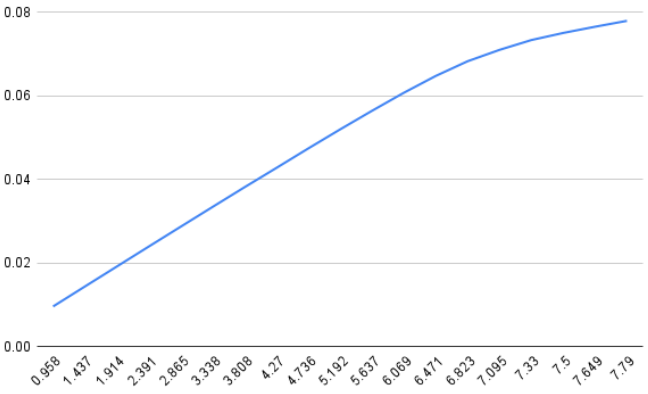
(e) I_D vs V_DS @$V_{GS} = 2.5V$

VDD	V(RD)	ID	VDS
1	0.7955	0.007955	0.2
1.5	0.9507	0.009507	0.54
2	1.005	0.01005	1
2.5	1.0248	0.010248	1.48
3	1.0172	0.010172	1.97
3.5	1.0314	0.010314	2.45
4	1.0465	0.010465	2.94
4.5	1.065	0.01065	3.42
5	1.106	0.01106	3.91
5.5	1.122	0.01122	4.39
6	1.14	0.0114	4.79
6.5	1.16	0.0116	5.13
7	1.179	0.01179	5.45
7.5	1.235	0.01235	5.76
8	1.327	0.01327	6.05
8.5	1.45	0.0145	6.33
9	1.616	0.01616	6.61
9.5	1.815	0.01815	6.84
10	2.08	0.0208	7.07

(f) Lab 2 2-2A-I Table @$V_{GS} = 2.5V$

VDD	V(RD)	ID	VDS
1	0.958	0.00958	0.03
1.5	1.437	0.01437	0.06
2	1.914	0.01914	0.08
2.5	2.391	0.02391	0.1
3	2.865	0.02865	0.13
3.5	3.338	0.03338	0.16
4	3.808	0.03808	0.19
4.5	4.27	0.0427	0.23
5	4.736	0.04736	0.27
5.5	5.192	0.05192	0.32
6	5.637	0.05637	0.38
6.5	6.069	0.06069	0.46
7	6.471	0.06471	0.59
7.5	6.823	0.06823	0.81
8	7.095	0.07095	1.12
8.5	7.33	0.0733	1.47
9	7.5	0.075	1.84
9.5	7.649	0.07649	2.22
10	7.79	0.0779	2.6

(g) I_D vs V_DS @$V_{GS} = 3V$



(h) Lab 2 2-2A-I Table @$V_{GS} = 3V$

MOSFET Bias Circuit

Design Objective

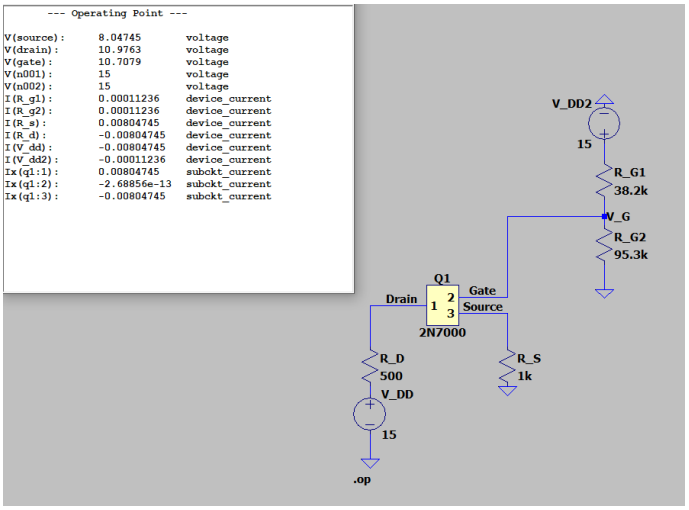
In this lab we bias a MOSFET for use in both saturation and triode regions. This allows us to maintain a stable DC operating point.

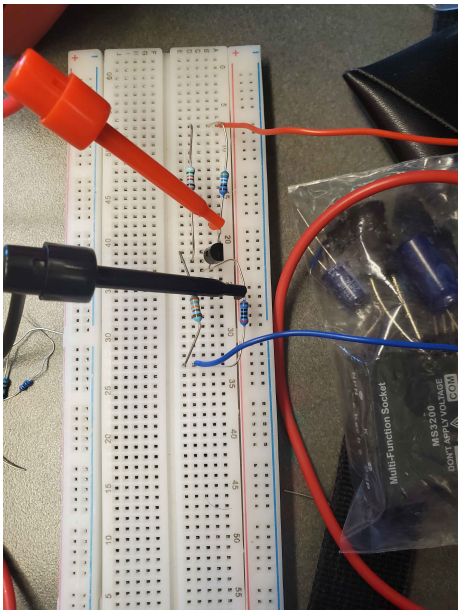
Circuit Design Outline

Using our calculated resistors of 38.2$k\Omega$ and 95.3$k\Omega$ combined with our given resistance values of 500Ω and 200Ω and connecting them to our NMOS transistor in the configureation shown below we can bias our circuit so that the current across the 500Ω and 200Ω (I_D) is 10mA. By inputting a voltage of 15V at the leg of the 500Ω resistor we can achive 10mA across the resistors.

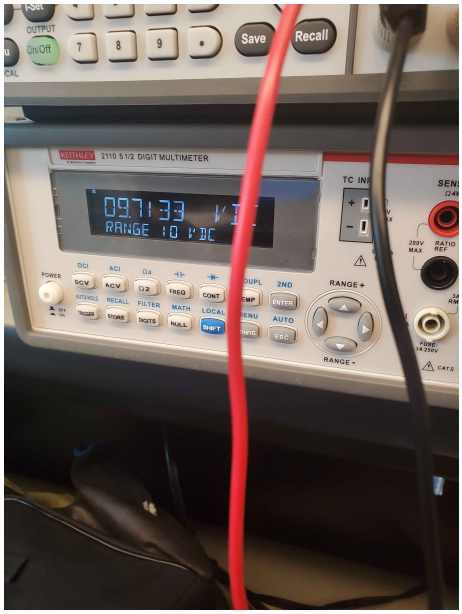
Figure -1: Bias Circuit

(a) Bias Circuit Sim





(b) Bias Circuit Image



(c) Bias Circuit Measurement

Measurement and Simulation Results

Analysis

- **1. Calculate expected V_G, I_D and V_{DS}**

  Using $V_{GS} = V_G$ - V_S and a voltage divider accross the $38.2k\Omega$ and $95.3k\Omega$ resistors we find that $V_G = 10.708$V.

  Using the equation $I_D = k_n(V_{GS} - V_T)^2$ we can solve for I_D obtaining $I_D = 10.84mA$ using $k_n = 0.0011$ and $V_T = 1.6$

  V_{DS} is therefore found using $V_{DS} = V_D$ - V_S where V_D is found using I_D, V_{DD}, and the 500Ω resistor. This gives us $V_{DS} = 7.411V$

- **2. Compare to simulated results for V_G, I_D and V_{DS}**

  The simulated results for V_G, I_D and V_{DS} all line up with what we observed during our measurements. The % difference between the calculated and simulated values are found at a 2% difference (10.84mA vs 11.04mA).

- **3. Comment on discrepancies**

  Discrepancies appear from the natural impedance of the NMOS transistor; and the transience of the Gate-Voltage causing a natural and slow rise. As Semiconducting Materials in real life are difficult to keep at a consistent voltage due to them being VERY sensitive and dependent on temperature.

Summary & Conclusions

In this lab, we analysed; characterised; and designed with an NMOSFET transistor for the I_D over both the V_{GS} and V_{DS} region, but also the biasing effects of voltage-dividing over V_G

Addendum Pages

Figure -1: Jason Truong Addendum

(a) Lab Design Calculations

$$I_D = I_S(e^{qV_D / NkT} - 1)$$

Where,

I_D = Diode current in amps

I_S = Saturation current in amps
(typically 1×10^{-12} amps)

e = Euler's constant (~ 2.718281828)

q = charge of election (1.6×10^{-19} coulombs)

V_D = Voltage applied across diode in volts

N = "Nonideality" or "Emission" coefficient
(typically between 1 and 2)

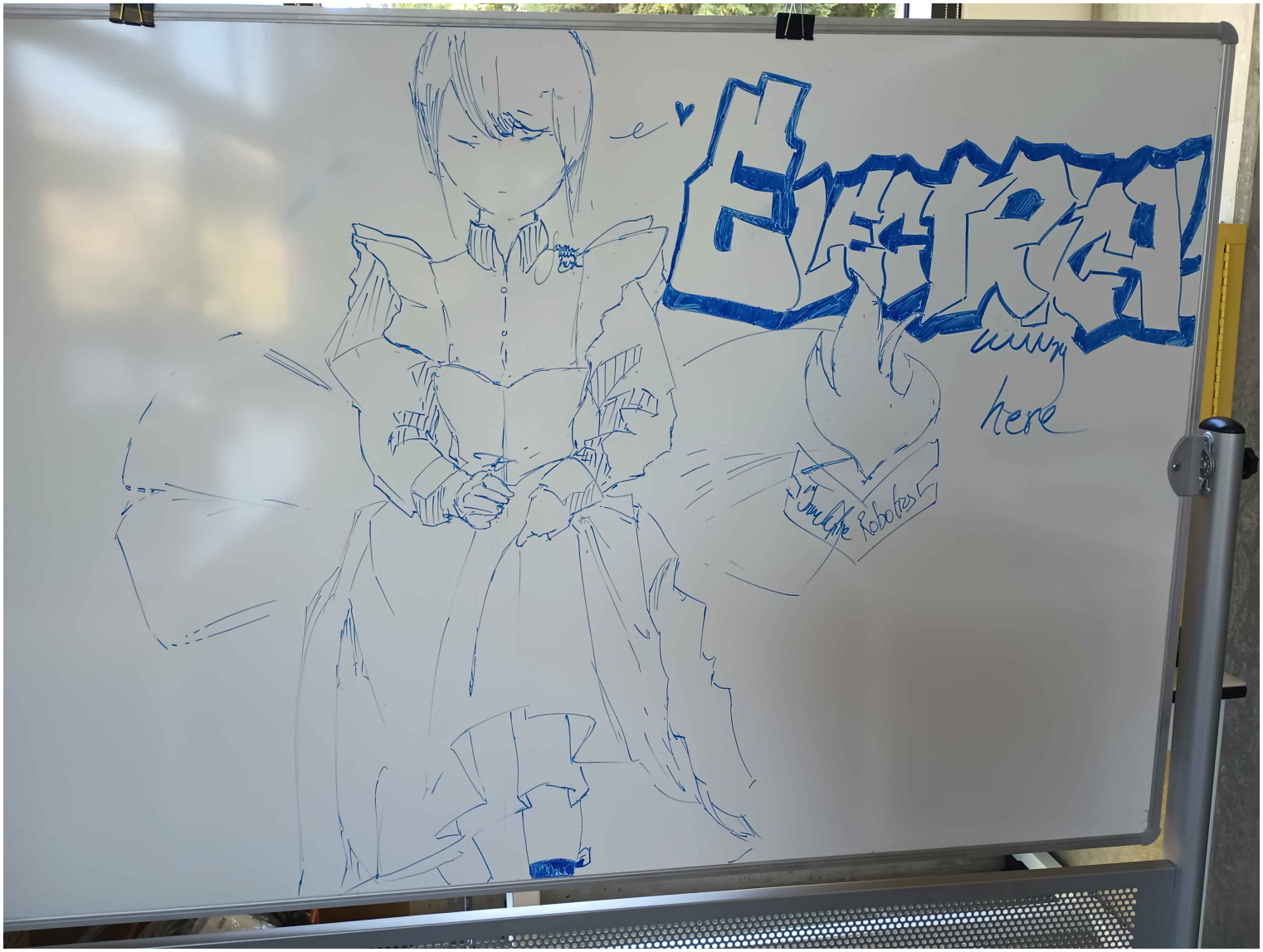
k = Boltzmann's constant (1.38×10^{-23})

T = Junction Temperature in Kelvins

Bibliography

Cited:

- Lab 1 Manual
- Sedra, Adel, and Kenneth Smith. Microelectronic Circuits. S.L., Oxford Univ Press Us, 2019.



(a) Keep believing in yourself.