University of Washington

BEE331 Lab 2

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MOSFET Bias Circuit

Design Objective

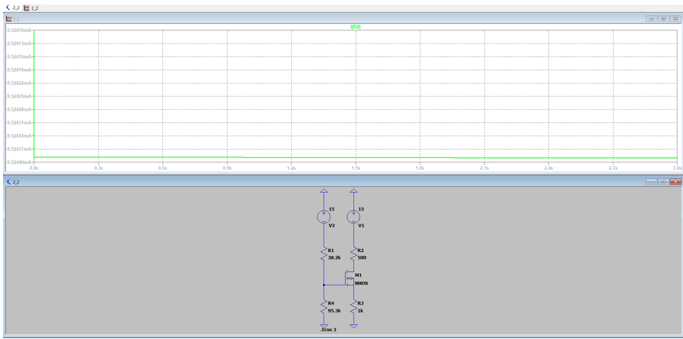
In this lab we bias a MOSFET for use in both saturation and triode regions. This allows us to maintain a stable DC operating point.

Circuit Design Outline

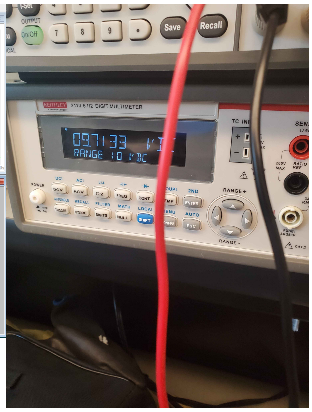
Using our calculated resistors of $38.2k\Omega$ and $95.3k\Omega$ combined with our given resistance values of 500Ω and 200Ω and connecting them to our NMOS transistor in the configureation shown below we can bias our circuit so that the current across the 500Ω and 200Ω (I_D) is 10mA. By inputting a voltage of 15V at the leg of the 500Ω resistor we can achive 10mA across the resistors.

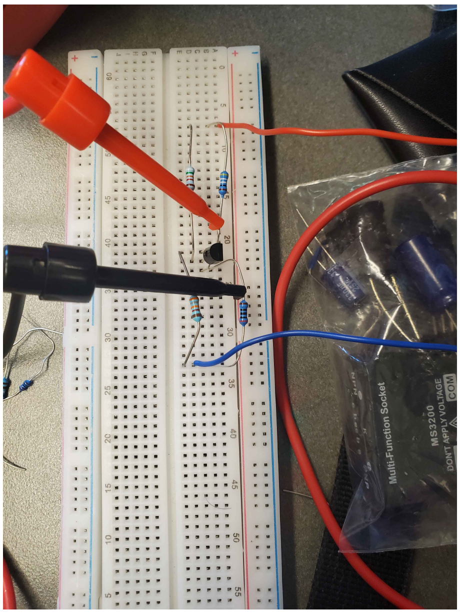
Figure 1: Bias Circuit

(a) Bias Circuit Sim



(b) Bias Circuit Measurement





(c) Bias Circuit Image

Measurement and Simulation Results

Analysis

- **1. Calculate expected V_G, I_D and V_{DS}**

  Using $V_{GS} = V_G$ - V_S and a voltage divider accross the $38.2k\Omega$ and $95.3k\Omega$ resistors we find that $V_G = 10.708$V.

  Using the equation $I_D = k_n(V_{GS} - V_T)^2$ we can solve for I_D obtaining $I_D = 10.39mA$

  V_{DS} is therefore found using $V_{DS} = V_D$ - V_S where V_D is found using I_D, V_{DD}, and the 500Ω resistor. This gives us $V_{DS} =$

- **2. Compare to simulated results for V_G, I_D and V_{DS}**

  The simulated results for V_G, I_D and V_{DS} all line up with what we observed during our measurements. The % difference between the calculated and simulated values were about

- **3. Comment on descrepancies**

Summary & Conclusions