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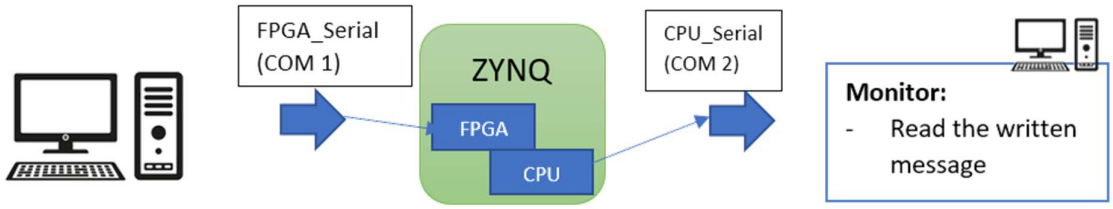
Embedded Systems 2025

SDU

Assignment 1: From FPGA (PL) to CPU (PS)

Aim: learning how to communicate between the FPGA and the CPU via BRAM while testing different UART connections.

- **Design** a digital circuit that stores a message from a PL UART entry and reads it through PS UART.



- **Document** the outcome of these exercises:
  - explain the used components.
  - how does the circuit work?
  - how is the design validated through simulation?
- **Make** a video of the final implementation showing the testing process. Include the video link (e.g., YouTube) in the report.

*Use parts of the code and screenshots from the simulator to answer these questions.

Submission place: Itslearning/Resources.

The is no page limit but use them wisely. The hand-in should be in pdf format on itslearning before 23:59 05/10/2025.