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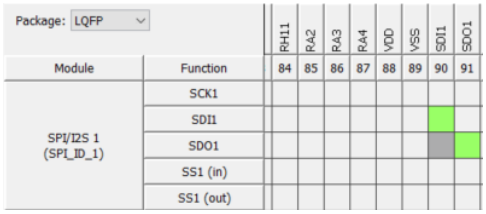
PIC32MZ EF STK to WINC1500

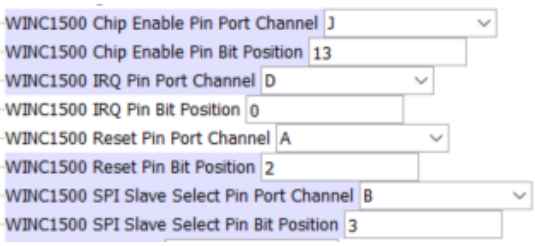
The purpose of this document is to provide brief instruction on how to connect a WINC1500 Xplained Pro development board to a PIC32MZ EF STK to demonstrate WINC1500 support within Harmony.

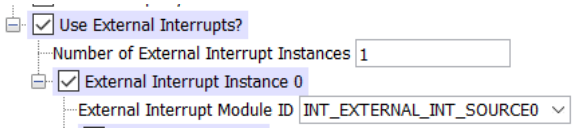
> Important: Before starting, connect WINC1500 Xplained Pro dev board to a supported SAMD21 Xplained Pro board (or any supported dev board). Using Atmel Studio, open or create an ASF WINC1500 Firmware Updater project and follow instructions in the user guide located in the /docs folder. WINC1500 module must be running FW v19.5.2 or greater for SoftAP function. DFU from within Harmony application will be supported in the future. Contact WSG apps to obtain WINC1500 update image.

Wire wrap connections to connect PIC32MZ EF STK to WINC1500 Xplained Pro dev board as indicated in wiring chart in the wiring section of this document. Recommend using a male-male header on the WINC1500, if possible, to make it easy to remove WINC1500 for other use.

Open Harmony “wifi_easy_conguration” project from Harmony v2.02b or later. Select project configuration ”pic32mz_ef_sk__ioexp__winc__freertos”. Start MHC and make the following changes.

- In MHC Pin Manager, modify SPI MOSI and MISO port pins to reflect connections in wiring chart.
  - 

- In MHC Options tab navigate to “Harmony Framework Configuration/Drivers/Wi-Fi” and modify according to the wiring chart.
  - 

- In MHC Options tab, navigate to “Harmony Framework Configuration /System Services/Interrupts” and change external source to INT_EXTERNAL_INT SOURCE0.
  - 

- WAKE pin is not controlled by the WINC1500 driver. In MHC Pin Settings, set this pin to a High Output.
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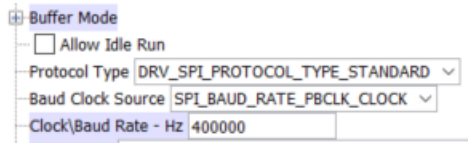
- In MHC Options tab “Harmony Framework Configuration/Drivers/SPI/SPI Driver Instance 0”, slow down SPI port since we are using wire wrap and not PCB trace connections. The speed will depend on the length and gauge of your wiring. I was able to run a 4MHz clock w/o issues.
  - 

- Save MHC settings and Generate code.
  - No manual source code modification is necessary.
- Build and program device in release or debug mode.
- Connect computer to PIC32MZ EF STK via USB device connection to verify operation. Open serial terminal session; hit any key to view console messages. Successful initialization should output the following:
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TCP/IP Stack: Initialization Started
No stored Wi-Fi configuration found in NVM
Using default Wi-Fi configuration
SYS_Initialize: The MPFS2 File System is mounted

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*** Wi-Fi TCP/IP EZConfig Demo ***
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Chip ID 1503a0
DriverVerInfo: 0x13521352

WINC1500 Firmware Data:
Firmware Ver : 19.5.2 SVN Rev 14274
Firmware Built at Jan 26 2017 Time 22:13:34
Firmware Min Driver Ver : 19.3.0
Driver Ver: 19.5.2 SVN Rev 13445
Driver SVN URL trunk
Driver Built at Mar  2 2017 Time 21:44:09

Module MAC: F8:F0:05:F2:FD:41
TCP/IP Stack: Initialization Ended - success
Scan is completed successfully
WINC1500: De-initializing . . .
WINC1500: NVM operation succeeded
Chip ID 1503a0
DriverVerInfo: 0x13521352

WINC1500 Firmware Data:
Firmware Ver : 19.5.2 SVN Rev 14274
Firmware Built at Jan 26 2017 Time 22:13:34
Firmware Min Driver Ver : 19.3.0
Driver Ver: 19.5.2 SVN Rev 13445
Driver SVN URL trunk
Driver Built at Mar  2 2017 Time 21:44:09

Module MAC: F8:F0:05:F2:FD:41
POWER SAVE Disabled

Start Wi-Fi Connection . . .
Soft AP is enabled, SSID: MCHPSoftAP
  Interface WINC1500 on host MCHPBOARD_W     - NBNS enabled
WINC1500 IPv4 Address: 192.168.1.1
Client ec:1f:72:db:52:0f is connected
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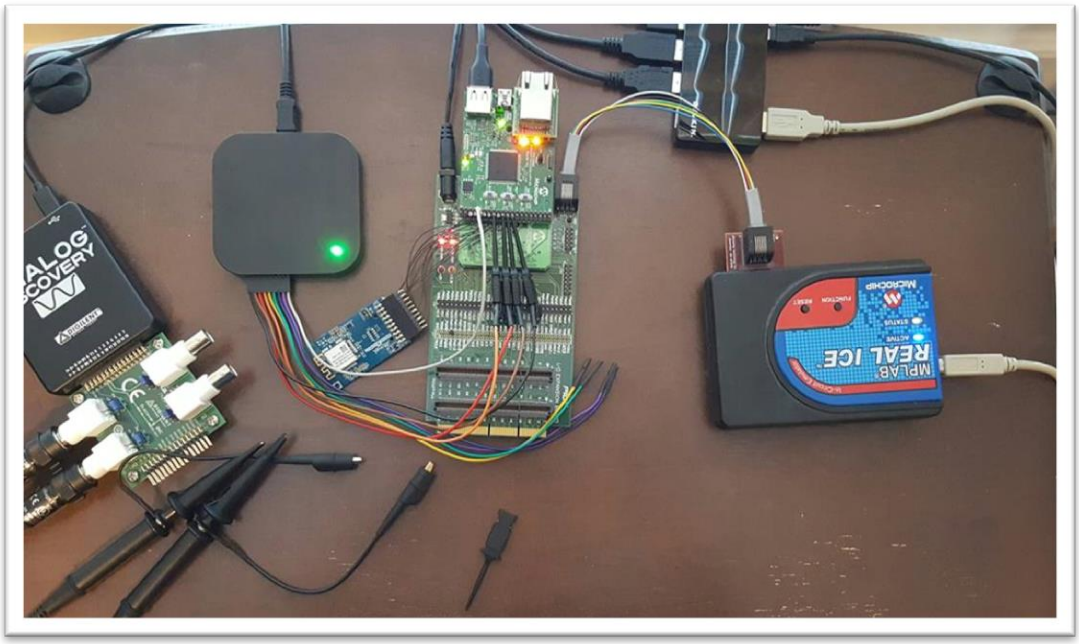
** Note: When operating HTTP server demo web page, response may be slow due to decreased SPI data rates.*

Wiring Chart for PIC32MZ EF STK to WINC1500 Xplained Pro Demo.

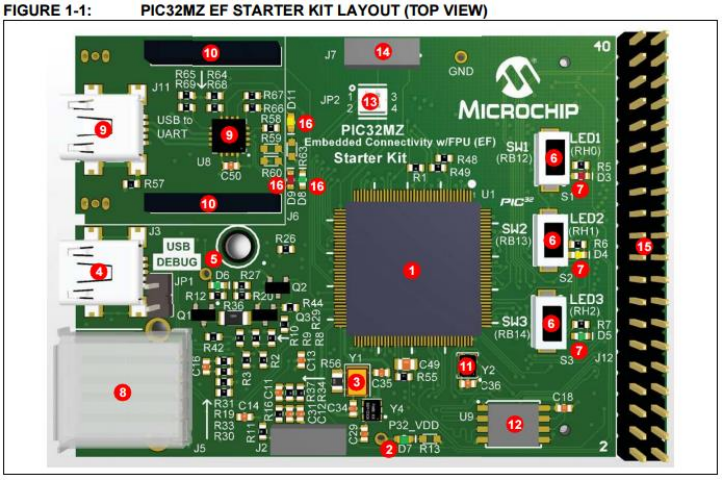
Function	WINC1500 Xpl Pro Header Pin	PIC32MZ EF STK 40 Pin Header (wire wrapped settings)	PIC32MZ EF STK default (for reference)
RESET_N	5	5 (RA2)	RF0
WAKE	6	7 (RA14)	NC
IRQ_N	9	11 (RD0, INT0)	RE8
CHIP_EN	10	13 (RJ13)	RE0
SPI_SSN	15 (SPI_SS)	15 (RB3)	RE9
SPI_MOSI	16 (SPI_MOSI)	19 (RF5, SDO1)	RD10 (SDO1)
SPI_MISO	17 (SPI_MISO)	21 (RF4, SDI1)	RD14 (SDI1)
SPI_SCK	18 (SPI_SK)	23 (RD1, SCK1)	RD1 (SCK1)
Vcc	20	17	
GND	19	9	

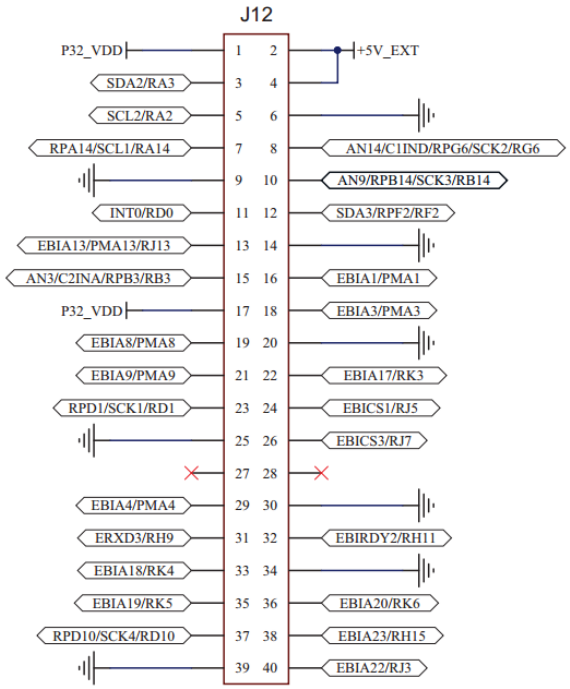


**note: it is not necessary to use the I/O expansion board and adapter.*

PIC32MZ EF Starter Kit Information:

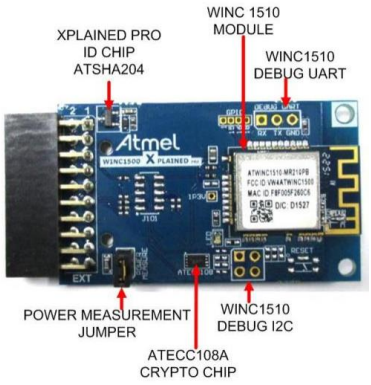
FIGURE 1-1: PIC32MZ EF STARTER KIT LAYOUT (TOP VIEW)





0.1" (2.54mm) 2X20 Male Header

WINC1500 Xplained Pro Eval Board Info:



ATWINC1510-MR210PB

The ATWINC1510-MR210PB main control pins are connected to the Xplained Pro extension header.

Table 4-4. ATWINC1510-MR210PB Connection

Pin on EXT connector	Pin on ATWINC1510 module	Function
5	4	RESET_N.
6	11	WAKE.
9	13	IRQ_N.
10	22	CHIP_EN.
15	16	SPI_SSN.
16	15	SPI_MOSI.
17	17	SPI_MISO.
18	18	SPI_SCK.

Table 4-1. ATWINC1500 Xplained Pro Extension Header

Pin on EXT	Function	Description
1	ID	Communication line to ID chip.
2	GND	Ground.
3	NC	
4	NC	
5	ATWINC1500 RESET	Active-low hard reset.
6	ATWINC1500 WAKE	Host wake control.
7	NC	
8	NC	
9	ATWINC1500 IRQ	ATWINC1500 interrupt output.
10	ATWINC1500 CHIP ENABLE	Active-high module enable signal.
11	I^2C SDA	Data line of I^2C interface (connected to ATECC108A/508A).
12	I^2C SCL	Clock line of I^2C interface (connected to ATECC108A/508A).
13	UART RX	Receive pin of target MCU UART interface (NC by default).
14	UART TX	Transmit pin of target MCU UART interface (NC by default).
15	ATWINC1500_SS	Chip select signal.
16	SPI_MOSI	Master out, Slave in signal of target MCU SPI interface.
17	SPI_MISO	Master in, Slave out signal of target MCU SPI interface.
18	SPI_SCK	Clock line of SPI interface.
19	GND	Ground.
20	VCC	Target supply voltage.

Xplained Pro Header Pinout:

TABLE 2-3: J12 CONNECTIONS

Function 1	Function 2	Pin	Pin	Function 2	Function 1
—	+3V3	1	2	+5V	—
RA3	SDA2	3	4	+5V	—
RA2	SCL2	5	6	GND	—
RA14	—	7	8	UxTX	RG6
—	GND	9	10	UxRX	RB14
RD0	—	11	12	—	RF2
RJ13	—	13	14	GND	—
RB3	—	15	16	—	RK1
—	+3V3	17	18	—	RK2
RF5	MOSI	19	20	GND	—
RF4	MISO	21	22	—	RK3
RD1	SCLK	23	24	—	RJ5
—	GND	25	26	—	RJ7
—	No Connect	27	28	No Connect	—
RH7	—	29	30	GND	—
RH9	—	31	32	—	RH11
RK4	—	33	34	GND	—
RK5	—	35	36	—	RK6
RD10	—	37	38	—	RH15
—	GND	39	40	—	RJ3