**Assignment IV: Advanced CUDA**

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Link to Github repository: <https://github.com/TheKastenkarl/DD2360HT22>

**Exercise 1 - Thread Scheduling and Execution Efficiency**

1. **Assume X=800 and Y=600. Assume that we decided to use a grid of 16X16 blocks. That is, each block is organized as a 2D 16X16 array of threads. How many warps will be generated during the execution of the kernel? How many warps will have control divergence? Please explain your answers.**

Size of block array:

* In x-direction:
* In y-direction:

Total number of warps:

Explanation of how thread blocks are divided into warps: [Link](https://stackoverflow.com/questions/6177202/how-are-2d-3d-cuda-blocks-divided-into-warps) (TLDR: Threads are numbered in order within blocks so that threadIdx.x varies the fastest, then threadIdx.y the second fastest varying, and threadIdx.z the slowest varying.)

Number of warps with control divergence:

Chart, bar chart

Description automatically generated

* In last row: No control divergences because a single warp either doubles a pixel value in all threads or in no thread. 🡪 0 warps
* In last column: No control divergences because the size of all threads in x-direction is equivalent to the size of the image. 🡪 0 warps
* Total number of warps with control divergence: 0

1. **Now assume X=600 and Y=800 instead, how many warps will have control divergence? Please explain your answers.**

Size of block array:

* In x-direction:
* In y-direction:

Number of warps with control divergence:

Chart, bar chart

Description automatically generated

* In last row: No control divergences because the size of all threads in y-direction is equivalent to the size of the image. 🡪 0 warps
* In last column: Control divergence in all warps because a single warp always includes threads where pixel values have to be doubled and threads where this is not done. 🡪 8 \* 50 warps
* Total number of warps with control divergence: 400 warps

1. **Now assume X=600 and Y=799, how many warps will have control divergence? Please explain your answers.**

Size of block array:

* In x-direction:
* In y-direction:

Number of warps with control divergence:

Chart

Description automatically generated

* In x-direction: Control divergence for every warp in the last row. 🡪 8 \* 50 warps
* In last row: Control divergence in one warp per block because the warp which covers the last two rows of the thread block performs both pixel value doubling (second last row) and no pixel value doubling (last row). 🡪 1 \* 38 warps
* We counted ne warp in the thread block in the bottom right corner twice, so we have to subtract one warp.
* Total number of warps with control divergence: 437

**Exercise 2 - CUDA Streams**

1. **Compared to the non-streamed vector addition, what performance gain do you get? Present in a plot (you may include comparison at different vector length).**

I use nvprof for measuring the times as it is simpler and more accurate (<https://stackover-flow.com/questions/30371030/understanding-cuda-profiler-output-nvprof>).

Used segment size: S\_seg = inputLength / NUMSTREAMS

Command: nvprof ./lab4\_ex2 <vector-length>

*Chart, bar chart

Description automatically generatedNon-streamed vector addition:*

*Streamed vector addition:*

Chart, bar chart

Description automatically generated

As you can see, the streamed vector addition is much faster than the non-streamed vector addition, especially for large vector sizes.

1. **Use nvprof to collect traces and the NVIDIA Visual Profiler (nvvp) to visualize the overlap of communication and computation. To use nvvp, you can check** [**Tutorial: NVVP - Visualize nvprof Traces**](https://canvas.kth.se/courses/36161/pages/tutorial-nvvp-visualize-nvprof-traces)**.**

Used segment size: S\_seg = inputLength / NUMSTREAMS

Used vector length: 8388608

Command: nvprof --output-profile hw4\_ex2\_profile\_8388608.nvprof -f ./lab4\_ex2 8388608

Graphical user interface, table

Description automatically generated with medium confidence

By zooming in, you can see that communication and computation overlap:

Chart

Description automatically generated

For comparison, here the times when we only use a single stream:

Graphical user interface

Description automatically generated

1. **What is the impact of segment size on performance? Present in a plot (you may choose a large vector and compare 4-8 different segment sizes).**

Used vector length: 8388608

Command: nvprof --output-profile hw4\_ex2\_profile\_8388608.nvprof -f ./lab4\_ex2 8388608

A picture containing bar chart

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You can see clearly that the segment size should not be chosen to small. This is because with small segment sizes you get a lot of overhead as a result of the large number of CUDA API calls (like cudaMemcpyAsync).

**Exercise 3 - Pinned Memory and Unified Memory**

1. **What are the differences between pageable memory and pinned memory, what are the tradeoffs?**

Pinned memory are virtual memory pages that are specially marked so that they cannot be paged out. Pageable memory can be paged out. If a source or destination of a cudaMemcpy() in the host memory is not allocated in pinned memory, it needs to be first copied to a pinned memory (🡪 extra overhead). However, pinned memory is a limited resource and it is much more

expensive to allocate and deallocate. [Source: Lecture slides]

1. **Compare the profiling results between your original code and the new version using pinned memory. Do you see any difference in terms of the breakdown of execution time after changing to pinned memory?**
2. **What is a managed memory? What are the implications of using managed memory?**

Managed memory (or Unified Memory) is a single memory address space accessible from any

processor in a system. Hence, allocated data can be read or written from code running on either CPUs or GPUs. The CUDA system software takes care of migrating memory pages to the memory of the accessing processor. [Source: Lecture slides]

1. **Compare the profiling results between your original code and the new version using managed memory. What do you observe in the profiling results?**

**Exercise 4 - Heat Equation with using NVIDIA libraries**

1. Run the program with different dimX values. For each one, approximate the FLOPS (floating-point operation per second) achieved in computing the SMPV (sparse matrix multiplication). Report FLOPS at different input sizes in a FLOPS. What do you see compared to the peak throughput you report in Lab2?
2. Run the program with dimX=128 and vary nsteps from 100 to 10000. Plot the relative error of the approximation at different nstep. What do you observe?
3. Compare the performance with and without the prefetching in Unified Memory. How is the performance impact? [Optional: using nvprof to get metrics on UM]