MSP430F5419A Device Erratasheet

1 Revision History

✓ The check mark indicates that the issue is present in the specified revision.

The revision of the device can be identified by the revision letter on the Package Markings or by the HW_ID located inside the TLV structure of the device

Errata Number	Rev H	Rev G	Rev F	Rev E	Rev D
ADC25	✓	✓	✓	✓	✓
ADC27		✓		✓	✓
ADC42	✓	✓	✓	✓	✓
CPU26	✓	✓	✓	✓	✓
CPU27	✓	✓	✓	✓	✓
CPU28	✓	✓	✓	✓	✓
CPU29	✓	✓	✓	✓	✓
CPU30	✓	✓	✓	✓	✓
CPU31	✓	✓	✓	✓	✓
CPU32	✓	✓	✓	✓	✓
CPU33	✓	✓	✓	✓	✓
CPU34	✓	✓	✓	✓	✓
CPU35	✓	✓	✓	✓	✓
CPU37	✓	✓	✓	✓	✓
CPU39	✓	✓	✓	✓	✓
CPU40	✓	✓	✓	✓	✓
DMA4	✓	✓	✓	✓	✓
DMA7	✓	✓	✓	✓	✓
DMA8	✓	✓	✓	✓	✓
DMA10	✓	✓	✓	✓	✓
EEM8					✓
EEM9	✓	✓	✓	✓	✓
EEM11	✓	✓	✓	✓	✓
EEM13	✓	✓	✓	✓	✓
EEM14	✓	✓	✓	✓	✓
EEM16	✓	✓	✓	✓	✓
EEM17	✓	✓	✓	✓	✓
EEM19	✓	✓	✓	✓	✓
EEM21	✓	✓	✓	✓	✓
EEM23	✓	✓	✓	✓	✓
FLASH33	✓	✓	✓	✓	✓
FLASH34	✓	✓	✓	✓	✓
FLASH35					✓
FLASH37		✓		✓	✓

Errata Number	Rev H	Rev G	Rev F	Rev E	Rev D
JTAG20	✓	✓	✓	✓	✓
MPY1	✓	✓	✓	✓	✓
PMM9	✓	✓	✓	✓	✓
PMM10		✓		✓	✓
PMM11	✓	✓	✓	✓	✓
PMM12	✓	✓	✓	✓	✓
PMM14	✓	✓	✓	✓	✓
PMM15	✓	✓	✓	✓	✓
PMM17		✓		✓	✓
PMM18	✓	✓	✓	✓	✓
PMM20	✓	✓	✓	✓	✓
PORT16	✓	✓	✓	✓	✓
PORT19	✓	✓	✓	✓	✓
RTC3	✓	✓	✓	✓	✓
RTC6	✓	✓	✓	✓	✓
SYS10		✓		✓	✓
SYS12		✓		✓	✓
SYS16	✓	✓	✓	✓	✓
TA20	✓	✓	✓	✓	✓
TAB23		✓		✓	✓
UCS6		✓		✓	✓
UCS7	✓	✓	✓	✓	✓
UCS9		✓		✓	✓
UCS10		✓		✓	✓
UCS11	✓	✓	✓	✓	✓
USCI26	✓	✓	✓	✓	✓
USCI30		✓		✓	✓
USCI31	✓	✓	✓	✓	✓
USCI35	✓	✓	✓	✓	✓
USCI39	✓	✓	✓	✓	✓
USCI40	✓	✓	✓	✓	✓
WDG4	✓	✓	✓	✓	✓

2 Package Markings

PZ100 *LQFP (PZ) 100 Pin*

YM = Year and Month Date Code
LLLL = Assembly Lot Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

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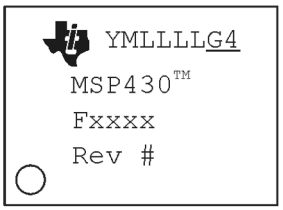

YM = Year and Month Date Code
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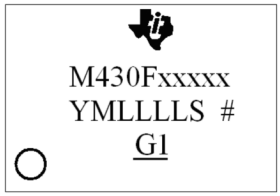
Note: Package marking with "TM" applies only to devices released after 2011.

ZQW113 *BGA (ZQW), 113 Pin*



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3 TLV Hardware Revision

Die Revision	TLV Hardware Revision
Rev H	17h
Rev G	16h
Rev F	15h
Rev E	14h
Rev D	N/A

Further guidance on how to locate the TLV structure and read out the HW_ID can be found in the device User's Guide.

4 Detailed Bug Description

ADC25 *ADC12_A Module*

Function Write to ADC12CTL0 triggers ADC12 when CONSEQ = 00

Description If ADC conversions are triggered by the Timer_B module and the ADC12 is in single-channel single-conversion mode (CONSEQ = 00), ADC sampling is enabled by write access to any bit(s) in the ADC12CTL0 register. This is contrary to the expected behavior that only the ADC12 enable conversion bit (ADC12ENC) triggers a new ADC12 sample.

Workaround When operating the ADC12 in CONSEQ=00 and a Timer_B output is selected as the sample and hold source, temporarily clear the ADC12ENC bit before writing to other bits in the ADC12CTL0 register. The following capture trigger can then be re-enabled by setting ADC12ENC = 1.

ADC27 *ADC12_A Module*

Function Integral and differential non-linearity exceed specifications

Description The ADC12_A integral and differential non-linearity may exceed the limits specified in the data sheet under the following conditions:

- If the internal voltage reference generator is used

and

- If the reference voltage is not buffered off-chip

and

- If fADC12CLK > 2.7 MHz

The non-linearity can be up to tens of LSBs. This is due to the internal reference buffer providing insufficient drive for the switched capacitor array of the ADC12_A.

Workaround (1) Turn on the output of the internal voltage reference to increase the drive strength of the reference to the ADC_12 core:

- If REFMSTR bit in REFCTL0 is 0 (allowing Shared REF to be controlled by ADC_A reference control bits)

Set ADC12REFON bit in ADC12CTL0 = 1

and

Set ADC12REFOUT bit in ADC12CTL2 = 1

- If REFMSTR bit in REFCTL0 is 1

Set REFON and REFOUT bits in REFCTL0 = 1

(2) Ensure fADC12CLK < 2.7 MHz. Depending on the frequency of the source of fADC12CLK (ACLK, MCLK, SMCLK, or MODOSC), select the divider bits accordingly.

- If fADC12CLK = MODOSC

(ADC12OSC) ADC12CTL1 |= ADC12DIV_1; // Divide clock by 2

- If fADC12CLK = ACLK/SMCLK/MCLK > 2.7 MHz.

Use ADC12DIVx and/or ADC12PDIVx bits to reduce the selected clock frequency to between 0.45 MHz and 2.7 MHz.

ADC42 *ADC12_A Module*

Function ADC stops converting when successive ADC is triggered before the previous conversion ends

Description Subsequent ADC conversions are halted if a new ADC conversion is triggered while ADC is busy. ADC conversions are triggered manually or by a timer. The affected ADC modes are:

- sequence-of-channels

- repeat-single-channel

- repeat-sequence-of-channels (ADC12CTL1.ADC12CONSEQx)

In addition, the timer overflow flag cannot be used to detect an overflow (ADC12IFGR2.ADC12TOVIFG).

Workaround 1. For manual trigger mode (ADC12CTL0.ADC12SC), ensure each ADC conversion is completed by first checking ADC12CTL1.ADC12BUSY bit before starting a new conversion.

2. For timer trigger mode (ADC12CTL1.ADC12SHP), ensure the timer period is greater than the ADC sample and conversion time.

To recover the conversion halt:

1. Disable ADC module (ADC12CTL0.ADC12ENC = 0 and ADC12CTL0.ADC12ON = 0)

2. Re-enable ADC module (ADC12CTL0.ADC12ON = 1 and ADC12CTL0.ADC12ENC = 1)

3. Re-enable conversion

CPU26 *CPUXv2 Module*

Function CALL SP does not behave as expected

Description When the intention is to execute code from the stack, a CALL SP instruction skips the first piece of data (instruction) on the stack. The second piece of data at SP+2 is used as the first executable instruction.

Workaround Write the op code for a NOP as the first instruction on the stack. Begin the intended subroutine at address SP + 2.

CPU27 *CPUXv2 Module*

Function Program Counter (PC) is corrupted during the context save of a nested interrupt

Description When a low power mode is entered within an interrupt service routine that has enabled nested interrupts (by setting the GIE bit), and the instruction that sets the low power mode is directly followed by a RETI instruction, an incorrect value of PC + 2 is pushed to the stack during the context save. Hence, the RETI instruction is not executed on return from the nested interrupt and the PC becomes corrupted.

Workaround Insert a NOP or __no_operation() intrinsic function between the instruction that sets the lower power mode and the RETI instruction.

CPU28 *CPUXv2 Module*

Function PC is corrupted when using certain extended addressing mode combinations

Description An extended memory instruction that modifies the program counter executes incorrectly when preceded by an extended memory write-back instruction under the following conditions:

First instruction:

2-operand instruction, extended mode using (register,index), (register,absolute), OR (register,symbolic) addressing modes

Second instruction:

2-operand instruction, extended mode using the (indirect,PC), (indirect auto-increment,PC), OR (indexed [with ind 0], PC) addressing modes

Example:

BISX.A R6,&AABCD

ANDX.A @R4+,PC

Workaround 1. Insert a NOP or a __no_operation() intrinsic function between the two instructions

Or

2. Do not use an extended memory instruction to modify the PC

CPU29 *CPUXv2 Module*

Function Using a certain instruction sequence to enter low power mode(s) affects the instruction width of the first instruction in an NMI ISR

Description If there is a pending NMI request when the CPU enters a low power mode (LPMx) using an instruction of Indexed source addressing mode, and that instruction is followed by a 20-bit wide instruction of Register source and destination addressing modes, the first instruction of the ISR is executed as a 20-bit wide instruction.

Example:

main:

...

MOV.W [indexed],SR ; Enter LPMx

MOVX.A [register],[register] ; 20-bit wide instruction

...

ISR_start:

MOV.B [indexed],[register] ; ERROR - Executed as a 20-bit instruction!

Note: [] indicates addressing mode

Workaround 1. Insert a NOP or a __no_operation() intrinsic function following the instruction that enters the LPMx using indexed addressing mode

OR

2. Use a NOP or a __no_operation() intrinsic function as first instruction in the ISR

OR

3. Do not use the indexed mode to enter LPMx

CPU30 *CPUXv2 Module*

Function ADDA, SUBA, CMPA [immediate],PC behave as if immediate value were offset by -2

Description The extended address instructions ADDA, SUBA, CMPA in immediate addressing mode are represented by 4-bytes of opcode (see the MSP430F5xx Family User's Guide MSP430F5xx Family User's Guide for more details). In cases where the program counter (PC) is used as the destination register only 2 bytes of the current instruction's 4-byte opcode are accounted for in the PC value. The resulting operation executes as if the immediate value were offset by a value of -2.

Ideal: ADDA #Immediate-4, PC

...is equivalent to...

Actual: ADDA #Immediate-2, PC

** NOTE: The MOV instruction is not affected **

Workaround 1) Modify immediate value in software to account for the offset of 2.

OR

2) Use extended 20-bit instructions (addx.a, subx.a, cmpx.a).

CPU31 *CPUXv2 Module*

Function SP corruption

Description When the instruction PUSHX.A is executed using the indirect auto-increment mode with the stack pointer (SP) as the source register [PUSHX.A @SP+] the SP is consequently corrupted. Instead of decrementing the value of the SP by four, the value of the SP is replaced with the data pointed to by the SP previous to the PUSHX.A instruction execution.

Workaround None. The compiler will not generate a PUSHX.A instruction that involves the SP.

CPU32 *CPUXv2 Module*

Function CALLA PC executes incorrectly

Description When the instruction CALLA PC is executed, the program counter (PC) that is pushed onto the stack during the context save is incorrectly offset by a value of -2.

Workaround None. The compiler will not generate a CALLA PC instruction.

CPU33 *CPUXv2 Module*

Function CALLA [indexed] may corrupt the program counter

Description When the Stack Pointer (SP) is used as the destination register in the CALLA index(Rdst) instruction and is preceded by a PUSH or PUSHX instruction in any of the following addressing modes: Absolute, Symbolic, Indexed, Indirect register or Indirect auto increment, the "index" of the CALLA instruction is not sign extended to 20-bits and is always treated as a positive value. This causes the Program Counter to be set to a wrong address location when the index of the CALLA instruction represents a negative offset.

NOTE:

1. This erratum only applies when the instruction sequence is: PUSH or PUSHX followed by CALLA index(SP)

2. This erratum does not apply if the PUSH or PUSHX instruction is used in the Register or Immediate addressing mode

3. This erratum only applies when SP is used as the destination register in the CALLA index(Rdst) instruction

Workaround Place a "NOP" instruction in between the PUSH or PUSHX and the CALLA index(SP) instructions.

NOTE: This bug has no compiler impact as the compiler will not generate a CALLA instruction that uses indexed addressing mode with the SP.

CPU34 *CPUXv2 Module*

Function CPU may be halted if a conditional jump is followed by a rotate PC instruction

Description If a conditional jump instruction (JZ, JNZ, JC, JNC, JN, JGE, JL) is followed by an Address Rotate instruction on the PC (RRCM, RRAM, RLAM, RRUM) and the jump is not performed, the CPU is halted.

Workaround Insert a NOP between the conditional jump and the rotate PC instructions.

CPU35 *CPUXv2 Module*

Function Instruction BIT.B @Rx,PC uses the wrong PC value

Description The BIT(.B/.W) instruction in indirect register addressing mode uses the wrong PC value. This instruction is represented by 2 bytes of opcode. If the Program Counter (PC) is used as the destination register, the 2 opcode bytes of the current BIT instruction are not accounted for. The resulting operation executes the instruction using the wrong PC value and this affects the results in the Status Register (SR).

Workaround None.

Note: The compiler will not generate a BIT instruction that uses the PC as an operand.

CPU37 *CPUXv2 Module*

Function Wrong program trace display in the debugger while using conditional jump instructions

Description The state storage window displays an incorrect sequence of instructions when:

1. Conditional jump instructions are used to form a software loop

AND

2. A false condition on the jump breaks out of the loop

In such cases the trace buffer incorrectly displays the first instruction of the loop as the instruction that is executed immediately after exiting the loop.

Example:

Actual Code:

```
mov #4,R4
LABEL mov #1,R5
dec R4
```

jnz LABEL

mov #2,R6

nop

State Storage Window Displays:

LABEL mov #1,R5

dec R4

jnz LABEL

mov #1,R5

nop

Workaround None

Note: This erratum affects the trace buffer display only. It does not affect code execution in debugger or free run mode

CPU39 *CPUXv2 Module*

Function PC is corrupted when single-stepping through an instruction that clears the GIE bit

Description Single-stepping over an instruction that clears the General Interrupt Enable bit (for example DINT or BIC #GIE,SR) when the GIE bit was previously set may corrupt the PC. For example, the DINT or BIC #GIE,SR is a 2-byte instruction. Single stepping through this instruction increments the PC by a value of 4 instead of 2 thus corrupting the next PC value.

Note: This erratum applies to debug mode only.

Workaround Insert a NOP or __no_operation() intrinsic immediately after the line of code that clears the GIE bit.

CPU40 *CPUXv2 Module*

Function PC is corrupted when executing jump/conditional jump instruction that is followed by instruction with PC as destination register or a data section

Description If the value at the memory location immediately following a jump/conditional jump instruction is 0X40h or 0X50h (where X = don't care), which could either be an instruction opcode (for instructions like RRCM, RRAM, RLAM, RRUM) with PC as destination register or a data section (const data in flash memory or data variable in

RAM), then the PC value is auto-incremented by 2 after the jump instruction is executed; therefore, branching to a wrong address location in code and leading to wrong program execution.

For example, a conditional jump instruction followed by data section (0140h).

@0x8012 Loop DEC.W R6

@0x8014 DEC.W R7

@0x8016 JNZ Loop

@0x8018 Value1 DW 0140h

Workaround In assembly, insert a NOP between the jump/conditional jump instruction and program code with instruction that contains PC as destination register or the data section.

In C, no workaround is necessary since the compiler automatically generates the necessary NOPs.

DMA4 *DMA Module*

Function Corrupted write access to 20-bit DMA registers

Description When a 20-bit wide write to a DMA address register (DMAxSA or DMAxDA) is interrupted by a DMA transfer, the register contents may be unpredictable.

Workaround

1. Design the application to guarantee that no DMA access interrupts 20-bit wide accesses to the DMA address registers.

OR

2. When accessing the DMA address registers, enable the Read Modify Write disable bit (DMARMWDIS = 1) or temporarily disable all active DMA channels (DMAEN = 0).

OR

3. Use word access for accessing the DMA address registers. Note that this limits the values that can be written to the address registers to 16-bit values (lower 64K of Flash).

DMA7 *DMA Module*

Function DMA request may cause the loss of interrupts

Description If a DMA request is received during the time when a module register (containing interrupt flags) is accesses with read-modify-write instruction these module-specific interrupts can get lost during the read-modify-write execution.

Workaround

1. Use a read of Interrupt Vector registers to clear interrupt flags and do not use read-modify-write instruction.

2. Disable all DMA channels during read-modify-write instruction of specific module registers containing interrupts flags while these interrupts are activated.

DMA8 *DMA Module*

Function DMA can corrupt values on write-access to program stack

Description If the DMA controller makes a write access to the stack while executing one of the following instructions, the data that is written may be corrupted.

CALLA [REG | IDX | SYM | ABS | IND | INA | IMM]

PUSHX.A [IDX | SYM | ABS | IND | IMM | INA]

PUSHX.A [REG]

PUSHM.A [REG]

POPM.A [REG]

Note: [...] denotes an addressing mode

Workaround Do not declare function-scope variables. Declare all variables that are intended to be modified by the DMA as global- or file-scope such that they are allocated in the data section of RAM and not on the program stack.

DMA10 *DMA Module*

Function	DMA access may cause invalid module operation
Description	The peripheral modules MPY, CRC, USB, RF1A and FRAM controller in manual mode can stall the CPU by issuing wait states while in operation. If a DMA access to the module occurs while that module is issuing a wait state, the module may exhibit undefined behavior.
Workaround	Ensure that DMA accesses to the affected modules occur only when the modules are not in operation. For example with the MPY module, ensure that the MPY operation is completed before triggering a DMA access to the MPY module.

EEM8 *EEM Module*

Function	Debugger stops responding when using the DMA
Description	In repeated transfer mode, the DMA automatically reloads the size counter (DMAxSZ) once a transfer is complete and immediately continues to execute the next transfer unless the DMA Enable bit (DMAEN) has been previously cleared. In burst-block transfer mode, DMA block transfers are interleaved with CPU activity 80/20% - of ten CPU cycles, eight are allocated to a block transfer and two are allocated for the CPU. Because the JTAG system must wait for the CPU bus to be clear to halt the device, it can only do so when two conditions are met: - Three clock cycles after any DMA transfer, the DMA is no longer requesting the bus. and - The CPU is not requesting the bus. Therefore, if the DMA is configured to operate in the repeat burst-block transfer mode, and a breakpoint is set between the line of code that triggers the DMA transfers and the line that clears the DMAEN bit, the DMA always requests the bus and the JTAG system never gains control of the device.
Workaround	When operating the DMA in repeat burst-block transfer mode, set breakpoint(s) only when the DMA transfers are not active (before the start or after the end of the DMA transfers).

EEM9 *EEM Module*

Function	Combined triggers on the PUSH instruction may be missed
Description	When the PUSH instruction is used in any addressing mode except register or immediate modes, a combined trigger may be missed when its conditions are defined by a PUSH instruction fetch and a successful match of the value being pushed onto stack.
Workaround	None

EEM11 *EEM Module*

Function	Conditional register write trigger fails while executing rotate instructions
Description	A conditional register write trigger will fail to generate the expected breakpoint if the trigger condition is a result of executing one of the following rotate instructions: RRUM,RRCM, RRAM and RLAM.
Workaround	None

NOTE: This erratum applies to debug mode only.

EEM13 *EEM Module*

Function Halting the debugger does not return correct PC value when in LPM

Description When debugging, if the device is in any low power mode and the debugger is halted, the program counter update by the debugger is corrupted. The debugger is unable to halt at the correct location.

Workaround None.

NOTE: This erratum applies to debug mode only.

EEM14 *EEM Module*

Function Single-step or breakpoint on module registers with WAIT capability may not work

Description In debug mode, the CPU clock is driven independently from the wait inputs of device modules (i.e., MULT, USB, RF1A, CRC). As a result, an EEM halt on an access to the module data registers (breakpoint or single-step) may show incorrect results due to incomplete execution.

Workaround Do not single-step through a data register access that holds the CPU to provide a valid result. Place breakpoints after the affected register is accessed and sufficient clock cycles have been provided.

NOTE: This erratum applies to debug mode only.

EEM16 *EEM Module*

Function The state storage display does not work reliably when used on instructions with CPU Wait cycles.

Description When executing instructions that require wait states; the state storage window updates incorrectly. For example a flash erase instruction causes the CPU to be held until the erase is completed i.e. the flash puts the CPU in a wait state. During this time if the state storage window is enabled it may incorrectly display any previously executed instruction multiple times.

Workaround Do not enable the state storage display when executing instructions that require wait states. Instead set a breakpoint after the instruction is completed to view the state storage display.

NOTE: This erratum affects debug mode only.

EEM17 *EEM Module*

Function Wrong Breakpoint halt after executing Flash Erase/Write instructions

Description Hardware breakpoints or Conditional Address triggered breakpoints on instructions that follow Flash Erase/Write instructions, stops the debugger at the actual Flash Erase/Write instruction even though the flash erase/write operation has already been executed. The hardware/conditional address triggered breakpoints that are placed on either the next two single opcode instructions OR the next double opcode instruction that follows the Flash Erase/Write instruction are affected by this erratum.

Workaround None. Use other conditional/advanced triggered breakpoints to halt the debugger right after Flash erase/write instructions.

NOTE: This erratum affects debug mode only.

EEM19 *EEM Module*

Function DMA may corrupt data in debug mode

Description When the DMA is enabled and the device is in debug mode, the data written by the DMA may be corrupted when a breakpoint is hit or when the debug session is halted.

Workaround Do not halt or use breakpoints during a DMA transfer.

NOTE: This erratum applies to debug mode only.

EEM21 *EEM Module*

Function LPMx.5 debug limitations

Description Debugging the device in LPMx.5 mode might wake the device up from LPMx.5 mode inadvertently, and it is possible that the device enters a lock-up condition; that is, the device cannot be accessed by the debugger any more.

Workaround Follow the debugging steps in Debugging MSP430 LPM4.5 SLAA424 .

EEM23 *EEM Module*

Function EEM triggers incorrectly when modules using wait states are enabled

Description When modules using wait states (USB, MPY, CRC and FRAM controller in manual mode) are enabled, the EEM may trigger incorrectly. This leads to wrong profile counter, data watch points, and state storage functions.

Workaround None.

NOTE: This erratum affects debug mode only.

FLASH33 *FLASH Module*

Function Flash erase/program with fsystem <160kHz causes code execution to fail

Description A flash erase or flash program operation with the system frequency (fsystem) <160kHz

causes the program execution (executing out of main or info memory) that follows to fail.

Workaround Make sure the fsystem >160kHz before doing a flash erase or program operation.

FLASH34 *FLASH Module*

Function Concurrent flash read during bank erase fails

Description Code residing in flash cannot be executed during a bank erase.

Workaround Place the code to be executed during bank erase in RAM.

FLASH35 *FLASH Module*

Function Flash read error may cause invalid memory access

Description Flash memory accesses are always 32-bit wide and performed on 32-bit boundaries. A read error when accessing flash may corrupt the most significant bit (MSB) in a 32-bit access when programmed as a logic 0.

When affected flash is idle, the read disturb may occur on the first flash access that follows any of the listed events:

- On reset issued at RST input pin

- On wakeup from low-power modes when accessing interrupt vector addresses

located at addresses <0x8000

- When moving program execution from unaffected to affected areas of flash

- When accessing affected flash after execution from RAM

Workaround See Flash Read Error and Susceptibility for MSP430F54xxA (SLAA470) for detailed background information and possible workaround(s).

FLASH37 *FLASH Module*

Function Corrupted flash read when SVM low-side flag is triggered

Description If the SVM low side is enabled, a change in the VCORE voltage level (an increase in the VCORE level) may cause the currently executed read operation from flash to be incorrect and may lead to unexpected code execution or incorrect data. This can happen under any one of the following conditions:

- When the VCORE is changed in application, the SVM low side is used to indicate if the core voltage has settled by using the SVMDLYIFG flag. The failure occurs only when a flash access is concurrent to the expiration of the settling time delay.

- Unexpected changes in the VCORE voltage level

For code examples and detailed guidance on the PMM operation and software APIs for PMM configuration see the driverlib APIs from 430Ware (MSP430Ware).

Workaround - Execute the procedure to change the VCORE level from RAM.

or

- If executing from flash, follow the procedure below when increasing the VCORE level. Note: To apply this workaround, the SVM low-side comparator must operate in normal

```
mode (SVMLFP = 0 in SVMLCTL).
// Set SVM highside to new level and check if a VCore increase is possible
SVSMHCTL = SVMHE | SVSHE | (SVSMHRRL0 * level);
// Wait until SVM highside is settled
while ((PMMIFG & SVSMHDLYIFG) == 0);
// Clear flag
PMMIFG &= ~SVSMHDLYIFG;
// Set also SVS highside to new level
// Vcc is high enough for a Vcore increase
SVSMHCTL |= (SVSHRVL0 * level);
// Wait until SVM highside is settled
while ((PMMIFG & SVSMHDLYIFG) == 0);
// Clear flag
PMMIFG &= ~SVSMHDLYIFG;

//**************flow change for errata workaround ************
// Set VCore to new level
PMMCTL0_L = PMMCOREV0 * level;

// Set SVM, SVS low side to new level
SVSMLCTL = SVMLE | (SVSMLRRL0 * level)| SVSLE | (SVSLRVL0 * level);
// Wait until SVM, SVS low side is settled
while ((PMMIFG & SVSMLDLYIFG) == 0);
// Clear flag
PMMIFG &= ~SVSMLDLYIFG;
//**************flow change for errata workaround ************
```

JTAG20 *JTAG Module*

Function BSL does not exit to application code

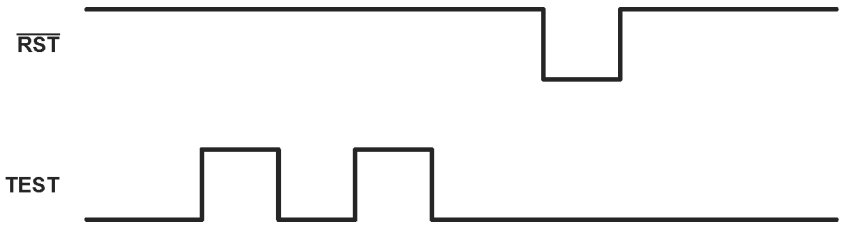
Description The methods used to exit the BSL per MSP430 Programming Via the Bootstrap Loader (SLAU319) are invalid.

Workaround To exit the BSL one of the following methods must be used.

- A Power cycle

or

- Toggle the TEST pin twice when nRST is high and then pull nRST low.



Note: This sequence is not subject to timing constraints and the appropriate level transitions are sufficient to trigger an exit from BSL mode.

MPY1 *MPY Module*

Function Save and Restore feature on MPY32 not functional

Description The MPY32 module uses the Save and Restore method which involves saving the multiplier state by pushing the MPY configuration/operand values to the stack before using the multiplier inside an Interrupt Service Routine (ISR) and then restoring the state by popping the configuration/operand values back to the MPY registers at the end of the ISR. However due to the erratum the Save and Restore operation fails causing the write operation to the OP2H register right after the restore operation to be ignored as it is not preceded by a write to OP2L register resulting in an invalid multiply operation.

Workaround None. Disable interrupts when writing to OP2L and OP2H registers.

Note: When using the C-compiler, the interrupts are automatically disabled while using the MPY32

PMM9 *PMM Module*

Function False SVSxIFG events

Description The comparators of the SVS require a certain amount of time to stabilize and output a correct result once re-enabled; this time is different for the Full Performance versus the Normal mode. The time to stabilize the SVS comparators is intended to be accounted for by a built-in event-masking delay of 2 us when Full Performance mode is enabled.

However, the comparators of the SVS in Full Performance mode take longer than 2 us to stabilize so the possibility exists that a false positive will be triggered on the SVSH or SVSL. This results in the SVSxIFG flags being set and depending on the configuration of SVSxPE bit a POR can also be triggered.

Additionally when the SVSxIFGs are set, all GPIOs are tri-stated i.e. floating until the SVSx comparators are settled.

The SVS IFG's are falsely set under the following conditions:

1. Wakeup from LPM2/3/4 when SVSxMD = 0 (default setting) && SVSxFP=1. The SVSx comparators are disabled automatically in LPM2/3/4 and are then re-enabled on return to active mode.

2. SVSx is turned on in full performance mode (SVSxFP=1).

3. A PUC/POR occurs after SVSx is disabled. After a PUC or POR the SVSx are enabled automatically but the settling delay does not get triggered. Based on SVSxPE bit this may lead to POR events until the SVS comparator is fully settled.

Workaround For each of the above listed conditions the following workarounds apply:

1. If the Full Performance mode is to be enabled for either the high- or low-side SVS

comparators, the respective SVSxMD bits must be set (SVSxMD = 1) such that the SVS comparators are not temporarily shut off in LPM2/3/4. Note that this is equivalent to a 2 uA (typical) adder to the low power mode current, per the device-specific datasheet, for each SVSx that remains enabled.

2. The SVSx must be turned on in normal mode (SVSxFP=0). It can be reconfigured to use full performance mode once the SVSx/SVMx delay has expired.

3. Ensure that SVSH and SVSL are always enabled.

PMM10 *PMM Module*

Function SVS/SVM flags disabled after Power Up Clear reset

Description SVS/SVM interrupt flag functionality is disabled after a Power Up Clear (PUC) Reset if the SVS was disabled before the PUC reset was applied.

Workaround A write access to the intended SVSx register after PUC re-enables the SVS & SVM interrupt flags.

PMM11 *PMM Module*

Function MCLK comes up fast on exit from LPM3 and LPM4

Description The DCO exceeds the programmed frequency of operation on exit from LPM3 and LPM4 for up to 6 us. This behavior is masked from affecting code execution by default: SVSL and SVML run in normal-performance mode and mask CPU execution for 150 us on wakeup from LPM3 and LPM4. However, when the low-side SVS and the SVM are disabled or are operating in full-performance mode (SVMLE = 0 and SVSLE = 0, or SVMLFP = 1 and SVSLFP = 1) AND MCLK is sourced from the internal DCO running over 4 MHz, 7 MHz, 11 MHz, or 14 MHz at core voltage levels 0, 1, 2, and 3, respectively, the mask lasts only 2 us. MCLK is, therefore, susceptible to run out of spec for 4 us.

Workaround Set the MCLK divide bits in the Unified Clock System Control 5 Register (UCSCTL5) to divide MCLK by two prior to entering LPM3 or LPM4 (set DIVMx = 001). This prevents MCLK from running out of spec when the CPU wakes from the low-power mode. Following the wakeup from the low-power mode, wait 32, 48, 80, or 100 cycles for core voltage levels 0, 1, 2, and 3, respectively, before resetting DIVMx to zero and running MCLK at full speed [for example, __delay_cycles(100)].

PMM12 *PMM Module*

Function SMCLK comes up fast on exit from LPM3 and LPM4

Description The DCO exceeds the programmed frequency of operation on exit from LPM3 and LPM4 for up to 6 us. When SMCLK is sourced by the DCO, it is not masked on exit from LPM3 or LPM4. Therefore, SMCLK exceeds the programmed frequency of operation on exit from LPM3 and LPM4 for up to 6 us. The increased frequency has the potential to change the expected timing behavior of peripherals that select SMCLK as the clock source.

Workaround - Use XT2 as the SMCLK oscillator source instead of the DCO.

or

- Do not disable the clock request bit for SMCLKREQEN in the Unified Clock System Control 8 Register (UCSCTL8). This means that all modules that depend on SMCLK to

operate successfully should be halted or disabled before entering LPM3 or LPM4. If the increased frequency prevents the proper function of an affected module, wait 32, 48, 80, or 100 cycles for core voltage levels 0, 1, 2, or 3, respectively, before re-enabling the module [for example, __delay_cycles(100)].

PMM14 *PMM Module*

Function

Increasing the core level when SVS/SVM low side is configured in full-performance mode causes device reset

Description

When the SVS/SVM low side is configured in full performance mode (SVSMLCTL.SVSLFP = 1), the setting time delay for the SVS comparators is ~2us. When increasing the core level in full-performance mode; the core voltage does not settle to the new level before the settling time delay of the SVS/SVM comparator expires. This results in a device reset.

Workaround

When increasing the core level; enable the SVS/SVM low side in normal mode (SVSMLCTL.SVSLFP=0). This provides a settling time delay of approximately 150us allowing the core sufficient time to increase to the expected voltage before the delay expires.

PMM15 *PMM Module*

Function

Device may not wake up from LPM2, LPM3, or LPM4

Description

Device may not wake up from LPM2, LPM3 or LMP4 if an interrupt occurs within 1 us after the entry to the specified LPMx; entry can be caused either by user code or automatically (for example, after a previous ISR is completed). Device can be recovered with an external reset or a power cycle. Additionally, a PUC can also be used to reset the failing condition and bring the device back to normal operation (for example, a PUC caused by the WDT).

This effect is seen when:

- A write to the SVSMHCTL and SVSMLCTL registers is immediately followed by an LPM2, LPM3, LPM4 entry without waiting the requisite settling time ((PMMIFG.SVSMLDLYIFG = 0 and PMMIFG.SVSMHDLYIFG = 0)).

or

The following two conditions are met:

- The SVSL module is configured for a fast wake-up or when the SVSL/SVML module is turned off. The affected SVSMLCTL register settings are shaded in the following table.

	SVSLE	SVSLMD	SVSLFP	AM, LPM0/1 SVSL state	Manual SVSMLACE = 0 LPM2/3/4 SVSL State	Automatic SVSMLACE = 1 LPM2/3/4 SVSL State	Wakeup Time LPM2/3/4
SVSL	0	x	x	OFF	OFF	OFF	$t_{WAKE-UP\ FAST}$
	1	0	0	Normal	OFF	OFF	$t_{WAKE-UP\ SLOW}$
	1	0	1	Full Performance	OFF	OFF	$t_{WAKE-UP\ FAST}$
	1	1	0	Normal	Normal	OFF	$t_{WAKE-UP\ SLOW}$
	1	1	1	Full Performance	Full Performance	Normal	$t_{WAKE-UP\ FAST}$
	SVMLE	SVMLFP		AM, LPM0/1 SVML state	Manual SVSMLACE = 0 LPM2/3/4 SVML State	Automatic SVSMLACE = 1 LPM2/3/4 SVML State	Wakeup Time LPM2/3/4
SVML	0	x		OFF	OFF	OFF	$t_{WAKE-UP\ FAST}$
	1	0		Normal	Normal	OFF	$t_{WAKE-UP\ SLOW}$
	1	1		Full Performance	Full Performance	Normal	$t_{WAKE-UP\ FAST}$

and

-The SVSH/SVMH module is configured to transition from Normal mode to an OFF state when moving from Active/LPM0/LPM1 into LPM2/LPM3/LPM4 modes. The affected SVSMHCTL register settings are shaded in the following table.

SVSH	SVSHE	SVSHMD	SVSHFP	AM, LPM0/1 SVSH state	Manual SVSMHACE = 0 LPM2/3/4 SVSH State	Manual SVSMHACE = 1 LPM2/3/4 SVSH State
	0	x	x	OFF	OFF	OFF
	1	0	0	Normal	OFF	OFF
	1	0	1	Full Performance	OFF	OFF
	1	1	0	Normal	Normal	OFF
	1	1	1	Full Performance	Full Performance	Normal

SVMH	SVSHE	SVMHFP	AM, LPM0/1 SVSH state	Manual SVSMHACE = 0 LPM2/3/4 SVSH State	Manual SVSMHACE = 1 LPM2/3/4 SVSH State
	0	x	OFF	OFF	OFF
	1	0	Normal	Normal	OFF
	1	1	Full Performance	Full Performance	Normal

Workaround

Any write to the SVSMxCTL register must be followed by a settling delay (PMMIFG.SVSMLDLYIFG = 0 and PMMIFG.SVSMHDLYIFG = 0) before entering LPM2, LPM3, LPM4.

and

1. Ensure the SVSx, SVMx are configured to prevent the issue from occurring by the following:

- Configure the SVSL module for slow wake up (SVSLFP = 0). Note that this will increase the wakeup time from LPM2/3/4 to twakeupslow (~150 us).

or

- Do not configure the SVSH/SVMH such that the modules transition from Normal mode to an OFF state on LPM entry. Instead force the modules to remain ON even in LPMx. Note that this will cause increased power consumption when in LPMx.

Refer to the MSP430F5xx and MSP430F6xx Core Libraries (SLAA448) for proper PMM configuration functions.

Use the following function, PMM15Check (void), to determine whether or not the existing PMM configuration is affected by the erratum. The return value of the function is 1 if the configuration is affected, and 0 if the configuration is not affected.

```
unsigned char PMM15Check (void)
{
// First check if SVSL/SVML is configured for fast wake-up
if ( (!(SVSMLCTL & SVSLE)) || ((SVSMLCTL & SVSLE) && (SVSMLCTL & SVSLFP)) ||
(!(SVSMLCTL & SVMLE)) || ((SVSMLCTL & SVMLE) && (SVSMLCTL & SVMLFP)) )
{ // Next Check SVSH/SVMH settings to see if settings are affected by PMM15
if ((SVSMHCTL & SVSHE) && (!(SVSMHCTL & SVSHFP)))
{
if ( (!(SVSMHCTL & SVSHMD)) || ((SVSMHCTL & SVSHMD) &&
(SVSMHCTL & SVSMHACE)) )
return 1; // SVSH affected configurations
```

}

if ((SVSMHCTL & SVMHE) && (!(SVSMHCTL & SVMHFP)) && (SVSMHCTL & SVSMHACE))

return 1; // SVMH affected configurations

}

return 0; // SVS/M settings not affected by PMM15

}

}

2. If fast servicing of interrupts is required, add a 150us delay either in the interrupt service routine or before entry into LPM3/LPM4.

PMM17 *PMM Module*

Function Vcore exceed maximum limit of 2.0V.

Description If the device is switching between active mode and LPM2/3/4 with very high frequency, the core voltage of the device, VCORE, may rise incrementally until it is beyond 2.0 V, which is the maximum allowable limit for digital circuitry internal to the MSP430. This increase may remain undetected in an application with no functional impact but could potentially result in decreased endurance and increased wear over the lifetime of the device, because the digital circuitry is continually subjected to overvoltage.

The accumulation of Vcore affects only older lot trace codes of mentioned revisions.

Workaround The VCORE accumulation is fixed by enabling the prolongation mechanism in software. The following lines of code need to be implemented before periodic execution of LPM-to-AM-LPM. It is recommended to execute the code at program start:

ASM code:

mov.w #0x9602, &0110h;

bis.w #0x0800, &0112h;

C code:

(unsigned int)(0x0110)=0x9602;

(unsigned int)(0x0112)|=0x0800;

The automatic prolongation mechanism is disabled with a BOR and must be enabled after each boot code execution.

For detailed background information, affected LTCs and possible workaround(s) see Vcore Accumulation documentation in SLAA505.

PMM18 *PMM Module*

Function PMM supply overvoltage protection falsely triggers POR

Description The PMM Supply Voltage Monitor (SVM) high side can be configured as overvoltage protection (OVP) using the SVMHOVPE bit of SVSMHCTL register. In this mode a POR should typically be triggered when DVCC reaches ~3.75V.

If the OVP feature of SVM high side is enabled going into LPM234, the SVM might trigger at DVCC voltages below 3.6V (~3.5V) within a few ns after wake-up. This can falsely cause an OVP-triggered POR. The OVP level is temperature sensitive during fail scenario and decreases with higher temperature (85 degC ~3.2V).

Workaround Use automatic control mode for high-side SVS & SVM (SVSMHCTL.SVSMHACE=1). The SVM high side is inactive in LPM2, LPM3, and LPM4.

PMM20 *PMM Module*

Function Unexpected SVSL/SVML event during wakeup from LPM2/3/4 in fast wakeup mode

Description If PMM low side is configured to operate in fast wakeup mode, during wakeup from LPM2/3/4 the internal VCORE voltage can experience voltage drop below the corresponding SVSL and SVML threshold (recommendation according to User's Guide) leading to an unexpected SVSL/SVML event. Depending on PMM configuration, this event triggers a POR or an interrupt.

NOTE: As soon the SVSL or the SVML is enabled in Normal performance mode the device is in slow wakeup mode and this erratum does not apply.

In addition, this erratum has sporadic characteristic due to an internal asynchronous circuit. The drop of Vcore does not have an impact on specified device performance.

Workaround If SVSL or SVML is required for application (to observe external disruptive events at Vcore pin) the slow wakeup mode has to be used to avoid unexpected SVSL/SVML events. This is achieved if the SVSL or the SVML is configured in "Normal" performance mode (not disabled and not in "Full" Performance Mode).

PORT16 *PORT Module*

Function GPIO pins are driven low during device start-up

Description During device start-up, all of the GPIO pins are expected to be in the floating input state. Due to this erratum, some of the GPIO pins are driven low for the duration of boot code execution during device start-up, if an external reset event (via the RST pin) interrupted the previous boot code execution. Boot code is always executed after a BOR, and the duration of this boot code execution is approximately 500us.

For a given device family, this erratum affects only the GPIO pins that are not available in the smallest package device family member, but that are present on its larger package variants.

NOTE: This erratum does not affect the smallest package device variants in a particular device family.

Workaround Ensure that no external reset is applied via the RST pin during boot code execution of the device, which occurs 1us after device start-up.

NOTE: System application needs to account for this erratum in to ensure there is no increased current draw by the external components or damage to the external components in the system during device start-up.

PORT19 *PORT Module*

Function Port interrupt may be missed on entry to LPMx.5

Description If a port interrupt occurs within a small timing window (~1MCLK cycle) of the device entry into LPM3.5 or LPM4.5, it is possible that the interrupt is lost. Hence this interrupt will not trigger a wakeup from LPMx.5.

Workaround None

RTC3 *RTC Module*

Function Unreliable write to RTC register

Description A write access to the RTC registers (SEC, MIN, HOUR, DATE, MON, YEAR, DOW) may result in unexpected results. As a consequence the addressed register might not contain the written data, or some data can be accidentally written to other RTC registers.

Workaround Use the RTC library routines, available as F541x/F543x code examples on the MSP430 Code Examples page (www.ti.com/msp430 > Software > Code Examples), which use carefully aligned MOV instructions. Library is listed as RTC_Workaround.zip and includes both CCE and IAR example projects that show proper usage. Using this library, full access to RTC registers is possible.

RTC6 *RTC Module*

Function the step size of the RTC frequency adjustment is twice the specified size.

Description The step size of the RTC frequency adjustment is =4ppm/-8ppm. This is twice the size specified in the User's Guide.

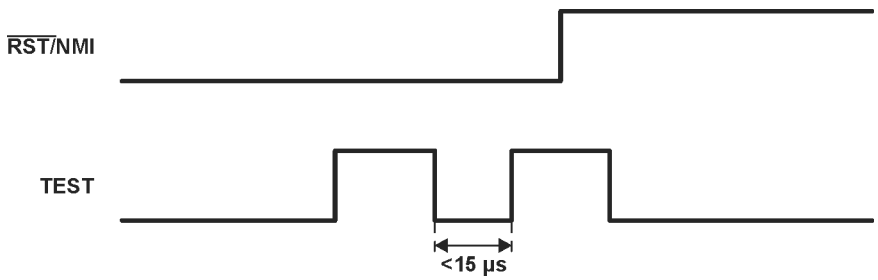
For up calibration this results in a step size per step of 8ppm (1024 cycles) instead of 4ppm (512 cycles). For down calibration this results in a step size per step of 4ppm (512 cycles) instead of 2ppm (256 cycles).

Workaround Half the calibration value written into RTCCAL register to compensate the doubled step size.

SYS10 *SYS Module*

Function BSL entry sequence is subject to specific timing requirements

Description The BSL entry sequence requires that the low phase of the TEST/SBWTCK pin does not exceed 15us. This timing requirement is faster than most PC serial ports can provide, as shown in the following picture. If this requirement is not met, the entry sequence fails and the SYSBSLIND is not set.



Workaround An external hardware solution is recommended to provide the appropriate BSL entry sequence. See http://processors.wiki.ti.com/index.php/BSL_(MSP430) for

recommendations on available BSL hardware.

SYS12 *SYS Module*

Function Invalid ACCVIFG when DVcc in the range of 2.4 to 2.6V

Description A Flash Access Violation Interrupt Flag (ACCVIFG) may be triggered by the Voltage Changed During Program Error bit (VPE) when DVcc is in the range of 2.4 to 2.6V. Although this behavior is expected according to the user's guide, the VPE does not signify an invalid flash operation has occured.

If the ACCVIE bit is set and a flash operation is executed in the affected voltage range, an unnecessary interrupt is requested. The bootstrap loader also cannot be used to execute write/erase flash operations in this voltage range, because it exits the flash operation and returns an error on an ACCVIFG event.

Workaround None

SYS16 *SYS Module*

Function Fast Vcc ramp after device power up may cause a reset

Description At initial power-up, after Vcc crosses the brownout threshold and reaches a constant level, an abrupt ramp of Vcc at a rate dV/dT > 1V/100us can cause a brownout condition to be incorrectly detected even though Vcc does not fall below the brownout threshold. This causes the device to undergo a reset.

Workaround Use a controlled Vcc ramp to power up the device.

TA20 *TIMER_A Module*

Function TA0 output connection to ADC12 is incompatible with previous device families

Description The Timer_A output signal, TA0, is connected to the ADC12. To be compatible with previous device families, should be connected to TA1.

Workaround Modify any existing code to use TA0 as opposed to TA1. In addition, Timer_B7 now supports TB0 or TB1 for usage with the ADC12.

TAB23 *TIMER_A/TIMER_B Module*

Function TAxR/TBxR read can be corrupted when TAxR/TBxR = TAxCCR0/TBxCCR0

Description When a timer in Up mode is stopped and the counter register (TAxR/TBxR) is equal to the TAxCCR0/TBxCCR0 value, a read of the TAR/TBR register may return an unexpected result.

Workaround 1. Use 'Up/Down' mode instead of 'Up' mode

OR

2. In 'Up' mode, use the timer interrupt instead of halting the counter and reading out the value in TAxR/TBxR

OR

3. When halting the timer counter in 'Up' mode, reinitialize the timer before starting to run

again.

UCS6 *UCS Module*

Function USCI source clock does not turn off in LPM3/4 when UART is idle

Description The USCI clock source (ACLK/SMCLK) remains enabled in LPM3 and LPM4 when the USCI is configured in UART mode and the communication is idle (UCSWRST = 0 but no TX or RX currently executing). This is contrary to the expected automatic clock activation described in the User's Guide and can lead to higher current consumption in low power modes, depending on the oscillator that feeds ACLK / SMCLK.

Workaround Use the oscillator that is already active in LPM3 (ACLK) to source the USCI and utilize the low-power baud rate generator (UCOS16 = 0). For UART baud rates where a fast SMCLK sourced by the internal DCO is required use LPM0 instead of LPM3.

UCS7 *UCS Module*

Function DCO drifts when servicing short ISRs when in LPM0 or exiting active from ISRs for short periods of time

Description The FLL uses two rising edges of the reference clock to compare against the DCO frequency and decide on the required modifications to the DCOx and MODx bits. If the device is in a low power mode with FLL disabled (LPM0 with DCO not sourcing ACLK/SMCLK or LPM2, LPM3, LPM4 where SCG1 bit is set) and enters a state which enables FLL (enter ISR from LPM0/LPM2 or exit active from ISRs) for a period less than 3x reference clock cycles, then the FLL will cause the DCO to drift.

This occurs because the FLL immediately begins comparing an active DCO with its reference clock and making the respective modifications to the DCOx and MODx bits. If the FLL is not given sufficient time to capture a full reference clock cycle (2 x reference clock periods) and adjust accordingly (1 x reference clock period), then the DCO will keep drifting each time the FLL is enabled.

Workaround (1) If DCO is not sourcing ACLK or SMCLK in the application, use LPM1 instead of LPM0 to make sure FLL is disabled when interrupt service routine is serviced.

(2) When exiting active from ISRs, insert a delay of at least 3 x reference clock periods. To save on power budget, the 3 x reference clock periods could also be spent in LPM0 with TimerA or TimerB using ACLK/SMCLK sourced from DCO. This way, the FLL and DCO are still active in LPM0.

UCS9 *UCS Module*

Function Digital Bypass mode prevents entry into LPM4

Description When entering LPM4, if an external digital input applied to XT1 in HF mode or XT2 is not turned off, the PMM does not switch to low-current mode causing higher than expected power consumption.

Workaround Before entering LPM4:

(1) Switch to a clock source other than external bypass digital input.

OR

(2) Turn off external bypass mode (UCSCTL6.XT1BYPASS = 0).

UCS10 *UCS Module*

Function Modulation causes shift in DCO frequency

Description When the FLL is enabled, the DCO frequency can be tracked automatically by modifying the DCOx and MODx bits. The MODx bits switch between the frequency selected by the DCO bits and the next-higher frequency set by (DCO + 1). The erroneous behavior is seen when the FLL is tracking close to a DCO step boundary and the MOD counter is expected to rollover, but instead the DCO bits increment and the MOD bits decrement. This causes the DCO to shift by up to 12% and remain at an increased frequency until approximately 15 REFCLK cycles have elapsed. The frequency reverts to the expected value immediately afterward.

For example, the modulator moves from DCOx = n and MODx = 31 to DCOx = n + 1

and MODx = 30, causing a large increase in the DCO frequency.

Applications could be impacted as follows:

When using the DCO frequency for asynchronous serial communication and timer operation, the effect can be seen as corrupted data or incorrect timing events.

Workaround (1) Turn off the FLL.

Or

(2) Implement a Software FLL, comparing the DCO frequency to a known reference such as REFO or LFXT1 using a timer capture and tuning the value of the DCO and MOD bits periodically.

Or

(3) Execute the following sequence in periodic intervals.

1. Disable peripherals sourced by the DCO such as UART and Timer.

2. Turn on the FLL.

3. Wait the worst case settling time of 32 X 32 X fFLLREFCLK to allow it to lock to the target frequency.

4. Turn off the FLL.

5. Compare the DCO frequency to a known reference such as REFO or LFXT1 using a timer capture.

- If the DCO frequency is higher than expected, repeat from step (2) until the

frequency reaches to the expected range.

- Else proceed with code execution.

See the application report UCS10 Guidance SLAA489 for more detailed information regarding working with this erratum. This erratum does not affect proper operation of the CPU when MCLK = DCO/FLL and is set to the maximum clock frequency specified in the device datasheet.

UCS11 *UCS Module*

Function Modifying UCSCTL4 clock control register triggers an erroneous clock source request

Description Changing the SELM/SELS/SELA bits in the UCSCTL4 register might trigger the respective clocks to select an incorrect clock source which requests the XT1/XT2 clock. If the crystals are not present at XT1/XT2 or present but not yet configured in the application firmware, then the respective XT1/XT2 fault flag is falsely set.

Workaround Clear all the fault flags in UCSCTL7 register once after changing any of the SELM/SELS/SELA bits in the UCSCTL4 register.

USCI26 *USCI Module*

Function Tbuf parameter violation in I2C multi-master mode

Description In multi-master I2C systems the timing parameter Tbuf (bus free time between a stop condition and the following start) is not guaranteed to match the I2C specification of 4.7us in standard mode and 1.3us in fast mode. If the UCTXSTT bit is set during a running I2C transaction, the USCI module waits and issues the start condition on bus release causing the violation to occur.

Note: It is recommended to check if UCBBUSY bit is cleared before setting UCTXSTT=1.

Workaround None

USCI30 *USCI Module*

Function I2C mode master receiver / slave receiver

Description When the USCI I2C module is configured as a receiver (master or slave), it performs a double-buffered receive operation. In a transaction of two bytes, once the first byte is moved from the receive shift register to the receive buffer the byte is acknowledged and the state machine allows the reception of the next byte.

If the receive buffer has not been cleared of its contents by reading the UCBxRXBUF register while the 7th bit of the following data byte is being received, an error condition may occur on the I2C bus. Depending on the USCI configuration the following may occur:

1) If the USCI is configured as an I2C master receiver, an unintentional repeated start condition can be triggered or the master switches into an idle state (I2C communication aborted). The reception of the current data byte is not successful in this case.

2) If the USCI is configured as I2C slave receiver, the slave can switch to an idle state stalling I2C communication. The reception of the current data byte is not successful in this case. The USCI I2C state machine will notify the master of the aborted reception with a NACK.

Note that the error condition described above occurs only within a limited window of the 7th bit of the current byte being received. If the receive buffer is read outside of this window (before or after), then the error condition will not occur.

Workaround a) The error condition can be avoided altogether by servicing the UCBxRXIFG in a timely manner. This can be done by (a) servicing the interrupt and ensuring UCBxRXBUF is read promptly or (b) Using the DMA to automatically read bytes from receive buffer upon UCBxRXIFG being set.

OR

b) In case the receive buffer cannot be read out in time, test the I2C clock line before the UCBxRXBUF is read out to ensure that the critical window has elapsed. This is done by checking if the clock line low status indicator bit UCSCLLOW is set for atleast three USCI bit clock cycles i.e. 3 X t(BitClock).

Note that the last byte of the transaction must be read directly from UCBxRXBUF. For all other bytes follow the workaround:

Code flow for workaround

(1) Enter RX ISR for reading receiving bytes

(2) Check if UCSCLLOW.UCBxSTAT == 1

(3) If no, repeat step 2 until set

(4) If yes, repeat step 2 for a time period > 3 x t (BitClock) where t (BitClock) = 1/ f (BitClock)

(5) If window of 3 x t(BitClock) cycles has elapsed, it is safe to read UCBxRXBUF

USCI31 *USCI Module*

Function Framing Error after USCI SW Reset (UCSWRST)

Description While receiving a byte over USCI-UART (with UCBUSY bit set), if the application resets the USCI module (software reset via UCSWRST), then a framing error is reported for the next receiving byte.

Workaround

1. If possible, do not reset USCI-UART during an ongoing receive operation; that is, when UCBUSY bit is set.

2. If the application software resets the USCI module (via the UCSWRST bit) during an ongoing receive operation, then set and reset the UCSYNC bit before releasing the software USCI reset.

Workaround code sequence:

```
bis #UCSWRST, &UCAxCTL1 ; USCI SW reset
;Workaround begins
bis #UCSYNC, &UCAxCTL0 ; set synchronous mode
bic #UCSYNC, &UCAxCTL0 ; reset synchronous mode
;Workaround ends
bic #UCSWRST, &UCAxCTL1 ; release USCI reset
```

USCI35 *USCI Module*

Function Violation of setup and hold times for (repeated) start in I2C master mode

Description In I2C master mode, the setup and hold times for a (repeated) START, $t_{SU,STA}$ and $t_{HD,STA}$ respectively, can be violated if SCL clock frequency is greater than 50kHz in standard mode (100kbps). As a result, a slave can receive incorrect data or the I2C bus can be stalled due to clock stretching by the slave.

Workaround If using repeated start, ensure SCL clock frequencies is < 50kHz in I2C standard mode (100 kbps).

USCI39 *USCI Module*

Function USCI I2C IFGs UCSTTIFG, UCSTPIFG, UCNACKIFG

Description Unpredictable code execution can occur if one of the hardware-clear-able IFGs UCSTTIFG, UCSTPIFG or UCNACKIFG is set while the global interrupt enable is set by software (GIE=1). This erratum is triggered if ALL of the following conditions are met:

1. Pending Interrupt: One of the UCxIFG=1 AND UCxIE=1 while GIE=0

2. The GIE is set by software (e.g. EINT)

3. The pending interrupt is cleared by hardware (external I2C event) in a time window of 1 MCLK clock cycle after the "EINT" instruction is executed.

Workaround Disable the UCSTTIFG, UCSTPIFG and UCNACKIFG before the GIE is set. After GIE is set, the local interrupt enable flags can be set again.

Assembly example:

bic #UCNACKIE+UCSTPIE+UCSTTIE, UCBxIE ; disable all self-clearing interrupts

NOP

EINT

bis #UCNACKIE+UCSTPIE+UCSTTIE, UCBxIE ; enable all self-clearing interrupts

USCI40 *USCI Module*

Function SPI Slave Transmit with clock phase select = 1

Description In SPI slave mode with clock phase select set to 1 (UCAxCTLW0.UCCKPH=1), after the first TX byte, all following bytes are shifted by one bit with shift direction dependent on UCMSB. This is due to the internal shift register getting pre-loaded asynchronously when writing to the USCIA TXBUF register. TX data in the internal buffer is shifted by one bit after the RX data is received.

Workaround Reinitialize TXBUF before using SPI and after each transmission.

If transmit data needs to be repeated with the next transmission, then write back previously read value:

```
UCAxTXBUF = UCAxTXBUF;
```

WDG4 *WDT Module*

Function The WDT failsafe can be disabled

Description The UCS is capable of masking clock requests (ACLK, SMCLK, MCLK) from peripheral modules; see request enable (REQEN) bits in the UCS control register, UCSCTL8.

The clock request logic of the UCS is used by the WDT module to ensure a fail-safe clock source in all low-power modes. Therefore, de-asserting the request enable bit of the watchdog clock source (xCLKREQEN = 0) allows the respective clock to be disabled upon entry into a low-power mode. Without an active clock source, the WDT timer stops incrementing and a watchdog event will not occur.

Workaround None

5 Document Revision History

Changes from family erratasheet to device specific erratasheet.

1. Errata RTC4 was removed
2. Errata EEM19 was added
3. Errata EEM21 was added
4. Errata USCI31 was added
5. "EEM8 is not impacting silicon revisions E

Changes from device specific erratasheet to document Revision A.

1. Errata DMA10 was added to the errata documentation.
2. Errata PORT19 was added to the errata documentation.
3. Errata PMM18 was added to the errata documentation.
4. Errata RTC6 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. DMA10 Workaround was updated.
2. DMA10 Description was updated.

Changes from document Revision B to Revision C.

1. Errata RTC3 was added to the errata documentation.
2. DMA10 Description was updated.

Changes from document Revision C to Revision D.

1. DMA10 Description was updated.
2. DMA10 Function was updated.

Changes from document Revision D to Revision E.

1. DMA10 Description was updated.
2. MPY1 Description was updated.
3. Errata EEM23 was added to the errata documentation.
4. Errata CPU43 was added to the errata documentation.

Changes from document Revision E to Revision F.

1. SYS16 Description was updated.
2. CPU43 Description was updated.
3. Device TLV Hardware Revision information added to erratasheet.

Changes from document Revision F to Revision G.

1. Errata PMM20 was added to the errata documentation.
2. Errata USCI35 was added to the errata documentation.

Changes from document Revision G to Revision H.

1. Errata UCS11 was added to the errata documentation.

Changes from document Revision H to Revision I.

1. EEM19 Workaround was updated.
2. EEM13 Workaround was updated.
3. EEM23 Workaround was updated.
4. EEM17 Description was updated.
5. EEM23 Description was updated.
6. EEM17 Workaround was updated.
7. PORT16 Workaround was updated.
8. CPU43 Description was updated.

9. EEM11 Workaround was updated.
10. EEM14 Workaround was updated.
11. EEM16 Description was updated.
12. PORT16 Description was updated.
13. EEM16 Workaround was updated.
14. EEM19 Description was updated.

Changes from document Revision I to Revision J.

1. DMA10 Workaround was updated.
2. DMA10 Description was updated.
3. DMA10 Function was updated.

Changes from document Revision J to Revision K.

1. CPU40 Workaround was updated.
2. EEM19 Workaround was updated.
3. Errata USCI39 was added to the errata documentation.
4. Package Markings section was updated.
5. EEM23 Workaround was updated.
6. EEM23 Description was updated.
7. Errata ADC42 was added to the errata documentation.
8. EEM23 Function was updated.
9. EEM19 Description was updated.

Changes from document Revision K to Revision L.

1. Errata USCI40 was added to the errata documentation.
2. Errata CPU43 was removed from the errata documentation.
3. PMM18 Workaround was updated.

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