

STUDIES ON RECTIFIERS AND POWER SUPPLY

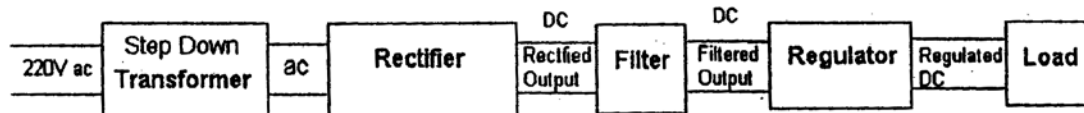


Fig.1 POWER SUPPLY BLOCK DIAGRAM

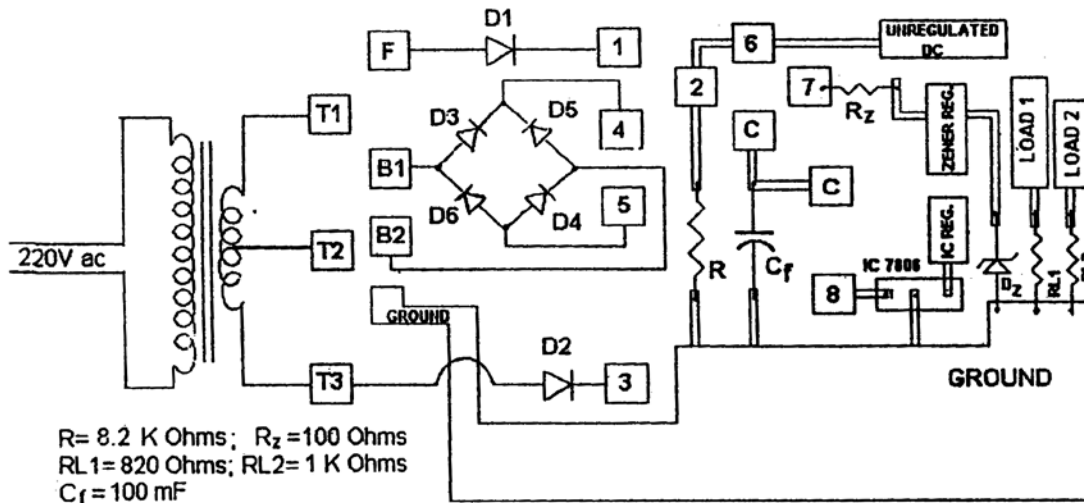


Fig.2 Circuit Board Layout.

EXPERIMENT :

1. Trace the circuit in the board. Locate in the board the various components shown in Fig.2. Identify in the given board the various blocks of Fig.1.
2. Observe (and record) the transformer secondary voltages between the terminals 'T1' & 'T2', 'T2' & 'T3', and between 'T1' and 'T3' using Oscilloscope.
3. Realize the half wave rectifier using the steps given in Note I (i) below.
4. Observe the rectified waveform across 'Unregulated DC' & 'Ground' using Oscilloscope.
5. Determine V_m and calculate $V_r(\text{rms})$ the rms value of the ac component (see Fig.3).
6. Switch the oscilloscope vertical input between ac and dc positions, observe the shift in the display and thereby obtain the dc component V_{dc} . A higher Volts/div may be needed to keep the shift within the screen. Measure V_{dc} using multimeter and compare.
7. Calculate the ripple factor $= V_r(\text{rms})/V_{dc}$.
8. Filter the rectified waveform using the steps given in Note II below.
9. Use the Oscilloscope to observe the ripple in the filtered output waveform. Using triangular waveform approximation obtain $V_r(\text{rms})$ the rms value of the ac component. Repeat steps 6 and 7 to get the ripple factor with capacitor filter.
10. Realize the full wave rectifier of Note I(ii) below. Repeat steps 4 to 9.
11. Realize the full wave Bridge rectifier of Note I(iii) below. Repeat steps 4 to 9.
12. **Voltage Regulation:**
 - (a) Make the half wave rectifier connections using Note I(i).
 - (b) Note that now the 'Unregulated DC' terminal is the 'Output' terminal. Obtain V_{NL} and V_{FL} using the steps given in Note III(i)-(iv).
 - (c) Calculate the voltage regulation $V.R. = (V_{NL} - V_{FL})/V_{FL}$.
 - (d) Realize the full wave rectifier using Note I(ii). Repeat steps 12(b) & 12(c).

P.T.O.

(e) Realize the Bridge rectifier using Note I(iii). Repeat steps 12(b) & 12(c).

(f) **Zener Diode Regulation:**

- (i) Obtain the full wave rectified and filtered voltage using Note I(ii) & II or I(iii) & II.
- (ii) Apply this voltage to the Zener Regulator by making the connections between terminals 'C' & '7'.
- (iii) The terminal 'Zener Regltd' is now the 'Output' terminal. Follow Note III(i)-(iv) to obtain V_{NL} and V_{FL} . Repeat step 12(c).

(g) **IC 7806 Regulation:**

- (i) Repeat steps 12(f)(i).
- (ii) Apply this voltage to the IC 7806 Regulator by connecting the terminals 'C' & '8'.
- (iii) The terminal 'IC Regltd' is now the 'Output' terminal. Follow Note III(i)-(iv) to obtain V_{NL} and V_{FL} . Repeat step 12(c).

NOTE:

I. **Rectifier Realizations:** Rectified output is obtained at the 'Unregulated DC' terminal, on making the following connections

- (i) **Half Wave:** Remove all connections. Join 'T1' & 'F', 'T2' & 'Ground', '1' & '2'.
- (ii) **Full Wave with center-tapped transformer:** Remove all connections. Join 'T1' & 'F', 'T2' & 'Ground', '3' & '1', '1' & '2'
- (iii) **Full Wave Bridge Rectifier:** Remove all connections. Join 'T1' & 'B1', 'T2' & 'B2', '5' & 'Ground', '4' & '2'.

II. **Filtering the Rectified Signal:** Connect the terminals '6' & 'C'. The filtered output is then available at the terminal 'Unregulated DC'.

III. **Output voltage across various Loads** is obtained as follows:

- (i) Measure voltage V_{NL} at the 'Output' terminal when no load is connected.
- (ii) Connect load R_{L1} by joining the terminals 'Load 1' and 'Output'. Measure the voltage at the 'Output' terminal.
- (iii) Disconnect R_{L1} . Connect load R_{L2} by joining the terminals 'Load 2' and the 'Output'. Measure the voltage at the 'Output' terminal.
- (iv) Apply full load by connecting together 'Load 1', 'Load 2', and 'Output'. Measure the full load voltage V_{FL} at the 'Output' terminal.

IV. **The ac readings** of the multimeter (or the ac millivoltmeter) is correct only for sinusoidal ac waveforms. The readings of these instruments will be in error when the input is half wave, or full wave or triangular wave.

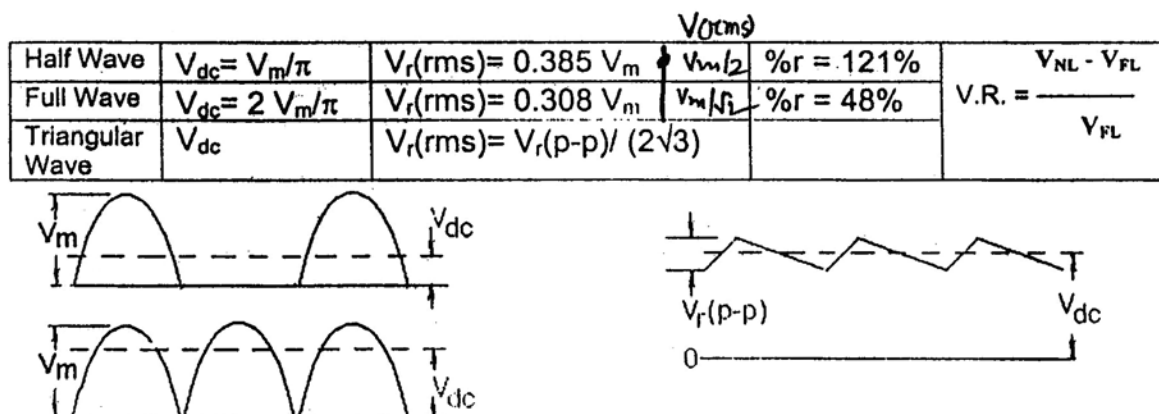


Fig.3

