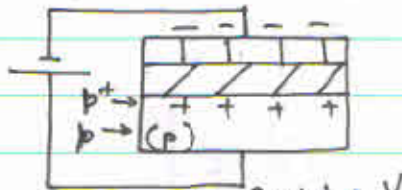
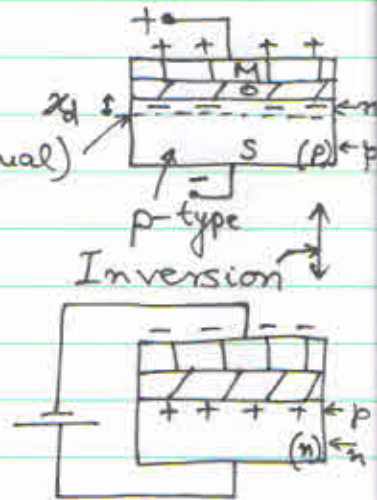
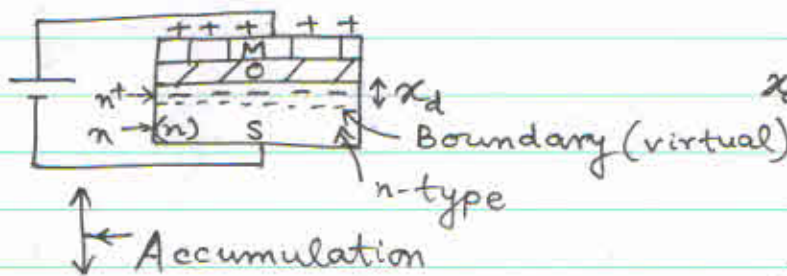
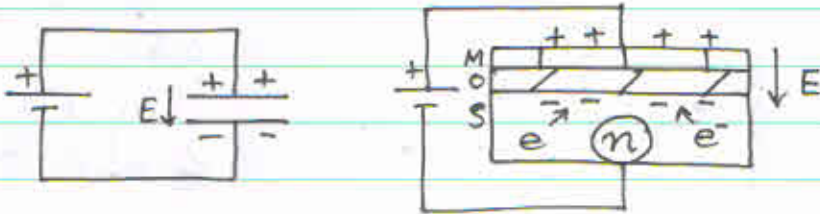
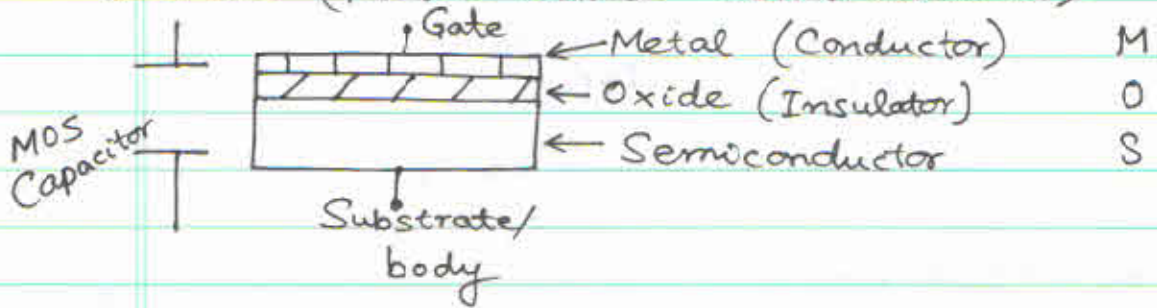
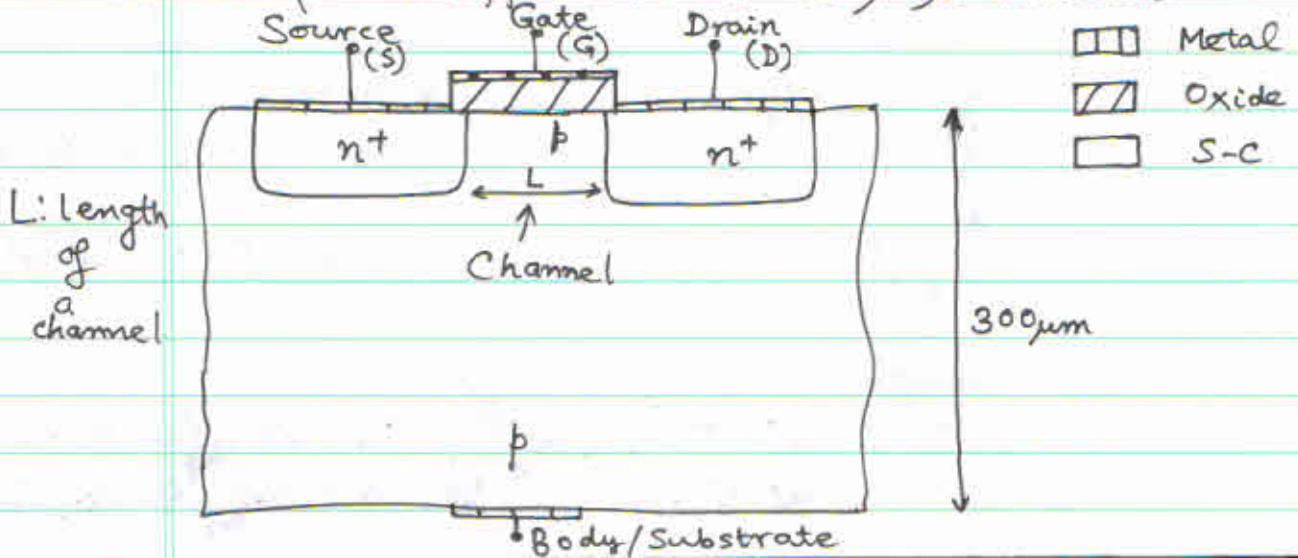


# FETs & MOSFETs

## 1. MOS (Metal Oxide Semiconductor):



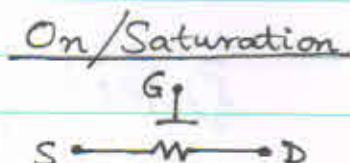
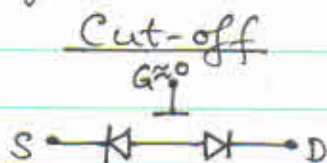
## 2. FET (Field Effect Transistor): a) Structure



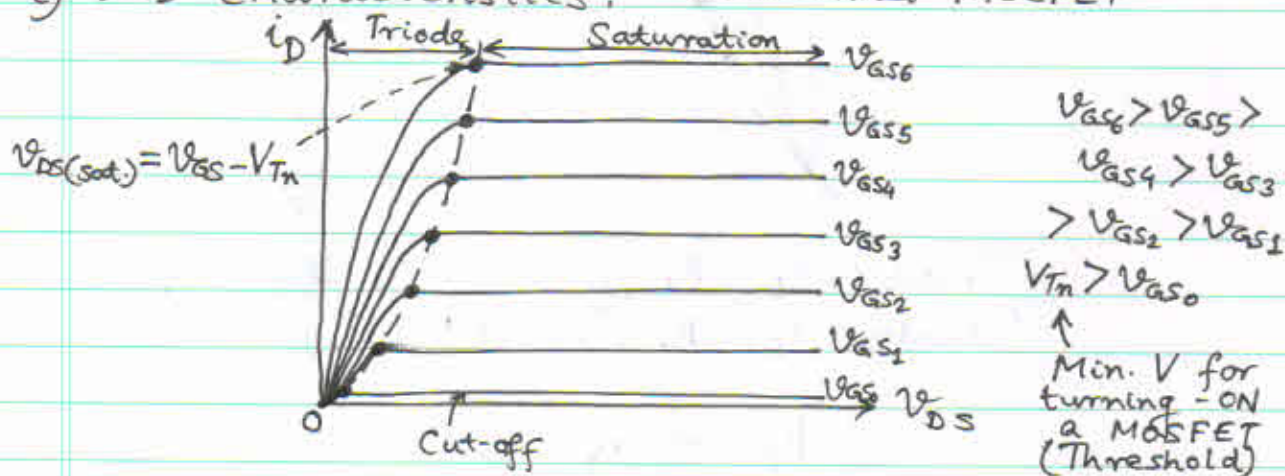
(Study the 3-D structure from the text book).

→ (or conductor)  
 Metal: Gold, aluminum, polysilicon  
 Oxide: Silicon di-oxide ( $\text{SiO}_2$ ) or silicon nitride ( $\text{Si}_3\text{N}_4$ )  
 → (or insulator)  
 Semiconductor: Silicon

b) Equivalent circuits: MOSFET



c) V-I characteristics: n-channel MOSFET



d) MOSFET equations (for <sup>drain</sup> current): n-channel

i) Triode/non-saturation:

$$I_D = \underbrace{\frac{1}{2} \cdot \frac{W}{L} \cdot \mu_n \cdot C_{ox}}_{\text{const.}} [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

$K_n$  (or transconductance parameter).

ii) Saturation:

$$I_D = K_n (V_{GS} - V_{TN})^2$$

$\mu_n$ : Mobility of  $e^-$

$C_{ox}$ : Gate oxide capacitance.

$W$ : Width of a MOSFET

$L$ : Channel length

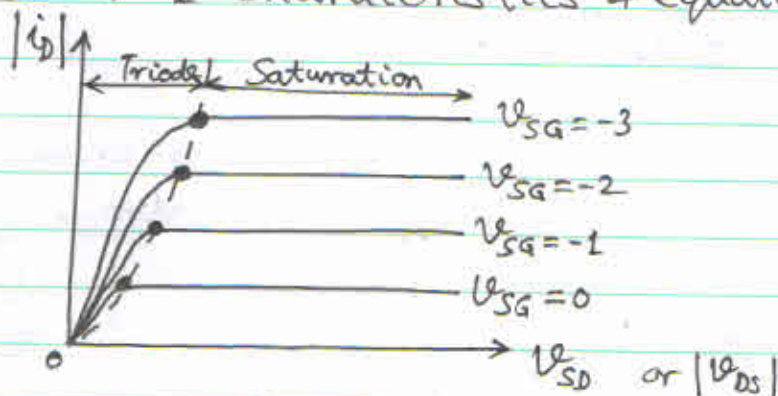
$V_{TN}$ : Threshold voltage (v-th)

e) MOSFET related equations:

$$r_o = \left. \frac{\Delta V_{DS}}{\Delta i_D} \right|_{V_{GS} = \text{const.}} = \infty \quad (\text{Small-signal resistance})$$

$$C_{ox} = \frac{\overset{\leftarrow E}{\epsilon_{ox}}}{\underset{\leftarrow d}{t_{ox}}} \quad (\text{Capacitance per unit area})$$

f) MOSFET V-I characteristics & equations: p-ch.



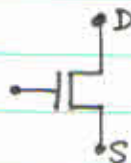
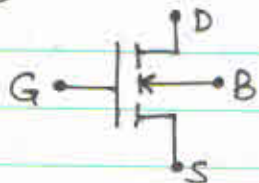
Triode:  $i_D = K_p [2(V_{SG} + V_{TP})V_{SD} - V_{SD}^2]$

Saturation:  $i_D = K_p (V_{SG} + V_{TP})^2$

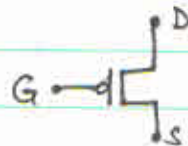
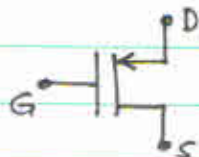
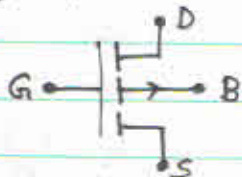
$$K_p = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W}{L}$$

h) Symbols: (Enhancement type MOSFETs)

i) n-channel

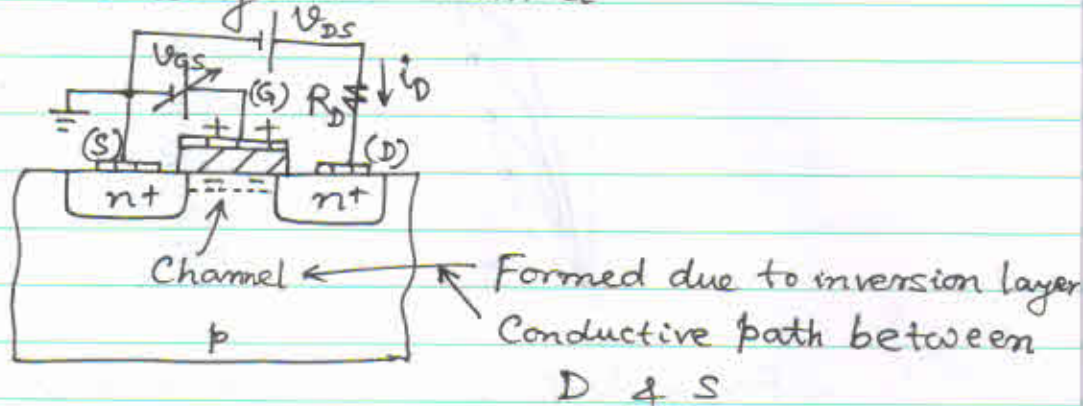


ii) p-channel



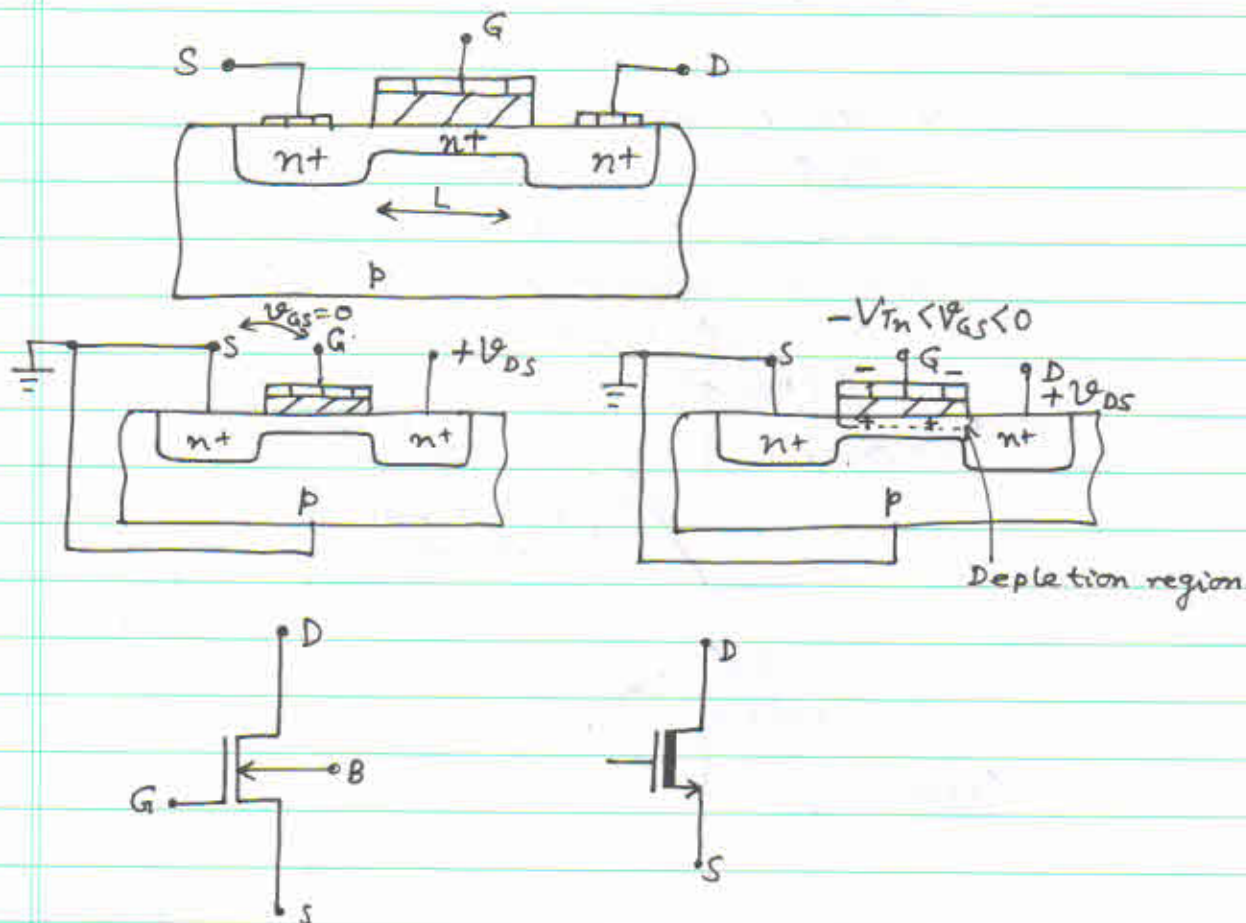


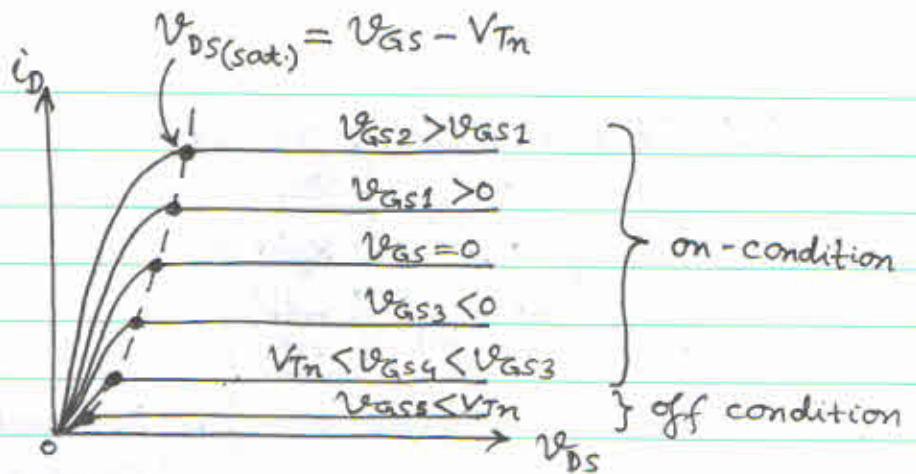
i) MOSFET biasing : n-channel



j) MOSFET types : 1) Enhancement (normally off-type)  
2) Depletion (normally on-type)

k) Depletion MOSFET: n-channel



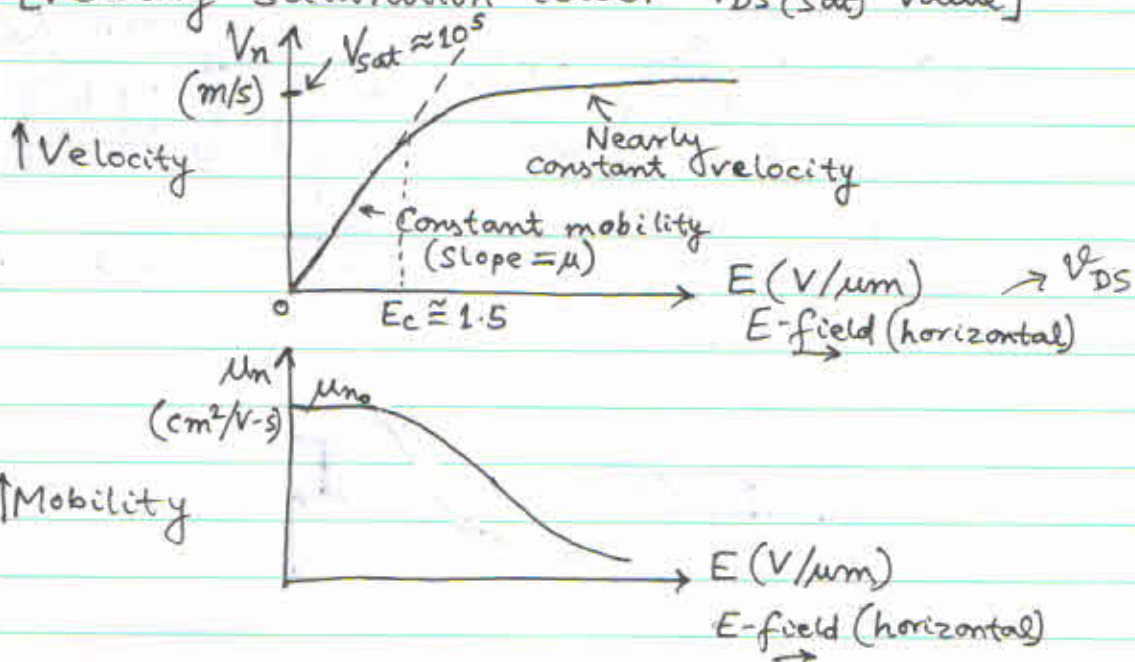


For a depletion mode n-channel MOSFET, a  $-v_{GS}$  below  $|V_{Tn}|$  turns 'off' the device. Otherwise, the MOSFET is naturally remains 'on'.

- i) Short-channel effects:  $L$  is reduced below  $2\mu m$
- 1)  $V_{Tn}$  depends on  $L$  &  $v_{DS}$  (directly proportional)
  - 2)  $\mu$  depends on  $E$ -field in the inversion layer. (vertical) (inversely proportional).

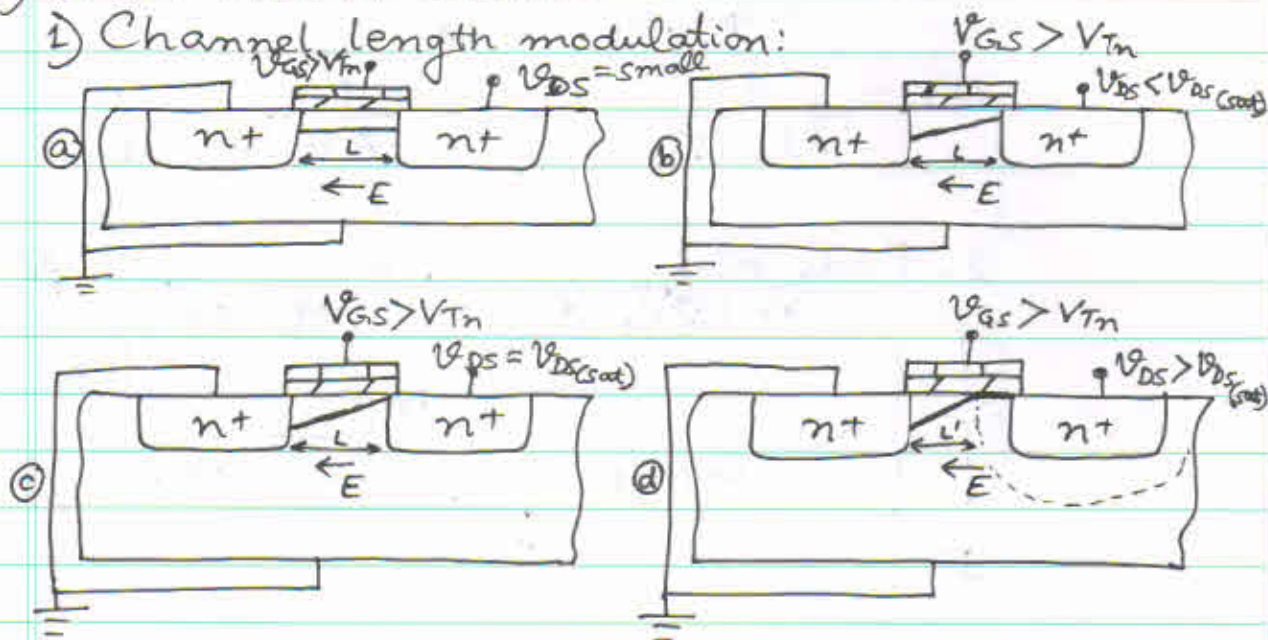
### 3) Velocity saturation:

$v_{DS} \uparrow$   $E$ -field (horizontal)  $\uparrow$  Velocity of carriers reaches a constant value (with further  $v_{DS} \uparrow$ )  
[Velocity saturation lower  $v_{DS}(sat)$  value]



m) Other MOSFET behavior:

1) Channel length modulation:

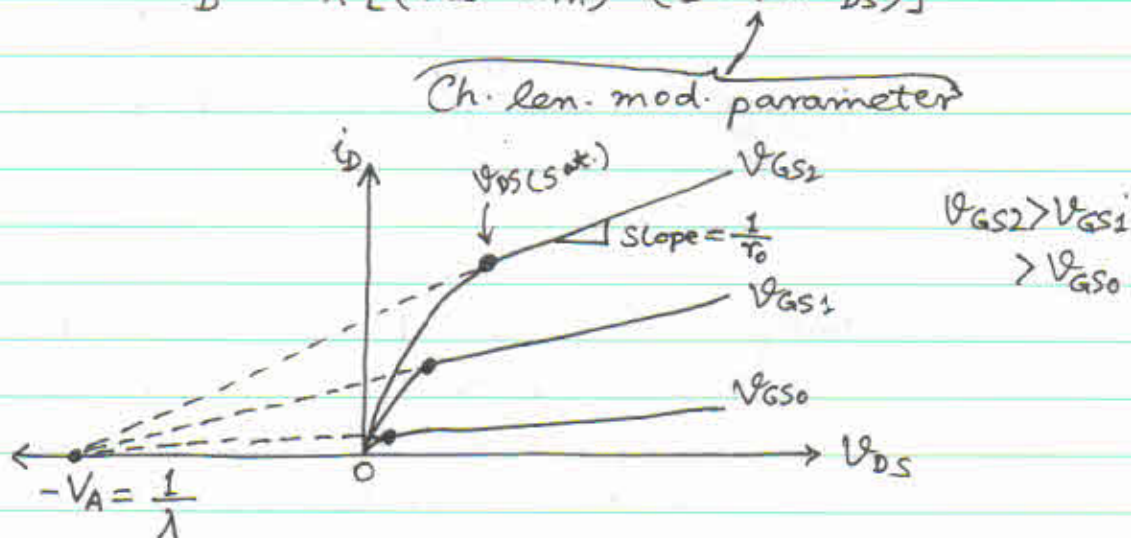


Regions of operation:

- Triode
- Triode
- Triode-saturation transition
- Saturation

The eq<sup>n</sup> for  $i_D$  is modified to: (due to channel length modulation)

$$i_D = K_n [(V_{GS} - V_{Tn})^2 (1 + \lambda \cdot V_{DS})]$$

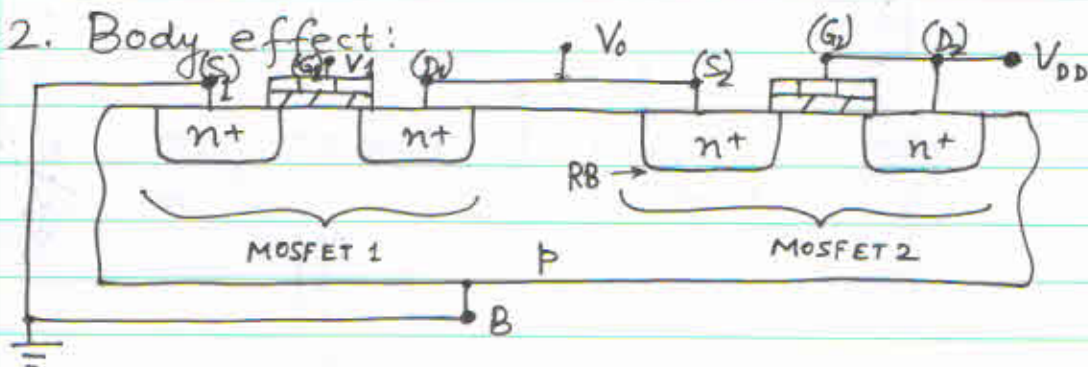




$$r_o = \left. \frac{\partial V_{DS}}{\partial I_D} \right|_{V_{GS} = \text{constant}}$$

$$\Rightarrow r_o = \frac{1}{\lambda \cdot K_n (V_{GS} - V_{Th})^2} = \frac{1}{\lambda \cdot I_{DQ}} = \frac{V_A}{I_{DQ}}$$

2. Body effect:



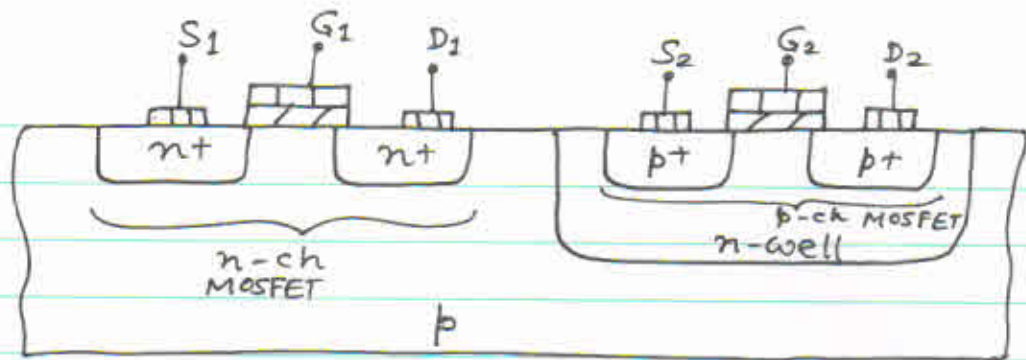
If, both the MOSFETs are conducting, the voltage at the (S<sub>2</sub>) of MOSFET 2 is not at 0V (or Gnd).  
 $\therefore V_{S2} \approx +ve V$

Junction between S<sub>2</sub> & B gets reverse biased (w.r.t. Gnd). This increases the  $V_{Th}$  of MOSFET 2, which is called a body effect (or  $V_T$  shift).

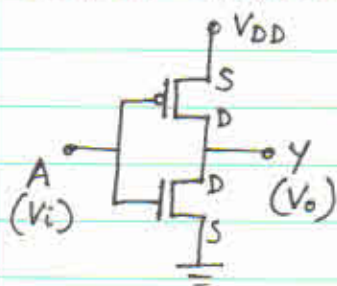
$$V_{Th} = V_{Th0} + \gamma \left[ \sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right]$$

Original threshold voltage  $\rightarrow V_{Th0}$   
 Body effect parameter  $\rightarrow \gamma$   
 Source to Body voltage  $\rightarrow V_{SB}$   
 Semiconductor parameter  $\rightarrow \phi_f$   
 $0.5V^{\frac{1}{2}}$   
 $\sim 0.35V$

n) Complementary MOSFETs: CMOS: NMOS + PMOS  
 $\hookrightarrow$  Uses both n-channel MOSFETs (NMOS) & p-channel MOSFETs (PMOS) together in an integrated circuit.



CMOS Inverter (NOT Gate) :



or

