Module 1 : Combinational Logic Circuits.

Assignment 3   Date: 28.01.2019

3. Suppose an n-bit Combinational ALU (n = 16 or 32 or 64) is to be designed using the bit-sliced architectural design methodology. Design and Test the i-th stage of such an ALU having two operand inputs and outputs supporting the following functions:

      Logical: AND, OR, NOT, NAND, NOR, XOR, EQUIVALENCE
      Arithmetic: ADD, SUBTRACT