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STUDIES ON LOGIC GATES:

AIM: To study logic gates

APPARATUS REQUIRED:

- Cathode Ray Oscilloscope
- Multimeter
- Connecting wires
- AC signal generator
- Printed circuit board
- DC power supply (5V)

THEORY:

Logic gates are elementary building blocks of ~~do~~ digital circuits. They can be binary (takes in two inputs) or unary (only one input. eg: NOT gate). Input can be • Low • High.

These are available in TTL (Transistor-Transistor Logic) or CMOS (Complementary metal-oxide silicon). TTL uses NPN and PNP BJTs and are utilised in this experiment for realising various logic gates.

A	B	AND $A \cdot B$	OR $A+B$	NAND $\overline{A \cdot B}$	NOR $\overline{A+B}$	XOR $A \cdot \bar{B} + \bar{A} \cdot B$	XNOR $\bar{A} \cdot \bar{B} + A \cdot B$
0	0	0	0	1	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	1	0	0	0	1

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I. LOGIC GATES USING ONLY NANDGATES :

All figures are in volts(V).

*) AND :

A		B		Y = A.B	
0	0	0	0	0.16	0
0	0	4.93	1	0.17	0
4.93	1	0	0	0.17	0
4.93	1	4.93	1	3.12	1

*) OR :

A		B		Y = A+B	
0	0	0	0	0.18	0
0	0	4.93	1	3.23	1
4.93	1	0	0	3.23	1
4.93	1	4.93	1	3.12	1

*) NOT : (Unary)

A		$Y = \bar{A}$	
0	0	3.12	1
4.93	1	0.12	0

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*) NOR gate :

A		B		$Y = \overline{A+B}$	
0	0	0	0	2.98	1
0	0	4.93	1	0.08	0
4.93	1	0	0	0.05	0
4.93	1	4.93	1	0.05	0

*) XOR gate :

A		B		$Y = \bar{A}.B + A.\bar{B}$	
0	0	0	0	0.08	0
0	0	4.90	1	2.96	1
4.90	1	0	0	2.98	1
4.90	1	4.90	1	0.08	0

XOR as controlled inverter :

1 KHz square waveform is applied to one of the inputs and the input is low (0V) or ~~Ip~~ invert. In this next table Invert input is kept high. Thus, the controlled inversion feature is realised.

i) Invert = Low :

A		B		Y	
0	0	0	0	0	0
1	1	0	0	0.84	1

ii) Invert = High :

A		B		Y	
0	0	4.93	1	0.82	1
1	1	4.93	1	0	0

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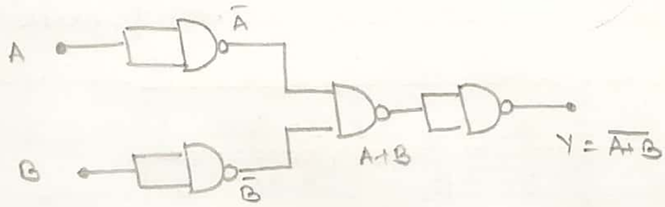
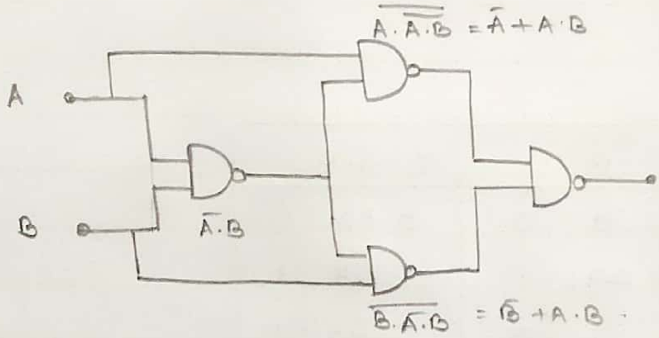


NAND gate



$$\overline{(\bar{A}+A\cdot B)\cdot(\bar{B}+\bar{A}\cdot B)}$$

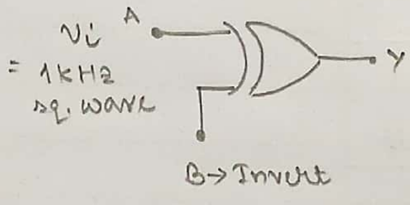
$$= A\cdot\overline{A\cdot B} + B\cdot\overline{A\cdot B}$$

$$= A\cdot(\bar{A}+\bar{B}) + B\cdot(\bar{A}+\bar{B})$$

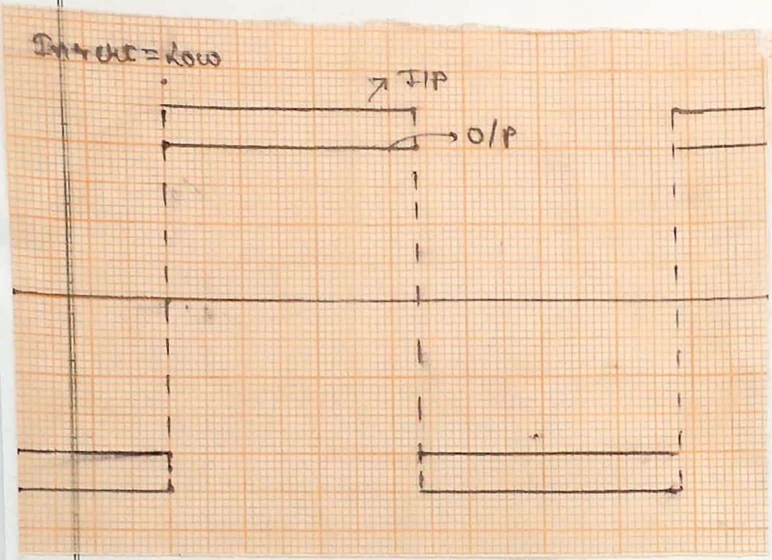
$$= A\cdot\bar{A} + A\cdot\bar{B} + B\bar{A} + B\cdot\bar{B}$$

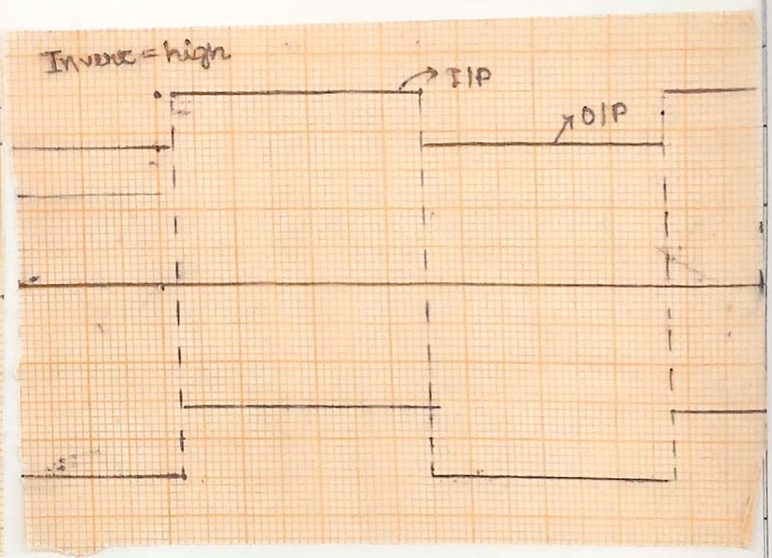
$$= A\cdot\bar{B} + B\cdot\bar{A}$$

XOR gate



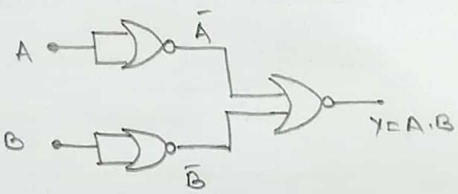
XOR as controlled inverter



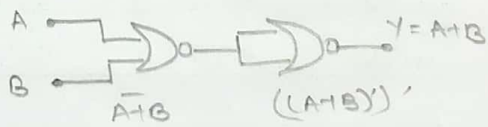


II) Different logic gates using only NOR gates:

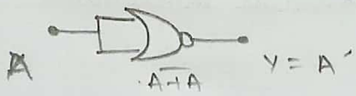
f = 300 Hz
V/div = 1V/div
T/div = 0.5 ms/div



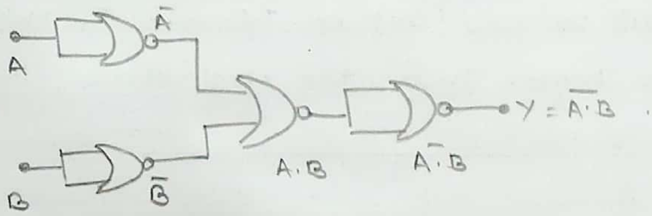
And gate



OR gate



NOT gate



NAND gate

II) LOGIC GATES USING ONLY NOR GATES:

*) AND:

A		B		Y = A·B	
0	0	0	0	0.16	0
0	0	4.93	1	0.17	0
4.93	1	0	0	0.17	0
4.93	1	4.94	1	3.13	1

*) OR:

A		B		Y = A+B.	
0	0	0	0	0.19	0
0	0	4.93	1	2.93	1
4.93	1	0	0	2.93	1
4.93	1	4.93	1	2.88	1

*) NOT:

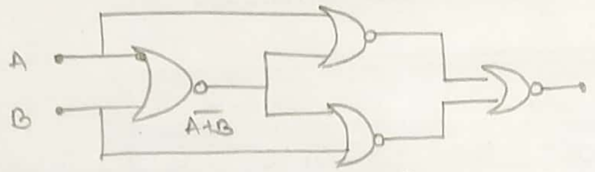
A		$Y = \bar{A}$	
0	0	2.93	1
4.93	1	0.17	0

*) NAND:

A		B		$Y = \overline{A \cdot B}$	
0	0	0	0	2.92	1
0	0	4.92	1	2.90	1
4.92	1	0	0	2.90	1
4.93	1	4.92	1	0.13	0

Teacher's Signature :

$(\overline{A+\overline{A+B}}) = \bar{A}\cdot A + \bar{A}\cdot B$



$Y = (\overline{\bar{A}\cdot B + \bar{B}\cdot A})$

$= (A+\bar{B})(B+\bar{A})$

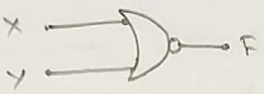
$= A\cdot B + \bar{B}\cdot\bar{A}$

$\bar{B}\cdot A + \bar{B}\cdot B$

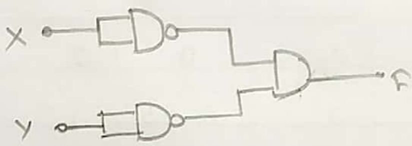
XNOR gate

III. Verification of De-morgan's Theorem:

a)

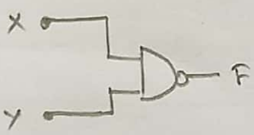


$F = (X+Y)'$

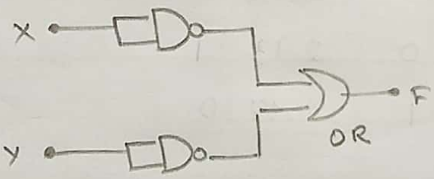


$F = X' . Y'$.

b)



$F = (X.Y)'$



$F = X' + Y'$.

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*) XNOR :

A		B		$Y = A\cdot\bar{B} + \bar{A}\cdot B$	
0	0	0	0	2.98	1
0	0	4.93	~~0~~1	0.16	0
4.92	1	0	0	0.16	0
4.92	1	4.92	1	2.89	1

III. VERIFICATION OF DE-MORGAN'S THEOREM :

a) $(X+Y)' = X'.Y'$

$(X+Y)'$ is realised with IC7402 and $X'.Y'$ using IC 7400 and IC 7408.

$F = (X+Y)'$						$F = X'.Y'$					
X		Y		C1 $(X+Y)'$		X		Y		C2 $X'.Y'$	
0~~0~~	0	0	0	3.10	1	0	0	0	0	2.41	1
0	0	4.91	1	0.16	0	0	0	4.82	1	0.27	0
4.90	1	0	0	0.17	0	4.90	1	0	0	0.21	0
4.93	1	4.93	1	0.17	0	4.91	1	4.89	1	0.23	0

Thus, comparing C1 and C2, we conclude
$(X+Y)' = X'.Y'$

$F = (X.Y)'$						$F = X'+Y'$					
X		Y		C3 $(X.Y)'$		X		Y		C4 $X'+Y'$	
0	0	0	0	2.73	1	0	0	0	0	2.41	1
0	0	4.89	1	2.86	1	0	0	4.71	1	2.83	1
4.85	1	0	0	2.85	1	4.70	1	0	0	2.83	0
4.92	1	4.93	1	0.16	0	4.70	1	4.70	1	0.21	0

comparing C3 and C4, $\therefore (X.Y)' = X'+Y'$

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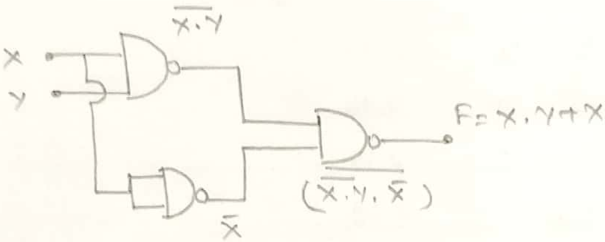
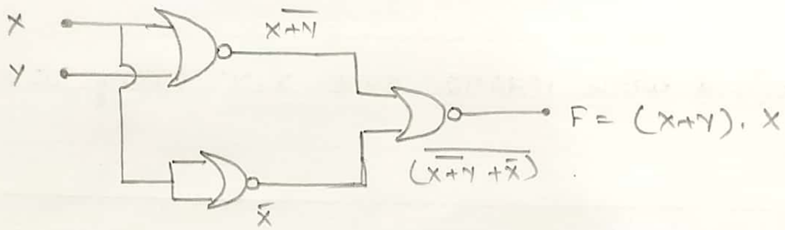
IV Verification of Theorems in Switching Algebra :

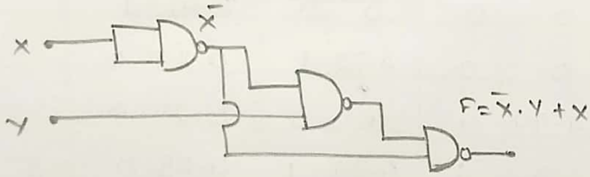
a)



b)

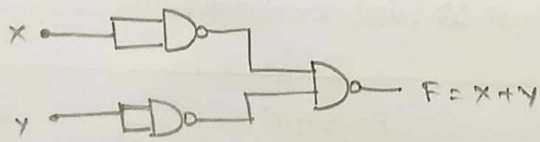


c)



$((\overline{\overline{\bar{X} \cdot Y}) \cdot \bar{X}})$

$= \bar{X} . Y + X$ (De-morgan's law)



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IV VERIFICATION OF THEOREMS IN SWITCHING ALGEBRA :

a) $F = X + X.Y$ and $F = X$

X		Y		C_1 $F = X + X.Y$		C_2 $F = X$	
0	0	0	0	0.26	0	0	0
0	0	4.89	1	0.35	0	0	0
4.89	1	0	0	3.87	1	4.88	1
4.89	1	4.88	1	3.89	1	4.88	1

Comparing C_1 and C_2, we conclude $X + X.Y = X$.

b) $F = X.(X+Y)$ and $F = X$

X		Y		C_3 $F = (X+Y).X$		C_4 $F = X$	
0	0	0	0	0.32	0	0	0
0	0	4.72	1	0.29	0	0	0
4.89	1	0	0	3.91	1	4.92	1
4.89	1	4.94	1	4.24	1	4.93	1

comparing C_3 and C_4 we conclude $X.(X+Y) = X$.

c) $F = X + X'.Y$ and $F = X + Y$

X		Y		C_5 $F = X + X'.Y$		C_6 $F = X + Y$	
0	0	0	0	0.16	0	0.19	0
0	0	4.92	1	2.92	1	3.23	1
4.92	1	0	0	2.93	1	3.23	1
4.93	1	4.92	1	2.99	1	3.12	1

Comparing C_5 and C_6 we conclude $X + X'Y = X + Y$

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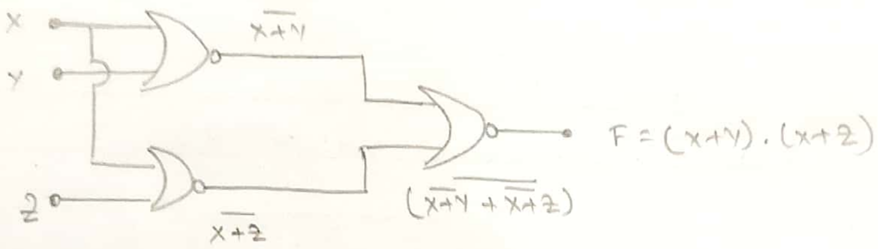
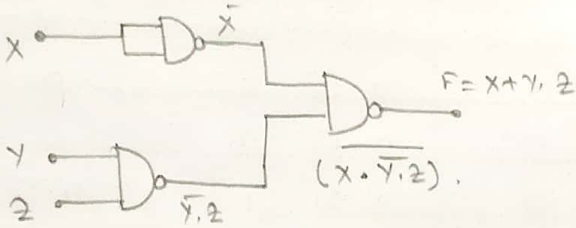
d)



x
y
z
$\overline{x+y}$
$\overline{x+z}$
$(\overline{\overline{x+y} + \overline{x+z}})$
$F = (x+y).(x+z)$



x
y
z
$\bar{x}$
$\overline{y.z}$
$(\overline{x.\overline{y.z}})$.
$F = x+y.z$

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d) $F = (X+Y) \cdot (X+Z)$ and $F = X + Y \cdot Z$

X		Y		Z		C1 $(X+Y)\cdot(X+Z)$	
0	0	0	0	0	0	0.45	0
0	0	0	0	4.92	1	0.20	0
0	0	4.93	1	0	0	0.25	0
0	0	4.04	1	4.92	1	3.39	1
4.94	1	0	0	0	0	3.12	1
4.93	1	0	0	4.93	1	3.32	1
4.94	1	4.92	1	0	0	3.01	1
4.94	1	4.92	1	4.92	1	3.02	1

X		Y		Z		C2 $X+Y\cdot Z$	
0	0	0	0	0	0	0.40	0
0	0	0	0	4.92	1	0.31	0
0	0	4.93	1	0	0	0.29	0
0	0	4.93	1	4.92	1	2.60	1
4.91	1	0	0	0	0	2.83	1
4.92	1	0	0	4.92	1	3.49	1
4.92	1	4.88	1	0	0	2.12	1
4.92	1	4.93	1	4.93	1	3.43	1

Comparing C1 and C2, we conclude that $(X+Y)\cdot(X+Z) = X + Y\cdot Z$.

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DISCUSSION :

Different logic gates were realised and verified in the circuit board using NAND and NOR gates. Representative logic gate diagrams were drawn. Since all other gates can be realised using NOR and NAND gates, they are also called 'universal gates'.

Then we observed function of XOR gate as controlled inverter. We get non-inverted O/P if invert is kept low and inverted O/P if invert is kept high.

We verified De-morgan's Theorems and we state the generalised theorem:

$$(A_1 + A_2 + \dots A_n)' = A_1' \cdot A_2' \cdot \dots A_n'$$

$$(A_1 \cdot A_2 \cdot \dots A_n)' = A_1' + A_2' + \dots A_n'.$$

Lastly, various Theorems in switching Algebra were proved using logic gates.

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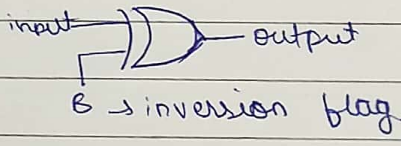
Discussion :-

By Chelsi Raheja
16CS10013

1. logic Gates are building blocks of digital circuits made by transistor - transistor logic (TTL) or complementary metal-oxide silicon (CMOS).

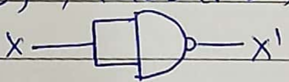
2. NAND and NOR gates are known as universal gates because gates like OR, AND, XOR can be obtained by combination of several NAND gates and NOR gates. This was realised during the experiment.

3. XOR was observed and used ~~to~~ as controlled invertor. by using the input at B to be 0 as inversion disabled and 1 as inversion enabled.



~~4.~~

4. De Morgan's Theorem was verified using 7408 (AND), 7432 (OR) 7400 (NAND), 7402 (NOR). Inversion was done using NAND gate



$$(A_1 + A_2 + A_3 + \cdots + A_n)' = A_1' \cdot A_2' \cdot A_3' \cdots A_n'$$

$$(A_1 \cdot A_2 \cdots A_n)' = A_1' + A_2' + A_3' + \cdots + A_n'$$

5 Verification of theorems in ~~it~~ switching algebra was proved and it can be concluded that complicated circuit giving ~~same~~ output can be deduced to much simpler circuit with same output like one of the input can be derived from combination of that input with another one. It can be used to derive an input out of their combination.

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