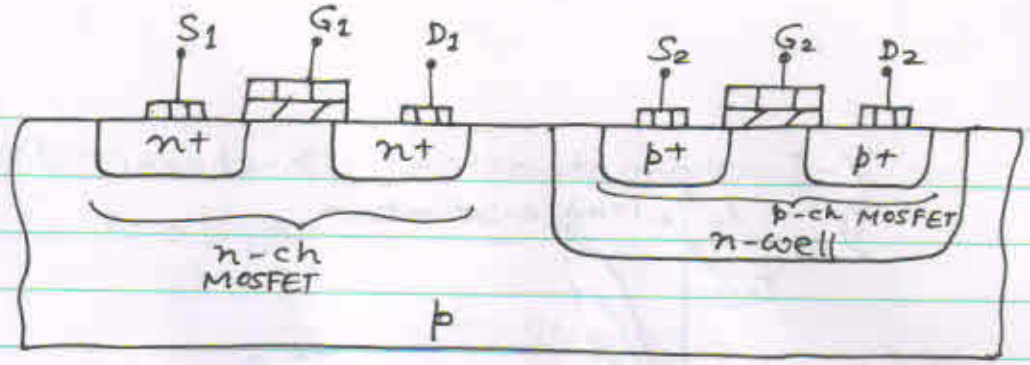
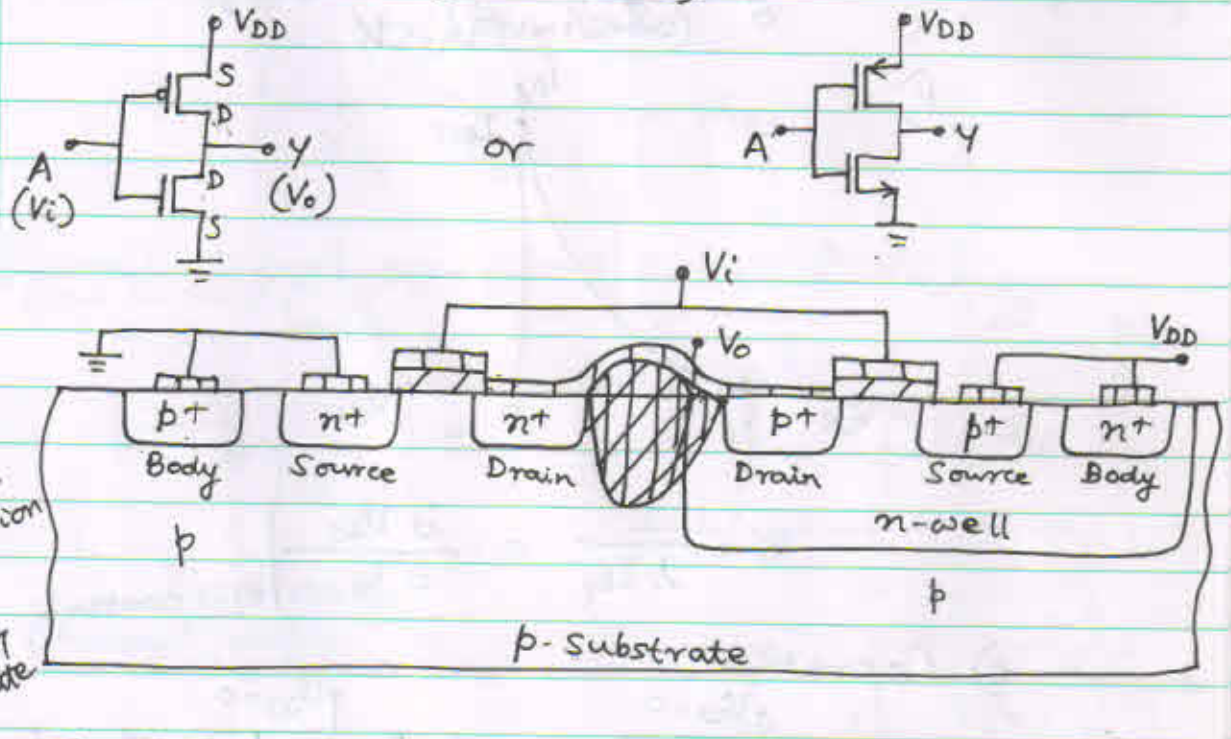
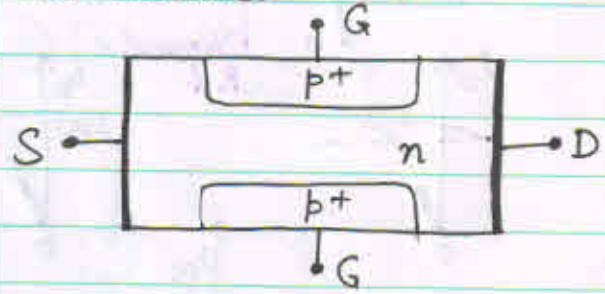


CMOS Inverter (NOT Gate):



3. Junction Field Effect Transistor (JFET):

a. Structure:



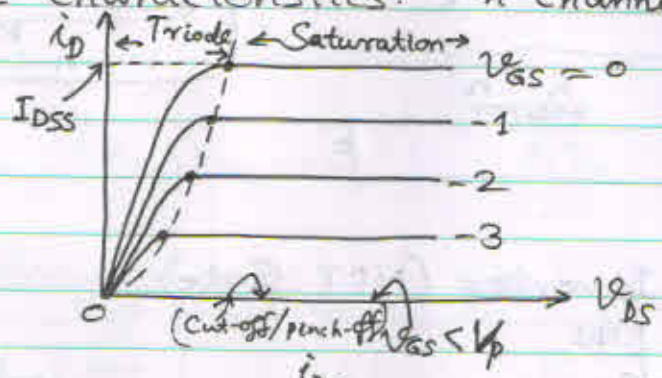
Symbol:

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS})$$

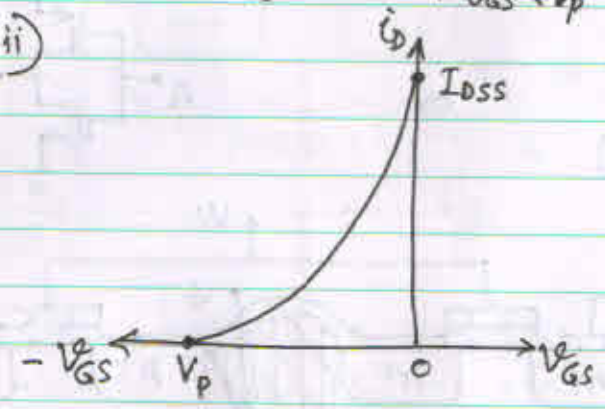
- I_D @ $v_{GS} = 0$
- V_P: Pinch-off voltage
- λ: Ch. len. modulation parameter

V-I characteristics: n-channel JFET

i)

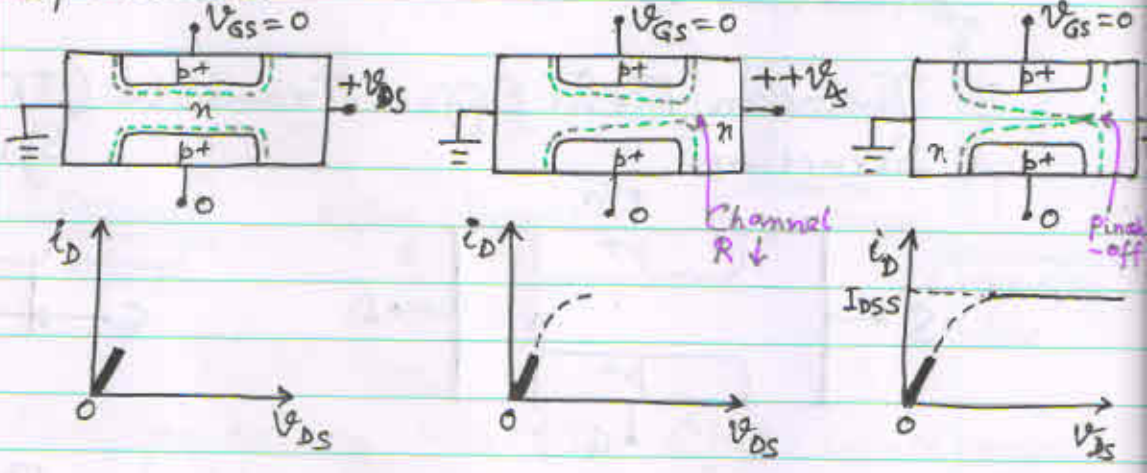


ii)



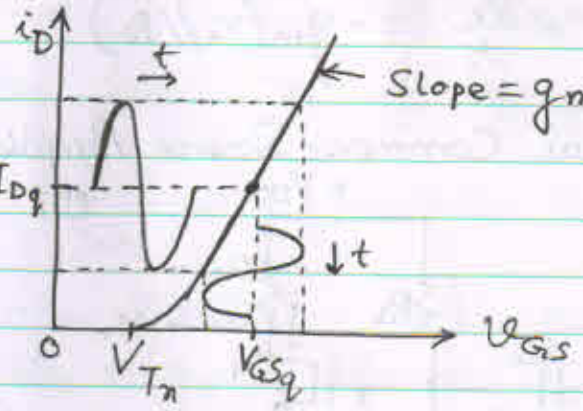
$$r_o = \frac{1}{\lambda I_{DQ}} = \left.\frac{\partial v_{DS}}{\partial i_D}\right|_{v_{GS}=\text{constant}}$$

b) Operation:



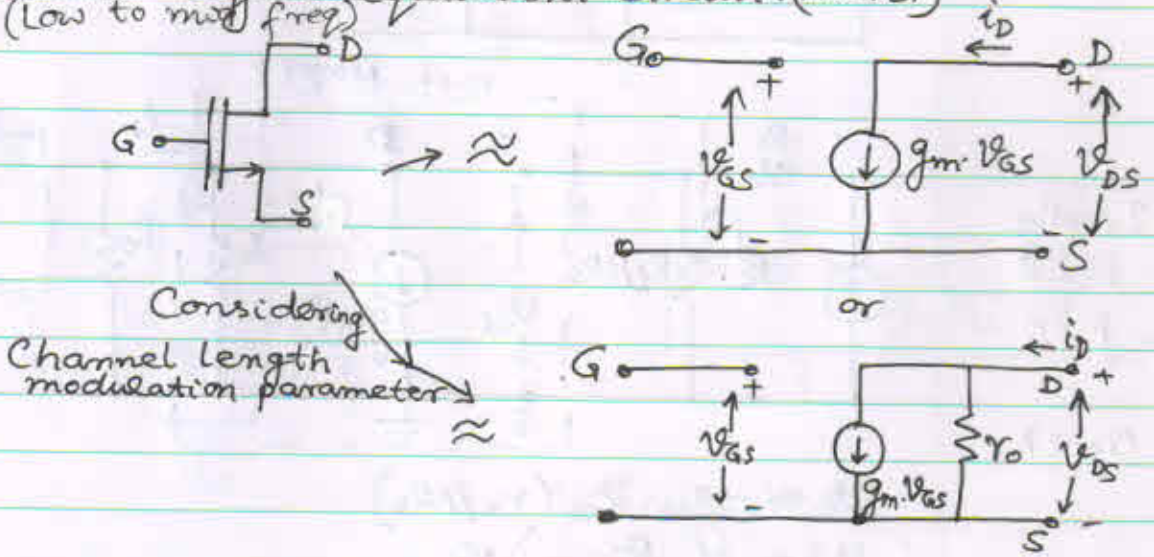
4.a. MOSFET amplifier: n-ch (common-source)

i_D Vs. v_{GS}

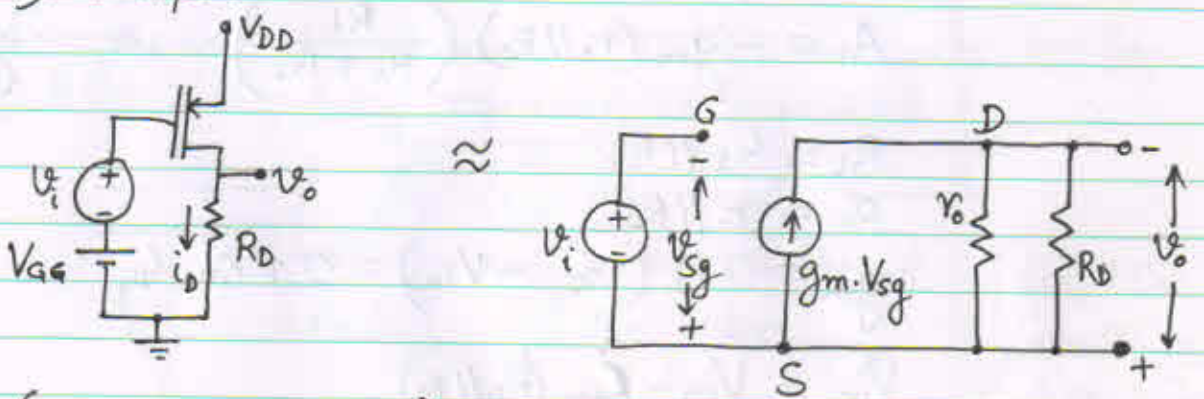


$$g_m = 2\sqrt{K_n I_{DQ}}$$

b. i) Small-signal equivalent circuit: (MOSFET)
(Low to mid freq)



ii) Example:



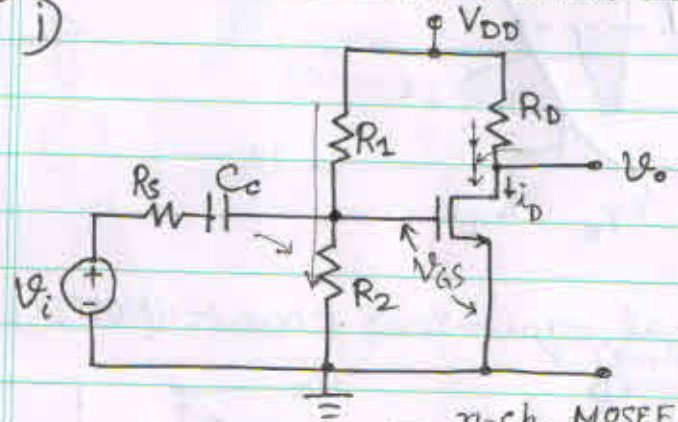
(Common-Source amp.)

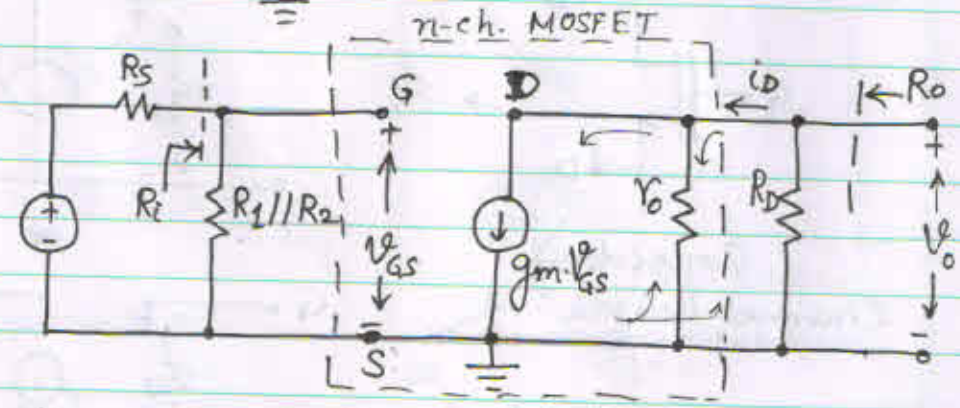
$$V_o = g_m \cdot V_{sg} (r_o // R_D) \qquad [\text{O/P V}]$$

$$A_v = \frac{v_o}{v_i} = -g_m (r_o // R_D) \qquad [\text{V-gain}]$$

c) Practical Common-Source Amplifier:

i)





Ideally:
$R_i \cong \infty$
$R \cong 0$

$r_o \to \infty$

$$v_o = -g_m \cdot v_{GS} (r_o // R_D)$$

$$v_{GS} = \left(\frac{R_i}{R_i + R_S}\right) v_i$$

$$A_v = -g_m (r_o // R_D) \left(\frac{R_i}{R_i + R_S}\right) \quad \text{or} \quad -g_m (r_o // R_D)$$

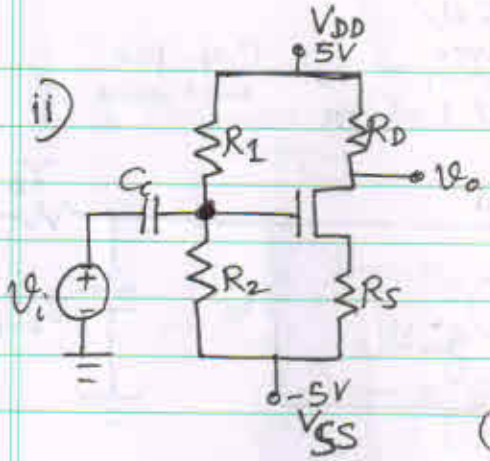
$$R_i = R_1 // R_2$$

$$R_o = r_o // R_D$$

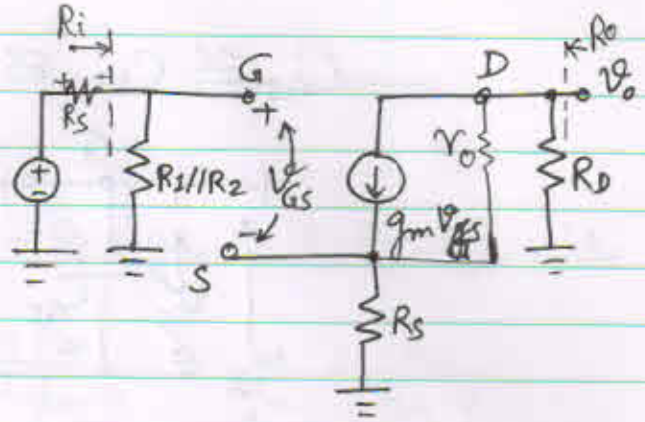
$$g_m = 2 K_n (V_{GS_Q} - V_{Tn}) = 2\sqrt{K_n \cdot i_{D_Q}}$$

$$V_{DS_Q} = V_{DD} - I_{D_Q} (R_D // r_o)$$

ii)



$\approx$



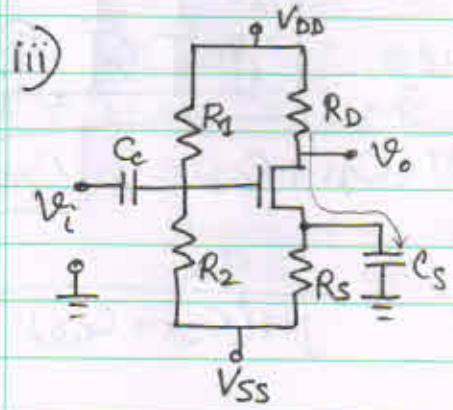
$(r_o//R_D)$ or

$v_o = -g_m \cdot v_{GS} (R_D)$ (or) $-g_m \cdot v_{GS} (R_D // r_o)$

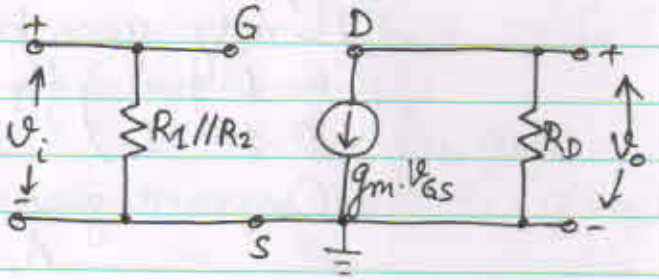
$v_i = v_{GS} + (g_m \cdot v_{GS}) R_S = v_{GS} (1 + g_m \cdot R_S)$

$$A_v = \frac{v_o}{v_i} = \frac{-g_m (R_D) \text{ or } (R_D // r_o)}{1 + g_m \cdot R_S} \cong -\frac{R_D}{R_S}$$

iii)



$\approx$

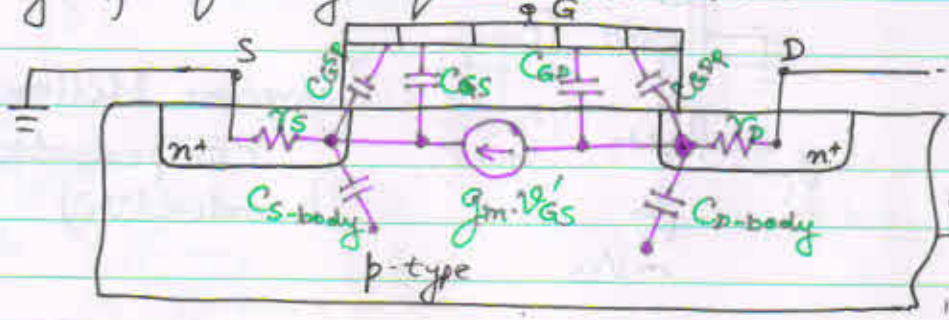


$v_o = -g_m \cdot v_{GS} \cdot R_D$

$A_v = -g_m \cdot R_D$

d) Frequency response of MOSFET circuits: High freq.

i) High frequency equivalent circuit:



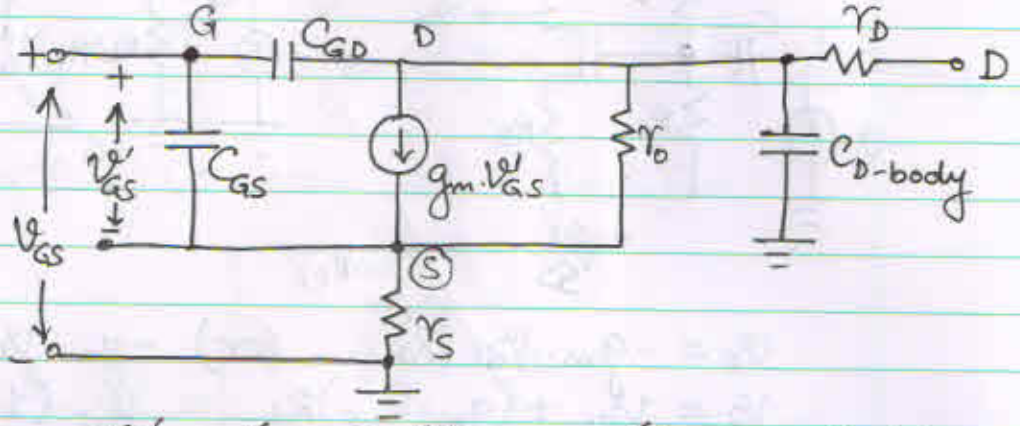
$C_{GS_p} \ll C_{GS}$

$C_{GD_p} \ll C_{GD}$

C_{GD_p} & C_{GS_p}

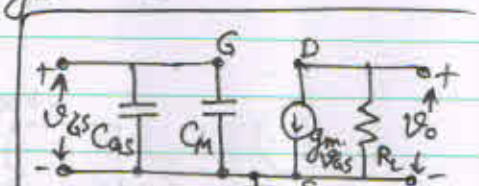
'p': Parasitic

$$C_{GS} \cong C_{GD} \cong \frac{1}{2} \overbrace{W.L}^{\text{Gate Area}} . C_{ox}$$ → Cap. per unit area



$$v_{GS} = v'_{GS} + (g_m . v'_{GS}) r_S = (1 + g_m . r_S) v'_{GS}$$

$$i_D = \left(\frac{g_m}{1 + g_m . r_S}\right) v_{GS} = g'_m . v_{GS}$$



$C_M = (1 + g_m . R_D) C_{GD}$

ii) Unity gain bandwidth:

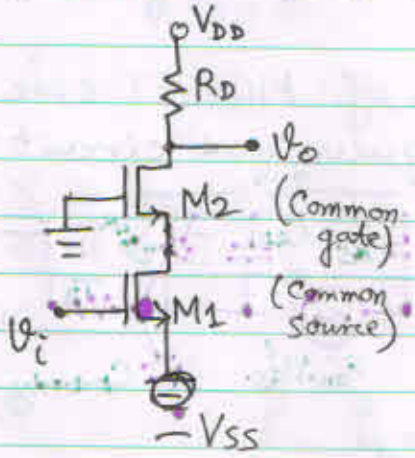
(Gain BW product @ gain = 1) $f_T = \dfrac{g_m}{2\pi(C_{GS} + C_{GD})}$

Current gain:

$$A_i = \frac{I_D}{I_i} \cong \frac{g_m}{j\omega(C_{GS} + C_{GD})}$$

e) Cascode circuit: Multi-stage amplifier:

i)

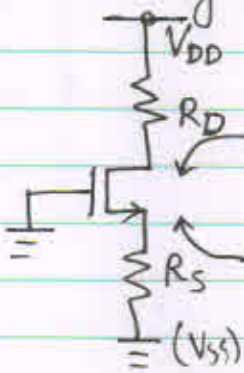


M1: Common source

M2: Common gate

Purpose: Miller capacitance compensation (increased bandwidth)

ii) Common gate : Impedance transformer:

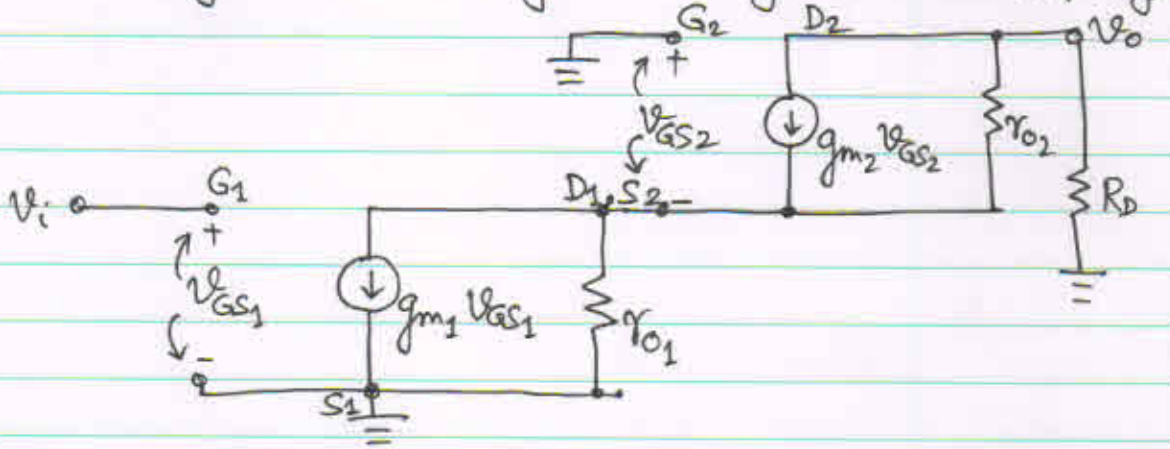


$$R_o = r_o + R_S + g_m \cdot r_o \cdot R_S \cong r_o + (g_m \cdot r_o) R_S$$

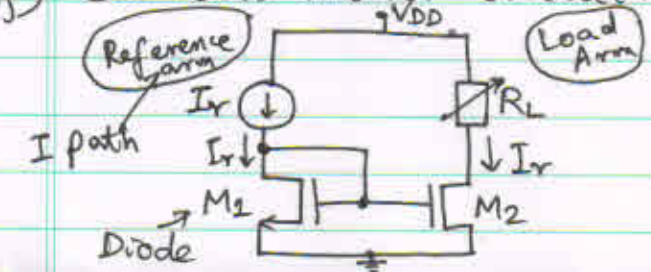
$$R_i = \frac{r_o + R_D}{1 + g_m \cdot r_o} \simeq \frac{1}{g_m} + \frac{R_D}{g_m \cdot r_o}$$

Looking into 'D': R_S increased (amplified) by $(g_m \cdot r_o)$
Looking into 's': R_D reduced by $(g_m \cdot r_o)$

i) continued
a) M_2 offers low R_i to M_1 (looking into 's' of M_2)
b) Gain of M_1 stage is reduced $\rightarrow C_{M_1} \downarrow \rightarrow f_T \uparrow$
c) M_2 compensates for gain (partially)
d) M_2 is unaffected by C_{M_2} since C_{M_2} gets charged & discharged through R_D & R_L (if any)



f) Current mirror circuit:



$I_{D_1} = I_{D_2}$
$V_{DS_1} \neq V_{DS_2}$