Module 3: Sequential Circuits and FSM

Assignment-1 Date: 11.03.2019

1. Design of flip-flops

   a) Implement a master-slave JK flip-flop using NAND gates, and verify its functionality.

   b) Configure it as a T flip-flop, and verify that it divides the frequency of an input pulse train by two.

   c) Implement D flip-flop using JK flip-flop (74LS73 / CD4027) and verify its functionality.

   d) Implement T flip-flop using D flip-flop (74LS74 / CD4013) and verify its functionality.