

25/3/21

HPCA - Short Test

Koushik
Roy
17CS30022

LD/ST - 2 cycles / 7 cycles
 ADD/SUB - 3 cycles
 MUL - 8 cycles
 BRANCH - 4 cycles

ROB Table

ROB	Type	Dest	Value	Done	Commit
ROB1	LD	R0	3	1	1
ROB2	MUL	R1	0	1	1
ROB3	ADD	R2	1	1	1
ROB4	SUB	R4	3	1	1
ROB5	MUL	R2	1	1	1
ROB6	ST	R4	-	1	1
ROB7	BNE	\emptyset	-	1	1
ROB8	LD	R0			
ROB9					
ROB10					
ROB11					
ROB12					

Instrn.

No.	Instrn	Issue	Exec	Write	Commit
1	LD R0 3(R2)	1/8	2	9	10
2	MUL R1 R0 R2	2/9	10	18	19
3	ADD R2 R1 R3	3/20	19	22	23
4	SUB R4 R0 R1	4/1	19	22	24
5	MUL R2 R2 R3	5/19	23	31	32
6	ST R4 3(R2)	6/	32	34	35
7	BNE R4 R2 1000	7/	23	X	36

LSQ

LS	Address	Value	Commit
LD	3		
ST	ROB5+3		
LD	3 + ROB5		

Reg File

R0	2
R1	0
R2	0
R3	1
R4	

RAT

R0	ROB1
R1	ROB2
R2	ROB3 ROB5
R3	
R4	

	Op	vj	vk	aj	ak	Dst Tag
MUL2	✓	3	0	ROB1		ROB2
MUL2	✓		1	ROB3		ROB5
ADD1	✓	0		ROB2		ROB3
ADD2	✓	3		ROB1	ROB2	ROB4