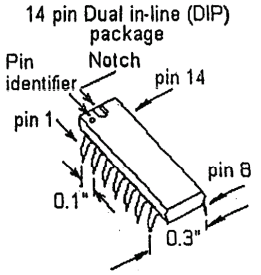
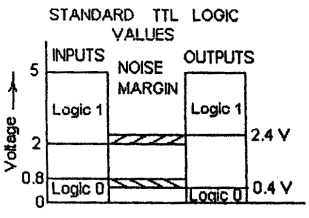
BASIC ELECTRONICS LABORATORY
EXPERIMENT NO: 6
STUDIES ON LOGIC GATES



A Note On the circuit layout: The board consists of 6 IC's. These are all quad two-input TTL logic gate IC's. The input/output pins of all IC's except 7402 (NOR) are same
These IC's are from top to bottom: 7408 (AND), 7432 (OR), 7400 (NAND), 7400 (NAND), 7402 (NOR), 7486 (XOR).



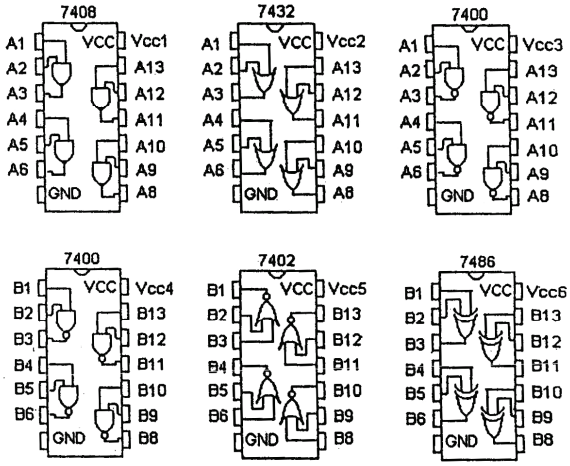
The **top (bottom) three** IC's form the group A (B) where each IC has its pins 1 to 6 connected to terminals **A1 to A6 (B1 to B6)** respectively. The pins 8 to 13 are connected to terminals **A8 to A13 (B8 to B13)** respectively.

Pin 7 of all six IC's are grounded. The V_{cc} pin 14 of each IC is individually connected to the respective terminals $V_{cc}1$ to $V_{cc}6$.

Applying a +5V supply to the V_{cc} pin of an IC activates (selects) it.

Logic Inputs: The available voltage for Logic High (Low) input is +5V (0V),

Caution: Atmost two IC may be selected simultaneously provided **only one** of the top A (bottom B) group of IC's 7408, 7432 or 7400 (group of IC's 7400, 7402 or 7486) is activated at any given time.



Experiment: In the following experiments consider all possible combinations of input logic levels. Note down in tabular form the measured voltages and then the corresponding logic levels. Connect the output to the LED input and then record the corresponding output voltage/logic levels. Thus obtain the truth table. Note that the LED lights up when the LED input is high. The Logic Gate diagrams below are drawn such that they have their inputs on the left and outputs on the right.

(I) Realize AND, OR, NOT, NOR, XOR logic elements using only NAND gates.

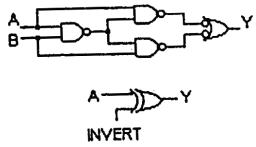
XOR gate as controlled inverter:

(i) Apply a 1 KHz (TTL compatible) square waveform to one of the inputs (A) of an XOR gate (which could be any one of the four XOR gates available in IC 7486).

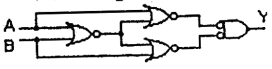
(ii) Keep the other input (instead of B lets call it INVERT) to the XOR gate low and compare the output (Y) and (A) input waveforms.

(iii) Keep the INVERT input high and compare the output (Y) and the (A) input waveforms. Observe the controlled inversion feature.

XOR Using NAND Gates



XNOR Using NOR Gates



(II) Realize AND, OR, NOT, NAND, XNOR logic elements using only NOR gates.

(III) **Verification of De Morgan's Theorems:** Implement the following:

(a) F= (X + Y)' using IC 7402 and compare with F= X' · Y' realized using IC 7400/7408.

(b) F= (X · Y)' using IC 7400 and compare with F= X' + Y' realized using ICs 7400/7432.

(IV) **Verification of Theorems in Switching Algebra:**

Realize

(a) F= X + X · Y using IC 7400 and compare with F= X.

(b) F= X · (X + Y) using IC 7402 and compare with F= X.

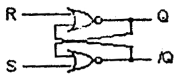
(c) F= X + X' · Y using IC 7400 and compare with F= X + Y realized using IC 7400.

(d) F= (X + Y) · (X + Z) using IC 7400 and compare with F= X + Y · Z realized using IC 7400.

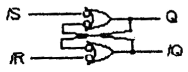
P.T.O.

(V) **LATCHES:**

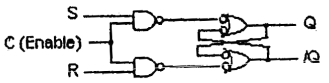
(a) Realize the S, R latch using IC 7402. Obtain the truth table.
(i) Apply S= 1, R= 1 and determine Q=?, /Q= ?.
(ii) Next apply S=0,R=0 and determine the new outputs Q=?,/Q=?.
(iii) Repeat steps (i), (ii) with variations of the sequence in which S=0, R=0 is applied. Explain the results.



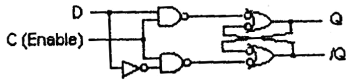
(b) Realize the /S, /R latch using IC 7400. Obtain the truth table.
(i) Apply /S= 0, /R= 0 and determine Q= ?, /Q= ?.
(ii) Next apply /S=1, /R=1 and determine the new outputs Q=?, /Q=?.
(iii) Repeat steps (i), (ii) with variations of the sequence in which /S=1, /R=1 is applied. Explain the results.



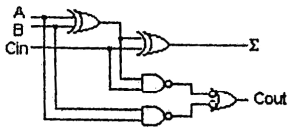
(c) Realize the S, R latch with enable using IC 7400. Obtain the truth table.
(i) Observe the outputs for the following sequence of inputs: C=0, S=1, R=1; C=1, S=1, R=1; and then C=0, S=1, R=1.
(ii) Repeat step (i) and explain your results.

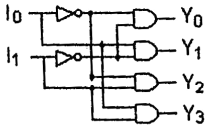


(d) Realize the D latch using ICs 7400.



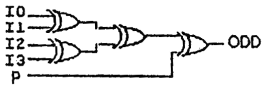
(VI) Realize the Full Adder using IC 7400 and IC 7486.	(VII) Realize the 2 to 4 Decoder using IC 7408 and IC 7400.

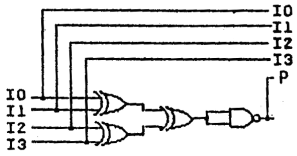




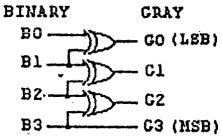
(VIII) **Parity Generator/Checker:** Error detecting codes use an extra bit called parity bit, to detect errors in the transmission and storage of data. In an Odd Parity code, the parity bit (P) is chosen so that the total number of 1 bits in a code word is odd.

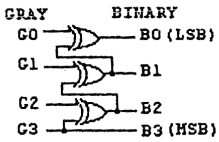
(a) Realize an Odd Parity Checker for a 5 bit input word using IC 7486.	(b) Realize a Parity generator if the parity of the 5 bit code I0, I1, I2, I3 & P is Odd independent of the 4 bit input word.



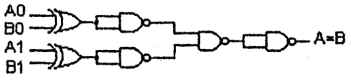


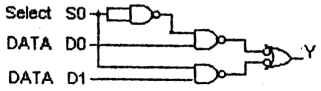
(IX) Realize 4 bit binary to Gray code conversion logic using IC 7486.	(X) Realize 4 bit Gray code to binary conversion logic using IC 7486.

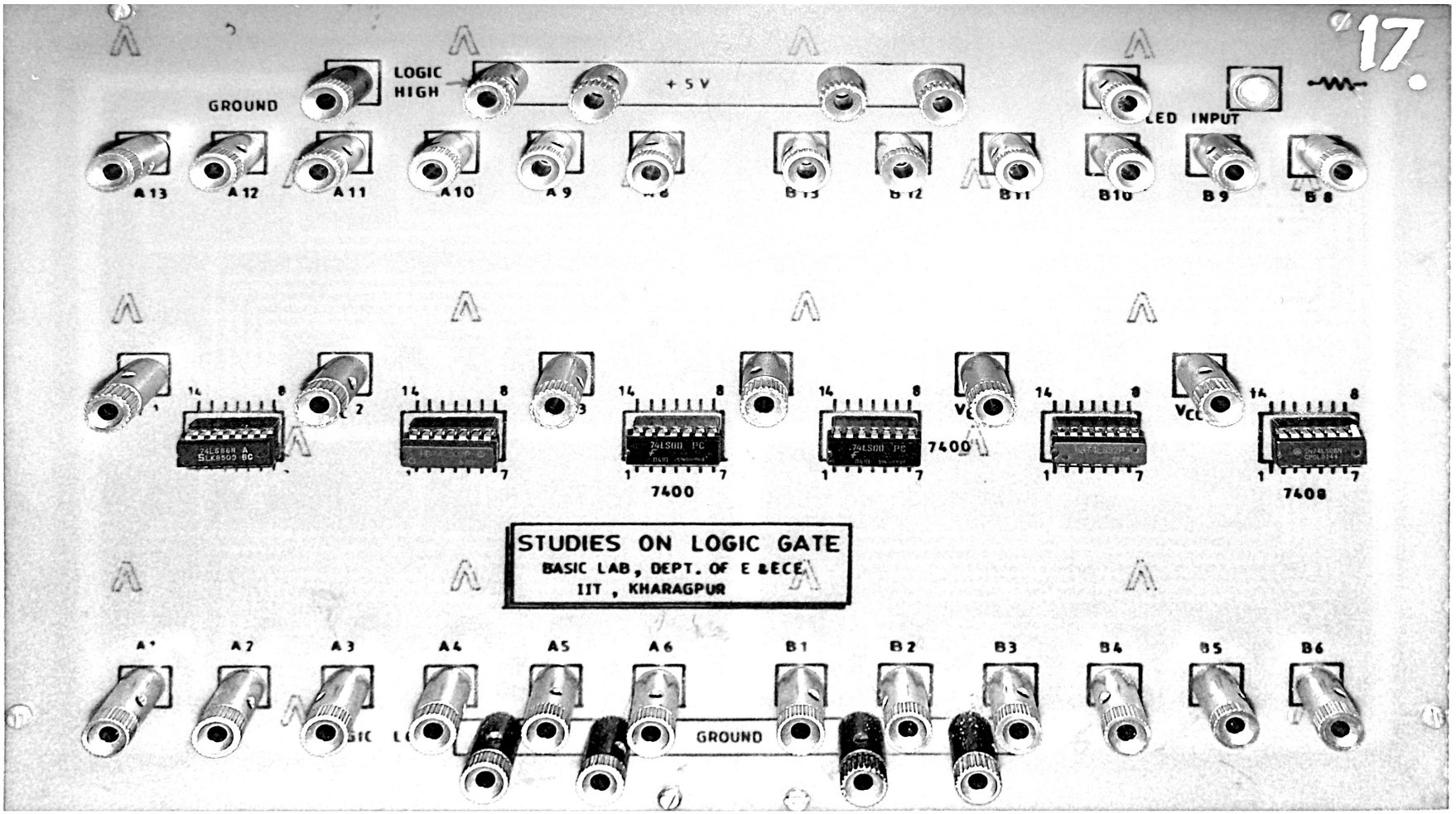




(XI) **Comparators:** Realize using IC 7486 and IC 7400 a logic circuit to compare binary numbers containing two bits.	(XII) **Multiplexer (data selector):** Realize the 2- input multiplexer using IC 7400






17.
GROUND
LOGIC HIGH
+5V
LED INPUT
A13
A12
A11
A10
A9
B11
B10
B9
B8
7400
7400
7400
STUDIES ON LOGIC GATE
BASIC LAB, DEPT. OF E &ECE
IIT , KHARAGPUR
A1
A2
A3
A4
A5
A6
B1
B2
B3
B4
B5
B6
GROUND