Tutorial - II (ROB and LSQ)

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Reorder Buffer Example

Sequence	Instruction	Operands		
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R4	R1	R2

Consider the above instruction set compromising of 6 instructions. Assume there are two independent execution units for ADD/SUB and MUL/DIV with a 3-entry and 2-entry reservation station per unit respectively. The Reorder Buffer can hold upto 6 instructions. The instructions are issued and committed in order. Fill up the table with the cycle number of each operation for all the instructions under these assumptions.

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
ARF: Architected Register File
RAT: Register Allocation Table

Cycle Number 0

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

Register Allocation Table (RAT)

R1	
R2	
R3	
R4	
R5	
R6	
R7	
R8	

ROB Table

Entry	Inst	Dst	Value	Done
ROB1				
ROB2				
ROB3				
ROB4				
ROB5				
ROB6				

Cycle Table

Inst	Issue	Exec	Write	Commit
1				
2				
3				
4				
5				
6				

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
ARF: Architected Register File
RAT: RegisterAlias Table

Cycle Number **1**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	DIV	ROB1	45	5			

Values in registers

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	
R2	ROB1
R3	
R4	
R5	
R6	
R7	
R8	

ROB Table

Entry	Type	Dst	Value	Done
ROB1	DIV	R2		
ROB2				
ROB3				
ROB4				
ROB5				
ROB6				

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1			
2				
3				
4				
5				
6				

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **2**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	DIV	ROB1	45	5			

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB2
R2	ROB1
R3	
R4	
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2				
ROB3				
ROB4				
ROB5				
ROB6				

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2			
3				
4				
5				
6				

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
ARF: Architected Register File
RAT: RegisterAlias Table

Cycle Number **2**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

RS for MUL/DIV

	Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
		MUL	ROB2	3	4			

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB2
R2	ROB1
R3	
R4	
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2	MUL	R1		
ROB3				
ROB4				
ROB5				
ROB6				

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2			
3				
4				
5				
6				

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **3**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	ADD	ROB3	1	2			

RS for MUL/DIV

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB2
R2	ROB1
R3	ROB3
R4	
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2	MUL	R1	12	
ROB3	ADD	R3		
ROB4				
ROB5				
ROB6				

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2	3	13	
3	3			
4				
5				
6				

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **4**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	MUL	ROB4			ROB2	ROB3	

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB4
R2	ROB1
R3	ROB3
R4	
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2	MUL	R1	12	
ROB3	ADD	R3	3	
ROB4	MUL	R1		
ROB5				
ROB6				

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2	3	13	
3	3	4	5	
4	4			
5				
6				

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **5**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	SUB	ROB5		3	ROB4		

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	MUL	ROB4		3	ROB2		

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB4
R2	ROB1
R3	ROB3
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2	MUL	R1	12	
ROB3	ADD	R3	3	✓
ROB4	MUL	R1		
ROB5	SUB	R4		
ROB6				

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2	3	13	
3	3	4	5	
4	4			
5	5			
6				

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **6**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	SUB	ROB5		3	ROB4		
	ADD	ROB6			ROB5	ROB1	

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	MUL	ROB4		3	ROB2		

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	ROB1
R3	ROB3
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2	MUL	R1	12	
ROB3	ADD	R3	3	✓
ROB4	MUL	R1		
ROB5	SUB	R4		
ROB6	ADD	R1		

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2	3	13	
3	3	4	5	
4	4			
5	5			
6	6			

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **13**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	SUB	ROB5		3	ROB4		
	ADD	ROB6			ROB5	ROB1	

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	MUL	ROB4	12	3			

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	ROB1
R3	ROB3
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2	MUL	R1	12	✓
ROB3	ADD	R3	3	✓
ROB4	MUL	R1	36	
ROB5	SUB	R4		
ROB6	ADD	R1		

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2	3	13	
3	3	4	5	
4	4			
5	5			
6	6			

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **14**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	SUB	ROB5		3	ROB4		
	ADD	ROB6			ROB5	ROB1	

RS for MUL/DIV

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	ROB1
R3	ROB3
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2	MUL	R1	12	✓
ROB3	ADD	R3	3	✓
ROB4	MUL	R1	36	
ROB5	SUB	R4		
ROB6	ADD	R1		

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2	3	13	
3	3	4	5	
4	4	14	24	
5	5			
6	6			

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
ARF: Architected Register File
RAT: Register Allocation Table

Cycle Number **24**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	SUB	ROB5	36	3			
	ADD	ROB6			ROB5	ROB1	

RS for MUL/DIV

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	ROB1
R3	ROB3
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2	MUL	R1	12	✓
ROB3	ADD	R3	3	✓
ROB4	MUL	R1	36	✓
ROB5	SUB	R4	33	
ROB6	ADD	R1		

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2	3	13	
3	3	4	5	
4	4	14	24	
5	5			
6	6			

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **25**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	ADD	ROB6			ROB5	ROB1	

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	ROB1
R3	ROB3
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2	MUL	R1	12	✓
ROB3	ADD	R3	3	✓
ROB4	MUL	R1	36	✓
ROB5	SUB	R4	33	
ROB6	ADD	R1		

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2	3	13	
3	3	4	5	
4	4	14	24	
5	5	25	26	
6	6			

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **26**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	ADD	ROB6		33	ROB1		

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	ROB1
R3	ROB3
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	
ROB2	MUL	R1	12	✓
ROB3	ADD	R3	3	✓
ROB4	MUL	R1	36	✓
ROB5	SUB	R4	33	✓
ROB6	ADD	R1		

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2	3	13	
3	3	4	5	
4	4	14	24	
5	5	25	26	
6	6			

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **42**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp
	ADD	ROB6	33	9			

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	-23
R2	16
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	ROB1
R3	ROB3
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	DIV	R2	9	✓
ROB2	MUL	R1	12	✓
ROB3	ADD	R3	3	✓
ROB4	MUL	R1	36	✓
ROB5	SUB	R4	33	✓
ROB6	ADD	R1		

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	
2	2	3	13	
3	3	4	5	
4	4	14	24	
5	5	25	26	
6	6			

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **43**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	-23
R2	9
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	~~ROB1~~
R3	ROB3
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1	~~DIV~~	~~R2~~	~~9~~	✓
ROB2	MUL	R1	12	✓
ROB3	ADD	R3	3	✓
ROB4	MUL	R1	36	✓
ROB5	SUB	R4	33	✓
ROB6	ADD	R1	42	

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	43
2	2	3	13	
3	3	4	5	
4	4	14	24	
5	5	25	26	
6	6	43	44	

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **44**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	12
R2	9
R3	45
R4	5
R5	3
R6	4
R7	1
R8	2

Register Alias Table (RAT)

R1	ROB6
R2	
R3	ROB3
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1				
ROB2	MUL	R1	12	✓
ROB3	ADD	R3	3	✓
ROB4	MUL	R1	36	✓
ROB5	SUB	R4	33	✓
ROB6	ADD	R1	42	✓

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	43
2	2	3	13	44
3	3	4	5	
4	4	14	24	
5	5	25	26	
6	6	43	44	

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **45**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

RS for MUL/DIV

	Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	12
R2	9
R3	3
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	
R3	~~ROB3~~
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1				
ROB2				
ROB3	ADD	R3	3	✓
ROB4	MUL	R1	36	✓
ROB5	SUB	R4	33	✓
ROB6	ADD	R1	42	✓

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	43
2	2	3	13	44
3	3	4	5	45
4	4	14	24	
5	5	25	26	
6	6	43	44	

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **46**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	36
R2	9
R3	3
R4	5
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	
R3	
R4	ROB5
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1				
ROB2				
ROB3				
ROB4	MUL	R1	36	✓
ROB5	SUB	R4	33	✓
ROB6	ADD	R1	42	✓

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	43
2	2	3	13	44
3	3	4	5	45
4	4	14	24	46
5	5	25	26	
6	6	43	44	

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **47**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	36
R2	9
R3	3
R4	33
R5	3
R6	4
R7	1
R8	2

RAT

R1	ROB6
R2	
R3	
R4	~~ROB5~~
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1				
ROB2				
ROB3				
ROB4				
ROB5	SUB	R4	33	✓
ROB6	ADD	R1	42	✓

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	43
2	2	3	13	44
3	3	4	5	45
4	4	14	24	46
5	5	25	26	47
6	6	43	44	

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number **48**

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	42
R2	9
R3	3
R4	33
R5	3
R6	4
R7	1
R8	2

RAT

R1	~~ROB6~~
R2	
R3	
R4	
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1				
ROB2				
ROB3				
ROB4				
ROB5				
ROB6	ADD	R1	42	✓

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	43
2	2	3	13	44
3	3	4	5	45
4	4	14	24	46
5	5	25	26	47
6	6	43	44	48

Add: 1 Cycle
Mul: 10 Cycles
Div: 40 Cycles

RS: Reservation Station
ROB: Reorder Buffer
RAT: Register Allocation Table

Cycle Number

Instructions				
1	DIV	R2	R3	R4
2	MUL	R1	R5	R6
3	ADD	R3	R7	R8
4	MUL	R1	R1	R3
5	SUB	R4	R1	R5
6	ADD	R1	R4	R2

RS for ADD/SUB

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

RS for MUL/DIV

Busy	Op	Dst-Tag	V_j	V_k	Q_j	Q_k	Dsp

Values in regesters

R1	42
R2	9
R3	3
R4	33
R5	3
R6	4
R7	1
R8	2

RAT

R1	
R2	
R3	
R4	
R5	
R6	
R7	
R8	

ROB Table

	Type	Dst	Value	Done
ROB1				
ROB2				
ROB3				
ROB4				
ROB5				
ROB6				

Cycle Table

Inst	Issue	Exec	Write	Commit
1	1	2	42	43
2	2	3	13	44
3	3	4	5	45
4	4	14	24	46
5	5	25	26	47
6	6	43	44	48

ROB and LSQ example

Consider the given instruction set compromising of 12 instructions. Assume there are two independent execution unit, one for ADD/SUB and one for MUL/DIV with a 3-entry and 2-entry reservation station per unit respectively and one load/store execution unit. The Reorder Buffer can hold upto 12 instructions and Load Store Queue can hold upto 6 entries. The branch predictor takes the decision of always Not Taken. The instructions set are issued and committed in order. Fill up the table with the cycle number of each operation for all the instructions under these assumptions.

ROB	Type	Destination	Value	
1	DIV	R1	R2	R3
2	LD	R4	10(R2)	
3	BNE	R1	R2	label
4	SUB	R1	R2	R3
5	LD	R2	15(R1)	
6	ST	R5	10(R3)	
7	ADD	R1	R1	R2
8	SUB	R4	R4	R3
9	ST	R3	30(R6)	
10	ADD	R5	R2	R3
11	LD	R4	0(R3)	
12	LD	R1	0(R6)	

Cache hit

Cache miss
(10 cycles penalty)

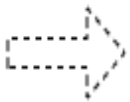
```
Load/Store: 1 cycle
Add/Sub: 2 cycles
Mul: 10 cycles
DIV: 20 cycles
Branch decision: 2 cycles
```

Register content	
R1	12
R2	80
R3	40
R4	56
R5	30
R6	10

Commit

Issue

Sequence	Instruction	Issue	Execute	Write	Commit
1	DIV R1, R2, R3	1	2	22	23
2	LD R4, 10(R2)	2	3	4	24
3	BNE R1, R2, label	3	23		25
4	SUB R1, R2, R3	4	5	7	
5	LD R2, 15(R1)	5	23	~~33~~	
6	ST R5, 10(R3)	6	7	8	
7	ADD R1, R1, R2	7	~~34~~	~~36~~	
8	SUB R4, R4, R3	8	9	11	
9	ST R3, 30(R6)	9	10	11	
10	ADD R5, R2, R3	10	~~37~~	~~39~~	
11	LD R4, 0(R3)	11	12	13	
12	LD R1, 0(R6)	12	13	23	



Issue

CYCLE: 25

ROB Table

ROB	Type	Destination	Value	Done	Commit
ROB1	DIV	R1	2	1	1
ROB2	LD	R4	11	1	1
ROB3	BNE	R1	!	1	1
ROB4	SUB	R1	40	1	0
ROB5	LD	R2			0
ROB6	ST	R5	10	1	0
ROB7	ADD	R1			0
ROB8	SUB	R4	16	1	0
ROB9	ST	R3	15	1	0
ROB10	ADD	R5			0
ROB11	LD	R4	15	1	0
ROB12	LD	R1	2	1	0

Regester content

R1	~~12~~ 2
R2	80
R3	40
R4	~~56~~ 11
R5	30
R6	10

RAT

R1	~~ROB1~~ ROB7
R2	ROB5
R3	
R4	~~ROB2~~
R5	
R6	

RS for ADD/SUB

Op	Dst-Tag	V_j	V_k	Q_j	Q_k
~~SUB~~	~~ROB4~~	~~80~~	~~40~~		
ADD	ROB7	2		ROB1	ROB5
~~SUB~~	~~ROB8~~		~~10~~	~~ROB2~~	
ADD	ROB10		40	ROB5	

RS for MUL/DIV

Op	Dst-Tag	Tag1	Tag2	Val1	Val2
DIV	ROB1	80	40		

LSQ

L/S	Address	Value	Commit
LD	80+10=90	11 (assume)	
LD	ROB1+15=17	5 (assume)	
ST	10+40=50	10 (assume)	
ST	30+10=40	15 (assume)	
LD	40	15	
LD	10	2 (assume)	

Thank You [1]

[1] Most of the material are taken from the famous book on Comp Arch by Hen/Pat, Comp Arch course by Milos Prvulovic for teaching purposes