The University of Manchester
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Project Report 2024

My Little Operating System

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Abstract

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Acknowledgements

Thanks page?

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Aims

This project will be based upon the following goals

- A basic implementation of processes, which can run arbritrary user code
- A scheduler that schedules processes interactively
- Memory management, to ensure that user code has limited access to memory
- IO, for example a text input and output, or other visual methods of output

1.2 Motivations

This project is an exploration of concepts and methods of operating systems, with the overall goal to implement these concepts to create a simple operating system. In addition to this, the project will be done using a board that implements the open source, RISC-V processor architecture, which will require research into the operation of RISC-V, as well as any implementation specific features to the board in use. The board used will be the Sifive Hifive1 Rev B. The main goal is the implementation of an interactive scheduler to run multiple processes at once, as this is something that will not be implemented unless part of an operating system.

1.3 Project Plan

The initial part of this project will be detemining an appropriate microcontroller board and setting up the toolchain required to compile and load code onto the board. Following this, the basic components of the system will be set up, such as the interrupt handler. Simple IO will be setup, to allow for ease of debugging, which will then be reimplemented later to be consistent with other IO elements. The implementation of processes will be split into multiple parts, such as the storage of process information, the creation of processes, the scheduling of processes and the deletion of processes. As part of this, memory management will be developed at the same time, as a basic implementation is required for user code to function.

1.4 Report Outline

- Introduction: This chapter gives the basic overview of the planned project
- Background: This chapter will introduce key concepts to enable a more comprehensive understanding of the projects details
- Design: This chapter will outline the key design decisions made before and during the project
- Implementation: This chapter will give details on the practical implementation of concepts and designs mentioned in previous chapters
- Evaluation: This chapter will discuss the implementation and findings made during the implementation
- Conclusion: This chapter will give a summary of how the aims of the project were met

Chapter 2

Background

Important texts

Modern operating systems tanenbaum Risc-v specification user level Risc-v specification machine level Risc-v programming

All sifive documentation Getting started Board manual core complex manual Schematics

Risc-v reference doc

Comparison of Riscv and ARM, and possibly comparisons with CISC systems if possible

functions

Interrupts and system calls

priveledge modes and how they are handled

Scheduling Algorithms Batch interactive Real time

Round robin Job estimation Lottery systems

Memory Basic Address spaces Maybe mentions of virtual and what would be required

How are stacks handled?

Chapter 3

Design

Board settings Clock settings, for both clocks

Purpose of both clocks

High frequency clock Uses Clock frequency UART, which is used for IO QSPI, which is used for flash communication

Pll and divider can be used with both ring osc and external crystal

Low frequency clock Uses Machine clock/real time clock Time based interrupts

Divider can be used for ring oscilattor

Ring oscilattor default large range of frequencies Less accurate, can varie during execution

External crystal Constant (with possible pll and div) constant frequency once turned on

toolchain Compiler/assembler choice as opposed to using premade tools

development purely on memory -¿ flash Exclusion of double tap bootloader

Linker discussion?

scheduler Discuss choices Interactive

Round robin with Quantum of x

Chapter 4

Outcome

Chapter 5

Evaluation

Chapter 6

Conclusions and further work