Why can't you use both pins PA0 and PC0 for external interrupts at the same time?

You can't use both PA0 and PC0 for external interrupts at the same time because they are multiplexed onto EXTI0. Only one or the other can be selected at a time.

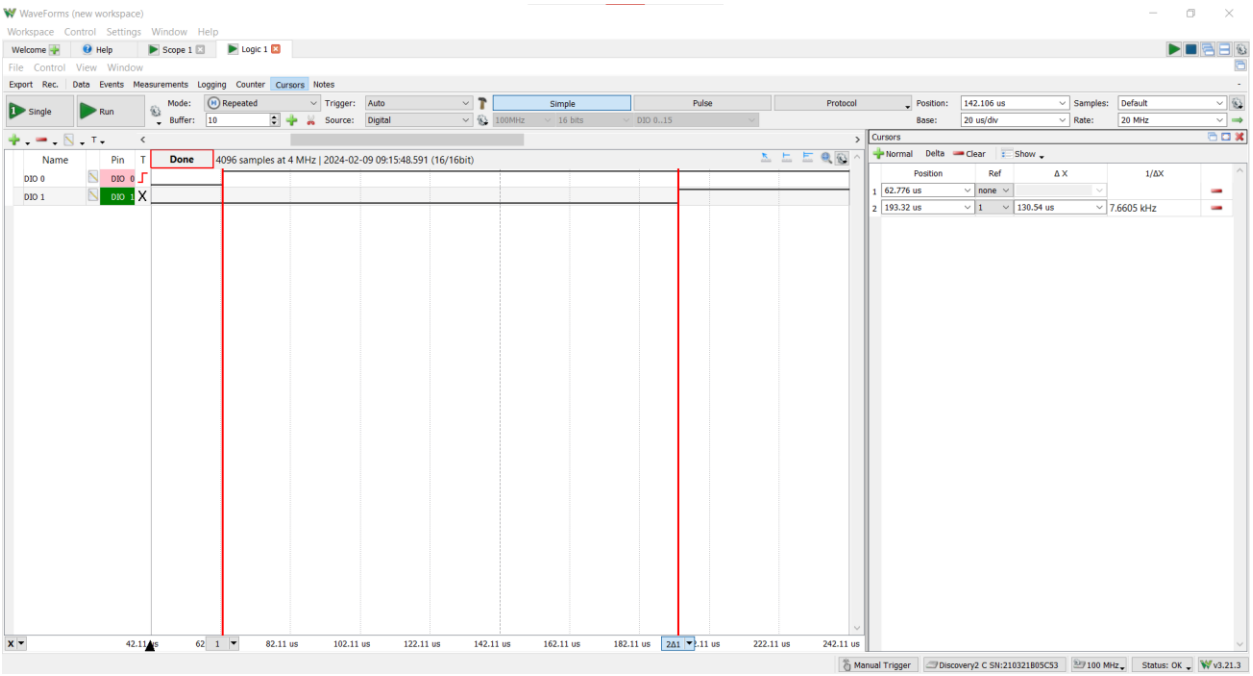
What software priority level gives the highest priority? What level gives the lowest?

The highest priority level is -3, which is the non-maskable interrupt. The lowest priority on the other hand (for this microcontroller at least) is 3.

How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented

The NVIC has 8 bits reserved in its priority registers for each interrupt. However, this microcontroller only implements the two MSB bits within this register, with everything else [5:0] being read as zeroes.

What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.



Using a counter going up to 3,000,000 for a more visible delay, the latency between pushing the button and seeing the LED change is approximately 130 microseconds.