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CE III year/II semester
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Lab Report - 2

Task 1: Arithmetic logic unit (ALU) design

Components

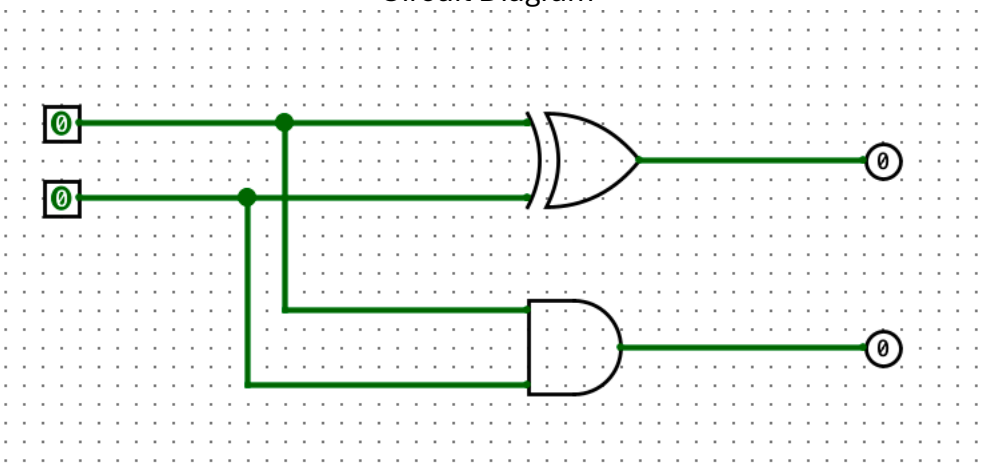
Half Adder

A half-adder is a fundamental digital circuit used in computing and digital electronics to perform the addition of two single-bit binary numbers. It is the simplest form of an adder, forming the basic building block for more complex adder circuits like full adders and multi-bit adders.

Components of a Half Adder

Inputs: The half adder takes two single-bit binary inputs, often labeled as A and B.
Outputs: It produces two outputs:
Sum (S): The result of the binary addition of A and B.
Carry (C): The carry-out bit that indicates if there is an overflow from the sum.

Circuit Diagram



Truth table

Inputs		Outputs	
A	**B**	**Sum**	**Carry**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder

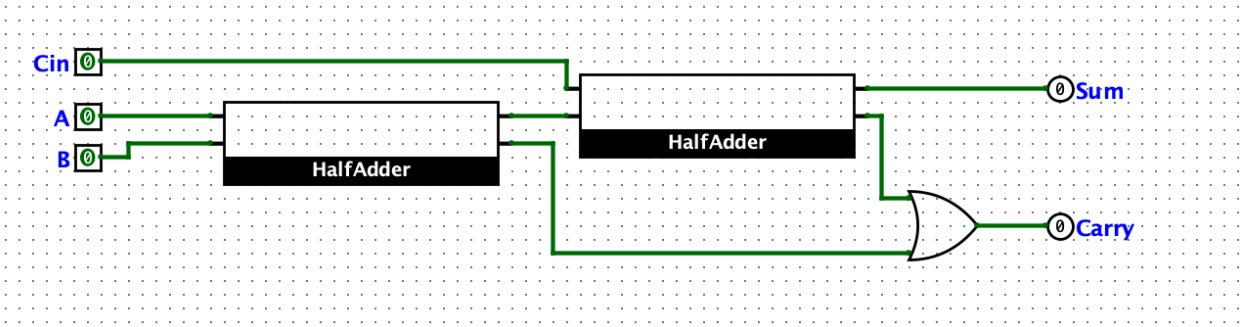
A full adder is an essential digital circuit used to perform the addition of binary numbers. Unlike a half adder, which can only add two single-bit numbers without considering a carry input, a full adder can add three single-bit numbers: two significant bits and an additional carry-in bit from a previous addition. This capability makes the full adder a crucial component for constructing multi-bit binary adders used in arithmetic logic units (ALUs) and other digital systems.

Components of a Full Adder

Inputs:
A: First binary digit.
B: Second binary digit.
Cin (Carry-in): Carry from the previous lower significant bit addition.

Outputs:
Sum (S): The result of the binary addition of A, B, and Cin.
Carry-out (Cout): The carry generated from the addition, which will be used as the carry-in for the next higher significant bit.

Circuit Diagram



Truth Table

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Multiplexer

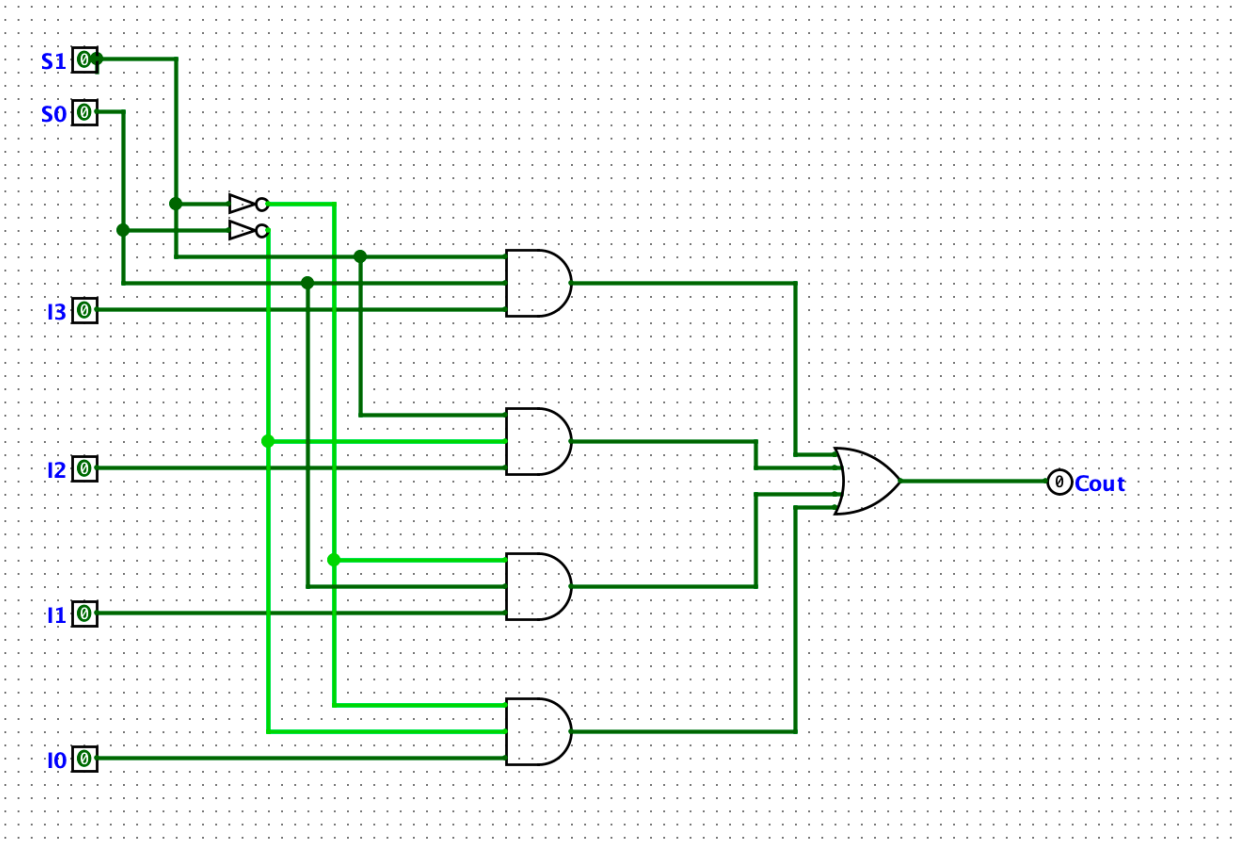
A multiplexer, often abbreviated as MUX, is a fundamental digital component used in electronics to select one of many input signals and forward the selected input to a single output line. It functions as a data selector, allowing multiple input signals to share one device or resource, such as an analog-to-digital converter or a data bus, thereby reducing the number of required data paths.

Components and Functionality
Inputs: A multiplexer has multiple input lines.

Select Lines: It has a set of select lines or control lines. These select lines determine which input is connected to the output.

Output: A single output line that carries the signal from the selected input.

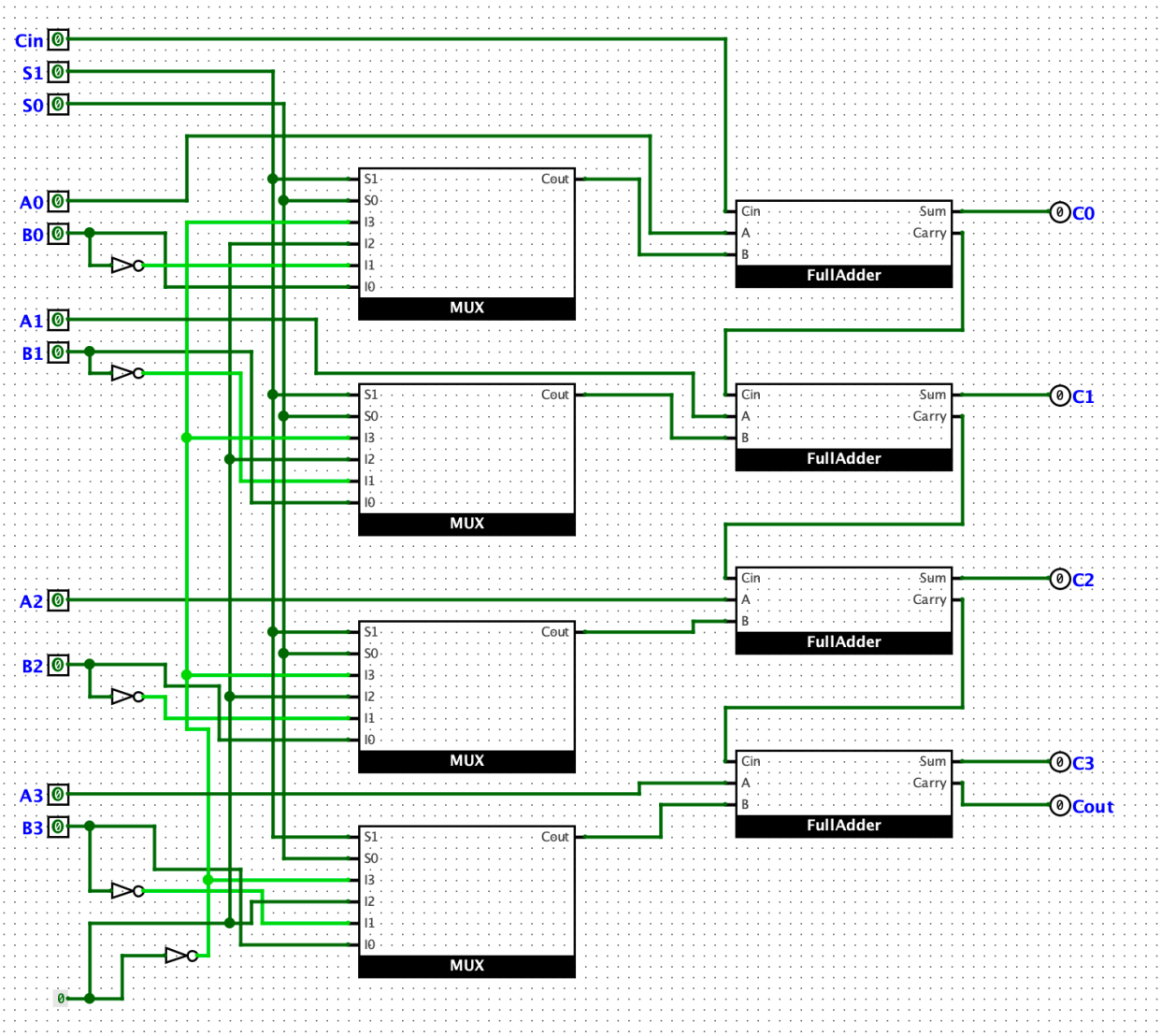
Circuit Diagram



Truth table

INPUTS			Output
S_2	S_1	S_0	Y
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

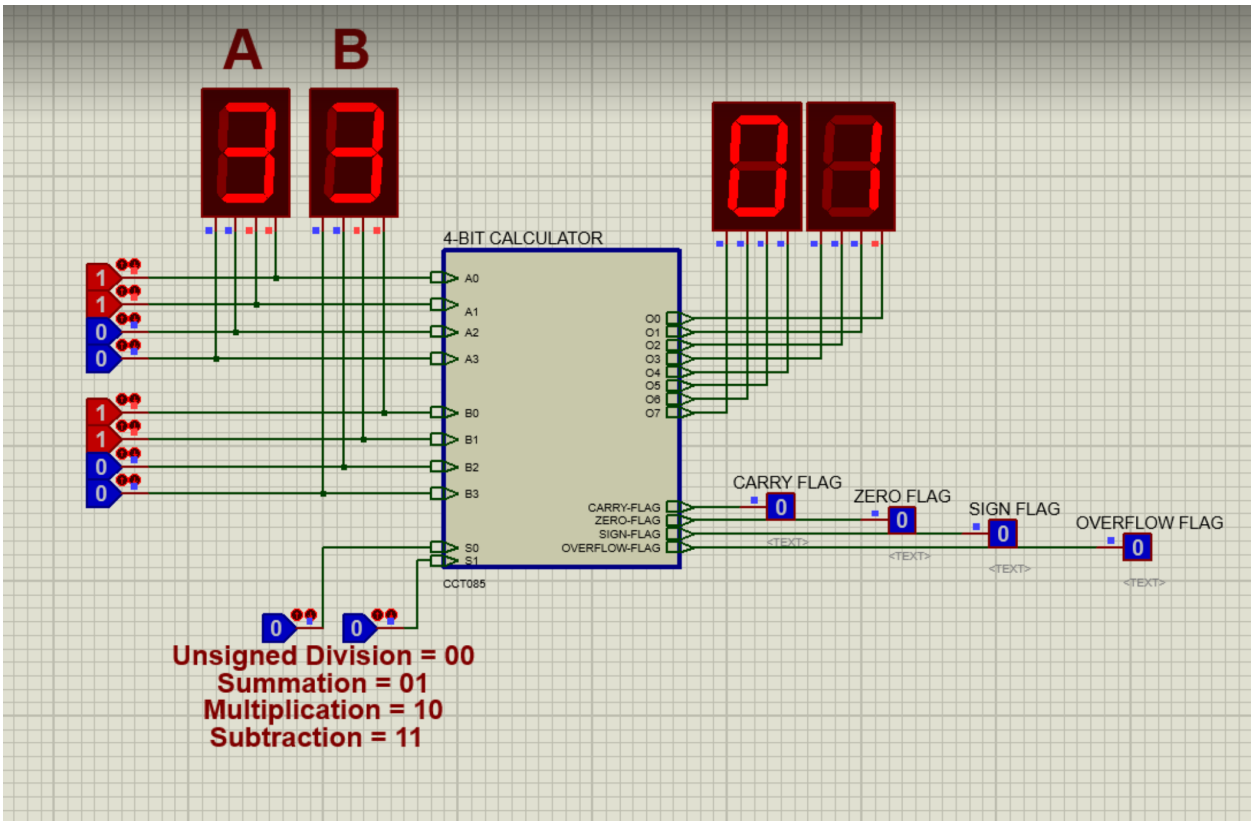
Arithmetic Logic Unit

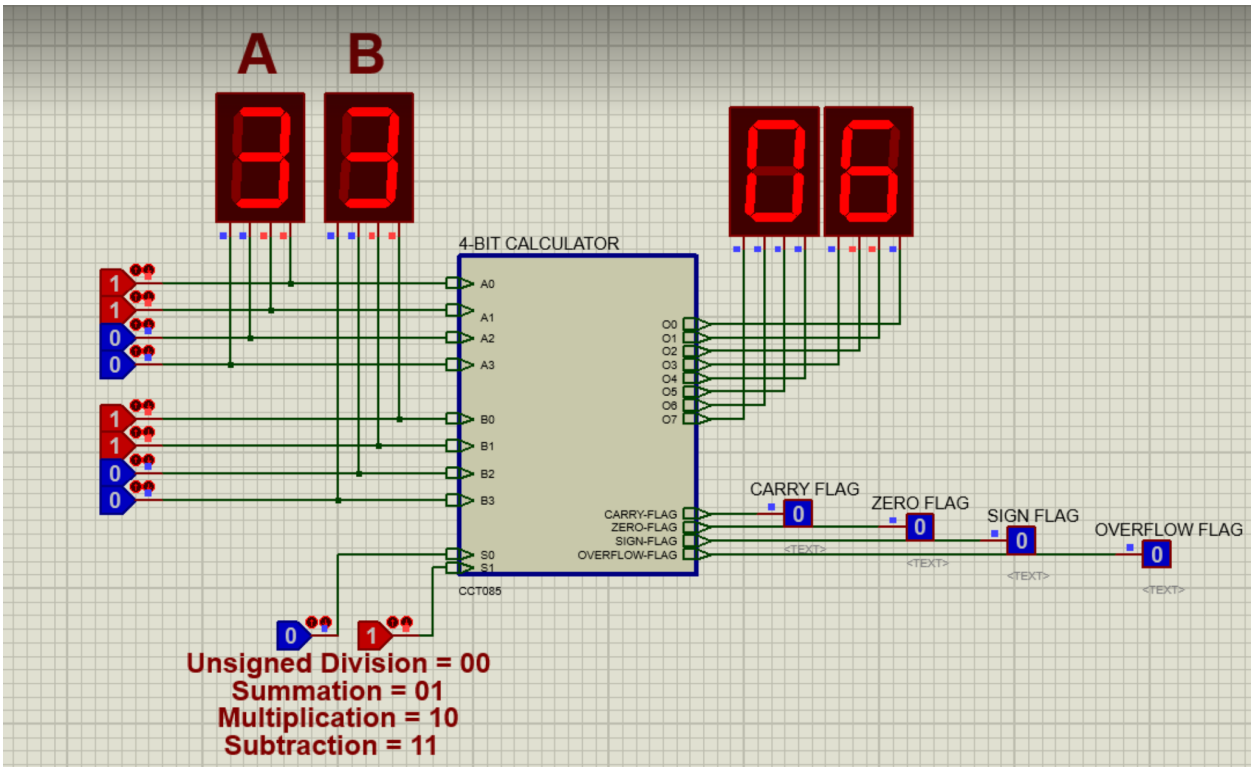

Cin
S1
S0
A0
B0
A1
B1
A2
B2
A3
B3
0
S1
S0
I3
I2
I1
I0
Cout
MUX
Cin
A
B
Sum
Carry
FullAdder
C0
C1
C2
C3
Cout

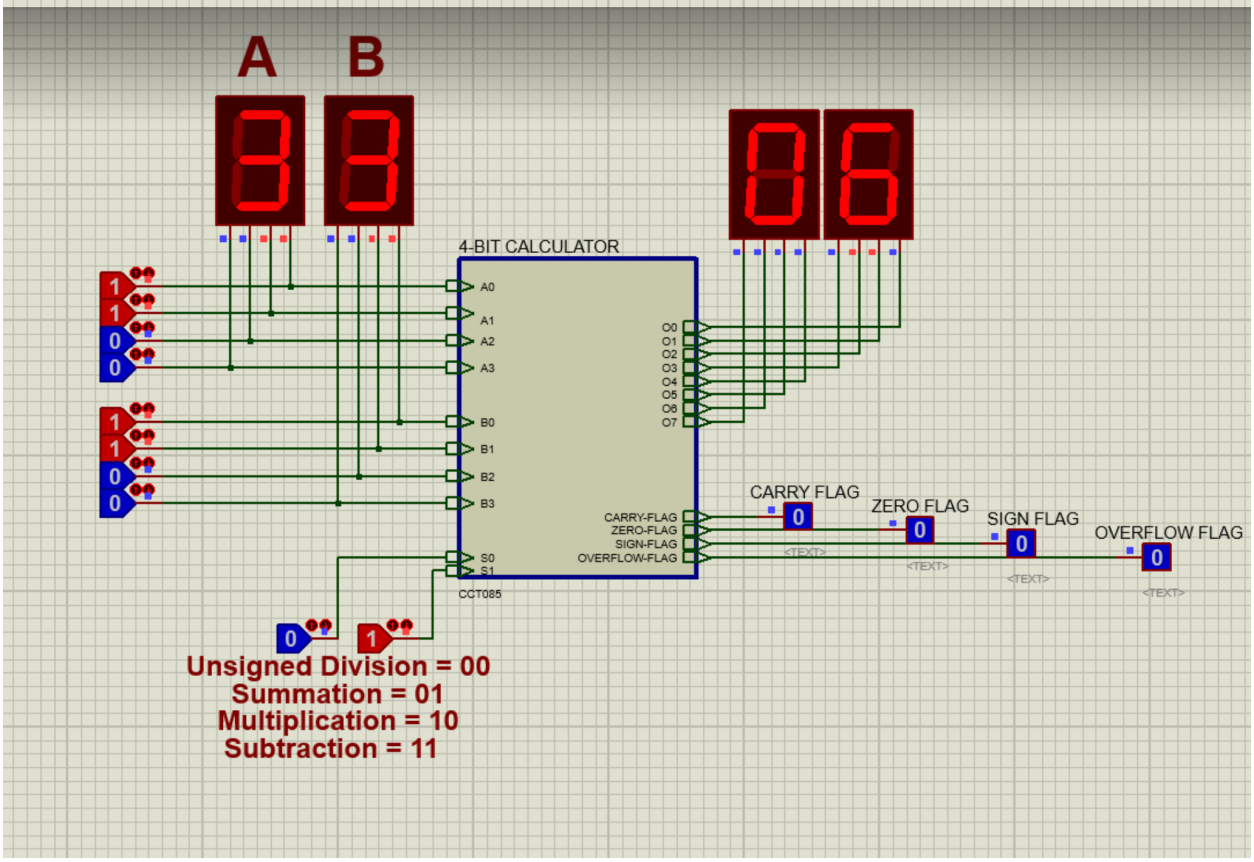
Task 2: Design a Calculator

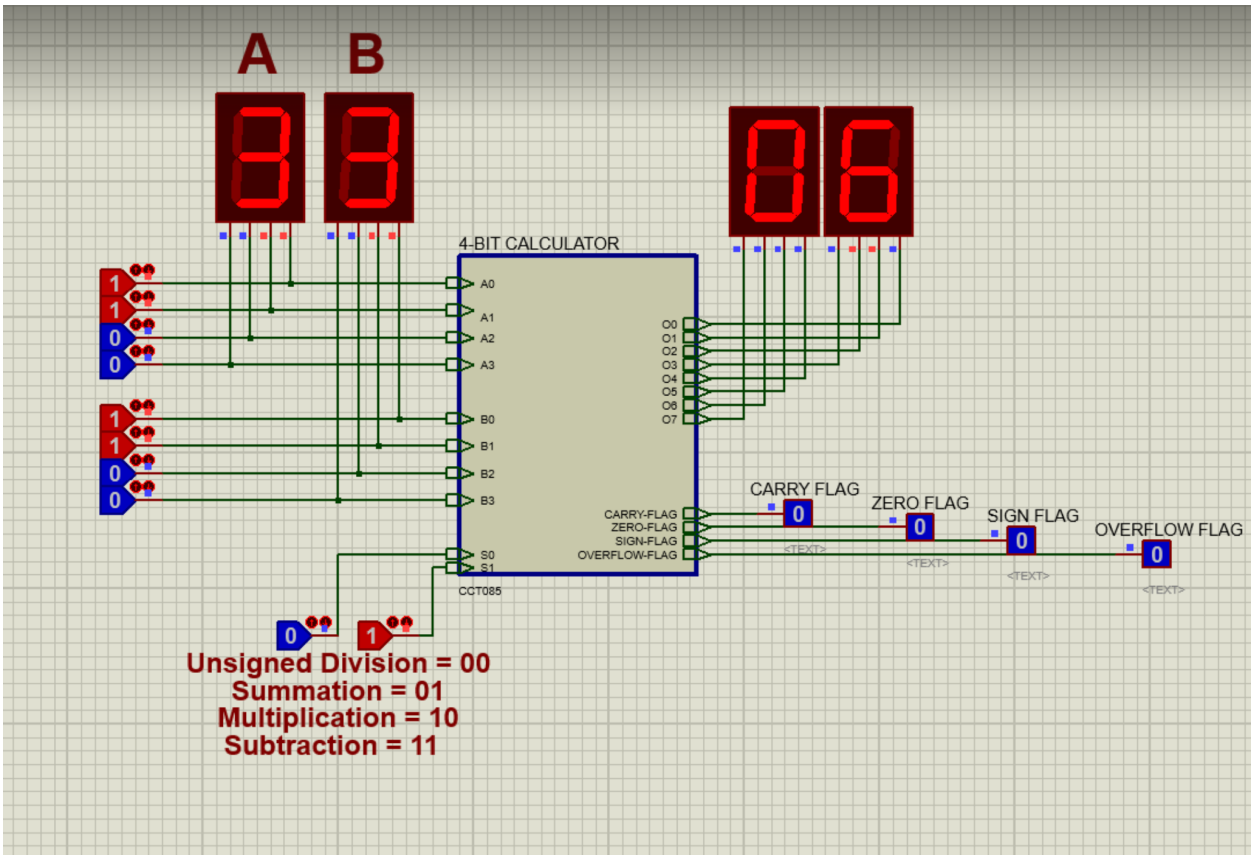
Components

ALU



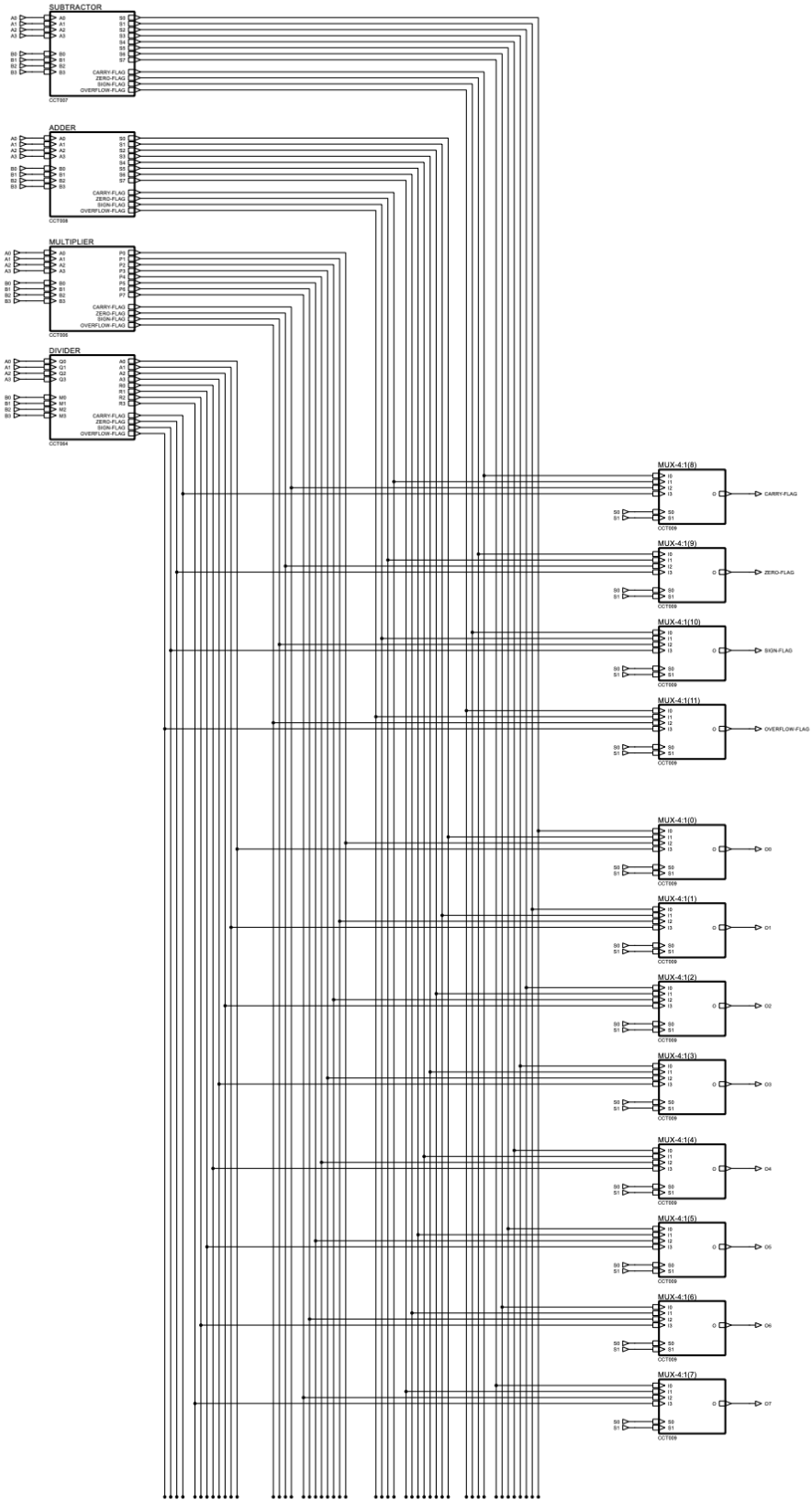

A
B
4-BIT CALCULATOR
A0
A1
A2
A3
B0
B1
B2
B3
S0
S1
CCT085
O0
O1
O2
O3
O4
O5
O6
O7
CARRY-FLAG
ZERO-FLAG
SIGN-FLAG
OVERFLOW-FLAG
CARRY FLAG
ZERO FLAG
SIGN FLAG
OVERFLOW FLAG
Unsigned Division = 00
Summation = 01
Multiplication = 10
Subtraction = 11


A
B
4-BIT CALCULATOR
A0
A1
A2
A3
B0
B1
B2
B3
S0
S1
CCT085
O0
O1
O2
O3
O4
O5
O6
O7
CARRY-FLAG
ZERO-FLAG
SIGN-FLAG
OVERFLOW-FLAG
CARRY FLAG
ZERO FLAG
SIGN FLAG
OVERFLOW FLAG
Unsigned Division = 00
Summation = 01
Multiplication = 10
Subtraction = 11

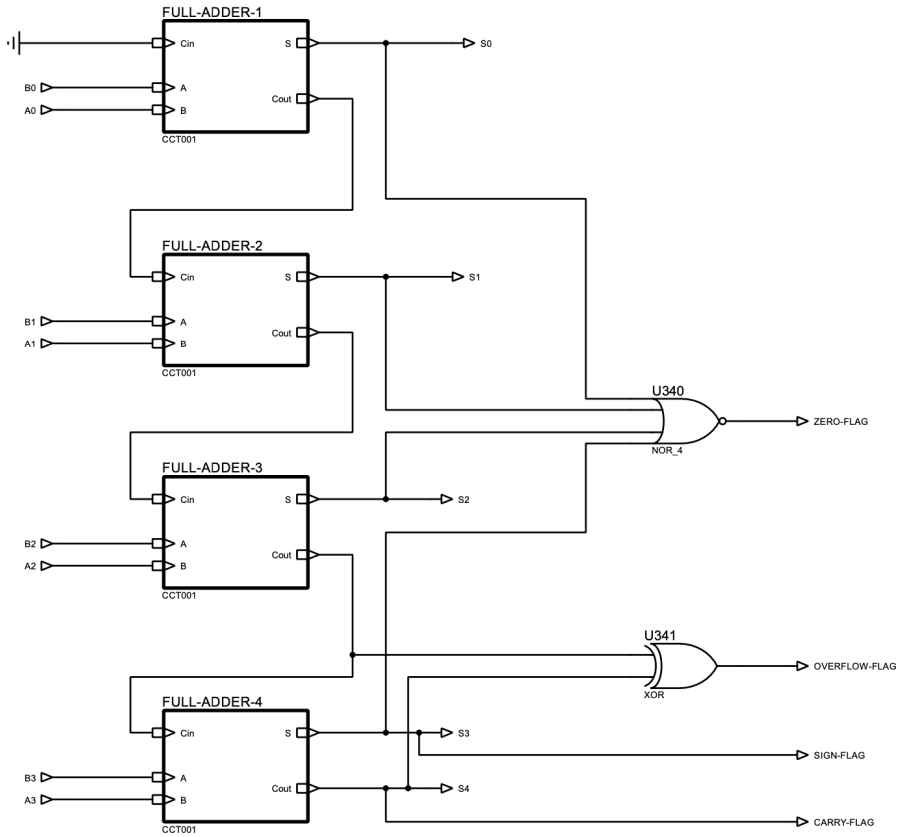


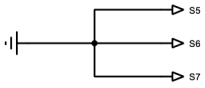
Internal Circuit for ALU

ALU internal

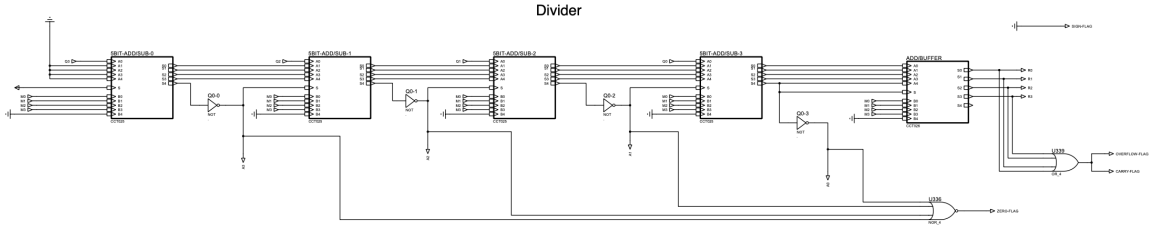


Adder

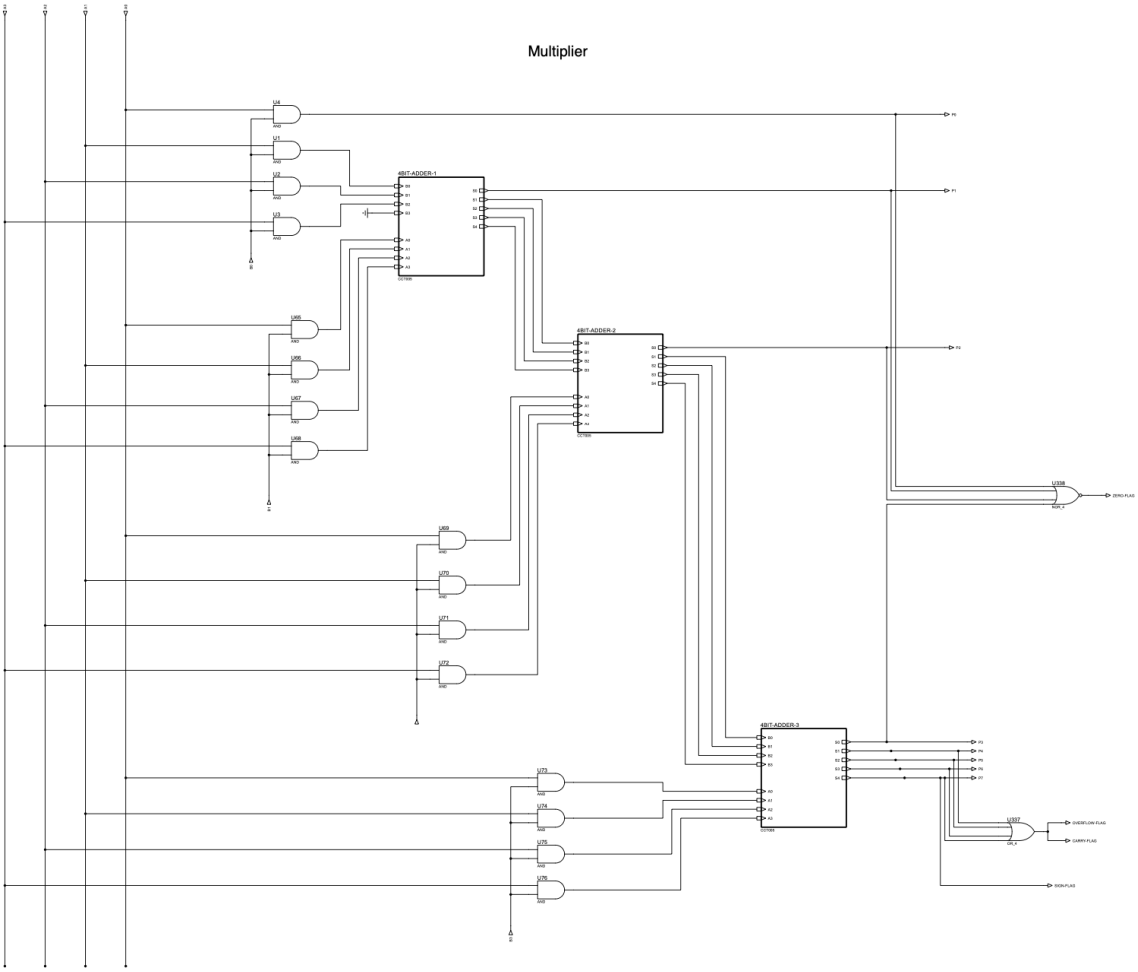




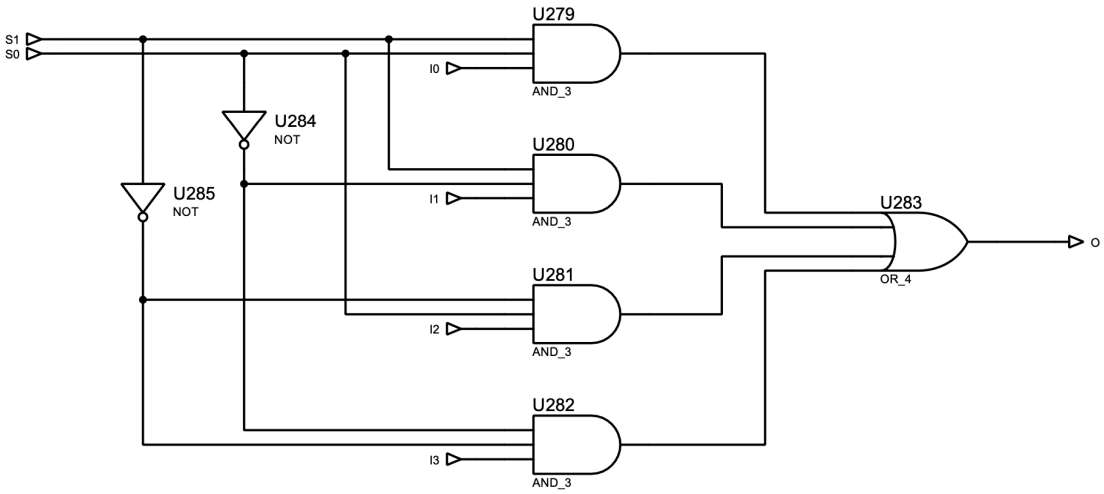
Divider



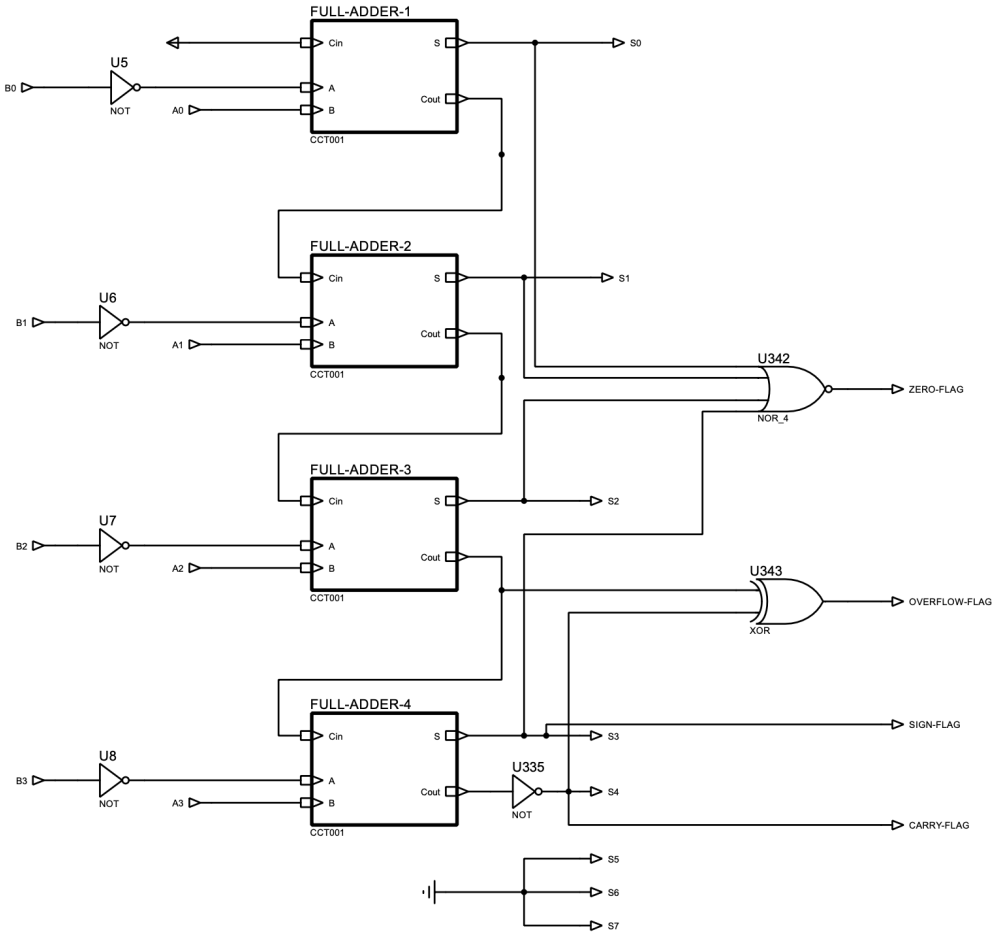
Multiplier

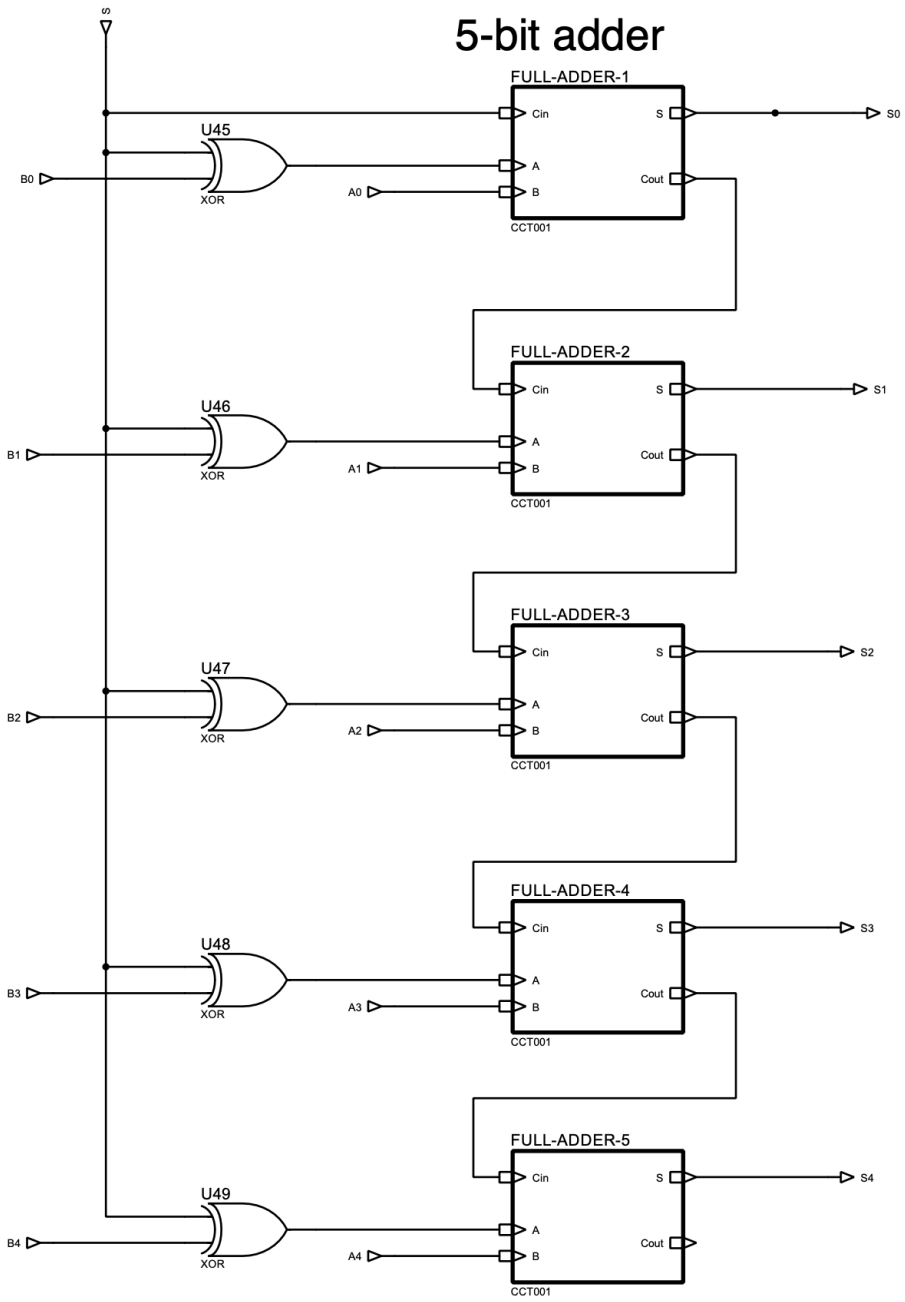

4BIT-ADDER-1
4BIT-ADDER-2
4BIT-ADDER-3
U4
U5
U2
U3
U66
U56
U67
U68
U69
U70
U71
U72
U73
U74
U75
U76
U338
U337
P0
P1
P2
P3
P4
P5
P6
P7
ZERO FLAG
OVERFLOW FLAG
CARRY FLAG
SIGN FLAG

MUX


S1
S0
U279
I0
AND_3
U284
NOT
U280
I1
AND_3
U285
NOT
U283
OR_4
O
U281
I2
AND_3
U282
I3
AND_3

Flags


FULL-ADDER-1
Cin
S
S0
U5
B0
A
Cout
NOT
A0
B
CCT001
FULL-ADDER-2
Cin
S
S1
U6
B1
A
Cout
NOT
A1
B
CCT001
U342
ZERO-FLAG
NOR_4
FULL-ADDER-3
Cin
S
S2
U7
B2
A
Cout
NOT
A2
B
CCT001
U343
OVERFLOW-FLAG
XOR
FULL-ADDER-4
Cin
S
S3
SIGN-FLAG
U8
B3
A
U335
Cout
S4
NOT
NOT
A3
B
CARRY-FLAG
CCT001
S5
S6
S7



Conclusion

Using the above components, the Calculator was designed using proteus.