CS 303 Logic and Digital System Design Assigned : 24/03/2023
Homework #02 Due : 31/03/2023

A 3-bit input octal to seven segment decoder is to be designed. The circuit will accept binary combinations 000, 001, 010, 011, 100, 101, 110, 111, and drive a seven segment display to show 0, 1, 2, 3, 4, 5, 6, 7, respectively.

1. Construct the truth tables for segment outputs a through g with d2, d1, and d0 as inputs.
2. Design 7 circuits to individually drive the segments, composed of AND, OR and INV gates.
3. Demonstrate your solution by simulating this circuit using *Digital*. Your circuit is expected to replace the block labeled "oct2seven" in Fig. 1.

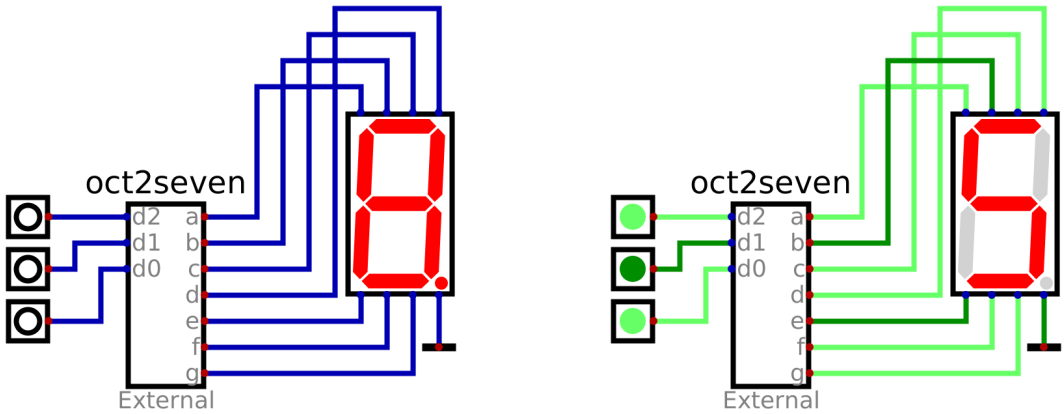

Fig. 1: An octal to seven segment decoder with 3-bit input (left), and sample run (right.)

Submit:

1. Your truth tables and drawings of designed circuits (as a .pdf file)
2. Your *Digital* simulation file (with .dig extension.)

Note: Make sure you submit a single .dig file which does not require an additional .dig file for sub-circuits. Erase the *oct2seven* block and place your circuit (composed of an appropriate number of AND, OR and INV gates) on the top level design.

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