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SM74HC595D

A brief

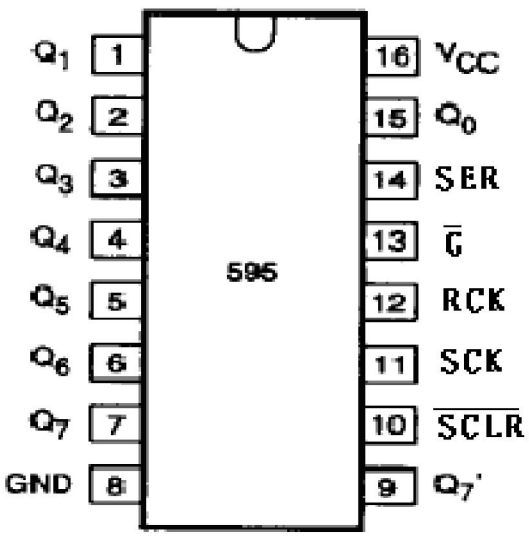
SM74HC595D It is a kind 8 Bit latch, 8 Bit serial input, 8 Bit serial / parallel output string - And shift register and the output of the common tristate led Driver chip. have 8 Bit shift register memory and a tri-state output. The shift register memory and a clock, respectively. Data SCK The rising edge of the input, in RCK Rising edge to go into the storage registers. The shift register has a serial input shift (SER), And a serial output (Q7 '), And an asynchronous reset low, there is a parallel storage register 8 Bits, with three-state output bus, when the enable G

(Low), the output data stored in the register to the bus. It can be manufactured by other companies 74HC595 Fully compatible.

Second, the functional characteristics:

- have 8 Bit serial input;
- have 8 Bit serial and parallel output;
- A shift register directly cleared to "zero" function;
- And it has a latch 3 State output;
- Through 50MHz Shift clock;
- Operating Voltage: 2V-6V

Third, the pin map



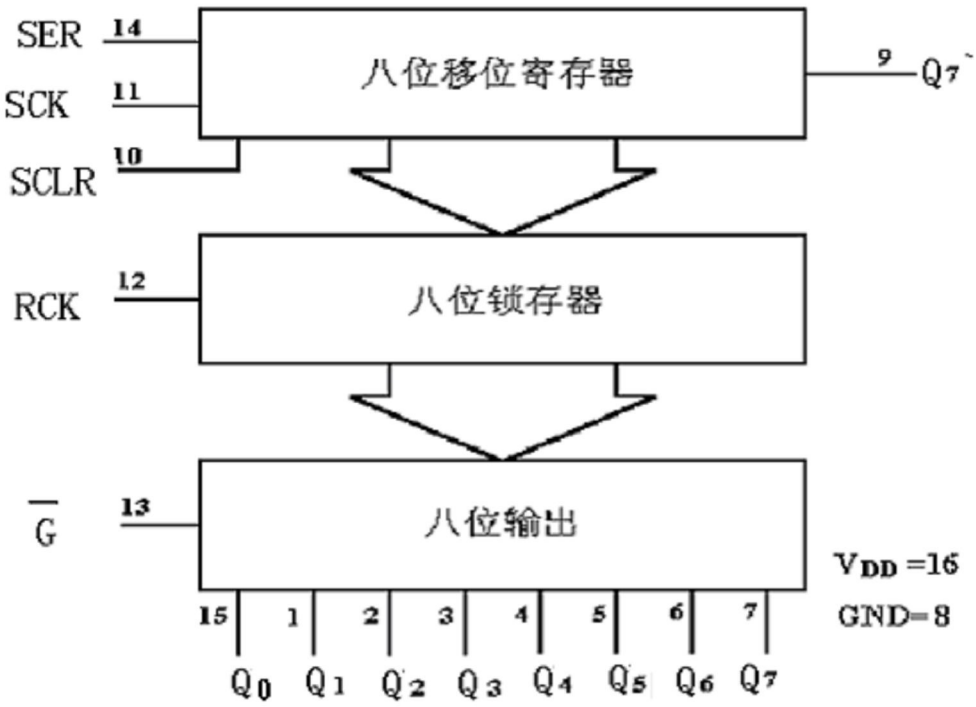
Fourth, pin function definitions

Pin Number	symbol	Pin Function
10	$\overline{SCLR}$	Reset terminal
11	SCK	The shift register clock, the rising edge of the shift
12	RCK	Latch register clock rising edge of the
13	$\overline{G}$	An output enable terminal, so that a low level, the output of the gate; is high **Level, the output of 3 state**
14	SER	Serial data input terminal
15 , 1--7	Q0 ---- Q7	Parallel outputs
9	Q7`	Serial Output
8	GND	Logically
16	V_{cc}	Power supply terminal

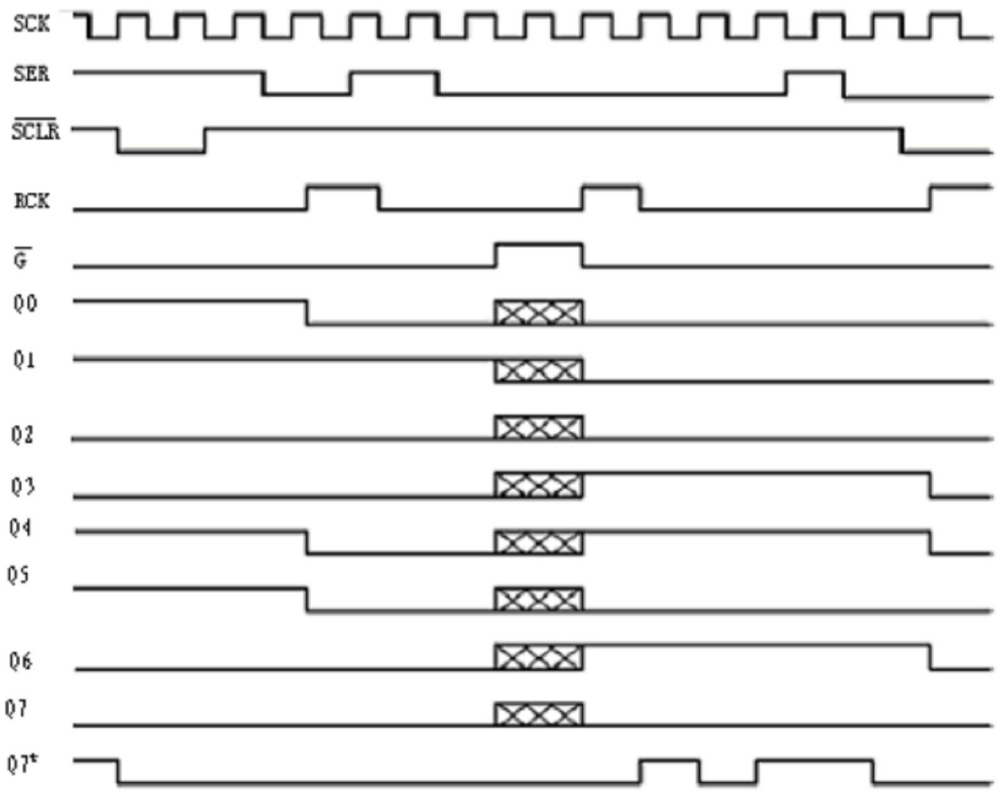
Fifth, the truth table function

RCK	SCK	$\overline{SCLR}$	$\overline{G}$	Features
X	X	X	H	**Q0 --- Q7 for 3 state,**
X	X	L	L	**The shift register is cleared to "zero" Q7` = 0**
X	↑	H	L	**Shift register memory, $Q_N = Q_{N-1}$, Q_A = SER**
↑	X	H	L	Values stored in the shift register

Six, logic diagram



Seven, work timing diagram



Eight, DC Characteristics

symbol	parameter	condition	VCC	T = 25 0 Typical values	unit
V_{IH}	Enter the most high low voltage		2.0V 4.5V 6.0V	1.5 3.15 4.2	V
V_{IL}	Most low-level input high voltage		2.0 V 4.5V 6.0V	0.5 1.35 1.8	
V_{OH}	The most high output Small value	$V_{IV} = V_{IH}$ or V_{IL} $\| I_{OUT} \| \le 20$ uA	2.0V 4.5V 6.0V	1.9 4.4 5.9	
	Q7`	$V_{IV} = V_{IH}$ or V_{IL} $\| I_{OUT} \| \le 4.0$ mA $\| I_{OUT} \| \le 5.2$ mA	4.5V 6.0V	3.84 5.34	
	Q0 ---- Q7	$V_{IV} = V_{IH}$ or V_{IL} $\| I_{OUT} \| \le 6.0$ mA $\| I_{OUT} \| \le 8.2$ mA	4.5V 6.0V	3.84 5.34	
V_{OL}	Most low-level output Great value	$V_{IV} = V_{IH}$ or V_{IL} $\| I_{OUT} \| \le 20$ uA	2.0V 4.5V 6.0V	0.1 0.1 0.1	V
	Q7`	$V_{IV} = V_{IH}$ or V_{IL} $\| I_{OUT} \| \le 4.0$ mA $\| I_{OUT} \| \le 5.2$ mA	4.5V 6.0V	0.33 0.33	V
	Q0 ---- Q7	$V_{IV} = V_{IH}$ or V_{IL} $\| I_{OUT} \| \le 6.0$ mA $\| I_{OUT} \| \le 7.8$ mA	4.5V 6.0V	0.33 0.33	
I_{IN}	Maximum input current	V_{IN} = VCC or GND	6.0V	± 1.0	uA
I_{OZ}	maximum 3 State Outputs Leakage Current	V_{out} = VCC or GND G = V_{IH}	6.0V	± 5.0	uA
I_{CC}	The maximum quiescent current	V_{out} = VCC or GND I_{OUT} = 0 uA	6.0V	80	uA

Nine, AC Electrical Characteristics

GND = 0 , $T_r = T_f = 6$ns, $C_L = 50$ PF VCC = 4.5V

symbol	parameter	T temperature + 25 0 Least	Typical	maximum	unit	Waveform chart
t_{PHL} / t_{PLH}	Shift clock edge to Q7` Output delay	-	15	twenty two	ns	Map 1
t_{PHL} / t_{PLH}	Memory clock edge to Output Delay	-	16	twenty two		Map 2
t_{PHL}	To reset valid edge Q7` Output delay	-	20	40		Map 4
t_{PZH} / t_{PZL}	3 State of the output enable signal to the active edge time	-	twenty one	35		Map 5
t_{PZH} / t_{PZL}	3 State of the time disable signal is active the output edge	-	18	30		Map 5
t_W	Shift clock width	10	20	-		Map 1
t_W	Store clock width	10	20	-		Map 2
t_W	Reset time width	15	25	-		Map 4
t_{SU}	Data storage setup time	16	25	-		Map 3
t_{SU}	Shift data setup time	16	25	-		Map 2
t_h	Data Hold Time	3	12	-		Map 3
t_{rem}	Reset the time shift clock	10	17	-		Map 4
f_{max}	The maximum clock frequency RCK or SCK	30	52	-	MHz	Map 1 , 2

X. AC waveform diagram characteristic

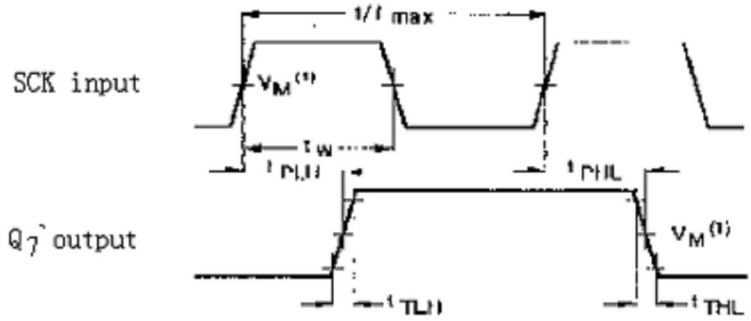


图1

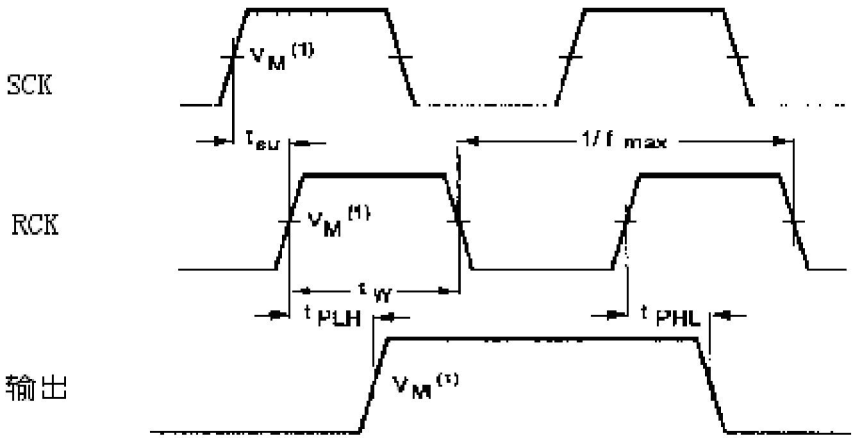


图2

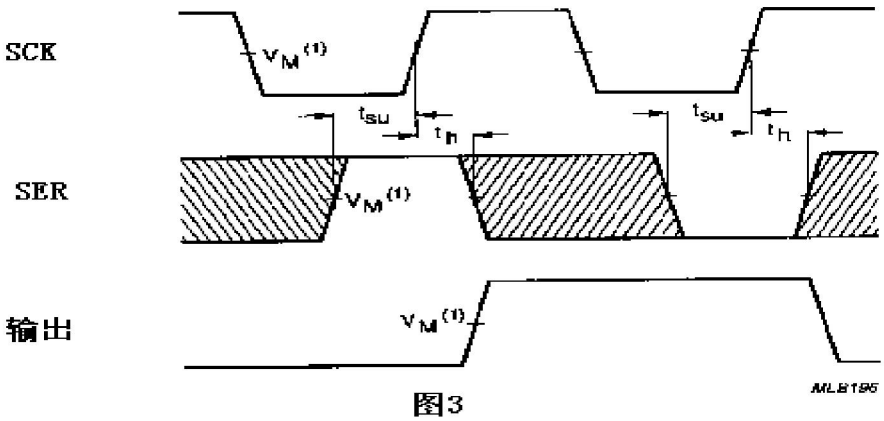


图3

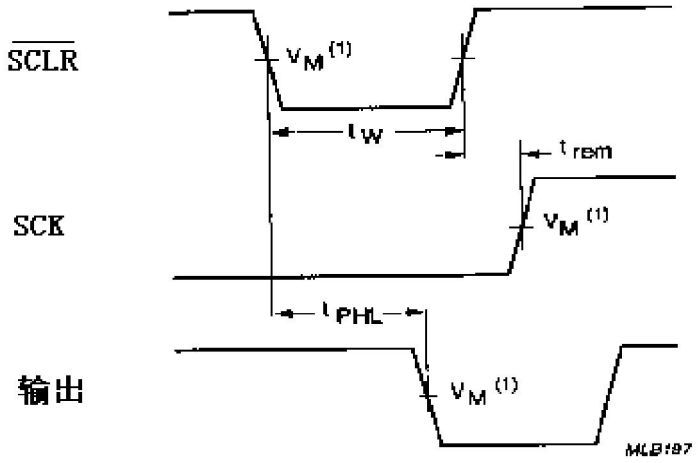


图4

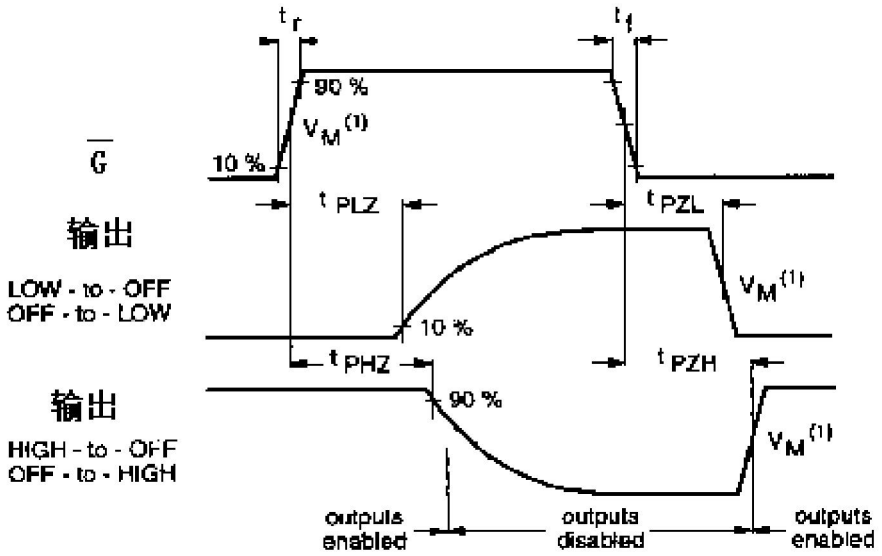
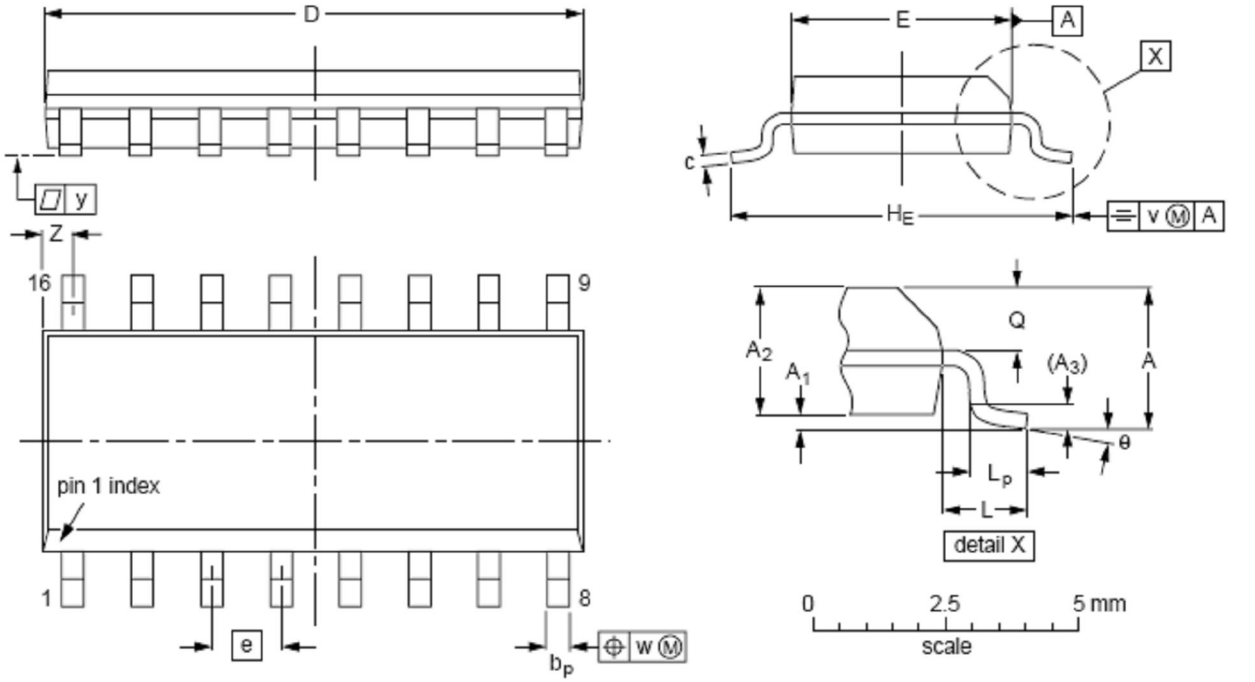


图5

XI schematic package



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	