ECE 4723/6723 Embedded Systems Lab (section 2)

Team Scons Sucks

Task 2: ESOS and the ECE 4723/6723 Target Board

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Schematic Errata

- Missing connection between RTS pin 6 of FTDI and MCLR on pin 1 of SV1
- Missing connection between RXD on SV1 headers to RF0 on H1 headers
- Missing connection between R7, R6, and V0. V0 is still connected to R7. Connection is needed between left pad (if silkscreen is read in natural orientation) of R7 to left pad of R6
- The SDA and SCL pins are not connected to the SCL1/RG2 and SDA1/RG3 pins.
- Cannot determine what VICP or PGLVP on SV1 are or should be connected to.