

# **bq76PL455A 16-Cell Industrial Integrated Battery Monitor with Passive Cell Balancing**

## **1 Features**

- Monitors and Balances 6-to-16 Cells per Device
- Highly Accurate Monitoring
  - High Performance 14-bit Analog-to-Digital Converter (ADC) With Internal Reference
  - All Cells Converted in 2.4 ms (Nominal)
  - Eight AUX Inputs for Temperature and Other Sensors with Input Voltage of 0 V to 5 V
  - Internal Precision Reference
- Integrated Protector With Separate Vref for Overvoltage (OV) and Undervoltage (UV) Comparators and Programmable V<sub>CELL</sub> Set Points
- Engineered for High System Robustness
  - Up to 1-Mb/s Stackable Isolated Differential-UART
  - Up to 16 ICs in Daisy-Chain With Twisted Pair
  - Passes Bulk Current Injection (BCI) Test
  - Designed for Robust Hot-Plug Performance
- Passive Balancing with External n-FETs and Active Balancing with EMB1428Q/EMB1499Q

## **2 Applications**

- Energy Storage (ESS) and UPS
- E-Bikes, E-Scooters

## **3 Description**

The bq76PL455A device is an integrated 16-cell battery monitoring and protection device, designed for high-reliability, high-voltage industrial applications. The integrated high-speed, differential, capacitor-isolated communications interface allows up to sixteen bq76PL455A devices to communicate with a host through a single high-speed Universal Asynchronous Receiver/Transmitter (UART) interface.

The bq76PL455A monitors and detects several different fault conditions, including: overvoltage, undervoltage, overtemperature, and communication faults. Six GPIO ports as well as eight analog AUX ADC inputs are included for additional monitoring and programmable functionality. A secondary thermal shutdown is included for further protection.

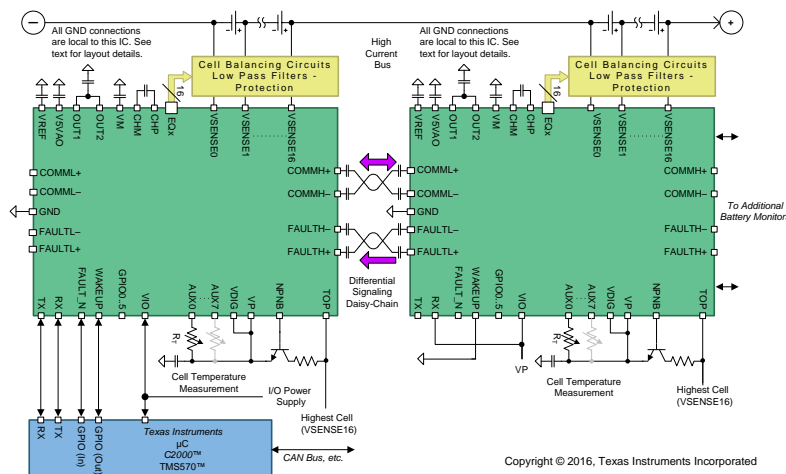
The bq76PL455A has features that customers may find useful to help them meet functional safety standard requirements. See [Safety Manual for bq76PL455A-Q1](#) (SLUUB67).

### **Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq76PL455A	TQFP (80)	12.00 mm x 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### **Simplified Schematic**



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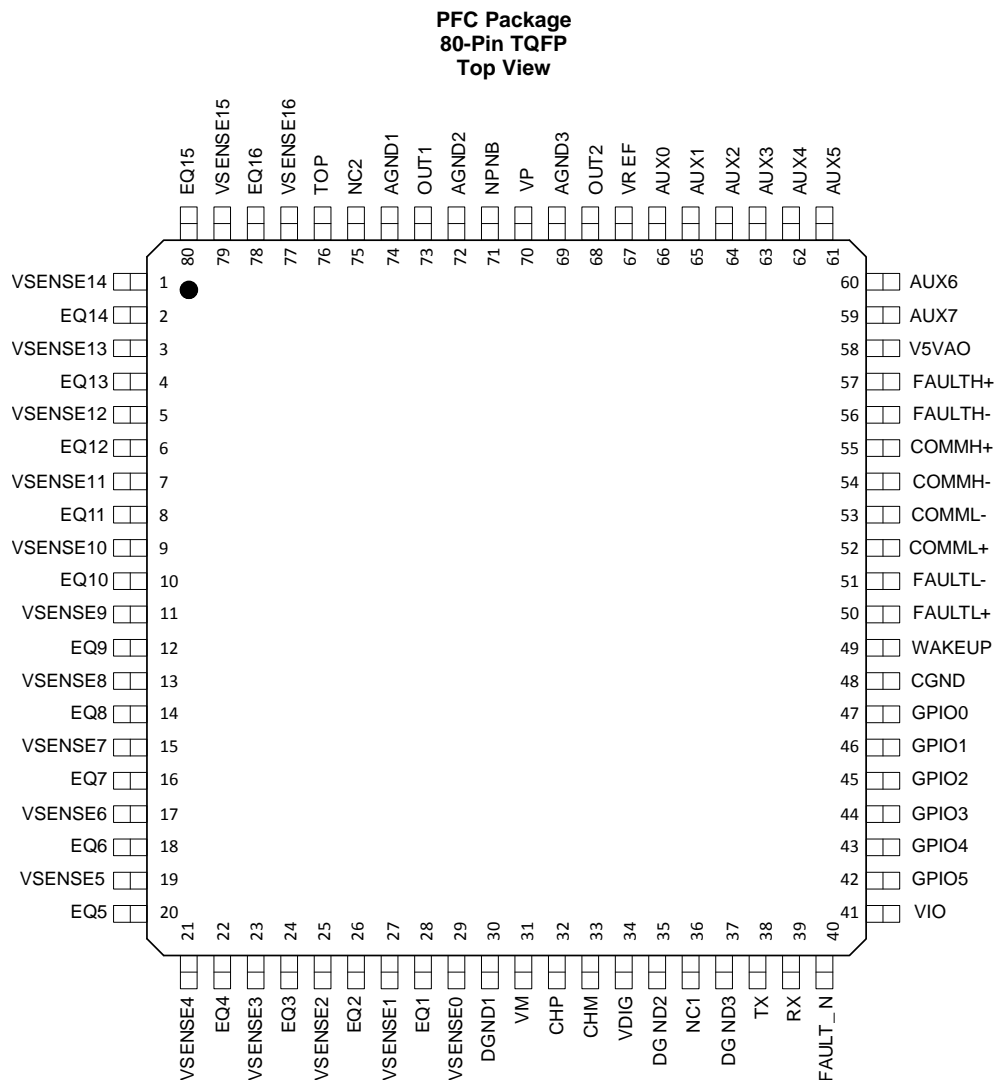
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2016) to Revision A	Page
Deleted reference to ISO26262	1
Changed references of automotive to industrial throughout document	1
Added table notes to <i>ESD Ratings</i> table	7
Added <i>Receiving Notification of Documentation Updates</i> section	119

## 5 Pin Configuration and Functions



**Pin Functions**

NAME		TYPE <sup>(1)</sup>	DESCRIPTION
PIN	NO.		
AGND1	74	P	Analog Ground <sup>(2)</sup> . Connect to ground plane.
AGND2	72	P	Analog Ground <sup>(2)</sup> for VREF. Internally shorted to AGND3, also make this connection externally in the printed-circuit board (PCB) layout. Connect to ground plane.
AGND3	69	P	Analog Ground <sup>(2)</sup> for VREF. Internally shorted to AGND2, also make this connection externally in the PCB layout. Connect to ground plane.
AUX0	66	AI	Ground referenced general-purpose analog measurement input.
AUX1	65	AI	Ground referenced general-purpose analog measurement input.
AUX2	64	AI	Ground referenced general-purpose analog measurement input.
AUX3	63	AI	Ground referenced general-purpose analog measurement input.
AUX4	62	AI	Ground referenced general-purpose analog measurement input.
AUX5	61	AI	Ground referenced general-purpose analog measurement input.
AUX6	60	AI	Ground referenced general-purpose analog measurement input.
AUX7	59	AI	Ground referenced general-purpose analog measurement input.

### Pin Functions (continued)

NAME		TYPE <sup>(1)</sup>	DESCRIPTION
PIN	NO.		
CGND	48	P	Communication ground <sup>(2)</sup> . Connect to ground plane.
CHM	33	P	Charge pump <i>flying</i> capacitor connection. Connect a 22-nF ceramic capacitor <sup>(3)</sup> between this pin and CHP.
CHP	32	P	Charge pump <i>flying</i> capacitor connection. Connect a 22-nF ceramic capacitor <sup>(3)</sup> between this pin and CHM.
COMMH–	54	DIO	Inverting, high-side differential connection to the COMML– pin of the higher adjacent module in a daisy chain. Leave this pin unconnected if not used.
COMMH+	55	DIO	Non-inverting, high-side differential connection to the COMML+ pin of the higher adjacent module in a daisy chain. Leave this pin unconnected if not used.
COMML–	53	DIO	Inverting, low-side differential connection to the COMMH– pin of the lower adjacent module in a daisy chain. Leave this pin unconnected if not used.
COMML+	52	DIO	Non-inverting, low-side differential connection to the COMMH+ pin of the lower adjacent module in a daisy chain. Leave this pin unconnected if not used.
DGND1	30	P	Digital Ground <sup>(2)</sup> . Connect to ground plane.
DGND2	35	P	Digital Ground <sup>(2)</sup> . Connect to ground plane.
DGND3	37	P	Digital Ground <sup>(2)</sup> . Connect to ground plane.
EQ1	28	DO	Cell Equalization control output used to drive an external N-FET balancing cell 1. May leave this pin unconnected if not used.
EQ2	26	DO	Cell Equalization control output used to drive an external N-FET balancing cell 2. May leave this pin unconnected if not used.
EQ3	24	DO	Cell Equalization control output used to drive an external N-FET balancing cell 3. May leave this pin unconnected if not used.
EQ4	22	DO	Cell Equalization control output used to drive an external N-FET balancing cell 4. May leave this pin unconnected if not used.
EQ5	20	DO	Cell Equalization control output used to drive an external N-FET balancing cell 5. May leave this pin unconnected if not used.
EQ6	18	DO	Cell Equalization control output used to drive an external N-FET balancing cell 6. May leave this pin unconnected if not used.
EQ7	16	DO	Cell Equalization control output used to drive an external N-FET balancing cell 7. May leave this pin unconnected if not used.
EQ8	14	DO	Cell Equalization control output used to drive an external N-FET balancing cell 8. May leave this pin unconnected if not used.
EQ9	12	DO	Cell Equalization control output used to drive an external N-FET balancing cell 9. May leave this pin unconnected if not used.
EQ10	10	DO	Cell Equalization control output used to drive an external N-FET balancing cell 10. May leave this pin unconnected if not used.
EQ11	8	DO	Cell Equalization control output used to drive an external N-FET balancing cell 11. May leave this pin unconnected if not used.
EQ12	6	DO	Cell Equalization control output used to drive an external N-FET balancing cell 12. May leave this pin unconnected if not used.
EQ13	4	DO	Cell Equalization control output used to drive an external N-FET balancing cell 13. May leave this pin unconnected if not used.
EQ14	2	DO	Cell Equalization control output used to drive an external N-FET balancing cell 14. May leave this pin unconnected if not used.
EQ15	80	DO	Cell Equalization control output used to drive an external N-FET balancing cell 15. May leave this pin unconnected if not used.
EQ16	78	DO	Cell Equalization control output used to drive an external N-FET balancing cell 16. May leave this pin unconnected if not used.
FAULT_N	40	DO	Single-ended active-low fault output. Leave this pin unconnected if not used.
FAULTH–	56	DI	Inverting, high-side differential connection to the FAULTL– pin of the higher adjacent module in a daisy chain. Leave this pin unconnected if not used.

### Pin Functions (continued)

NAME		TYPE <sup>(1)</sup>	DESCRIPTION
PIN	NO.		
FAULTH+	57	DI	Non-inverting, high-side differential connection to the FAULTL+ pin of the higher adjacent module in a daisy chain. Leave this pin unconnected if not used.
FAULTL–	51	DO	Inverting, low-side differential connection to the FAULTH– pin of the lower adjacent module in a daisy chain. Leave this pin unconnected if not used.
FAULTL+	50	DO	Non-inverting, low-side differential connection to the FAULTH+ pin of the lower adjacent module in a daisy chain. Leave this pin unconnected if not used.
GPIO0	47	DIO	General Purpose I/O. Optionally use this pin as an external FAULT input or address assignment. <i>Do not allow GPIO pins to float when configured as inputs.</i>
GPIO1	46	DIO	General Purpose I/O. Optionally use this pin as an external FAULT input or address assignment. <i>Do not allow GPIO pins to float when configured as inputs.</i>
GPIO2	45	DIO	General Purpose I/O. Optionally use this pin as an external FAULT input or address assignment. <i>Do not allow GPIO pins to float when configured as inputs.</i>
GPIO3	44	DIO	General Purpose I/O. Optionally use this pin as an external FAULT input or address assignment. <i>Do not allow GPIO pins to float when configured as inputs.</i>
GPIO4	43	DIO	General Purpose I/O. Optionally use this pin as an external FAULT input or address assignment. <i>Do not allow GPIO pins to float when configured as inputs.</i>
GPIO5	42	DIO	General Purpose I/O. Optionally use this pin as an external FAULT input. <i>Do not allow GPIO pins to float when configured as inputs.</i>
NC1	36	NC	Do not connect to this pin. <i>This pin must remain floating for correct operation.</i>
NC2	75	NC	Do not connect to this pin. <i>This pin must remain floating for correct operation.</i>
NPNB	71	AO	Internal voltage regulator controller output pin. Connect to the base of the external NPN transistor. Leave unconnected if not used.
OUT1	73	AO	Analog multiplexer output. Connect a 390-pF filter capacitor type C0G or NP0 between this pin and AGND. Connect externally to pin OUT2. Internally tied to pin OUT2.
OUT2	68	AI	ADC input pin. Connect externally to pin OUT1. Internally tied to pin OUT1.
RX	39	DI	Single-ended UART receive input. This pin must be either: <ul style="list-style-type: none"> <li>Driven from a UART signal OR</li> <li>Pulled up to VIO</li> </ul> Do not allow this pin to float at any time.
TOP	76	P	Power supply input and module voltage-measurement pin. Connect to the top cell of the module through a series resistor. Requires a decoupling capacitor <sup>(3)</sup> from TOP to the ground plane. See <a href="#">TOP Pin Connection</a> for details. Locate decoupling capacitor as close to pin as possible. The low-pass filter created by the RC should have a tau similar to the low-pass filter used in the VSENSE circuits. See <a href="#">VP Regulated Output</a> or <a href="#">Application and Implementation</a> for component selection details.
TX	38	DO	Single-ended UART transmit output. Leave this pin unconnected if not used.
V5VAO	58	P	Connection to internal 5-V always-on supply. Decouple with a 4.7-μF capacitor <sup>(3)</sup> connected to the ground plane. Locate decoupling capacitor as close to pin as possible. This pin should not be used to supply external circuitry.
VDIG	34	P	5.3-V Digital Supply input. Always connect VDIG to VP with 1-Ω resistor. Decouple with 4.7-μF and 0.1-μF capacitors <sup>(3)</sup> in parallel to the ground plane. Locate decoupling capacitors as close to the VDIG pin as possible.
VIO	41	P	3-V to 5-V power input for IO supply. Connect this pin to the same power supply used to drive the source/receiver for the GPIO, FAULT_N, RX, and TX pins. Typically, connect this pin to VP/VDIG for all devices except the base device in the stack. In the base (or single) device, this pin is typically driven from the same supply as the microcontroller I/O pins. If VP/VDIG is connected as the power source, this pin should be decoupled with a 0.1-μF capacitor <sup>(3)</sup> to the digital ground plane. Place a 1-Ω resistor in series from VP to VIO. Locate the decoupling capacitor as close to the VIO pin as possible. If another supply is used, decouple with parallel 10-μF and 0.1-μF capacitors <sup>(3)</sup> .
VM	31	P	Internal –5-V charge pump output. Decouple with 4.7-μF and 0.1-μF capacitors <sup>(3)</sup> in parallel to the ground plane. Locate decoupling capacitor as close to pin as possible.

### Pin Functions (continued)

NAME		TYPE <sup>(1)</sup>	DESCRIPTION
PIN	NO.		
VP	70	P	5.3-V regulated analog power supply input/sense pin. Connect to external NPN transistor's emitter and decouple with a 0.1-μF capacitor <sup>(3)</sup> to AGND and a 4.7-μF capacitor <sup>(3)</sup> in series with a 0.390-Ω resistor to GND. Locate decoupling capacitors as close to the VP pin as possible. Always connect VDIG to VP with 1-Ω resistor.
VREF	67	P	VREF output filter pin. Decouple with parallel 0.1-μF and 1.8-μF (25 V+) capacitors <sup>(3)</sup> to the ground plane. Locate decoupling capacitors as close to the pin as possible. To maintain measurement fidelity, do not place external loads on this pin.
VSENSE0	29	AI	Connect to the negative pin of the 1 <sup>st</sup> cell.
VSENSE1	27	AI	Channel 1. Connect to the positive pin of the 1 <sup>st</sup> cell.
VSENSE2	25	AI	Channel 2. Connect to the positive pin of the 2 <sup>nd</sup> cell.
VSENSE3	23	AI	Channel 3. Connect to the positive pin of the 3 <sup>rd</sup> cell.
VSENSE4	21	AI	Channel 4. Connect to the positive pin of the 4 <sup>th</sup> cell.
VSENSE5	19	AI	Channel 5. Connect to the positive pin of the 5 <sup>th</sup> cell.
VSENSE6	17	AI	Channel 6. Connect to the positive pin of the 6 <sup>th</sup> cell.
VSENSE7	15	AI	Channel 7. Connect to the positive pin of the 7 <sup>th</sup> cell.
VSENSE8	13	AI	Channel 8. Connect to the positive pin of the 8 <sup>th</sup> cell.
VSENSE9	11	AI	Channel 9. Connect to the positive pin of the 9 <sup>th</sup> cell.
VSENSE10	9	AI	Channel 10. Connect to the positive pin of the 10 <sup>th</sup> cell.
VSENSE11	7	AI	Channel 11. Connect to the positive pin of the 11 <sup>th</sup> cell.
VSENSE12	5	AI	Channel 12. Connect to the positive pin of the 12 <sup>th</sup> cell.
VSENSE13	3	AI	Channel 13. Connect to the positive pin of the 13 <sup>th</sup> cell.
VSENSE14	1	AI	Channel 14. Connect to the positive pin of the 14 <sup>th</sup> cell.
VSENSE15	79	AI	Channel 15. Connect to the positive pin of the 15 <sup>th</sup> cell.
VSENSE16	77	AI	Channel 16. Connect to the positive pin of the 16 <sup>th</sup> cell.
WAKEUP	49	DI	Wakeup input. Pull this pin low or tie to ground if not used. <i>Do not allow this pin to float at any time.</i>

(1) Key: AI = analog input; AO=analog output; DI = digital input; DO= digital output; DIO= digital I/O; P= Power; NC= no connect.

(2) Externally connected pins as common ground or GND in the design. See [Grounding](#) for details.

(3) All capacitors are type X7R or better, unless otherwise noted.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over specified Ambient Temperature range (unless otherwise noted) <sup>(1)(2)</sup>

		MIN	MAX	UNIT
VP		–0.3	6	V
VDIG		–0.3	6	V
VIO		–0.3	6	V
AUX0–7	Lesser of two MAX values	–0.3	6 or (VP + 0.3)	V
	Lesser of two MAX values	–0.3	6 or (V5VAO + 0.3)	V
COMMH+, COMMH–, COMML+, COMMH–, FAULTH+, FAULTH–, FAULTL+, FAULTL–	AC pulse specification <sup>(3)</sup> for these eight pins only: V <sub>pk</sub> maximum ≤ 6.5 V for 100 ns or less, 100 kHz ≤ f ≤ 400 MHz	–0.3	6.5	V <sub>pk</sub>
GPIO0–5	Lesser of two MAX values	–0.3	6 or (VIO + 0.3)	V
RX	Lesser of two MAX values	–0.3	6 or (VIO + 0.3)	V
TOP <sup>(4)</sup>		–0.3	88	V
TOP to VSENSE16 delta <sup>(4)(5)</sup>	(VSENSE16 + 5.5 V) ≥ TOP ≥ (VSENSE16 – 1 V)	(VSENSE16 – 1 V)	(VSENSE16 + 5.5 V)	V
VSENSE0		–0.3	0.3	V
VSENSEn – VSENSEn–1	n = 1 to 16	–0.3	5.5	V
	n = 1 to 16, 0.1% duty cycle	–0.3	6.5	
WAKEUP		–0.3	6	V
Ambient free-air temperature, T <sub>A</sub>		–40	105	°C
Junction temperature, T <sub>J</sub>		–40	125	°C
Storage temperature, T <sub>stg</sub>		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Unless otherwise noted, voltages are given with respect to device commons (AGND1–3, DGND1–3, CGND) tied together (device VSS or GND).
- (3) Specified by design, not tested in production.
- (4) Must meet all stated conditions for the TOP pin at all times.
- (5) Must short the highest-connected cell to the unused VSENSEn inputs above it in configurations that use < 16 cells. For example, a 14-cell configuration must short pins VSENSE14, VSENSE15, VSENSE16.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	All pins	±2000	V
		All pins except 1, 20, 21, 40, 41, 60, 61, 76, and 80	±500	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	Pin 76	±450	
		Corner pins (1, 20, 21, 40, 41, 60, 61, and 80)	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



### 6.3 Recommended Operating Conditions

$T_A = 25^\circ\text{C}$  and  $TOP = 57.6\text{ V}$ ; Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  and  $TOP = 12\text{ V}$  to  $79.2\text{ V}$  (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{TOP}$	Supply voltage	$TOP - GND$ ( $V_{SENSE16} = TOP$ )	12		79.2	V
$V_{IO}$	Digital interface voltage		2.7		5.5	V
$V_{TOP\_DELTA}$	Max delta, TOP to highest cell <sup>(1)(2)</sup>	$V_{SENSE16} - TOP$		0	300	mV
$I_{IO}$	Output current, any one pin	GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, TX, FAULT_N			5	mA
$I_{IO\_T}$	Output current, sum of	GPIO0 + GPIO1 + GPIO2 + GPIO3 + GPIO4 + GPIO5 + TX + FAULT_N			20	mA

- $V_{SENSE}$  input measurement accuracy is degraded when  $V_{TOP\_DELTA}$  is exceeded. Delta cannot exceed the limit in the [Absolute Maximum Ratings](#) table.
- Must short the highest-connected cell to the unused  $V_{SENSEn}$  inputs above it in configurations that use  $< 16$  cells. For example, a 14-cell configuration must short pins  $V_{SENSE14}$ ,  $V_{SENSE15}$ , and  $V_{SENSE16}$ .

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		bq76PL455A	UNIT
		TQFP (PFC)	
		80 PINS	
$R_{\theta JA}$ , High K	Junction-to-ambient thermal resistance	44.3	$^\circ\text{C/W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.4	$^\circ\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	21.5	$^\circ\text{C/W}$
$\Psi_{JT}$	Junction-to-top characterization parameter	0.2	$^\circ\text{C/W}$
$\Psi_{JB}$	Junction-to-board characterization parameter	21	$^\circ\text{C/W}$
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	—	$^\circ\text{C/W}$

- For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 6.5 Electrical Characteristics: Supply Current<sup>(1)</sup>

The following applies to all Electrical Characteristics in the following tables, unless otherwise noted: TYP values are stated in each table where  $VP = V_{DIG} = 5.3\text{ V}$ ,  $V_{IO} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  and  $V_{CELL} = 3.6\text{ V}$  ( $V_{CELL} = V_{SENSEn} - V_{SENSEn-1}$ ;  $n=1$  to 16),  $TOP = 57.6\text{ V}$ . MIN/MAX values are stated where  $VP = V_{DIG} = 5.3\text{ V}$ ,  $V_{IO} = 5\text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ ,  $1\text{ V} < V_{CELL} < 4.95\text{ V}$ ,  $12\text{ V} \leq TOP < 79.2\text{ V}$  and  $GND = 0\text{ V}$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IDLE}$	Total input current from the monitored cells. Power state: IDLE <sup>(2)</sup>	4	5	7	mA
$I_{TOP\_IDLE}$	Input current into TOP pin, IDLE mode Power state: IDLE <sup>(2)</sup>	250	350	450	$\mu\text{A}$
$I_{SLEEP}$	Total input current from the monitored cells into TOP pin Power state: SHUTDOWN <sup>(3)</sup> $VP = V_{DIG} = V_{IO} = 0\text{ V}$ , $TOP = 57.6$		22	50	$\mu\text{A}$
$I_{ACTIVE}$ <sup>(4)</sup>	Total input current from the monitored cells while communicating. Power state: IDLE plus comms <sup>(5)</sup> , differential comm capacitance 70 pF, no load on GPIO.		8		mA
$I_{VIO\_IDLE}$	VIO input current Power state: IDLE <sup>(2)</sup>		40		$\mu\text{A}$
$I_{SLP\_DELTA}$ <sup>(4)</sup>	Delta $I_{SHUTDOWN}$ between devices in a stack $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ for all devices		4	10	$\mu\text{A}$

- All internal pull-up and pull-down resistors are disabled and their current is not included in parameters listed in this table.
- IDLE mode defined as: device awake, ready for communications, and not communicating.
- SHUTDOWN mode defined as: test conditions, no communications, no wakeup tone activity, and no FAULT heartbeat.
- Specified from characterization data.
- ACTIVE mode defined as: UART, differential communications link, and FAULT heartbeat active.



## 6.6 VP 5.3-V Supply Regulation Voltage

Characteristics stated using NPN transistor in circuit rated at  $BV_{CEO} > 100V$ ,  $\beta \geq 100$  at 5 mA, Base-Collector C  $\leq 35$  pF,  $I_{COLLECTOR} > 100$  mA,  $R_{COLLECTOR} = 400 \Omega$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VP_{VR}$ Regulated Voltage		5.1	5.3	5.5	V
$I_{NPNB}$ External NPN base drive current		0.5			mA
$VP_{SD\_DLY}$ VP/VDIG delay before SHUTDOWN <sup>(1)</sup>		30	75	160	ms

- (1) Time measured from VP falling below threshold until the part enters SHUTDOWN, or from the part attempting to exit SHUTDOWN (wake-up) until re-entering SHUTDOWN.

## 6.7 VDD18 1.8-V Internal Digital Supply<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VDD18_{VO}$ VDD18 Output voltage <sup>(1)</sup>	As measured by internal ADC	1.7	1.8	1.9	V

- (1) Internal node only, no external access. This parameter is for internal measurement and verification purposes only.

## 6.8 V5VAO Analog Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V5VAO_{SD}$ Output Voltage	Power state: SHUTDOWN, VP = VDIG = VIO = 0 V	4	4.7	5.3	V
$V5VAO_{IDLE}$ Output Voltage	Power state: IDLE <sup>(1)</sup> , unloaded	VDIG – 0.5		VDIG	V

- (1) VDIG internally connected to V5VAO in IDLE mode.

## 6.9 VM –5-V Integrated Charge Pump

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VM_{VM\_ON}$ VM Output Voltage		–5.5	–5	–4.5	V
$f_{CP}$ Charge pump switching frequency			375		kHz
$VM_{TRIP}$ VM low-voltage monitor trip point			–3.8		V
$VM_{VO}$ Measured value read back from ADC VM monitor		–5.56	–5	–4.54	V

## 6.10 Analog-to-Digital Converter (ADC): Analog Front End

All ADC specifications stated are for the sampling intervals and register settings shown in [Table 3](#). A 390-pF capacitor is on pin OUT1.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$OUT1_{RANGE}$ Pin OUT1 Analog Front End / Level Shifter output voltage range		0		VP	V
$R_{OUT\_PIN}$ OUT1 pin internal series resistance		1	1.2	1.35	k $\Omega$

## 6.11 ADC: VSENSEn Cell Measurement Inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CELL_VR</sub>	Input voltage range	V <sub>CELL</sub> = VSENSEn – VSENSEn–1, n = 1 to 16	1		4.95	V
VCHERR25NB	Total Channel Measurement Accuracy at 25°C	VSENSE = 3.6 V		±0.75		mV
VCHERR	Total Channel Measurement Accuracy, temperature range of 0°C to 65°C <sup>(1)(2)</sup>	VSENSE = 1.5 V	–1.50		1.50	mV
		VSENSE = 2.0 V	–2.00		2.00	
		VSENSE = 3.3 V	–3.25		3.25	
		VSENSE = 3.6 V	–3.50		3.50	
		VSENSE = 4.2 V	–3.90		3.90	
		VSENSE = 4.5 V	–4.00		4.00	
VCHERR	Total Channel Measurement Accuracy, temperature range of –40°C to 85°C <sup>(1)(2)</sup>	VSENSE = 1.5 V	–2.85		2.85	mV
		VSENSE = 2.0 V	–3.00		3.00	
		VSENSE = 3.3 V	–4.75		4.75	
		VSENSE = 3.6 V	–5.00		5.00	
		VSENSE = 4.2 V	–5.50		5.50	
		VSENSE = 4.5 V	–5.75		5.75	
I <sub>SENSE_SEL</sub> <sup>(3)(4)</sup>	VSENSEn input current n = 1 to 16	VSENSEn–1 pin; on selected channel		2	7.6	μA
I <sub>SENSE_NSEL</sub>		Channel not selected		< ±100		nA
I <sub>SENSE_SD</sub>		VSENSEn input current in SHUTDOWN Mode		< ±100		nA
R <sub>SENSE_SEL</sub> <sup>(4)</sup>	VSENSE input resistance	Channel selected for conversion, measured differentially [VSENSEn–VSENSE(n–1)]		1		MΩ
OWD <sub>SR</sub>	Open-wire detection shunt resistance	Open-wire test mode, TSTCONFIG[4] = 1 all odd (CBENBL = 0xAA); or all even (CBENBL = 0x55) cell squeeze resistors on (alternate resistors only)	4			kΩ
LT_Drift <sub>VCHAN</sub>	Long-term drift (total channel path)	VSENSE = 4.5 V, T <sub>A</sub> = 65°C <sup>(5)</sup>		18.47		ppm/ 1000 hours
		VSENSE = 4.5 V, T <sub>A</sub> = 105°C <sup>(6)</sup>		50.24		
V <sub>ADC_REF_25</sub>	ADC reference			2.5		V
ERR <sub>ADC_REF_25</sub>	ADC reference error	0°C ≤ T <sub>A</sub> ≤ 65°C	–2.5		2.5	mV
		–40°C ≤ T <sub>A</sub> ≤ 85°C	–3.5		3.5	mV

(1) Error measured with averaging enabled.

(2) User adjustable Gain and Offset registers are provided for further error trim at VSGAIN and VSOFFSET, respectively.

(3) When the bq76PL455A is in IDLE power mode, but not converting any ADC input channel, the part idles the multiplexer on the highest channel enabled for conversions in the CHAN register.

(4) The current into VSENSEn = ISENSE\_SEL + VCELL/RSENSE\_SEL.

(5) Computed from the first 500-hour operating life test at a stress temperature of 65°C.

(6) Computed from the first 500-hour operating life test at a stress temperature of 105°C.

## 6.12 ADC: V<sub>MODULE</sub> Input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>MODULE_VR</sub>	Input voltage range	Measured from TOP to GND (AGND1)	V <sub>TOP</sub> MIN		V <sub>TOP</sub> MAX	V
V <sub>MODULE_ERR85</sub>	Total error from all internal sources	T <sub>A</sub> = −40°C to 85°C	−450	±100	450	mV

## 6.13 ADC: AUXn General Purpose Inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>AUX_VR</sub>	Input voltage range <sup>(1)</sup>	VP/VDIG = 5.3 V	0		5	V
V <sub>AUXERR65</sub>	Total AUX Channel Measurement Accuracy <sup>(2)</sup>	VAUX = 0.05 V, 0°C ≤ T <sub>A</sub> ≤ 65°C	−3	0.1	3	mV
		VAUX = 4.95 V, 0°C ≤ T <sub>A</sub> ≤ 65°C	−10	0.1	10	mV
V <sub>AUXERR85</sub>	Total AUX Channel Measurement Accuracy <sup>(2)</sup>	VAUX = 0.05 V, −40°C ≤ T <sub>A</sub> ≤ 85°C	−4.5	0.1	4.5	mV
		VAUX = 4.95 V, −40°C ≤ T <sub>A</sub> ≤ 85°C	−12.5	0.1	12.5	mV

(1) Specified by design, not tested in production.

(2) Calculated and statistically projected worst case from characterization data. Not tested in production.

## ADC: AUXn General Purpose Inputs (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DCL\_AUX}$	DC Leakage Current Channel not selected for conversion, TESTAUXPU = 0		< ±0.1		μA
$R_{IN\_AUX}^{(1)}$	Equivalent input resistance Channel selected In Acquisition Mode		> 3		MΩ
$C_{AUX}^{(1)}$	Input capacitance Channel selected		30		pF
$R_{AUX\_PU}$	Internal switched pull-up resistor per AUXn input, supplied from VP pin TESTAUXPU[n] = 1; n = 0 to 7	18	26	46	kΩ

## 6.14 ADC: Internal Temperature Measurement and Thermal Shutdown (TSD)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{INT\_AD}^{(1)}$	Internal temperature accuracy of analog die	–7	3	13	°C
$T_{INT\_DD}^{(1)}$	Internal temperature accuracy of digital die	–34	8	54	°C
$TSD_T^{(2)}$	Thermal shutdown, junction temperature both analog and digital dies Increasing temperature	115	140		°C

(1) Specified from characterization data, not tested in production.

(2) Specified by design, not tested in production.

## 6.15 Passive Balancing Control Outputs

PARAMETER <sup>(1)</sup>	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$EQ_{SR\_OFF}$	Output resistance, internally in series with driver EQn = 0 (OFF)	1.2	1.5	1.8	kΩ
$EQ_{SR\_ON}$		1.9	2.3	2.9	kΩ
$EQ_{VMIN}^{(2)}$	Cell voltage required for balancing	1.8			V
$VS1_{MIN}$	VSENSE1 minimum voltage for balancing <sup>(3)</sup>	1.8			V

(1) For more functional information, see [Passive Balancing](#).

(2) In the event of an open wire condition, if TSTCONFIG[EQ\_SQUEEZE\_EN] = 1 and this causes EQVMIN to be violated, it may be necessary to power down the device to disable the squeeze resistor.

(3) VSENSE1 minimum voltage required for correct operation of any or all EQn outputs. If VSENSE1 falls below this value, any or all other EQ outputs may fail to assert when requested. The opposite is not true. Outputs will not assert unintentionally when set to the OFF state.

## 6.16 Digital Input/Output: VIO-Based Single-Ended I/O

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	Logic-level output-voltage high FAULT_N, TX, GPIO $I_{LOAD} = 5\text{ mA}$	VIO – 0.7		VIO	V
$V_{OL}$	Logic-level output-voltage low FAULT_N, TX, GPIO $I_{LOAD} = 5\text{ mA}$	DGND		0.7	V
$V_{IH}$	Logic-level input-voltage high RX, GPIO	VIO – 0.7			V
$V_{IL}$	Logic-level input-voltage low RX, GPIO			0.7	V
$C_{DIG\_IN}$	Input Capacitance <sup>(1)</sup> RX, GPIO		5		pF
$R_{PU}$	GPIO0..5 pull-up resistor	13	17	25	kΩ
$R_{PD}$	GPIO0..5 pull-down resistor	16	22	31	kΩ
$I_{LKG}$	Input leakage source/sink current RX, GPIOx		< ±1		μA
$RXTX_{BAUD}$	RX/TX signaling rate <sup>(2)(3)</sup>	125		1000	Kbaud
$ERR_{BAUD\_RX}$	Input Baud rate error <sup>(1)</sup>	–3%		3%	
$ERR_{BAUD\_TX}$	Output Baud rate error <sup>(1)</sup>	–1.5%		1.5%	
$t_{COMM\_BREAK}$	Communications Clear (Break) <sup>(1)</sup>	10		15	bit periods
$t_{COMM\_RESET}$	Communications Reset <sup>(1)</sup>	200			μs

(1) Specified by design, not tested in production.

(2) Defaults: RX = TX = 250 kBd at communications RESET or (factory set) EEPROM setting at POR.

(3) Discrete rates only, not continuously variable.

## 6.17 Digital Input/Output: Daisy Chain Vertical Bus

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH_DCC_TX</sub>	Logic level output voltage high	Single driver loaded, I <sub>LOAD</sub> = 5 mA	VDIG-1	VDIG	V
V <sub>OL_DCC_TX</sub>	Logic level output voltage low	Single driver loaded, I <sub>LOAD</sub> = 5 mA	GND	1	V
T <sub>PD</sub>	Internal propagation delay, COMML to COMMH <sup>(1)</sup>		<60		ns
T <sub>DCC_BIT_TIME</sub>	Diff. Comms. Bit Time <sup>(1)</sup>		250		ns
f <sub>WAKE_TONE</sub>	WAKE TONE frequency <sup>(1)</sup>	50% duty-cycle WAKE TONE transmitted on differential pins COMMH+/COMMH-	100		kHz
t <sub>WAKE_TONE</sub>	WAKE TONE duration <sup>(1)</sup>	WAKE TONE transmitted on differential pins COMMH+/COMMH-	1		ms

(1) Specified by design, not tested in production.

## 6.18 Digital Input/Output: Wakeup

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IH_WAKEUP</sub>	WAKEUP high-input voltage	2.3			V
V <sub>IL_WAKEUP</sub>	WAKEUP low-input voltage			0.7	V
t <sub>WAKEUP_HOLD</sub> <sup>(1)</sup>	WAKEUP hold time (high-pulse width)	Pulse driven 0-1-0	100		μs
t <sub>WAKEUP_DLY</sub>	Delay between WAKEUP pin assertion and WAKETONE transmission	Typical application circuit with typical components as outlined in the <a href="#">Application and Implementation</a> section.	1.2		ms
t <sub>WAKE_TONE_DELAY_DC</sub>	Delay <sup>(2)</sup> between start of WAKETONE received and WAKETONE transmission	After POR exit condition [VDD18 <sub>VO</sub> > 1.7 V] is met.		1.2	ms
t <sub>WAKEUP_TO_DCOMM</sub>	Required delay from WAKETONE transmission to ready for differential communications <sup>(3)</sup>			1.1	ms
t <sub>WAKEUP_TO_UART</sub>	Required delay from WAKETONE transmission to ready for UART communications <sup>(3)</sup>			200	μs

(1) Pulses shorter than 100 μs may wake the device, but must maintain 100 μs to assure start up.

(2) Environmental noise may affect tone detection.

(3) Specified by design, not tested in production.

## 6.19 EEPROM

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
EE <sub>PGM</sub> <sup>(1)</sup>	EEPROM total program time <sup>(2)</sup>	No writes to the device are allowed during the programming cycle	210	500	ms
EE <sub>CYCLES</sub>	Erase / Program cycles <sup>(2)</sup>			5	cycles
EE <sub>RETN</sub>	Data retention <sup>(2)(3)</sup>		10		years

(1) Program EEPROM temperature (T<sub>A</sub>) between 0°C and 30°C.

(2) Specified by design, not tested in production.

(3) Erase / Program cycles not to exceed EE<sub>CYCLES</sub>.

## 6.20 Secondary Protector – Window Comparators

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OV <sub>RANGE</sub>	Over-voltage comparator register set-point limits <sup>(1)</sup>		2		5.175	V
UV <sub>RANGE</sub>	Under-voltage comparator register set-point limits <sup>(1)</sup>		0.7		3.875	V
OVUV <sub>STEP</sub>	Threshold step resolution			25		mV
ERR <sub>CMP_UV</sub>	Total UV threshold error (includes ERR <sub>VCOMP_REF_45</sub> )	Vin = 0.7 to 3.875 V	−50		50	mV
ERR <sub>CMP_UV_EXT</sub>	UV threshold error when range-extend bit is set	COMP_UV[COMP_TST_SHF_UV] = 1	−100		100	mV
ERR <sub>COMP_OV</sub>	Total OV threshold error (includes ERR <sub>VCOMP_REF_45</sub> )	Vin = 2 to 5.175 V	−50		50	mV
ERR <sub>COMP_OV_EXT</sub>	OV threshold error when range-extend bit is set	COMP_UV[COMP_TST_SHF_OV] = 1	−60		60	mV
V <sub>COMP_HYST</sub>	Threshold hysteresis	Hysteresis enabled; DEVCONFIG[COMP_HYST_EN] = 1	50	85	130	mV

(1) Normal range specification. Ranges can be extended by using the COMP\_UV[COMP\_TST\_SHF\_UV] and COMP\_OV[COMP\_TST\_SHF\_OV] bits. See register bit description in [Table 7](#) for additional details.

## Secondary Protector – Window Comparators (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T <sub>COMP_UV</sub>	UVP Response time	Overdrive = 100 mV	20		μs
T <sub>COMP_OV</sub>	OVP Response time	Overdrive = 100 mV	20		μs
V <sub>COMP_REF_45</sub>	Comparator reference	Measured by ADC as HREF - HREF_GND	4.5		V
ERR <sub>VCOMP_REF_45</sub>	Comparator reference error	0°C ≤ T <sub>A</sub> ≤ 65°C, measured by ADC	–22	–7	9.5
		–40°C ≤ T <sub>A</sub> ≤ 85°C, measured by ADC	–27	–7	15

## 6.21 Power-On-Reset (POR) and FAULT Flag Thresholds

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP <sub>FLT_TRIP</sub>	VP_FAULT voltage threshold, analog die	Falling VP	4.3	4.5	4.7
		Rising VP	4.3	4.5	4.7
VM <sub>FLT_TRIP</sub>	VM_FAULT voltage threshold, analog die	Falling VM (more negative)	–4.2	–4	–3.8
		Rising VM (more positive)	–3.9	–3.8	–3.7
DDIE <sub>POR</sub>	VP/VDIG POR voltage threshold, digital die	Falling voltage, VP connected to VDIG	3.9	4.15	4.4
		Rising voltage, VP connected to VDIG	4.1	4.5	4.7
V5VAO <sub>SD</sub>	V5VAO SHUTDOWN voltage threshold, digital die	Falling V5VAO	1.8	2.3	2.8
		Rising V5VAO		2.5	
VIO <sub>POR</sub>	VIO POR voltage threshold, digital die	Falling VIO	2.1	2.3	2.5
		Rising VIO	2.3	2.5	2.7
VIO <sub>SD_DLY</sub>	VIO delay before SHUTDOWN	VIO ≤ VIO <sub>POR</sub>	35	57	100

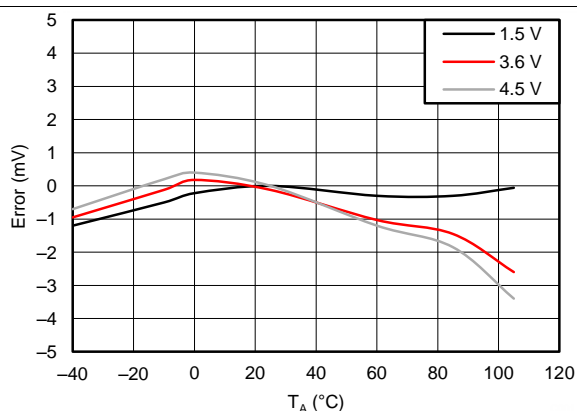
## 6.22 Miscellaneous

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>OSC</sub>	Main oscillator frequency (±1.5%)	47.28	48	48.72	MHz
f <sub>HBEAT</sub>	Fault tone (heartbeat) frequency at pins FAULTL±	No fault condition present, heartbeat enabled	10		kHz
HB <sub>PULSE</sub>	Fault heartbeat pulse width at pins FAULTL±	No fault condition present, heartbeat enabled	125		ns
t <sub>CKSUM_USER</sub>	Time to complete User-space checksum test <sup>(1)</sup>			5	ms
t <sub>CKSUM_TI</sub>	Time to complete TI-space checksum test <sup>(1)</sup>			5	ms
t <sub>CKSUM_PER</sub>	Period for automatic checksum updates <sup>(1)</sup>		2		μs
t <sub>ADCFullTest</sub>	Time to complete full ADC test <sup>(1)</sup>			450	ms
t <sub>ADCTest</sub>	Time to complete abbreviated ADC test <sup>(1)</sup>			15	ms
V <sub>HREF_GND_FAULT</sub>	Voltage threshold for 4.5-V reference ground fault <sup>(1)</sup>		0.96		V
V <sub>HREF_FAULT_OV</sub>	Overvoltage threshold for 4.5-V reference fault <sup>(1)</sup>		4.75		V
V <sub>HREF_FAULT_UV</sub>	Undervoltage threshold for 4.5-V reference fault <sup>(1)</sup>		4.25		V

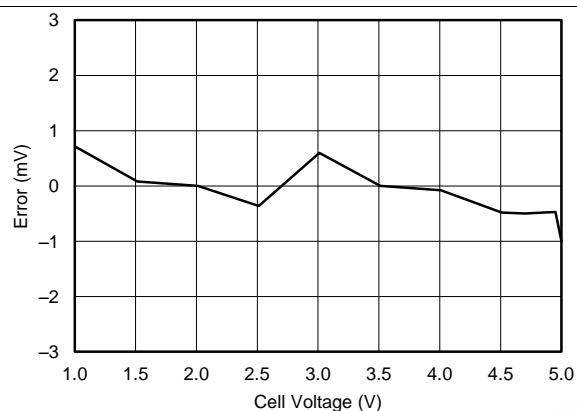
(1) Specified by design, not tested in production.

## 6.23 Typical Characteristics

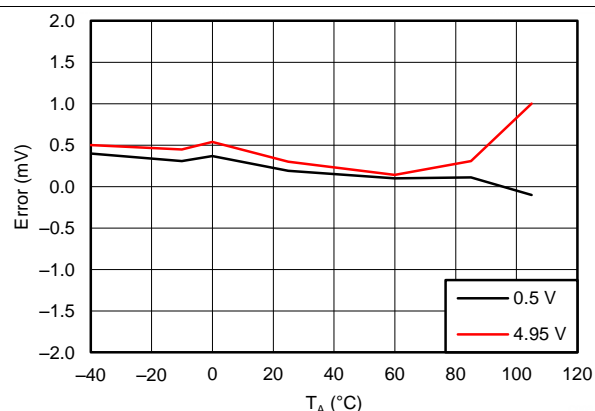
The following conditions apply: Typical Operating Circuit, VTOP = 60 V, 16 cells,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



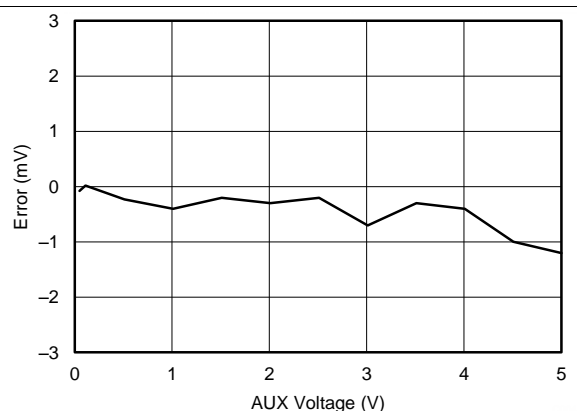
**Figure 1. Cell Voltage Measurement Error Versus Ambient Temperature**



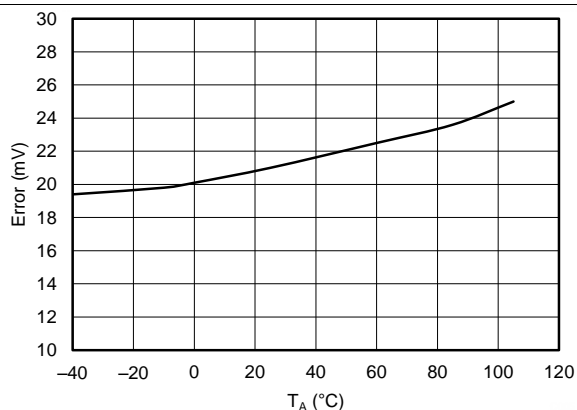
**Figure 2. Cell Voltage Measurement Error Versus Cell Voltage**



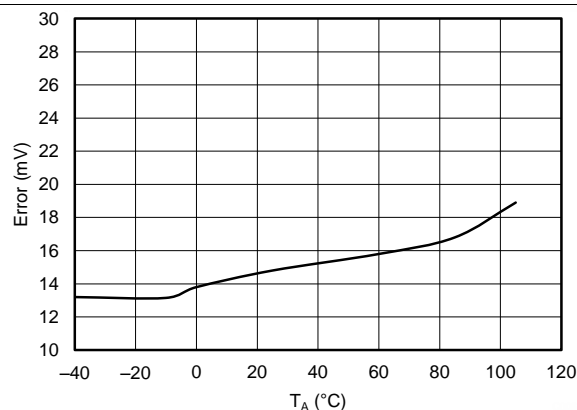
**Figure 3. AUX Measurement Error Versus Ambient Temperature**



**Figure 4. AUX Measurement Error Versus AUX Voltage**



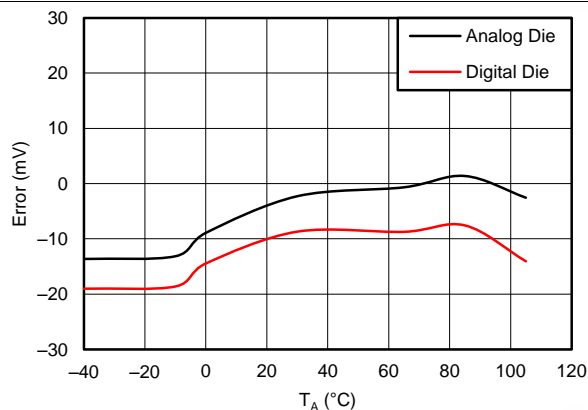
**Figure 5. Overvoltage Comparator Error Versus Ambient Temperature**



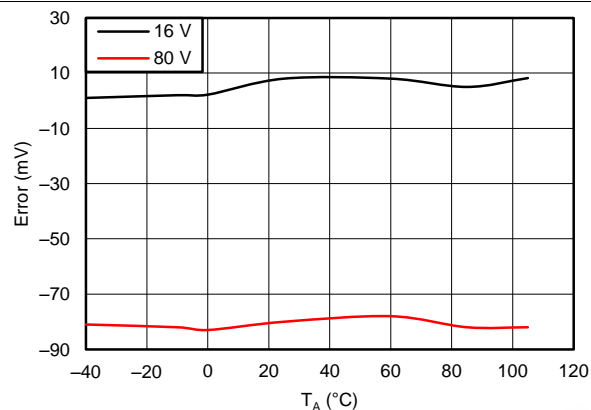
**Figure 6. Undervoltage Comparator Error Versus Ambient Temperature**

## Typical Characteristics (continued)

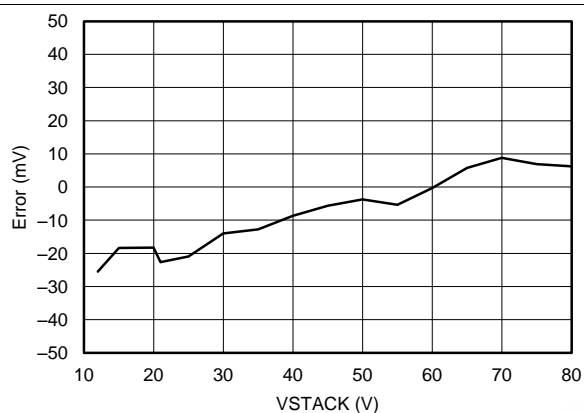
The following conditions apply: Typical Operating Circuit, VTOP = 60 V, 16 cells, T<sub>A</sub> = 25°C (unless otherwise noted)



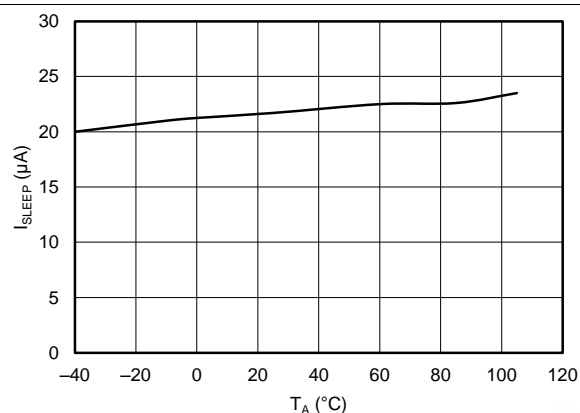
**Figure 7. DIE Temperature Measurement Error Versus Ambient Temperature**



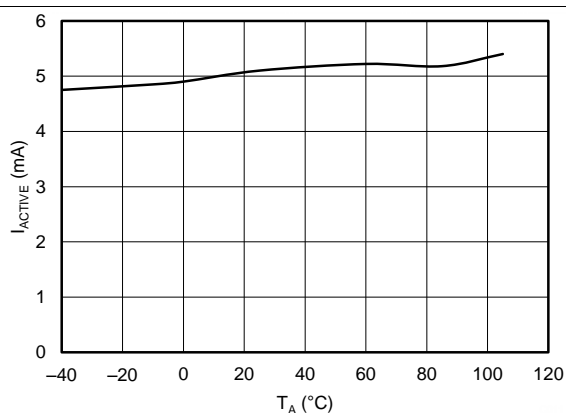
**Figure 8. Stack Measurement Error Versus Ambient Temperature**



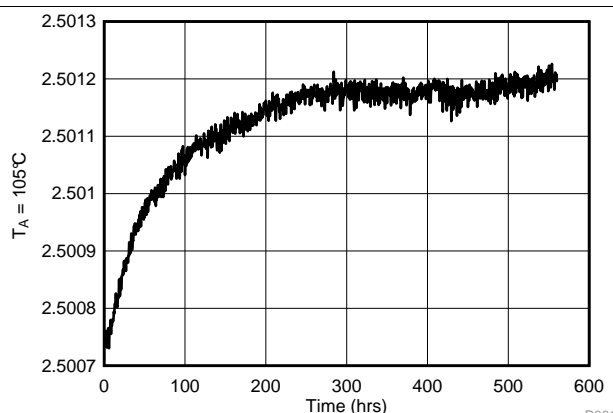
**Figure 9. Stack Measurement Error Versus Stack Voltage**



**Figure 10. SLEEP Current Versus Ambient Temperature**



**Figure 11. ACTIVE Current Versus Ambient Temperature**



**Figure 12. ADC VREF Long Term Drift at 105°C**



## 7 Detailed Description

### 7.1 Overview

The bq76PL455A is an integrated 16-cell monitor, protector, and cell balancer designed for high-reliability industrial applications with many built-in self-diagnostic features.

Up to 16 bq76PL455A devices can be connected in series using the high-speed differential communications interface, which has been evaluated for compliance with Bulk Current Injection (BCI) standards. This capacitor-isolated communications link provides effective common-mode noise rejection. The bq76PL455A communicates with the host through a high-speed UART interface. The bq76PL455A provides up to six general-purpose, programmable, digital I/O ports, as well as eight AUX ADC inputs, typically used to monitor externally supplied temperature sensors. Configuration of the digital I/O ports can be set to generate faults based on conditions set in register GP\_FLT\_IN. Further configuration of these faults can be for an indication of a fault on the FAULT\_N output pin.

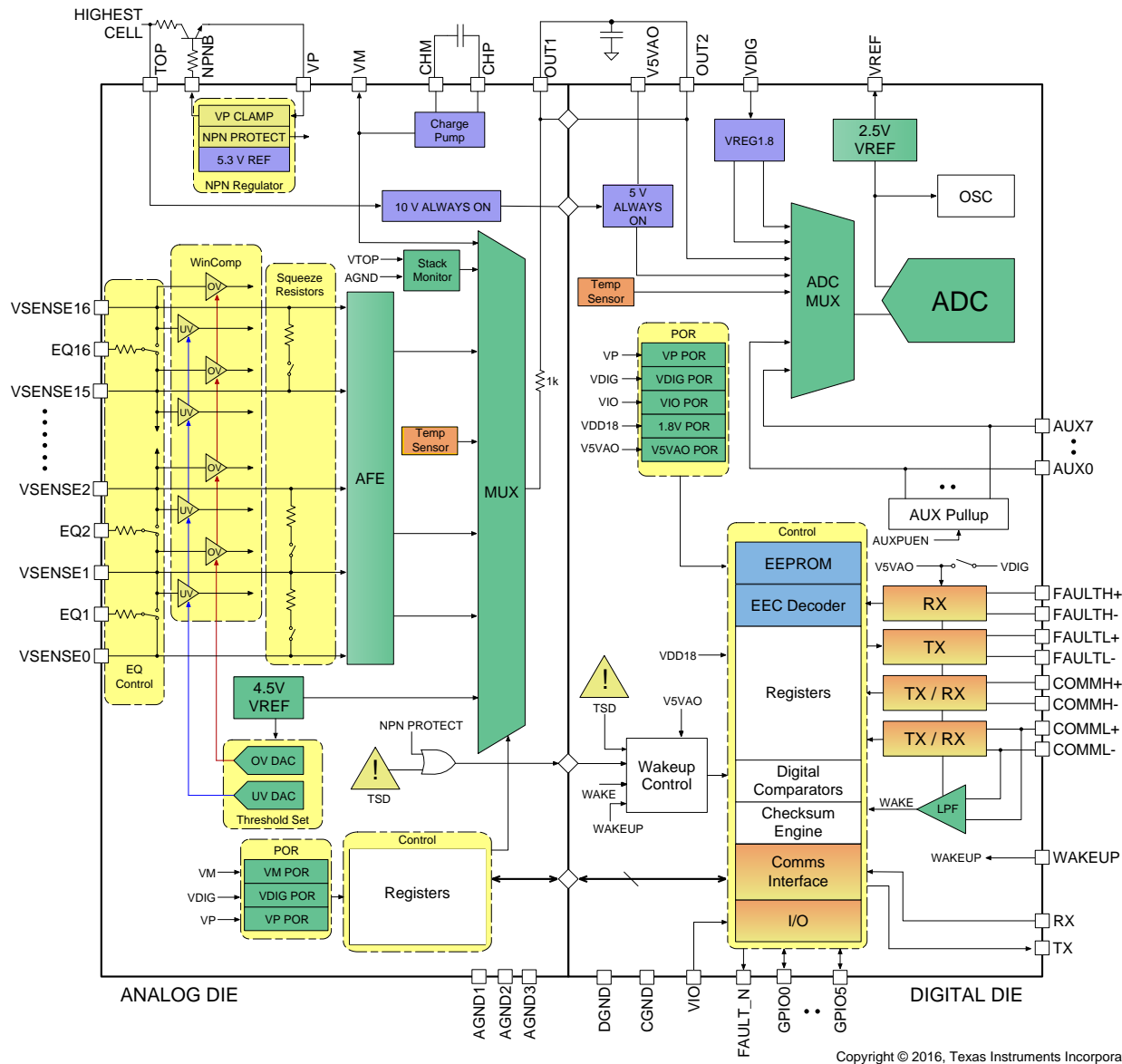
Designed for high-reliability industrial applications, the bq76PL455A includes many functional blocks and self-diagnostic test features covering defined single-fault conditions in analog and digital blocks. The host microcontroller receives fault notifications through a separate communications path. The device contains user-selectable self-test features to diagnose functional blocks within the device, such as automatic shutdown in the event of overtemperature, calibration integrity, and so forth. The [Safety Manual for bq76PL455A-Q1](#) (SLUUB67) is available upon request for reference to aid the user in the evaluation of the built-in test features of the bq76PL455A.

A provided built-in secondary protection block, with two dedicated programmable comparators per cell input, separately senses and reports overvoltage and undervoltage conditions. The comparators utilize a second separate testable internal band gap reference.

The bq76PL455A provides pins for direct drive of external N-FETs for passive cell balancing with power resistors. The balancing function configuration responds to on or off commands or specified to run for a specific time.

The device is powered from the stack of cells to which it is connected and all required voltages are generated internally.

## 7.2 Functional Block Diagram



### 7.3 Feature Description

### 7.3.1 Block Descriptions

#### 7.3.1.1 Power

The bq76PL455A operates from internally generated regulated voltages. The group of cells monitoring the device is the source for the internal regulators. Power comes from the most-positive and most-negative pins of the series-connected cells to minimize the likelihood of cell unbalancing. In most applications, the bq76PL455A operates using its internal supplies.



## Feature Description (continued)

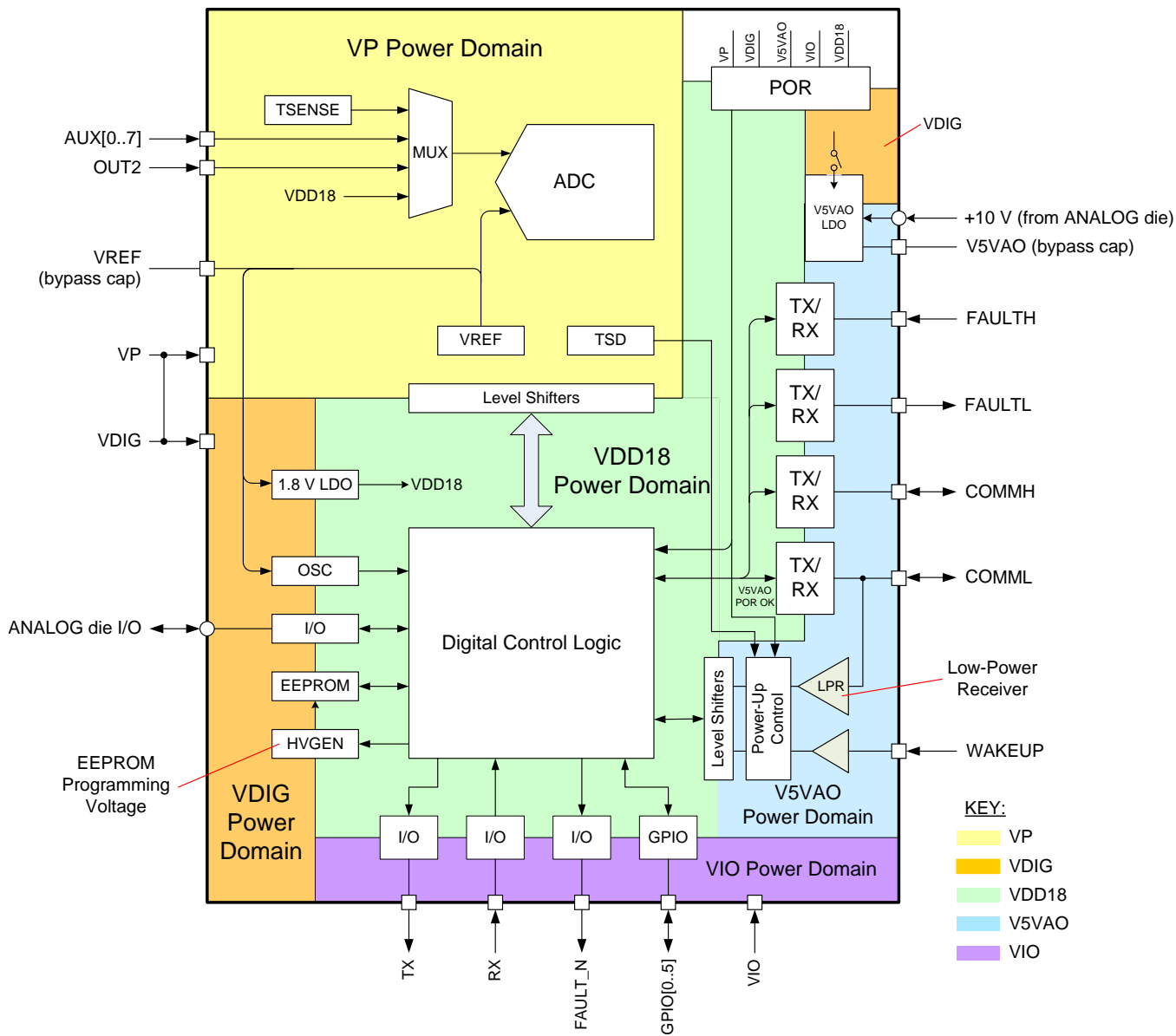
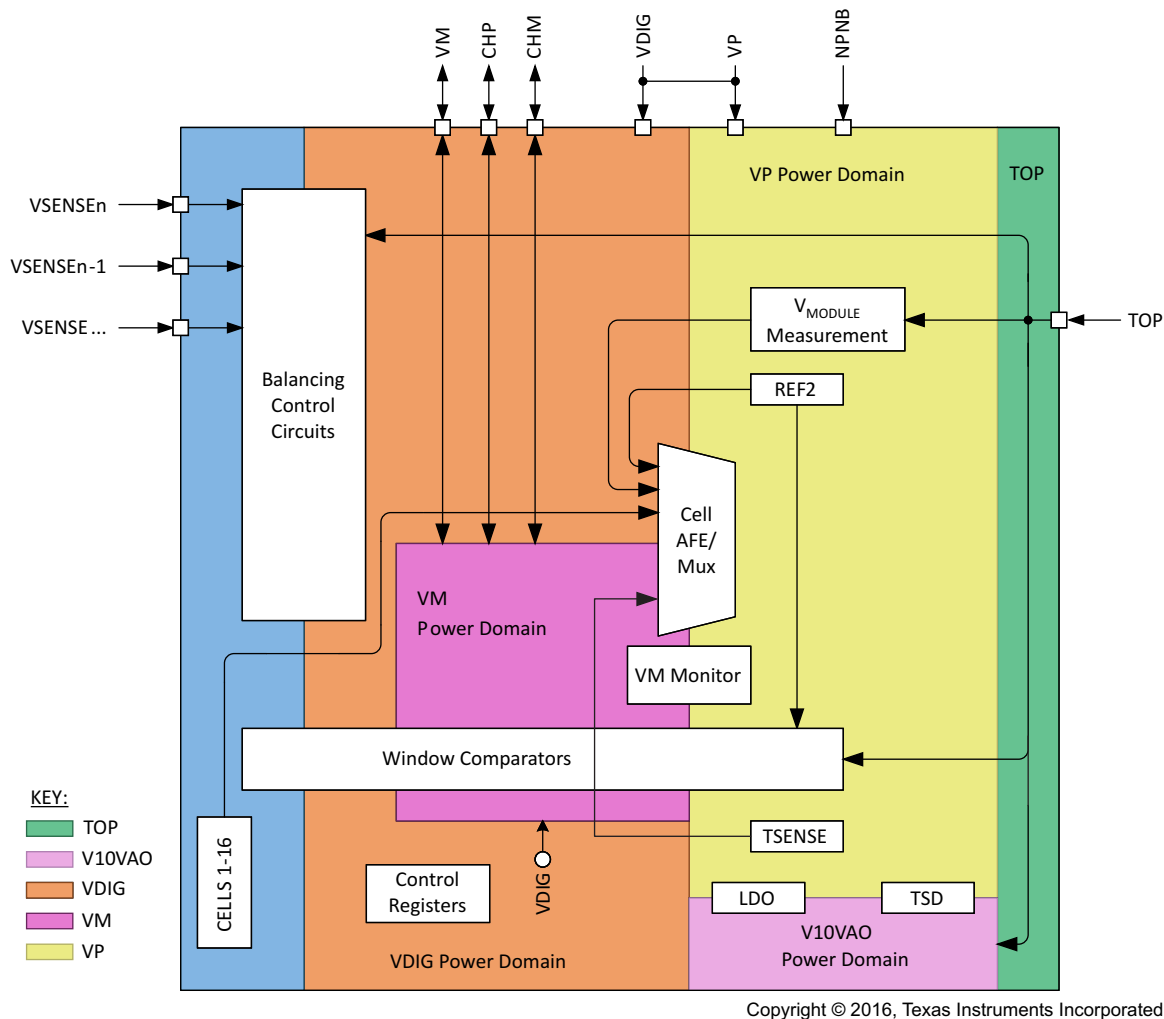


Figure 14. Digital Die Power Domains

## Feature Description (continued)



**Figure 15. Analog Die Power Domains**

### 7.3.1.1.1 TOP Pin Connection

The bq76PL455A has a connection from the top of the cell-module battery stack to the TOP pin, typically through an external-series resistor and capacitor to GND forming a low-pass filter. The low-pass filter design typically has a similar time constant to the VSENSE input pins. The minimum recommended values are 100  $\Omega$  and 0.1  $\mu\text{F}$ . See the [Application and Implementation](#) section for details.

### 7.3.1.1.2 V10VAO

V10VAO is an internal-only, always on, pre-regulator supplied from the TOP pin. It supplies the power to the V5VAO block, Analog Die TSD block, and VP control and regulator circuits. It is not externally accessible.

### 7.3.1.1.3 V5VAO

V5VAO is the always-on power supply that ensures power is supplied to the differential communications circuits (COMML+/-) and the WAKEUP input at all times. This ensures that the IC always detects the WAKEUP signal and the differential communications receive the WAKE tone. The V5VAO is supplied by a combination of an internal regulator and the VDIG supply. If VDIG falls below the normal operating voltage (during startup), the internal regulator supplies V5VAO. Once VDIG reaches regulation, V5VAO is supplied directly from VDIG.

## Feature Description (continued)

### NOTE

V5VAO can only supply enough power to meet internal IC requirements; it should not connect to external circuitry.

#### 7.3.1.1.4 VP Regulated Output

The bq76PL455A power comes directly from the cells to which it is connected. Current draw is from the top and bottom of the n-cell battery assembly, so that current through each cell is the same. An integrated linear regulator utilizes an external NPN transistor (Zetex ZXTN4004K or similar) to generate a nominal 5.3-V rail on pin VP. VP is both a power input and the sense node for this supply. The NPNB pin controls the external NPN transistor of the regulator. A capacitor or resistor-capacitor combination must connect externally from VP to GND, see [Pin Configuration and Functions](#) for details. VP must connect externally to VDIG and can optionally connect to VIO. Both of these connections are through series 1-Ω resistors and separately decoupled. This regulator is OFF in SHUTDOWN mode.

**Table 1. Recommended NPN Transistor Characteristics**

PARAMETER	DESCRIPTION	TEST CONDITION	TYPICAL VALUE	UNIT
BV <sub>CEO</sub>	Collector-Emitter voltage <sup>(1)</sup>		100	V
Beta β	Gain	at 5 mA	> 100	
C <sub>CB</sub>	Collector-Base capacitance		≤ 35	pF
P	Power handling <sup>(2)</sup>	See the following text for collector resistor details.	500	mW
IC	Collector current rating		> 100	mA

(1) Choose this value with respect to the locally supplied maximum-cell voltage and derate appropriately for operating conditions and temperature.

(2) Derate this value appropriately for operating conditions and temperature.

Add a collector resistor between the NPN collector and the TOP pin to reduce power dissipation in the NPN under normal and system fault conditions. The value of this resistor is chosen based on the minimum battery-stack voltage, the bq76PL455A VP/VDIG total load current, and the load current of any external I/O circuitry powered directly or indirectly by VP/VDIG. Also, the recommendation is to add a 1-μF decoupling capacitor directly from the collector to AGND.

#### 7.3.1.1.5 VDIG Power Input

VDIG is the digital voltage supply input. Always connect it to the VP pin, which normally receives power from the NPN. Optionally, an external supply may drive VDIG, but still must be connected to VP. This applies in all operating modes. The VDIG source is from VP through a 1-Ω resistor. Decouple VDIG with a separate capacitor at the pin.

#### 7.3.1.1.6 VDD18 Regulator

A provided internal regulator generates a 1.8-V digital supply for internal device use only. The 1.8-V supply does not require an external capacitor, and there is no pin or external connection. Faults on VDD18 that cause the voltage to drop below its regulation may cause UART communication errors. If the fault is caused by LDO\_TEST, reset or shutdown/wakeup the device to regain functionality.

#### 7.3.1.1.7 VIO Power Input

VIO is the voltage supply input used to power the digital I/O pins TX, RX, FAULT\_N, and GPIO<sub>n</sub>. VIO may connect to an externally regulated-supply rail, which is common to an I/O device such as a microcontroller. Alternately, the source for VIO may be from VP through a 1-Ω resistor. Decouple VIO with a separate capacitor at the pin.

If VIO does not have power, the part holds in reset and enters shutdown after a short delay. This gives a very good reset mechanism for non-stacked systems. Upon power up from a SHUTDOWN, the SHDN\_STS[GTSD\_PD\_STAT] bit will be set. This flag bit is the logical <OR> of this condition or triggering the thermal shutdown of the digital die in a die overtemperature situation.

### 7.3.1.1.8 VM Charge Pump

The included internal-charge pump is for biasing the Analog Front End (AFE) and other analog circuits. It requires an external flying capacitor connected between the CHP and CHM pins plus a storage capacitor on pin VM to generate a rail of  $-5\text{ V}$  for internal use. The charge pump (VM) is always on in IDLE and off in SHUTDOWN. VM requires the oscillator to be running and stable and does not start until the other supplies are above their POR thresholds. The VM charge pump will start ramping at the start of the WAKEUP tone on COMH.

### 7.3.2 Analog Front End (AFE)/Level Shifter

The bq76PL455A AFE allows monitoring of up to 16 cells. Provided for this purpose are seventeen VSENSE inputs, labeled VSENSE0 through VSENSE16. The programming for bq76PL455A can be set to sample all, or a subset, of the connected cells. Sampling always begins at the highest-selected cell and finishes with the lowest-selected cell. During measurement, the AFE selects the cell addressed by the logic block and level-shift the sensed cell voltage with a gain of 1 down to the ground-referred OUT1 pin. The output of the AFE (OUT1) has a See section " for component selection.

The analog output of the AFE connects to OUT1 through an internal  $1.2\text{-k}\Omega$  series resistor. Connect OUT1 externally to OUT2. At this external connection between the AFE and the ADC, the requirement is to place an external filter capacitor to form an RC filter to reduce noise bandwidth. A filter capacitor will increase the settling time of the signal presented to the ADC input. A trade-off can be made between ADC sample time, filtering, and accuracy. The AFE output must settle to within  $< 1/4$  of the ADC LSB for best measurement accuracy.

### 7.3.3 ADC

The ADC in the bq76PL455A is a 14-bit Successive Approximation Register (SAR) ADC. It has a fixed conversion (hold) time of  $3.44\text{ }\mu\text{s}$ , with a user-selectable sample interval or period between conversions. The user-selectable sample interval determines the acquisition (tracking) settling time between conversions, used mostly to allow the input capacitor on OUT1 to settle between conversions, and to allow for internal settling.

The ADC input mux on the digital die allows it to connect to the following:

- The AFE (analog die) mux output on OUT1 which measures:
  - Up to 16 cell voltage channels
  - The  $V_{\text{MODULE}}$  voltage
  - The internal temperature of the analog die
  - The REF2 analog die reference
  - The VM ( $-5\text{V}$ ) charge pump generated voltage supply on the analog die
- Measurement channels on the digital die:
  - The 8 AUX input channels
  - The VDD18  $1.8\text{-V}$  voltage supply on the digital die
  - The internal temperature of the digital die

The ADC can be set up to take single samples or multiple samples in one of two averaging modes. This selection is made using OVERSMPL[CMD\_OVS\_CYCLE].

#### 7.3.3.1 Channel Selection Registers

Program channels for measurement by setting bits in the CHANNELS and NCHAN registers. Each channel can be set up for measurement individually. User programmable correction factors are available for cell and AUX channels. Conversion times are individually user programmable for different types of inputs (that is, cells, AUX, and internal measurements).

The NCHAN register sets the number of VSENSE channels (cell inputs) for use by the device. Unused channels are dropped consecutively starting from channel 16. Set this register for the number of cells used, that is, for 14 cells, program  $0x0E$ . This register also sets mask cell overvoltage and undervoltage faults for unused channels, and turns off the UV and OV comparators associated with the channel. The idle channel (the channel the mux rests on between sample intervals) is set to the value in this register. This allows the OUT1 pin to hold the filter capacitor at the voltage, which will be sampled first on the next cycle.



### 7.3.3.2 Averaging

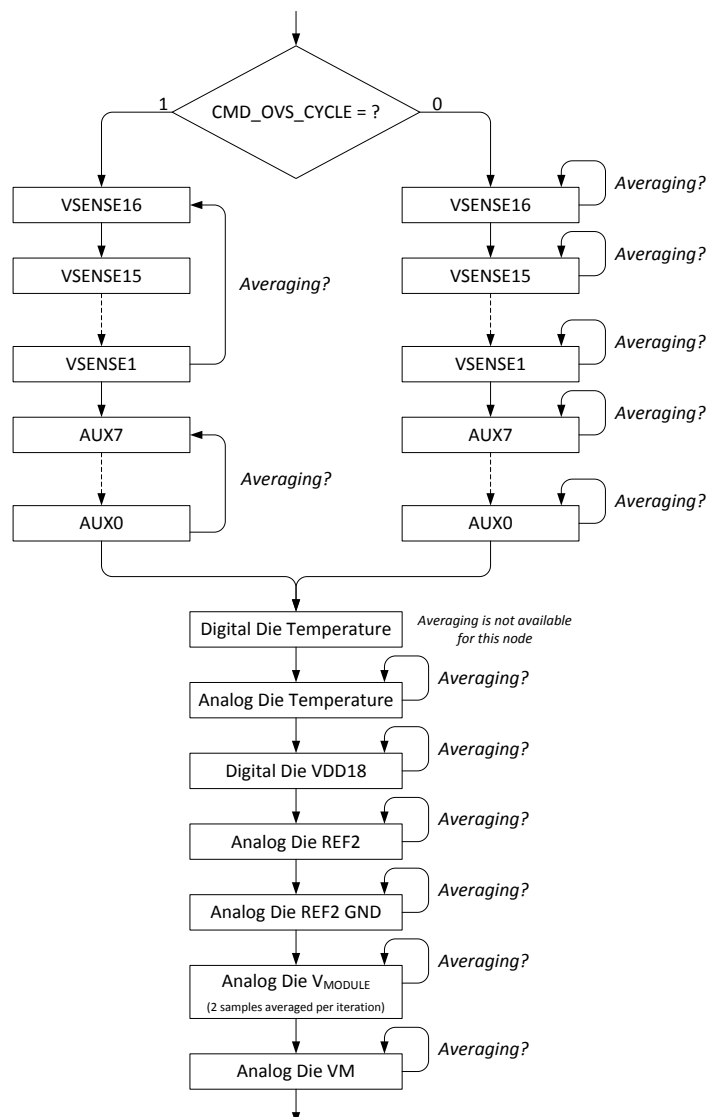
The oversampling for the ADC average measurements is programmable to 2, 4, 8, 16, or 32 times. Individual samples are arithmetically averaged by the bq76PL455A, which then outputs a single 16-bit (14 bits + 2 additional bits created by the averaging process) average measurement. The individual samples used to create the average value are not available.

As shown in Figure 16, the ADC averages any selected cell voltages first, then any selected AUX input channels, and then any remaining channels selected in the CHANNELS register in the order listed. Depending on the state of the CMD\_OVS\_CYCLE bit in the OVERSMPL register, oversampling of the Voltage and AUX channels follows one of the following procedures:

- Sampling each channel once and cycling through all channels before oversampling again in the case of CMD\_OVS\_CYCLE = 1 (cycled averaging) OR
- Sampling multiple times on a single channel before changing channel in the case of CMD\_OVS\_CYCLE = 0 (non-cycled averaging).

Figure 16 shows these on the left and right, respectively.

When oversampling, Table 2 shows the oversample periods for each channel after the first sample. The first sample can have a different period programmed (see Table 2), followed by all subsequent samples at different period shown in Table 3. The first sample and subsequent sample periods are separate of each other.



**Figure 16. Sampling/Oversampling (Averaging) Sequence**

**Table 2. Channel Sample Period Settings**

CHANNEL	FIRST SAMPLE	OTHER SAMPLES (AVERAGING)	
		CMD_OVS_CYCLE=0	CMD_OVS_CYCLE=1
VSENSEn (n=1..16)	ADC_PERIOD_VOL	CMD_OVS_HPER	ADC_PERIOD_VOL
AUXn (n=0..7)	ADC_PERIOD_AUXn	CMD_OVS_GPER	ADC_PERIOD_AUXn
DIGITAL DIE TEMP <sup>(1)</sup>	Approximately 50 $\mu$ s	n/a	n/a
ANALOG DIE TEMP	ADC_PERIOD_TEMP	CMD_OVS_HPER	CMD_OVS_HPER
VDD18	Approximately 30 $\mu$ s	CMD_OVS_GPER	CMD_OVS_GPER
ANALOG DIE VREF	ADC_PERIOD_REF	CMD_OVS_HPER	CMD_OVS_HPER
MODULE MONITOR <sup>(2)</sup>	ADC_PERIOD_MON	CMD_OVS_HPER	CMD_OVS_HPER
VM	ADC_PERIOD_VM	CMD_OVS_HPER	CMD_OVS_HPER

(1) Oversampling (averaging) is not available for this measurement.

(2) TSTCONFIG[MODULE\_MON\_EN] determines whether 2 conversions or 1 conversion takes place.

The ADC\_PERIOD\_VOL bits set the period between ADC samples for the indicated channels whether oversampling or not. When CMD\_OVS\_CYCLE = 1, the oversampling period of the Cell and AUX channels remains fixed at the single sample period of CELL\_SPER[ADC\_PERIOD\_VOL] and AUX\_SPER[ADC\_PERIOD\_AUX], respectively. Otherwise, if CMD\_OVS\_CYCLE = 0, then the oversample period for the Cell channels is set by bits CMD\_OVS\_HPER and for the AUX channels is CMD\_OVS\_GPER.

CMD\_OVS\_HPER must be programmed to 12.6  $\mu$ s and CMD\_OVS\_GPER can be programmed between 4.13  $\mu$ s and 12.6  $\mu$ s in the OVERSMPL register.

After the initial sample period performed per a single sample, oversampling on all other channels are at the CMD\_OVS\_GPER and CMD\_OVS\_HPER period settings as indicated in [Table 2](#).

Writing to the CMD register is used to start the voltage sampling process. This is usually done with a BROADCAST Write\_With\_Response\_Command sent to the CMD register. Using the BROADCAST version of the synchronously sample channels command will result in all devices in the stack sampling at the same time. That is, all devices begin sampling their respective cells, then AUX, and so on, simultaneously.

### 7.3.3.3 Recommended Sample Periods

Refer to [Table 3](#) for initial recommended settings. Other settings are possible; see the [Application and Implementation](#) section for additional information.

**Table 3. ADC Recommended Sample Periods and Setup**

MEASURED PARAMETER	PERIOD <sup>(1)</sup>		PERIOD REGISTER <sup>(2)</sup>	
	1 <sup>st</sup> SAMPLE	SAMPLES 2–8	NAME	AS SHIPPED
VCELL	60 $\mu$ s	12.6 $\mu$ s	CELL_SPER	0xBC
VAUX	12.6 $\mu$ s	12.6 $\mu$ s	AUX_SPER	0x44444444
VMODULE	1000 $\mu$ s	12.6 $\mu$ s	TEST_SPER	0xF999
Die Temp (ANL)	100 $\mu$ s	12.6 $\mu$ s	CELL_SPER	0xBC
Die Temp (DIG)	50 $\mu$ s <sup>(3)</sup>	N/A	N/A	N/A
VM	30 $\mu$ s	12.6 $\mu$ s	TEST_SPER	0xF999
VDD18	30 $\mu$ s	12.6 $\mu$ s	N/A	N/A
REF2	30 $\mu$ s	12.6 $\mu$ s	TEST_SPER	0xF999

(1) Sampling periods and averaging mode will affect device accuracy. Device accuracy and register settings (including the sampling period) used to achieve stated device accuracy are specified under "Electrical Characteristics, ADC" in [Analog-to-Digital Converter \(ADC\): Analog Front End](#). Other settings are possible. Device accuracy is not assured at settings other than those specified in the Electrical Characteristics tables.

(2) Other register settings used: OVERSMPL = 0x7B; PWRCONFIG = 0x80

(3) This is not a programmable parameter. No averaging is performed, but there is an inherent delay in the design for the ADC measurement of the die temperature.

### 7.3.3.4 VSENSE Input Channels

The VSENSE input channels measure the voltages of individual cells in the range of 1 V-to-4.95 V. Each input should connect to an external low-pass filter (LPF) to reduce noise at the input, and a Zener diode to provide protection to the device during random hot-plug cell connection. Typical values for the LPF range from 100 Ω to 1 kΩ, and 0.1 μF to 1 μF. Values outside this range may degrade accuracy due to system-level noise or from excessive IR loss in the series resistor.

Tie up unused inputs to the highest-connected cell. For example, in a 14-cell system, tied to VSENSE14 are unused inputs VSENSE15 and VSENSE16. Channels are used from lowest to highest, with VSENSE0 connected to the (–) terminal of the bottom cell.

The values returned from an ADC conversion for these channels convert to volts by:

$$V_{CELL} = [(2 \times VREF) / 65535] \times READ\_ADC\_VALUE \quad (1)$$

A number of factors affect total channel measurement accuracy, including, but not limited to, variations due to IR reflow, board-level stresses, any current leakage in external components, and the method of sampling. It is highly recommended that the end user perform GAIN and OFFSET calibration as described in the [Application and Implementation](#) section.

### 7.3.3.5 AUXn Input Channels

The AUXn input channels are used to measure external analog voltages from approximately 0 V to 5 V. A typical use for these channels is to measure temperature using thermistors. These channels require a simple external low-pass filter to reduce high frequency noise for best operation. The RC values correspond to the user's application requirements.

The values returned from an ADC conversion for these channels convert to volts by:

$$V_{AUX} = [(2 \times VREF) / 65535] \times READ\_ADC\_VALUE \quad (2)$$

### 7.3.3.6 V<sub>MODULE</sub> Measurement Result Conversion to Voltage

V<sub>MODULE</sub> is the voltage measured from the TOP pin to GND. The value scales by 25 with an internal resistor voltage divider. Setting TSTCONFIG[MODULE\_MON\_EN] enables measuring of VMODULE voltage. Enable or disable the measurement to aid with self-testing. When set to 0, the channel should measure close to 0 V.

The values returned from an ADC conversion for this channel converts to volts by:

$$V_{MODULE} = [(2 \times VREF) / 65535] \times READ\_ADC\_VALUE \times 25 \quad (3)$$

### 7.3.3.7 Digital Die Temperature Measurement

The temperature of the digital die may be measured as a part of the normal ADC measurement sequence by setting bit CHANNELS[CMD\_TSEL]. The reported result is the voltage from the temperature sensor, not the actual temperature.

No averaging is ever performed on this channel, but the timing will appear as if the requested oversampling was performed.

FAULT\_SYS[INT\_TEMP\_FAULT] is continuously updated based on the currently stored measurement result and threshold. To allow clearing of the fault, sample the temperature within a normal operating range.

Conversion formula:

$$\text{Internal Digital Die Temperature } ^\circ\text{C} = (V_{ADC} - 2.287) \times 131.944 \quad (4)$$

#### 7.3.3.7.1 Automatic Temperature Sampling

After initialization is complete, an internal timer will cause the digital-die temperature sensor sampling to be scheduled once per second. No oversampling is performed. If a command cycle occurs that samples the digital die temperature sensor, the timer resets. A command will interrupt an automatic temperature sample, but if the command does not sample the digital die temperature, the automatic temperature sample will occur as soon as the command completes. This can cause sample values to appear to change without a sample request.

### 7.3.3.8 Analog Die Temperature Measurement

The temperature measurement of the analog die is programmable as part of the normal ADC measurement sequence by setting bit CHANNELS[CMD\_HTSEL]. The reported result is the voltage from the temperature sensor, not the actual temperature.

There is no internal threshold checking for this value. For self-testing purposes, the expectation is that the microcontroller compares this value with the converted temperature from the digital die and decides if they are reporting the same temperature. The analog die temperature measurement is more accurate than the digital-die temperature measurement. Therefore, the digital die temperature measurement should be considered only a rough estimation of the temperature measured by the analog die temperature monitor. The host firmware must account for any offset between the two measurements.

Conversion formula:

$$\text{Internal Analog Die Temperature } ^\circ\text{C} = (V_{\text{ADC}} - 1.8078) \times 147.514$$

where

$$\bullet \quad V_{\text{ADC}} = [(2 \times V_{\text{REF}}) / 65535] \times \text{READ\_ADC\_VALUE} \quad (5)$$

### 7.3.3.9 VM Measurement Result Conversion to Voltage

There is no internal threshold checking of this value. The expectation is that the microcontroller checks that the value is within the appropriate range.

The value returned from an ADC conversion for this channel converts to volts by:

$$\text{VVM} = -2 \times [(2 \times V_{\text{REF}}) / 65535] \times \text{READ\_ADC\_VALUE} \quad (6)$$

### 7.3.3.10 V5VAO, VDIG, VDD18 Measurement Result Conversion to Voltage

The value returned from an ADC conversion for these channels converts to volts by:

$$V_{\text{ADC}} = [(2 \times V_{\text{REF}}) / 65535] \times \text{READ\_ADC\_VALUE} \quad (7)$$

There is no internal threshold checking of these values. The expectation is that the microcontroller checks that the values are within the appropriate ranges.

## 7.3.4 Thermal Shutdown

Thermal shutdown occurs when either one or both of the Thermal Shutdown (TSD) sensors on either die sense an overtemperature condition. The sensors operate separately without interaction and are separate from the analog and digital die sensors. Each has a separate register-status indicator flag. When a TSD fault occurs, the part immediately enters the SHUTDOWN state. To awake the part, follow the normal WAKEUP procedure. The bq76PL455A does not exit SHUTDOWN automatically. It cannot be awakened until the temperature falls below the TSD threshold. Upon waking up, either SHDN\_STS[GTSD\_PD\_STAT] or (SHDN\_STS[ANALOG\_PD\_STAT]&& SHDN\_STS[HTSD\_PD\_STAT]) bits will be set.

## 7.3.5 Voltage Reference (ADC)

The VREF pin receives a precise internal voltage reference for the ADC. Two parallel X7R or better filter capacitors between pins VREF and AGND are required for the reference; see [Application and Implementation](#) for recommended values and PCB layout considerations.

## 7.3.6 Voltage Reference (REF2)

The window comparators have a 4.5-V internal voltage reference provided. It does not go out to an external pin. To check the reference, select it with the CHANNELS[CMD\_REFSEL] bit.

## 7.3.7 Passive Balancing

Sixteen internal drivers control individual cell balancing through the pins labeled EQ1...EQ16. When the device issues a balance command through register CBENBL, the bq76PL455A asserts the EQ(N) output, switches to the VSENSE(N) rail and turns on Q<sub>BAL</sub>. With a de-asserted register bit, the EQn bit switches to the VSENSEn-1 rail, turns off Q<sub>BAL</sub>, and reduces the balancing current to zero. The squeeze (OWD) function must be disabled for correct balancing operation by setting TSTCONFIG[EQ\_SQUEEZE\_EN] = 0.

If CBCONFIG[BAL\_CONTINUE] is set to '0', then when there is a FAULT the bq76PL455A disables balancing. The CBENBL register bits clear to indicate this event. However, there is one exception. The USER checksum fault indicated by FALUT\_DEV[USER\_CKSUM\_FLT] does not disable balancing. The following describes the scenarios:

- BAL\_CONTINUE = 0: CBENBL is set to 0 and balancing is disabled until the fault and fault status bits are cleared. Information about what was being balanced is discarded. No change is made to the BAL\_TIME bits in CBCONFIG. The CBENBL register must then be rewritten with the desired balancing action.
- BAL\_CONTINUE = 1: There is no effect on CBENBL and CBCONFIG and any balancing in progress continues.

Changing the CBENBL register will create a checksum fault and cause FAULT\_DEV[USER\_CKSUM\_ERR] to be set. This may be a result of setting bits to enable balancing for cells, or the register being reset, because of a fault or CBTIME expiring.

The internal balancing control circuitry only powers up when any bit in CBENBL is set. See [Passive Cell Balancing Circuit](#) section for details on selecting the external passive balancing components.

### 7.3.8 General Purpose Input-Outputs (GPIO)

There are six GPIO pins available in the bq76PL455A. Registers GPIO\_xxx, located at addresses 0x78–7D, control GPIO behavior. Each can be programmed to be an input or output pin.

Each GPIO pin can have an internal pull-up or pull-down resistor enabled to keep the pin in a known state when power is not on for external circuitry. Configuration for pull-up or pull-down resistors is in the GPIO\_PU and GPIO\_PD registers. The pull-up/down resistors have internal connections to supply VIO. The resistor values are in the [Digital Input/Output: Wakeup](#) section of the Electrical Characteristics tables.

The GPIOs can also trigger a FAULT condition. Programmed GPIOs trigger a FAULT indication by setting bits in register GPIO\_FLT\_IN.

The FAULT\_GPI register and the DEVCONFIG[UNLATCHED\_FAULT] bit controls the behavior of the device in response to a FAULT triggered by an enabled GPIO pin. The usual pin configuration is to be an input in the GPIO\_DIR register when used to trigger faults.

### 7.3.9 UART Interface to Host Microcontroller

The UART follows the standard serial protocol of 8-N-1, where it sends information as a START bit, followed by eight data bits, and then followed by one STOP bit. In all, 10 bits comprise a character time. Received data bits are oversampled by 16 times to improve communication reliability.

The UART sends data on the TX pin and receives data on the RX pin. When the transmitter is idling (not sending data), TX = 1. The RX input pin idles in the same state, RX = 1. Hold the RX line high using a pull-up to VIO, if not used (that is, non-base device in the daisy chain). Do not allow the RX pin to float when VIO is present.

#### 7.3.9.1 UART Transmitter

The transmitter can be configured to wait a specified amount of time after the last bit reception and start of transmission using the TX\_HOLDOFF register. The TX\_HOLDOFF register specifies the number of bit periods that the bq76PL455A will wait to allow time for the microcontroller to switch the bus direction at the end of its transmission.

#### 7.3.9.2 UART Receiver

The UART interface design works in half-duplex. As a result, while the device is transmitting data on the TX pin, it ignores RX. To avoid collisions when sending data up the daisy-chain interface, the host microcontroller should wait until it receives all bytes of a transmission from the device to the microcontroller before attempting to send data or commands up the daisy-chain interface. If the microcontroller starts a transaction without waiting to receive the preceding transaction's response, the communication might hang up and the microcontroller may need to send Communication Clear (see [Communication Clear \(Break\) Detection](#)) or Communication Reset (see [Communication Reset Detection](#)) to restore normal communications.

### 7.3.9.3 Baud Rate Selection

The baud rate of the communications channel to the microcontroller is set in the COMCONFIG[BAUD] register for 125k-250k-500k-1M baud rates. The default rate after a communications reset is 250k. The default rate after a POR is the rate selected by the value stored in EEPROM for the COMCONFIG[BAUD] register.

When the value in this register changes, the new rate takes effect after the complete reception of a valid packet containing the new setting including the CRC. This should send the next packet at the new baud rate and all packets transmitted by the device will be at the new rate. It is possible to change the baud rate at any time and, optionally, store the new baud rate in the EEPROM as a new POR default. After changing the baud rate, observe a minimum wait period of 10  $\mu$ s before sending the first packet at the new baud rate.

The value in the COMCONFIG[BAUD] register only affects the baud rate used in microcontroller communications on the TX and RX pins. The daisy-chain vertical communication bus rate is at a higher fixed rate and not user modifiable. All devices in the stack must have the same baud rate setting as the base device to read data from stacked devices.

### 7.3.9.4 Communication Clear (Break) Detection

Use communications clear to reset the receiver to re-synchronize looking for the start of frame.

The receiver continuously monitors the RX line for a break (<BRK>) condition. A <BRK> is detected when the RX line is held low for at least  $t_{\text{COMM\_BREAKmin}}$  bit periods (approximately 1 character times). Sending for more than  $t_{\text{COMM\_BREAKmax}}$  bit periods may result in recognition of a communication reset instead of the intended communication clear. When detected, a <BRK> will set the STATUS[COMM\_CLEAR] flag.

### 7.3.9.5 Communication Reset Detection

Detection of a communication reset occurs when the RX line is held low for more than approximately  $t_{\text{COMM\_RESETmin}}$ . The primary purpose of sending a communications reset is to recover the device in the event the baud rate is inadvertently changed or unknown. The baud rate resets unconditionally to the FACTORY default value of 250 kb/s, REGARDLESS of the value stored in the EEPROM COMCONFIG register. This sets the baud rate to a known, fixed rate (250k baud), and the STATUS[COMM\_RESET] flag.

### 7.3.9.6 Communication Timeouts

Programming is available for two timeout values based on the absence of a valid packet from either UART or differential stack communications. The times are set in the two-bit fields of the Communications Timeout (CTO) register. A valid packet definition is any packet with a valid CRC.

#### 7.3.9.6.1 Communications Timeout Fault

Register CTO[COMM\_TMOUT\_PER] sets the period with no valid communications from either communications interface before sensing a COMM\_TIMEOUT fault.

Always set CTO[COMM\_TMOUT\_PER] to be set less than the CTO[COMM\_PD\_PER] to get a communications timeout fault before SHUTDOWN occurs.

#### 7.3.9.6.2 Communications Timeout Power-Down (SHUTDOWN)

CTO[COMM\_PD\_PER] forces the part to shut down when this time is exceeded without a valid communication from either the UART or the differential stack communications.

### 7.3.10 Stacked Daisy-Chain Communications

In the stacked configuration, the main microcontroller first communicates through a bq76PL455A device using the UART communications interface, see [Figure 17](#). Communication is then relayed up the chain of connected slave bq76PL455A devices using a proprietary differential communications protocol over AC-coupled differential links interconnected by the COMMH+/- and COMML+/- pins.

Each device in the daisy chain buffers the signal drive levels. The signal is not re-clocked or filtered; it passes through the device without change and the entire stack sees all data sequencing regardless of the target device. The packet is not validated before being transmitted to the next device in the daisy chain. The uniquely addressed or group addressed device acts on the command (that is, begins an ADC conversion of the inputs) as soon as it receives and validates the packet for correct address, message contents, and CRC.



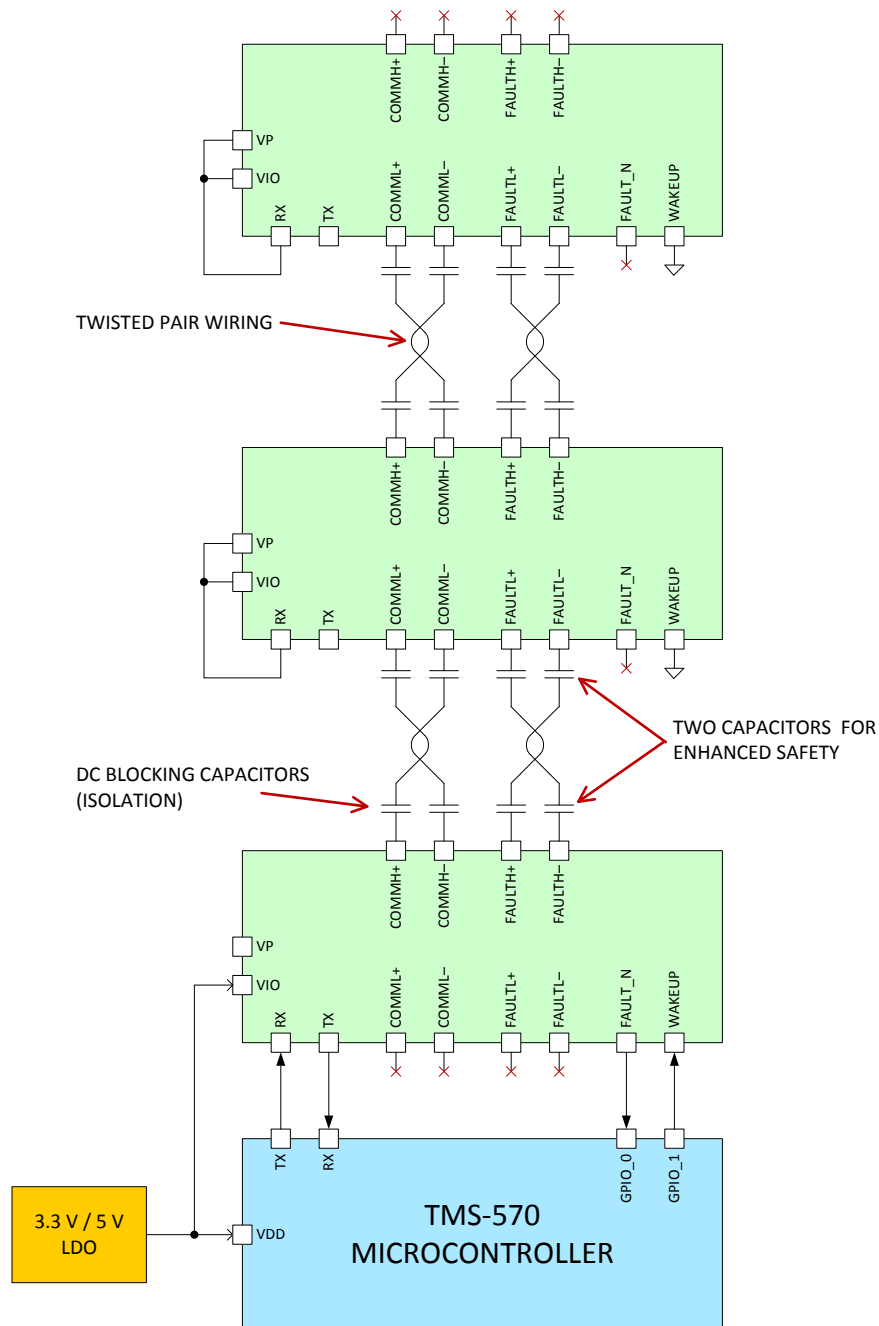


Figure 17. Simplified Stack Communications Connectivity

### 7.3.10.1 Differential Communications

The bq76PL455A uses two differential communications links, which perform different tasks. The hardware used for the transmitters and receivers are similar. The communications link used for data and commands (the vertical bus or VBUS) on the COMM+/- and COMMH+/- pairs is bidirectional, while the FAULTH+/- pins are receivers only, and the FAULTL+/- are transmitters only.

#### NOTE

The UART receiver (RX), COMMH+/- transmitters, and COMM+/- receivers cannot be disabled.



The base device sends and receives data through UART at variable baud rates from 125 kb/s to 1 Mb/s. The VBUS daisy chain operates at a fixed, nominal, data rate of 4 Mb/s using a proprietary asynchronous protocol. Each byte is sent as 10 bits at 250 ns/bit or 2.5  $\mu$ s/byte. The bottom device retransmits data from/to the differential serial interface on the single-ended interface connected to the host system at the baud rate selected for the single-ended serial interface. All bq76PL455As in the daisy-chain should be set to the same baud rate to align timing between the devices.

The VBUS interface uses a modified version of the UART protocol so it can easily translate to/from the UART protocol. Transmission of a bit requires 250 ns, including both half-bits. It is effectively a 4-MHz signal that is phase-shift keyed, so the resulting transmission will have both 4-MHz and 2-MHz components. See [Figure 18](#) for additional information.

### 7.3.10.2 Protocol Description

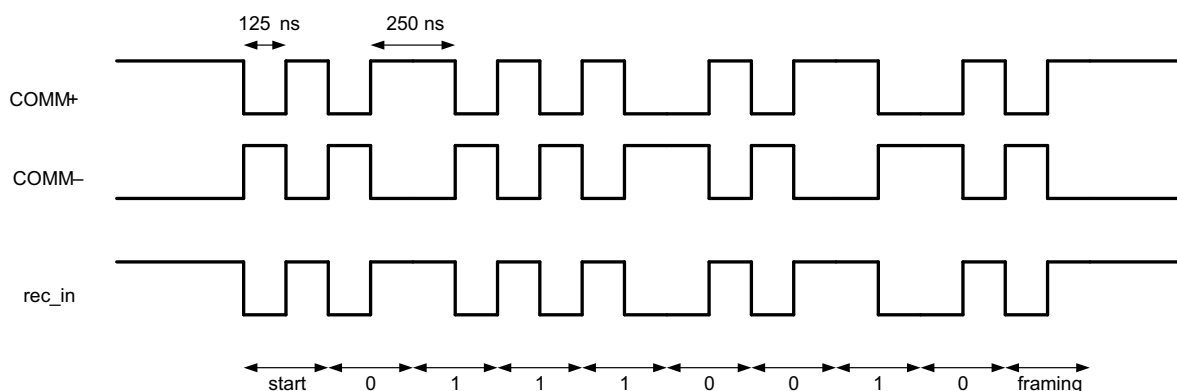
The differential VBUS uses an asynchronous byte-transfer protocol with one start bit, eight data bits, and an optional framing bit. The start bit is always a zero. Duplication of the LSB-first data occurs so that the transmission has no DC content. A zero is transmitted as one half-bit period low followed by one half-bit period high. Transmission of a one is as one half-bit period high followed by one half-bit period low. A framing bit of one will cause the byte to be discarded and the byte abort flag (FAULT\_COM[ABORT\_H or ABORT\_L]) to be set. Since the data transmit on the differential interface as it is being received from the single-ended UART interface, this is used to indicate that an erroneous stop bit was detected.

Each time the bq76PL455A detects a byte with a framing bit of zero, it is interpreted as a frame-initialization byte. If the prior frame was not completed, FAULT\_COM[FRAM\_ERR] is set.

If detection of the start bit occurs, the receiver samples the input on the fourth clock edge to produce the bit. Since a bit is always immediately followed by its complement, the two will be compared and the complement error flag (FAULT\_COM[COMP\_ERR\_H or COMP\_ERR\_L]) is set if they are not opposites. The first time such an error occurs during a frame, the assumption is that the first sampling of the bit (not the complement) is the correct one. (If this choice is incorrect, it should detect it as a CRC failure.) If such an error occurs more than once during a frame, the fatal-complement error flag (FAULT\_COM[COMP\_FLT\_H or COMP\_FLT\_L]) is set and the frame ignored. Since the device ignores the remainder of the frame, a FRAM\_ERR occurs when the next frame arrives.

While receiving a byte, the receiver will resynchronize on every falling edge. A falling edge is expected at least once every 3 bits. If the expected sampling point of the fourth bit does not detect a falling edge, the edge error flag (FAULT\_COM[EDGE\_ERR\_H or EDGE\_ERR\_L]) will be set and the receiver will return to idle, discarding the frame.

If the bq76PL455A device detects eight consecutive edge errors on the low-side interface (COMM\_L+/-) with no valid bytes being received, the block will be reset in the same manner as SOFT\_RESET. This allows a wakeup tone from the chip below in the stack to cause the part to reset.



**Figure 18. VBUS Data Example, 0x4E Sent**

### 7.3.11 Register and EEPROM

#### 7.3.11.1 Error Check and Correct (ECC) EEPROM

Register values for selected registers are permanently stored in EEPROM. All registers also exist as volatile storage locations at the same addresses, referred to as *shadow* registers. The volatile registers are for reading, writing, and device control. For a list of registers included in the EEPROM, see [Table 7](#).

At wakeup, the bq76PL455A first loads all shadow registers with default values from [Register Summary](#). Then the bq76PL455A loads the registers conditionally with EEPROM contents from the results of the Error Check and Correct (ECC) evaluation of the EEPROM.

The EEPROM is loaded to shadow registers in 64-bit blocks; each block has its own Error Check and Correct (ECC) value stored. The ECC detects a single bit (Single-Error-Correction) or double bit (Double-Error-Detection) changes in EEPROM stored data.

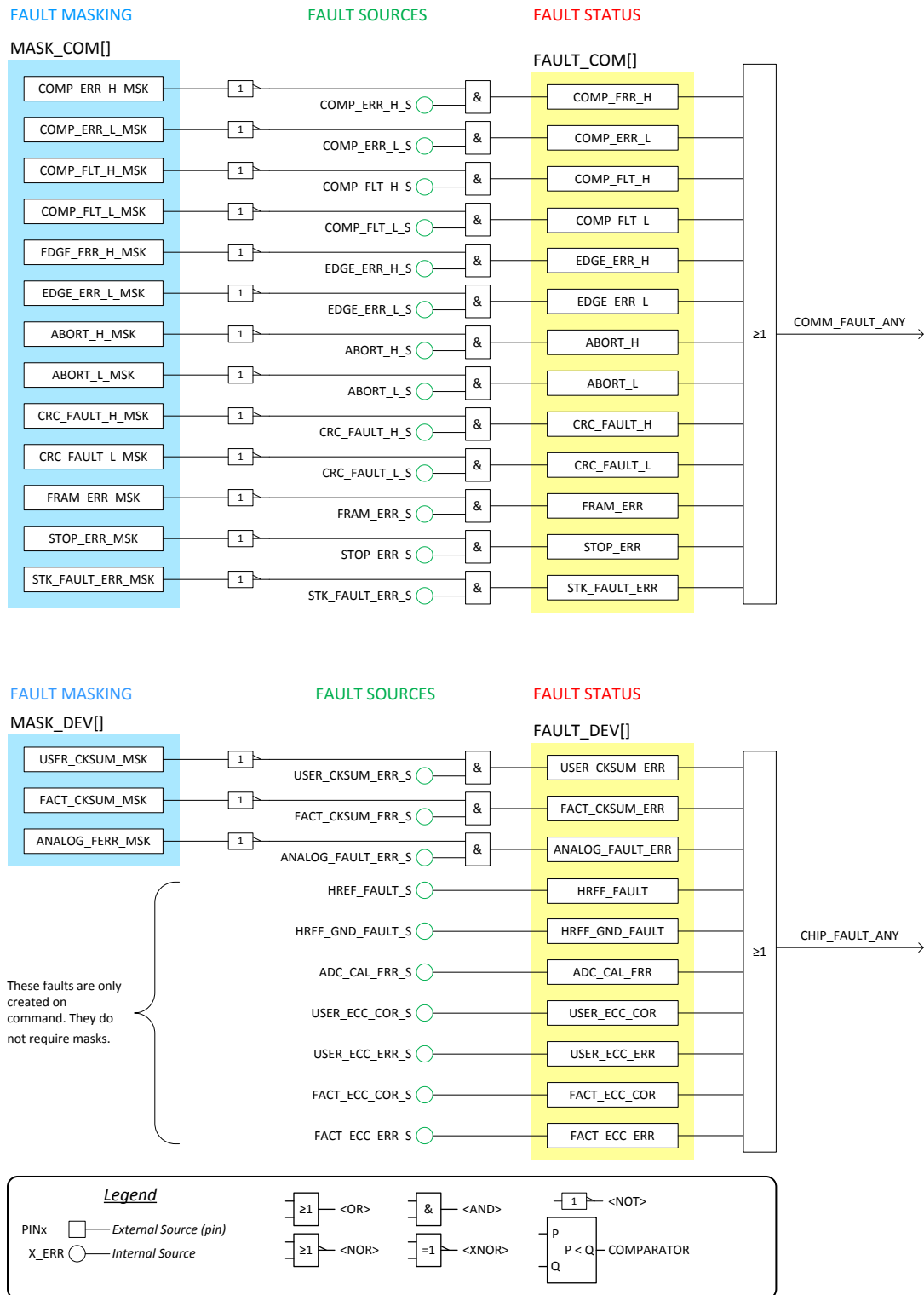
The ECC is calculated for each block, individually. Single-bit errors are corrected, double-bit errors are only detected, not corrected. A block with good ECC is loaded. A block with a single-bit error is corrected, and either FAULT\_DEV[USER\_ECC\_COR] or FAULT\_DEV[FACT\_ECC\_COR] bit is set to flag the corrected error event. The block is loaded to shadow registers after the single-bit error correction. Since the evaluation is on a block-by-block basis, it is possible for multiple blocks to have a single-correctable error per block and still be loaded correctly. Multiple bit errors can exist with full correction, as long as they are limited to a single error per block.

A block with a bad ECC comparison (two bit errors in one block) is not loaded and the FAULT\_DEV[USER\_ECC\_ERR] or FAULT\_DEV[FACT\_ECC\_ERR] bit is set to flag the failed bit-error event. The default value remains in the register. This allows some blocks to be loaded correctly (no fail or single bit corrected value) and some blocks not to load. Any time either of the FAULT\_DEV[\*\_ECC\_ERR] is set, and the condition is not cleared by a soft reset, the device has failed and should not be used.

### 7.3.12 FAULT Sensing and Signaling

A dedicated differential FAULT link allows each bq76PL455A in a stack of devices to signal the presence of any monitored and active/latched fault condition to the main microcontroller separately from the UART link. The FAULT\_H+/- and FAULT\_L+/- pins implement an AC-coupled differential-signaling scheme similar to communication pins COMML+/- and COMMH+/-, but using only a simple heartbeat signal to indicate normal or fault conditions by the presence or absence of a repetitive pulse, respectively. The low duty-cycle heartbeat stops anytime it senses a fault and the fault condition sets a bit in one of the FAULT\_\* registers. Masked faults have no effect on the heartbeat generation.

### 7.3.12.1 Fault Flow Schematics



**Figure 19. Digital Faults**

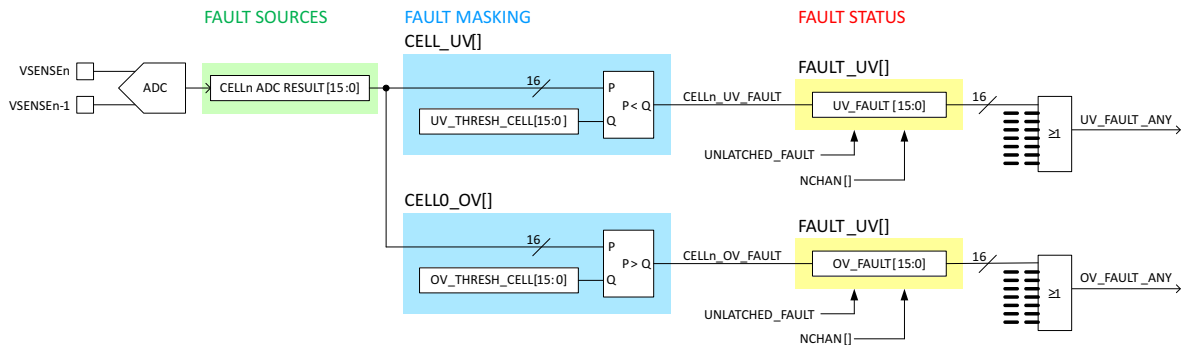
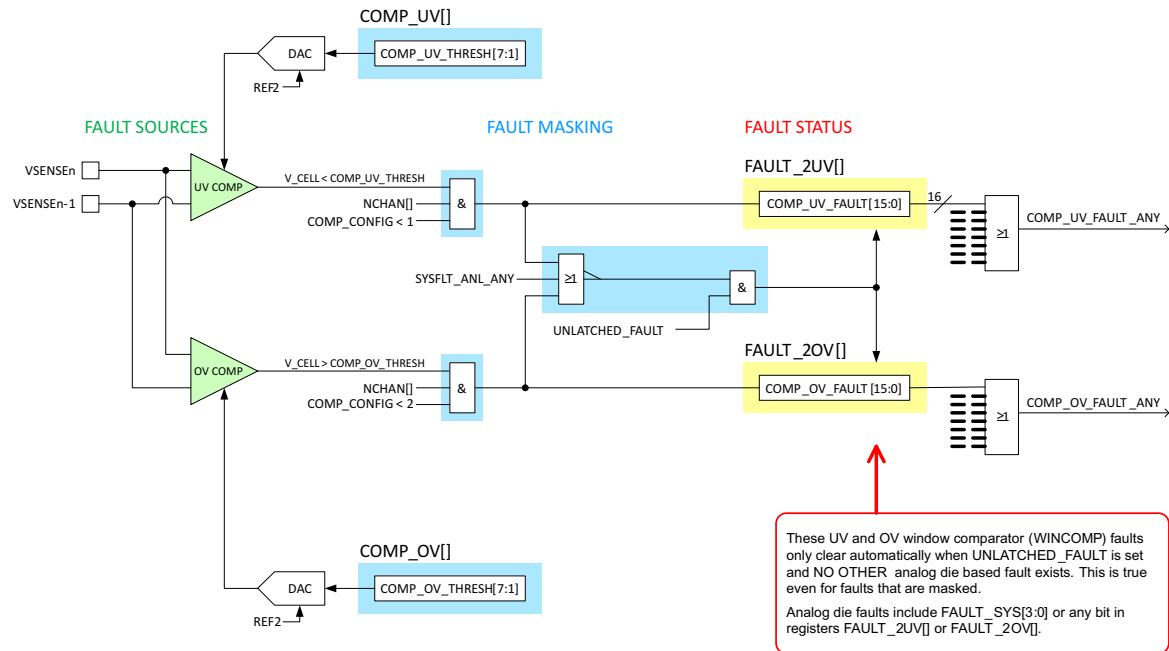
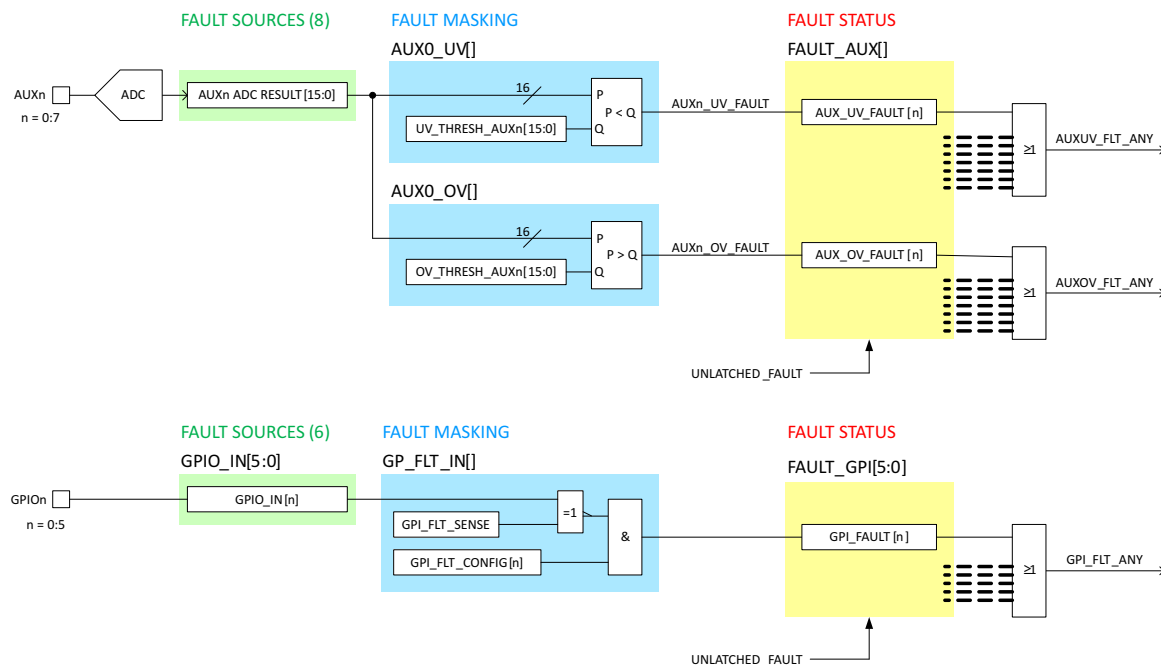
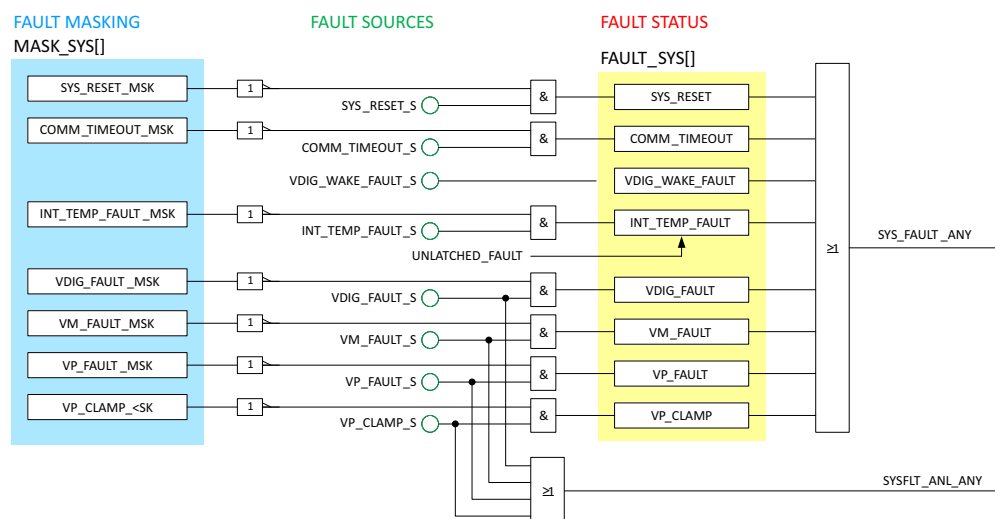


Figure 20. Analog Faults


**Figure 21. AUX and GPIO Pin Faults**

**Figure 22. System Faults**

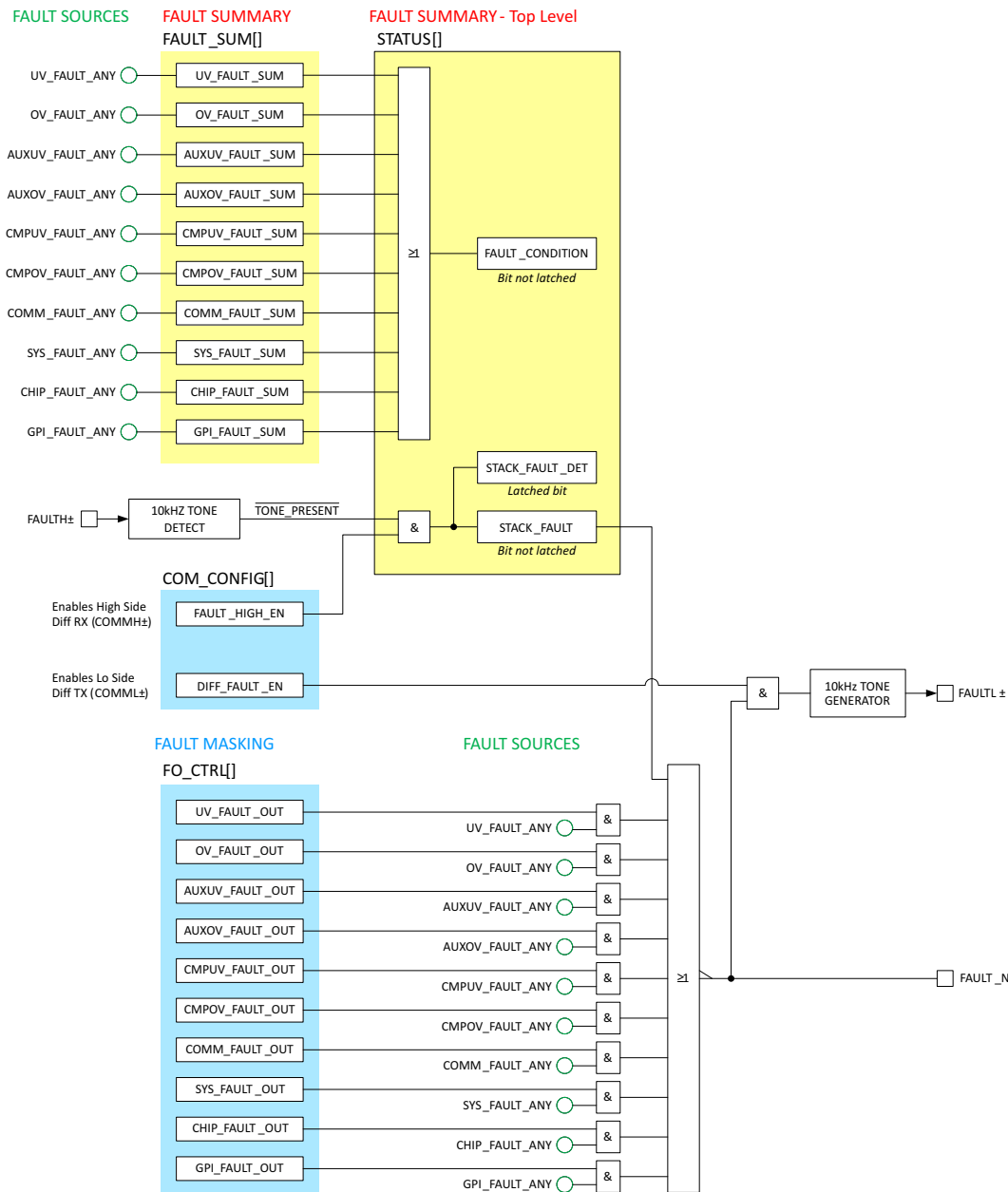


Figure 23. Fault Hierarchy Top-Level

### 7.3.12.2 FAULT Signaling

The FAULT bus transmits a simple heartbeat pulse at a fixed frequency when enabled and unmasked faults are not present. Masking a fault does not clear a pre-existing fault condition. A device sensing a fault condition stops transmitting the heartbeat to the ICs in the chain below. The ICs sense this condition in the stack below and then assert the FAULT\_N pins if configured to sense the lack of tone in COMCONFIG. FAULT\_N only asserts if the UART\_EN bit in COMCONFIG is set.

The differential signal lines are isolated between ICs by a DC blocking capacitor similar to the differential communications VBUS daisy chain. The capacitor typical rating is at a minimum of two times the stack voltage to provide plenty of standoff margins to handle system faults that expose the device to local hazardous voltages. One capacitor is sufficient for the normal operation of the device. The system designer may elect to use two capacitors, one at each end of the cable or PCB wiring, for an additional safety factor. In this case, use double the capacitor value from the normal requirement, so that the two capacitors in series result in the same value in the signal path.

The heartbeat derivation comes from the device main oscillator and is generated separately out of each device in the stack. The device does not copy or re-transmit the value from the device above it. The FAULT\_COM[STK\_FAULT\_ERR] that indicates a problem with the fault heartbeat is sensed individually by each device in the stack and may be tripped in some devices and not in others under some fault conditions.

The FAULT\_N pin signals faults from both internal sources and from ICs above in the stack, if enabled. Internal faults are on FAULT\_N depending on the enabled sources in the FO\_CTRL register. Faults from stacked devices above it are signaled on the FAULT\_N pin when enabled by COMCONFIG[FAULT\_HIGH\_EN]. The FAULT\_N pin always outputs a low signal in reset or shutdown.

### 7.3.12.3 Fault Sensing

Masking of fault sources may be in registers MASK\_COMM, MASK\_SYS, and MASK\_DEV. Masking a fault will prevent the flag from being set at a future time, but it will not clear an already set fault flag.

Any time an unmasked fault condition is triggered, the device sets a bit in the appropriate FAULT\_\* register at addresses 0x52–63.

When a device senses an unmasked fault or, with enabled fault communications, when the heartbeat from the device above stops, the FAULT\_N pin asserts low to signal the fault to a user circuit or microcontroller. Each device in the stack that sees one of these conditions asserts the FAULT\_N pin if the UART\_EN bit in COMCONFIG is set. The heartbeat stop and FAULT\_N pin assertions occur simultaneously.

Normally, after RESET, POR, or normal wakeup, user firmware must clear FAULT\_SYS[SYS\_RESET] to start the heartbeat. If there is an enabled stack communications interface, the heartbeat will start after clearing SYS\_RESET and receiving four cycles of the heartbeat on the north-interface FAULT pins. This typically requires a little more than approximately 400  $\mu$ s and results in clearing the STATUS[STACK\_FAULT] flag.

Faults propagate down the stack through the FAULT pins. The lower of two adjacent bq76PL455A devices monitors its FAULT pins for the propagated faults from the device above it in the stack.

When COMCONFIG[FAULT\_HIGH\_EN] = 1, the logic will monitor the receiver for falling edges. Under-frequency conditions will set the STATUS[STACK\_FAULT\_DET] and STATUS[STACK\_FAULT] flags. Note that this allows every other pulse to be lost without reporting an error.

Over-frequency conditions will set the FAULT\_COM[STK\_FAULT\_ERR] flag. Once proper signaling resumes on the high-side fault pin, it will again be possible to clear this fault.

The fault heartbeat stops and FAULT\_N asserts during any of the following conditions:

- The fault heartbeat stops on the high-side fault interface FAULT pins (if not configured to ignore it)
- Some automatic feature in the device detects a fault; that is, the secondary protector VSENSE comparators, checksum failure, automatic internal temperature sampling, and so forth
- A command to sample returned a value that was out of range and caused a fault
- An internal self-test fails

#### NOTE

The STK\_FAULT\_ERR may not be clearable under some conditions.

1. If a STK\_FAULT\_ERR is detected and then no more edges appear on the high-side fault pins (as would be the case if the chip above had a fault condition), it may be impossible to clear the STK\_FAULT\_ERR flag.
2. A masked STK\_FAULT\_ERR does not clear during initialization. As a result, there is an approximately 4.5- $\mu$ s window at startup during which, if the high-side fault receiver detects more than four falling edges, STK\_FAULT\_ERR will be set even though it is masked.



### 7.3.12.3.1 Fault Output Control

FO\_CTRL allows groups of enabled faults to drive the pin when the appropriate bit is set. When the register bit is set, any fault of the indicated type will cause the assertion of the fault outputs (FAULTL, FAULT\_N) if they are enabled—that is, FAULT\_N will be driven low and the tone on FAULTL pins will be stopped.

The following groups of faults are enabled in this register (see [FO\\_CTRL 0x6E–6F \(110–111\) Fault Output Control](#) for bit position details):

- Any UV fault (VSENSE inputs)
- Any OV fault (VSENSE inputs)
- Any UV fault (AUX inputs)
- Any OV fault (AUX inputs)
- Any UV fault (window comparators)
- Any OV fault (window comparators)
- Any communications fault (see FAULT\_COM)
- Any system fault (see FAULT\_SYS)
- Any device fault (see FAULT\_DEV)
- Any GPIO fault (see FAULT\_GPI)

### 7.3.12.3.2 Fault Masking

The following registers can enable or mask fault sources individually or in groups. Masking a fault prevents it from being set, but does not clear an existing fault bit.

- MASK\_COMM—Communications related faults
- MASK\_SYS—System faults in power supplies, over temperature, and so on
- MASK\_DEV—Internal register-checksum faults, and so on
- GP\_FLT\_IN—GPIO input level faults
- NCHAN—Masks faults for unused channels, turns off window comparators for unused channels

### 7.3.12.4 Fault Latching

When UNLATCHED\_FAULT is set, the bits in some of the fault registers (see the following text and [Register Details](#) for included registers) will automatically clear when the fault condition goes away. Continuously set faults will clear when the condition goes away. Faults set by an event will clear when the event occurs (such as a sampled channel will clear when that channel is sampled). In this mode, writing to the included fault registers will have no effect. Unlatched faults, when detected and cleared, can result in creating transient behavior for the associated flag bits, FAULT\_N, and FAULTL.

Changes to the DEVCONFIG[UNLATCHED\_FAULT] bit should only occur while no fault bits are set. The latched/unlatched status of fault bits is undefined when the UNLATCHED\_FAULT bit changes while a fault bit = 1.

Fault bits in the following registers are unaffected by the DEVCONFIG[UNLATCHED\_FAULT] bit and are always latched:

- FAULT\_COM—All bits
- FAULT\_SYS—All bits, except INT\_TEMP\_FAULT
- FAULT\_DEV—All bits

The DEVCONFIG[UNLATCHED\_FAULT] bit, when set, prevents the latching of fault bits in the following registers:

- FAULT\_UV—Undervoltage VSENSE ADC limit exceeded
- FAULT\_OV—Overvoltage VSENSE ADC limit exceeded
- FAULT\_AUX—Programmable AUX threshold in AUXn\_UV or AUXn\_OV exceeded
- FAULT\_2UV—Undervoltage VSENSE secondary protection comparator limit exceeded
- FAULT\_2OV—Overvoltage VSENSE secondary protection comparator limit exceeded
- FAULT\_SYS—INT\_TEMP\_FAULT bit only
- FAULT\_GPI—GPIO (programmable) logic input level triggered a fault

### 7.3.12.4.1 Special Considerations in Unlatched Fault Mode

In unlatched mode, when the FAULT\_2UV and FAULT\_2OV registers sense and record secondary protector (window comparator) faults and one or more other analog die faults (that is, VP\_FAULT, VDIG\_FAULT, or VM\_FAULT) are present, none of the mentioned faults will clear until all have been cleared, even if the cause of the fault has gone away. That is, they may appear latched until all these faults are clear.

If these faults (FAULT\_SYS[VP\_FAULT, VP\_CLAMP, VM\_FAULT, or VDIG\_FAULT]) are present, it is reasonable to assume that the comparators may not be functioning properly and/or may have stopped reporting a fault because they stopped functioning rather than the fault condition having gone away.

### 7.3.12.5 Fault Status and Fault Reset

The following registers can read or reset the fault status individually or in groups:

- STATUS—Sum of all faults plus stack fault conditions are in this register, some fault information bits are reset here. This register is at the top of the fault hierarchy.
- FAULT\_SUM—Groups of faults are summarized by single flags in this register and may be either read or reset here. This is level 2 of the fault hierarchy.
- FAULT\_UV—Undervoltage VSENSE ADC limit exceeded. This is level 3 of the fault hierarchy.
- FAULT\_OV—Overvoltage VSENSE ADC limit exceeded. This is level 3 of the fault hierarchy.
- FAULT\_AUX—Programmable AUX threshold in AUXn\_UV or AUXn\_OV exceeded. This is level 3 of the fault hierarchy.
- FAULT\_2UV—Undervoltage VSENSE secondary protection comparator limit exceeded. This is level 3 of the fault hierarchy.
- FAULT\_2OV—Overvoltage VSENSE secondary protection comparator limit exceeded. This is level 3 of the fault hierarchy.
- FAULT\_SYS—System level faults: power supplies, over temperature, communications timeout, and reset. This is level 3 of the fault hierarchy.
- FAULT\_GPI—GPIO (programmable) logic input level triggered a fault. This is level 3 of the fault hierarchy.
- FAULT\_COM—Communication faults. This is level 3 of the fault hierarchy.
- FAULT\_DEV—Device faults. This is level 3 of the fault hierarchy.

### 7.3.12.6 Checksum Faults

To discover changes to registers, the bq76PL455A constantly runs a background check on their contents by computing a checksum and comparing it to a stored value. The bq76PL455A detects changes approximately every two microseconds. The changes can be intentional (that is, a change written by the microcontroller), unintentional (due to an unexpected device or system fault), or, in some cases, the result of an automated operation (expiration of the balancing timer). The test runs against the registers in both a TI space and USER space. This includes most registers with changes that come from the microcontroller; consult [Register Summary](#) for an exact list of included locations.

The CSUM\_RSLT register holds the currently computed checksum value. It compares this value against the stored checksum value in register CSUM. To update the stored value, read the current value in CSUM\_RSLT and write it back to the CSUM register or compute the value as shown in [Computing User Checksum](#). A checksum saves to CSUM in EEPROM by setting MAGIC1 and MAGIC2 appropriately, then setting DEV\_CTRL[WRITE\_EEPROM]. The appropriate values for MAGIC1 and MAGIC2 definitions are in the [Register Details](#) section of this document in the bit description field for the WRITE\_EEPROM bit.

When CSUM and CSUM\_RSLT do not match, the FAULT\_DEV[USER\_CKSUM\_ERR] flag will be set until the condition is corrected. This fault flag is unlatched and will self-clear when a mismatch no longer occurs.

Continuous monitoring of the TI EEPROM space occurs in a similar fashion, concurrently with the monitoring of the USER space. If a register change is detected, the FAULT\_DEV[FACT\_CKSUM\_ERR] flag is set. If this ever occurs, the user firmware should perform a soft RESET of the part. This fault flag is not self-clearing. Write a 1 to the bit to clear it. If a soft reset does not correct the issue, do not use the device.

### 7.3.12.6.1 Checksum Testing

Each of the checksums (TI, USER spaces) has a test mode that causes each input bit in the checksum calculation (that is, the register bits that are part of the checksum calculation) to flip twice (once per clock) and the TEST\_CSUM register contains the count for the number of toggles on the checksums fault output. This helps to ensure that the background checksum testing described previously correctly discovers any bit that might be in the wrong state.

The user's firmware, usually as a part of self-testing and validation, can initiate the tests. The TESTCTRL[CKSUM\_TEST\_RUN] bits are set to begin the test on either the TI or USER space registers. See [TESTCTRL 0x20–21 \(32–33\) Test Control](#) for details of the bit settings.

#### NOTE

Other faults may be set in the process of running this procedure, but ignore those.

#### 7.3.12.6.1.1 Computing User Checksum

The user checksum is a 32-bit value computed using all the data values in the user data space. The computation is a simple 32 bit add of registers and constants concatenated into 32-bit values. The computation, shown below, consists of the data at the address specified or 0:

```

cust_cksum_calc =
{0, 0, 0, a3} +
{a4, a5, a6, a7} +
{0, 0, a10, a11} +
{0, a13, a14, a15} +
{a16, a17, a18, a19} +
{a20, a21, 0, 0} +
{0, 0, a30, a31}+
{0, 0, a34, a35}+
{a36, a37, 0, 0} +
{a40, 0, 0, 0}+
{0, 0,a50, a51}+
{a52, a53, a54, a55} +
{0, a61, a62, a63} +
{a64, a65, a66, a67} +
{a68, 0, 0, 0}+
{a104, a105, a106, a107} +
{a108, 0, a110, a111} +
{a120, a121, a122, a123} +
{0, a125, 0, 0}+
{a140, a141, a142, a143} +
{a144, a145, a146, a147} +
{a148, a149, a150, a151} +
{a152, a153, a154, a155} +
{a156, a157, a158, a159} +
{a160, a161, a162, a163} +
{a164, a165, a166, a167} +
{a168, a169, a170, a171} +
{a172, a173, a174, a175} +
{a176, a177, 0, 0} +
{a200, a201, a202, a203} +
{a204, a205, a206, a207} +
{0, 0, a210, a211} +
{a212, a213, a214, a215} +
{a216, a217, a218, a219} +
{a220, a221, a222, a223} +
{a224, a225, a226, a227};

```

#### NOTE

In the example code, a\_ refers to register address number. For example: a3 = register address 0x03.

### 7.3.12.7 AUXn OV/UV Threshold Faults

The AUXn input pins can trigger a fault indication. The OV and UV thresholds for each AUXn input can be set separately in the AUXn\_OV and AUXn\_UV registers. The result of each AUXn channel conversion is compared to these values. When the threshold is exceeded (less-than AUXn\_UV, greater-than AUXn[OV]), the FAULT\_N and FAULTL pins are asserted, if enabled. To stop unwanted FAULT pin assertions from one or more channels (but other channels are desired), set the threshold voltage settings for the undesired channels to their minimum and maximum values or only convert the desired channels.

FAULT\_AUX[AUX\_UV\_FAULT, AUX\_OV\_FAULT] will be continually set based on the currently stored ADC result and threshold. This allows testing of the threshold and fault by changing the threshold without having to sample the channel.

Example:

The design requires AUX0 and AUX1 undervoltage threshold at 1 V and AUX0 and AUX1 overvoltage threshold at 3 V. The design requires that no FAULT pin activation result from AUX UV or OV conditions on AUX2...AUX7. Set the following conditions:

AUX0\_UV = 1 V, AUX0\_OV = 3 V

AUX1\_UV = 1 V, AUX1\_OV = 3 V

AUX2\_UV = 0 V, AUX2\_OV = 5 V

AUX3\_UV = 0 V, AUX3\_OV = 5 V

AUX4\_UV = 0 V, AUX4\_OV = 5 V

AUX5\_UV = 0 V, AUX5\_OV = 5 V

AUX6\_UV = 0 V, AUX6\_OV = 5 V

AUX7\_UV = 0 V, AUX7\_OV = 5 V

### 7.3.12.8 Secondary Protectors: Analog Window Comparators for Cell UV/OV

Thirty-two analog comparators, connected in pairs as window comparators for the 16 channels, provide cell-voltage monitoring that is separate from the main acquisition path and work in parallel with the main ADC route. Configuration of the faults sensed by the analog window comparators is by the number of channels enabled in the NCHAN register. In case of malfunction of the AFE or ADC, the analog comparators will still be able to flag the crossing of the (register selectable) undervoltage and overvoltage comparator thresholds.

To avoid undesired comparator faults, two internal DACs set the separate overvoltage (COMP\_OV) and undervoltage (COMP\_UV) thresholds. The DACs use the REF2 (4.5 V) reference, which is a separate circuit from the 2.5 V (VREF) ADC reference. The OV threshold can range from 2 V to 5.175 V in steps of 25 mV. The UV threshold can range from 0.7 V to 3.875 V in steps of 25 mV.

#### NOTE

When the cell voltage is very close to the comparator thresholds, enabling or disabling cell balancing may result in transient comparator faults.

Use the DEVCONFIG[COMP\_CONFIG] register to enable OV and UV faults, OV-only faults, or no faults. Enabling UV-only faults is not possible.

#### NOTE

If the comparators are disabled then re-enabled during normal operation (such as after startup has occurred), the OV faults are signaled and must be manually cleared.

#### 7.3.12.8.1 Window Comparator Special Considerations

As shown in [Figure 24](#), there are resistors of approximately 100  $\Omega$  in series with each VSENSE pin that isolate the connections to the AFE from the secondary-protector circuits (window comparators). This isolator allows detection of common-cause failures affecting both the AFE and secondary-protector circuits.

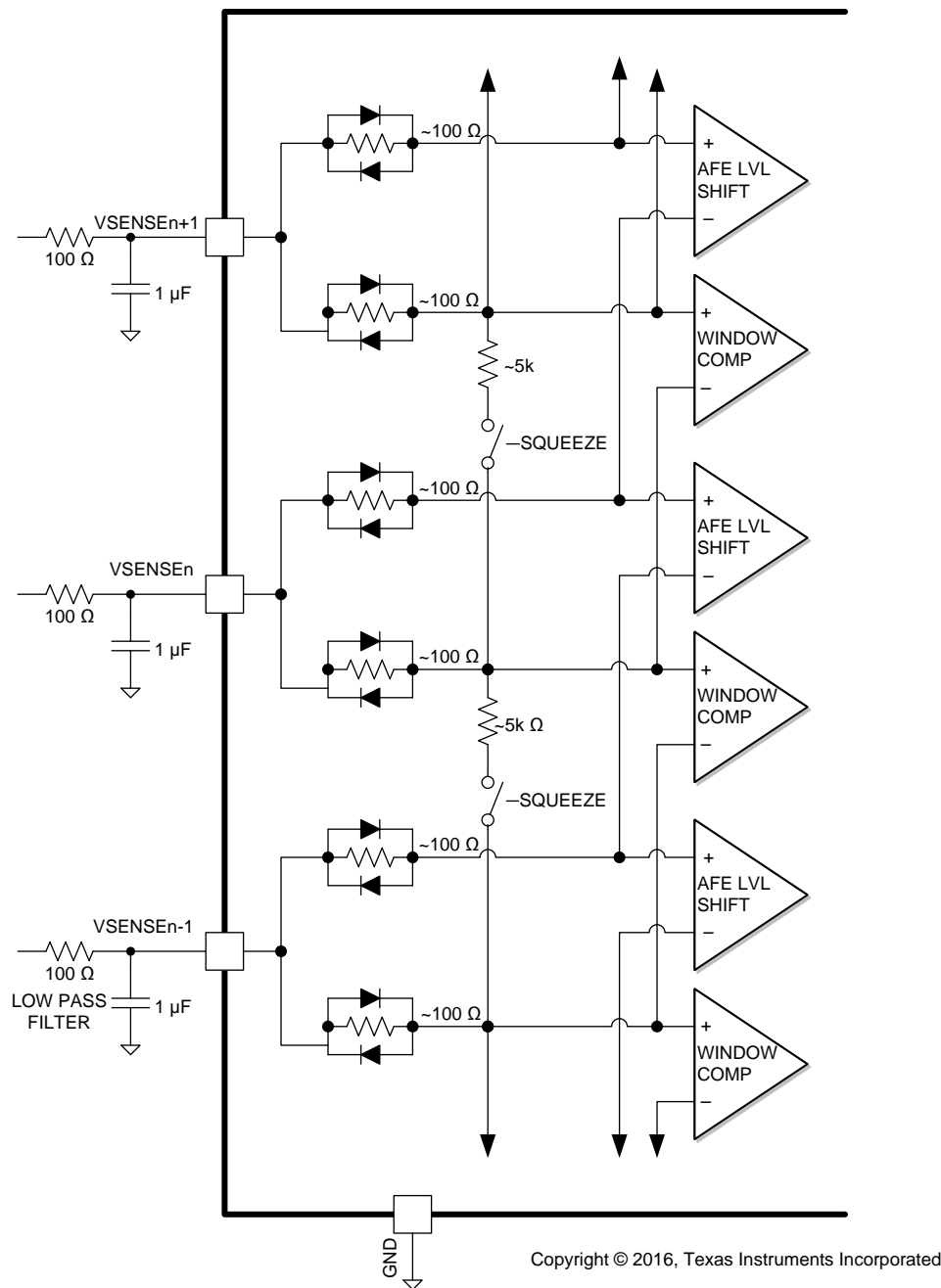
A Squeeze function in the device helps to detect open-sense wire (to the monitored cell) conditions. When the Squeeze function turns on, it places an approximately 5-k $\Omega$  resistance across adjacent VSENSE inputs, and creates an additional voltage drop through the approximately 100- $\Omega$  series resistors. This causes the apparent increase in the voltage applied to the window-comparator blocks immediately above, and below, the inputs that have the Squeeze resistor applied. Only the comparators can see the increased voltage not the AFE. This in turn may cause the OV comparator fault to trip, even if the external sense-pin voltage measurement says otherwise, depending on the OV threshold.

**CAUTION**

Using the Squeeze function under open wire conditions and with a broken connection to the external Zener may cause internal device damage to occur.

It is highly recommended to run all diagnostic tests on the bq76PL455A after correction of the open wire condition. Pay special attention to the validation of the window comparator accuracy against the AFE accuracy to ensure parametric compliance. In the event of non-compliance, remove the affected bq76PL455A device from service immediately.

In the example in [Figure 24](#), the Squeeze resistor is enabled for (across) VSENSEn-1 to VSENSEn. This will cause the apparent voltage seen by the comparators for cell n-1 and cell n+1 to increase. For the cell voltage of cell n, which in this example is approximately 3.6 V, there will be an additional drop on the internal lines going to the window-comparator block (but not to the AFE) of  $(3.6 \text{ V} / 5\text{K} \times 100 \times 2) =$  approximately 144 mV. This will also show up as an increase of approximately 72 mV on the cells above and below the cell being squeezed. Larger input resistors, such as 1 k $\Omega$ , will dominate this error source and may result in unexpected trips of the window comparators, depending on the threshold settings, and will change the manner in which the calculations suggested in this example are made.



**Figure 24. Window Comparator Input Configuration Overview**

### 7.3.12.9 Communications Faults

During the course of normal data communications, noise may induce errors in the bit stream. The errors may assert faults depending on the mask settings in the MASK\_COMM and MASK\_SYS registers.

- UART communications faults details are in [UART Interface to Host Microcontroller](#)
- Differential (VBUS) communications faults description is a part of the protocol description in [Protocol Description](#)

### 7.3.12.10 Communications Timeout Counters

Check the communication timeout counters by setting and reading the 24 most-significant bits of the timeout counter using COMM\_TIM\_CNT. A 4-kHz clock source drives the timeout counter. To aid this testing, CCNT\_RST\_OFF may be set so the communication sent to either set or monitor the counter does not reset the counter. The counter value may be set using COMM\_TIM\_CNT to enable faster testing of long periods. The bits that are not accessible are set to '1' by writing to this register, to test the counter rollovers quickly.

### 7.3.13 Built-in-Test Functions

To access the built-in-test functions, set bits in the various registers. The identification of these bits are in the descriptions of the appropriate registers and their bits in [Register Details](#).

#### 7.3.13.1 Safety Manual and FMEDA

The [Safety Manual for bq76PL455A-Q1](#) (SLUUB67) is available on ti.com. Please contact your TI Sales Associate or Applications Engineer for the [bq76PL455A-Q1 FMEDA](#) (SLUUB93).

## 7.4 Device Functional Modes

The bq76PL455A device has three power states (modes):

- SHUTDOWN (sleep)—The lowest power state used for long periods of inactivity to extend battery life.
- IDLE—The default condition when awake and ready to receive and execute commands.
- ACTIVE—The highest power state while communicating; that is, IDLE + communications activity.

### 7.4.1 SHUTDOWN

SHUTDOWN is the lowest power state available in the part. In this state, power is off and monitoring disabled for most internal blocks. Typically, SHUTDOWN is for long periods of inactivity when the battery is not being charged or discharged. The part must receive a high signal on the WAKEUP pin or a WAKEUP tone through the vertical communications bus to transition to the IDLE state.

To enter SHUTDOWN, remove external voltage sources of VP, VDIG, and all input voltage sources to AUX pins and other I/O pins. VIO can remain while in SHUTDOWN mode and GPIO can remain if based on VIO. While in SHUTDOWN mode, VP and VDIG must remain off or be disabled to avoid back powering the bq76PL455A through internal ESD structures. When VIO is lowered, the bq76PL455A will immediately go into reset. Holding VIO for longer than VIO<sub>SD\_DLY</sub> MAX will cause the device to enter SHUTDOWN mode.

The WAKEUP pin must be held in the low state to allow the device to enter and remain in the SHUTDOWN state (setting the pin low does not place the device in SHUTDOWN). If the WAKEUP pin remains in the high state, the device will cycle off and immediately back on. Operation is unpredictable if the WAKEUP pin floats, so take care to keep this pin in a defined state. This is not harmful to the device, but may not provide the expected behavior in the system.

If the NPN circuit is not used (external supply), VP and VDIG should turn off immediately after entering shutdown mode. Lowering VP and VDIG will also put the device in SHUTDOWN mode.

The part will enter SHUTDOWN when any of the following conditions occur:

- The user requested SHUTDOWN through a command by asserting DEV\_CTRL[PWRDN], usually with a broadcast form of the command. The WAKEUP pin on the base bq76PL455A must remain in the low state.
- There was a communications timeout caused by the timer set in register CTO[COMM\_PD\_PER] due to:
  - No valid frames (packets) received in the set period, <OR>
  - TSTCONFIG[CCNT\_RST\_OFF] is set and the timer expired whether valid frames were received or not, usually as a part of BIST.
- TSTCONFIG[VDIG\_TEST] was set at some time since the last SHUTDOWN <AND> VDIG dropped below its SHUTDOWN threshold (DDIE<sub>POR</sub>). Once set, subsequently clearing TSTCONFIG[VDIG\_TEST] will not disable this control even though the bit will read 0. It will not disable until the device enters shutdown.
- One of the two thermal shutdown (TSD) circuits sensed an overtemperature condition (there is one sensor on each die that operates separately, with separate register flag indicators).
- VIO was below its VIOPOR threshold for longer than VIO<sub>SD\_DLY</sub>.
- V5VAO was below the V5VAO<sub>SD</sub> POR threshold.



## Device Functional Modes (continued)

- Internal VP regulator is on and attempting to drive the NPNB signal, but VP remains below the internal VP POR threshold for longer than  $VP_{SD\_DLY}$ .

### NOTE

Once in the SHUTDOWN state, the part must be re-awakened to continue normal operations. See [Wakeup Behavior from SHUTDOWN](#).

### 7.4.2 Wakeup

The bq76PL455A device will wake up and enter the IDLE state when either of the following conditions occurs:

- WAKEUP pin is high
- COMML pins receive the WAKE tone

### 7.4.3 Wakeup Behavior from SHUTDOWN

The WAKEUP pin can bring the part from the SHUTDOWN state to the IDLE state. It can do this in any stack position. However, typically only the base device uses it when driven from a microcontroller. The pin is level sensitive and is normally at a low (logic-zero) level. When the part is in SHUTDOWN and the WAKEUP pin becomes high, the part will transition from SHUTDOWN to IDLE. After applying the high signal, the WAKEUP pin must de-assert and then return to the low state to allow the part to enter SHUTDOWN again. Upon changing state, the bq76PL455A will briefly transmit a differential wakeup tone on its COMMH+ and COMMH– pins to the next higher bq76PL455A, where that device's COMML+ and COMML– pins receives it.

### NOTE

The WAKEUP pin is usually kept in the de-asserted (low) state. If the pin is asserted (high) and then the device is commanded to SHUTDOWN, it will immediately reawaken and become IDLE. To prevent unexpected state transitions, this pin must not be floating. Make sure that the pin does not float if the device driving the pin has no power.

The bottom (*southernmost*) device in the stack sends the wakeup tone out of the COMMH pins in response to the WAKEUP pin assertion. The next device to the north receives the WAKEUP tone on its COMML pins. It awakens, which in turn sends the WAKEUP tone to the next device above it. The WAKEUP tone propagates up the stack in this way to wake all devices in the stack. While the part is in SHUTDOWN, the COMML pins are in receive mode, and no transmission will occur.

### 7.4.4 Power-On Reset (POR) or Wakeup

The IC's state machine fully resets at wakeup. Wakeup causes the VP/VDIG output to come up, which in turn brings up VDD18, providing power to portions of the analog circuits and to all of the core logic, including the registers and the EEPROM. This is effectively a POR of the part. All registers are loaded with values stored in EEPROM. Registers that are not loaded from EEPROM reset to their default values indicated in [Table 7](#).

### NOTE

Immediately following a reset for any reason, some faults are not valid (=0) until a sample is taken. All fault bits in registers FAULT\_UV, FAULT\_OV, and FAULT\_AUX are invalid. In addition, bits FAULT\_DEV[HREF\_FAULT, HREF\_GND\_FAULT] are also invalid. Reading a fault register will not cause the taking of a sample or updating of the bits. A command must be sent to the device to sample all channels to update the above listed fault bits, making them valid.



## Device Functional Modes (continued)

Note that this sequence is the same regardless of the reset source—POR, soft reset, wake tone received from the part below.

1. External NPN regulator circuit turns on. VP, VDIG, (and VIO if connected to VP) begin to ramp up. If VIO is supplied by an external source (such as the microcontroller I/O power supply), then VIO must be stable and greater than its POR threshold.
2. Once VDIG reaches its POR threshold, the internal 1.8 V (internal digital supply VDD) regulator begins to ramp up. Once VDIG reaches the POR threshold, VREF and the internal 1.8 V supply (VDD18) start up. The reference for the VDD (1.8 V) supply is VREF, so it will not reach its final operating voltage until VREF reaches its final voltage.
3. Once VP, VDIG, VIO, and VDD all reach their POR thresholds, the oscillator starts.
4. Once the oscillator is running, the Finite State Machine (FSM) starts up and begins sending the wake tone out of the high-side interface (COMMH±).
5. The FSM in turn waits approximately 10 µs for the EEPROM to be ready.
6. All system registers will be loaded from EEPROM.
7. Relevant information will be propagated to the Analog die registers, except regulator power down.
8. If GPIO addressing is enabled (DEVCONFIG[ADDR\_SEL] = 0), the GPIO[4:0] pins are sampled to determine the device's communication address and recorded in ADDR.
9. Sample the internal Digital-die temperature channel. This pre-loads the value, so temperature-based calibration will function properly. No other channels will be sampled during initialization and faults will not be generated from them until *after* they are sampled.
10. Clear any masked faults that could have occurred. This includes clearing threshold-based faults that are masked by their threshold.
11. Begin monitoring for UART communications.
12. Initialize Analog die faults. (Continue sequencing in parallel; do not wait for the following sub-sequence to complete.)
  - (a) Wait until no VM fault is reported from Analog die or the user writes '1' to STATUS[SYS\_INIT].
  - (b) Enable all Analog die fault registers.
  - (c) Set STATUS[SYS\_INIT] = 0.
13. Wait for wakeup tone to complete.
14. Begin monitoring for differential communications.
15. Once the FAULT\_SYS[SYS\_RESET] fault is cleared by the host microcontroller, turn off the external NPN-regulator circuit if the regulator is disabled (that is, DEVCNFIG[REG\_DISABLE] = 1).

While the system initialization sequence above is in progress (while SYS\_INIT reads '1'), many faults will not report properly and sampling commands may not function properly. Also, note that aborting the initialization sequence (by writing '1' to SYS\_INIT) may cause the reporting of erroneous faults and sampling of Analog channels to report invalid results until the VM voltage is up and stable.

Additionally, there is a delay associated with the enabling of the UART communications and a delay associated with the completion of the initialization process once the VM fault clears (or the user aborts the initialization sequence).

## Device Functional Modes (continued)

### 7.4.5 Calculating Wakeup Timing

The following sequence assumes that the microcontroller power circuit provides the VIO supply. The host microcontroller initiates the sequence and the VIO is up and stable. (The sequence does not change if VIO is tied to the regulator. However, if some other source is providing WAKEUP, but the microcontroller provides the VIO supply, the VIO supply needs to clear the POR threshold within VIOSD\_DLY of WAKEUP or the part will go back into shutdown.)

1. The user asserts the WAKEUP pin on the bottom board's base device.
2. At this point, the VP regulator will turn on and ramp the VP/VDIG supplies. The time required to reach the POR thresholds for VP/VDIG varies and is dependent on the designer's component selection. (Note that VP/VDIG/VIO must all reach their respective POR thresholds.) Once VP reaches its POR threshold, VREF will also need to ramp to its operating voltage.
3. The time from reaching the POR thresholds to the start of the wakeup tone being transmitted from the high-side interface is specified as  $t_{\text{WAKEUP\_DLY}}$ .
4. The time from the start of the wakeup tone being transmitted until communications are allowed to this part is specified as  $t_{\text{WAKEUP\_TO\_UART}}$ .

#### NOTE

It is acceptable to begin communicating with the part at this point, if it is the only part in the stack. If there are additional parts in the stack, you can still begin communicating with the bottom part at this point. However, this may cause communications error flags to get set in bq76PL455A parts positioned higher in the stack.

5. The time from the wakeup tone transmission from the high side of the device below (end of step 3), until the regulator turns on the current board, is  $(t_{\text{WAKE\_TONE\_DLY\_DC}} - t_{\text{WAKEUP\_DLY}})$ .
6. The regulator turns on and ramps the VP/VDIG/VREF/VIO supplies. As with the bottom device, this time is board dependent.
7. The time from reaching the POR thresholds to the start of the wakeup tone being transmitted from the high-side interface to the next device up the stack is specified as  $t_{\text{WAKEUP\_DLY}}$ . Note that for calculation purposes to group #5 and #7 together as  $t_{\text{WAKE\_TONE\_DLY\_DC}}$ .
8. The time from the wakeup tone being transmitted from the high-side interface until you are allowed to communicate with this part is specified as  $t_{\text{WAKEUP\_TO\_DCOMM}}$ .

If there are additional parts in the stack, apply steps 5–8 accordingly.

To compute the total time from assertion of WAKEUP to the stack being ready for communications, we will define:

- $t_{\text{BOT\_RAMP}}$  as the time needed for the supply ramp on the bottom board. The above steps must be used to determine the wakeup time for the bottom board.
- $t_{\text{STACK\_RAMP}}$  as the time needed for the supply ramp on all stacked boards
- $n_{\text{STACK\_BOARDS}}$  as the number of stacked boards (not including the bottom board)

If there is only one device, then the required delay from WAKEUP until it is acceptable to begin communicating will be:

$$t_{\text{BOT\_RAMP}} + t_{\text{WAKEUP\_DLY}} + t_{\text{WAKEUP\_TO\_UART}} \quad (8)$$

Else, if there is more than one board in the stack, the delay from WAKEUP until it is acceptable to begin communicating will be:

$$t_{\text{BOT\_RAMP}} + t_{\text{WAKEUP\_DLY}} + n_{\text{STACK\_BOARDS}} * (t_{\text{STACK\_RAMP}} + t_{\text{WAKE\_TONE\_DLY\_DC}}) + t_{\text{WAKEUP\_TO\_DCOMM}} \quad (9)$$

It is generally acceptable to start communicating with the stack once the bottom UART interface is ready for communications. However, parts above in the stack may not respond until their required times. It is also possible to cause communication error flags to be set in the parts above by doing this. As mentioned previously, the fastest way to get the stack talking (assuming all parts have the EEPROM burned for their stack location and configuration) may be to continuously send a read request to the top device until it responds and then clear all communications errors that occur because of this.

## Device Functional Modes (continued)

If you try to send communications to the bottom device before the UART interface is ready, it can get out of sync. To fix this, send a `comm_clear`. This is not necessary for parts on the differential interface, since they will re-synchronize to the bottom chip on every frame. Therefore, only the bottom chip can lose synchronization.

### 7.4.6 Soft Reset

Setting the `SOFT_RESET` bit in the `DEV_CTRL` register will not power down the device, but it will fully reset and restart the state machine per the sequence in [Power-On Reset \(POR\) or Wakeup](#). All ICs in the stack above the reset part will wake up if in SHUTDOWN and reset if awake.

### 7.4.7 Wakeup Behavior in IDLE Mode

When the bq76PL455A device receives a WAKEUP tone while it is already awake, it performs a reset. The device requires a series of pulses of the received WAKEUP tone to begin the reset process. Sending the tone will wake the device if asleep or reset it if idle. The result is that sending the wakeup tone to parts in the stack can be used to reset them and cause all to enter the IDLE state whether they were previously in SHUTDOWN or IDLE. This is another method to reset the state of all devices in the stack.

The device will generate a wakeup tone to the other devices *north* in the chain as a part of the reset sequence. As a result, each device above the device receiving the wake tone will in turn reset.

## 7.5 Command and Response Protocol

This protocol enables a single host, such as a microcontroller, to communicate with one or more bq76PL455A devices. The host initiates every transaction between the host and one or more bq76PL455A devices. The bq76PL455A will never send data to the host without first receiving a command frame from the host.

### NOTE

After each command frame is transmitted, the initiator should *always* wait for all expected responses to be returned (or a timeout in case of error) before initiating a new command frame.

The phrases *Write without Response* and *Write* or *write* are equivalent and synonymous, unless otherwise noted.

The phrases *Write with Response* and *Read* or *read* are equivalent and synonymous, unless otherwise noted.

### 7.5.1 Transaction Frame Description

The transaction frame format includes both Command Frames and Response Frames. There are five field types used within a transaction frame:

1. Frame Initialization
2. Device Address or Group ID
3. Register Address
4. Data
5. Cyclic Redundancy Check (CRC)

Note that not all byte types are part of every transaction frame.

## Command and Response Protocol (continued)

### 7.5.1.1 Frame Initialization Byte

The Frame Initialization Byte is always the first byte of the frame. In all cases, the length of the frame can be determined from this initial byte. Note that bit 7 identifies each frame as either a command frame or a response frame. The initialization byte is defined as follows for each of the two Frame Init types:

	7	6	5	4	3	2	1	0
Command Frame Init	FRM_TYPE = 1	REQ_TYPE			ADDR_SIZE	DATA_SIZE		
Response Frame Init	FRM_TYPE = 0	RESP_BYTES-1						

The descriptions for the fields shown in the frame initialization bytes are in [Table 4](#).

**Table 4. Frame Initialization Byte Fields**

	VALUE (BINARY)	DESCRIPTION
FRM_TYPE	0	Response Frame
	1	Command Frame
REQ_TYPE	000	Single Device Write with Response
	001	Single Device Write without Response
	010	Group Write with Response
	011	Group Write without Response
	100	Reserved
	101	Reserved
	110	Broadcast Write with Response
	111	Broadcast Write without Response
ADDR_SIZE <sup>(1)</sup>	0	8-bit Register Address
	1	16-bit Register Address
DATA_SIZE <sup>(2)</sup>	000	0 bytes
	001	1 byte
	010	2 bytes
	011	3 bytes
	100	4 bytes
	101	5 bytes
	110	6 bytes
	111	8 bytes
RESP_BYTES-1		Number of data bytes contained in response frame minus 1

(1) ADDR\_SIZE = 0 is recommended. All USER registers are addressable using an 8-bit register address.

(2) Data size of 7 bytes is not supported.

### 7.5.1.2 Device Address/Group ID Byte

The Device Address or Group ID Byte identifies the device or group of devices targeted by the command. Only those devices that contain a matching value in their Device Address Register (register address 10) or Group ID Register (register address 11) will respond to the command. The REQ\_TYPE field in the command frame will determine how to interpret this byte.

#### NOTE

Device Address/Group ID Byte is not present in a Broadcast command frame.

	7	6	5	4	3	2	1	0
Device Address or Group ID	Identifier of device(s) receiving communication (always one byte)							

### 7.5.1.3 Register Address Byte(s)

Register addresses can be one or two bytes in length. For single byte addresses (ADDR\_SIZE = 0), the MSB is not transmitted and is assumed to be 0.

	7	6	5	4	3	2	1	0
Register Address (MSB)	Register being targeted							
Register Address (LSB)								

### 7.5.1.4 Data Bytes

The basis of data byte interpretation is from the type of command frame being sent and the target register specified in the command frame.

For command frames targeted at the Command Register (address 2), the data contains the command, highest responding device address and, optionally, new data for the Command Channel Select Register (address 3–6) and Averaging Register (address 7).

For command frames targeted at other registers:

- If REQ\_TYPE is Write without Response, the data bytes contain the values to be written to the registers
- If REQ\_TYPE is Write with Response, the data bytes contain the values returned from the registers

	7	6	5	4	3	2	1	0
Data[0] ... Data[n]	Data Bytes (the number of bytes should match the DATA_SIZE field in the Frame Initialization byte)							

#### NOTE

Transactions with seven data bytes are not possible.

### 7.5.1.5 CRC Bytes

	7	6	5	4	3	2	1	0
CRC (MSB)	16-bit CRC (CRC-16-IBM—See <a href="#">CRC Description</a> )							
CRC (LSB)								

## 7.5.2 CRC Description

The standard CRC-16-IBM algorithm uses the following CRC generator polynomial:

$$X_{16} + X_{15} + X_2 + 1$$

In general, a CRC (cyclic redundancy check) represents the remainder of a process analogous to polynomial long division, where the frame being checked is *divided* by the generator. The CRC appended to the frame is the *remainder*. Because of this process, when the device receives a frame, the CRC calculated by the receiver across the entire frame including the transmitted CRC will be zero, indicating a correct transmission and reception. A non-zero result indicates a communication error.

The CRC calculation by the transmitter is in bit-stream order across the entire transmission frame (except for the CRC, of course). When determining bit-stream order for implementing the CRC algorithm, it is important to note that protocol bytes transmit serially, least-significant bit first.

An efficient, 8-bit parallel C function that can be utilized directly is included at the end of this section. The following pseudo-code algorithm is a more easily described bitwise implementation of the CRC algorithm utilizing the CRC-16-IBM generator polynomial:

```
CRC='0000_0000_0000_0000'
DIN={(frame in bit-stream order), '0000_0000_0000_0000'};
for n=0 to length_in_bits(DIN)-1{
    CRC15:0=[(CRC0^DINn), CRC15, (CRC14^CRC0), CRC13:2, (CRC1CRC0)];
};
```

In this notation, subscripts represent zero-based bit selection from either the frame-data bit stream or the 16-bit CRC (as it is being calculated); strings in single quotes (') represent binary constants; the caret (^) denotes a single-bit exclusive-or operation; and the curly-brace – comma ({a, b, ... c}) expressions denote bitwise concatenation. Underscores (\_) are only to enhance readability and can be ignored.

The 16-bit CRC is initialized to all 0-bits. DIN is the frame to be transmitted or received in bit-stream order, with sixteen 0-bits appended to the end. The expression *length\_in\_bits(DIN)* will equal the length of the input in bytes × 8 + 2. The *for* loop is intended to iterate over DIN one-bit at a time in bit-stream order. CRC<sub>15:0</sub> is the 16-bit CRC for transmittal (or checked in the case of a received frame). Note that the bitwise concatenation on the right-hand side of the CRC equation is also 16-bits in total length.

The bit numbers in the equation for the CRC (inside the *for* loop) have been chosen so that X16 in a formal mathematical description (such as the specification of the CRC-16-IBM generator polynomial) corresponds with bit 0 in the subscript notation in the pseudo-code. In the pseudo-code, bit 0 is the least-significant bit and is on the right-hand side of the concatenation. Bit0 is the first bit transmitted on the wire using serial communication. An artifact of this notation and algorithmic choice is that the final CRC of the algorithm is byte-reversed with respect to how the device will store the values in memory. Specifically, the byte labeled *CRC (MSB)* in the frame descriptions throughout this document is the *low* order byte of the CRC generated by both the pseudo-code and the C function, and the byte labeled *CRC (LSB)* is the *high* order-generated byte. The advantage of arranging the generated CRC word in this way is that no bit-level reversal is needed.

The following example will be useful to an algorithm implementer to verify that the final implementation is correct. In this example, an initiator (microcontroller) is generating a CRC for a command frame. The following is a sample frame for use:

	7	6	5	4	3	2	1	0
Command Frame Init	1	001 (binary)			0	001 (binary)		
Device Address	03							
Register Address	07							
Data	05							
CRC (MSB)	1E							
CRC (LSB)	CF							

For this example, by the time the *for* loop in the pseudo-code previously described is executed, CRC is 0 and DIN (in hex bytes) is 91, 03, 07, 05, 00, 00. In bit-stream order, this becomes:

DIN = '1000\_1001\_1100\_0000\_1110\_0000\_1010\_0000\_0000\_0000\_0000'

As the *for* loop executes, the CRC value, based on each subsequent bit of DIN, progresses as follows:

n	DINn	CRC15:0	n	DINn	CRC15:0	n	DINn	CRC15:0
0	1	1000 0000 0000 0000	16	1	0010 0001 1100 1001	32	0	0100 1010 0001 0101
1	0	0100 0000 0000 0000	17	1	0011 0000 1110 0101	33	0	1000 0101 0000 1011
2	0	0010 0000 0000 0000	18	1	0011 1000 0111 0011	34	0	1110 0010 1000 0100
3	0	0001 0000 0000 0000	19	0	1011 1100 0011 1000	45	0	0111 0001 0100 0010
4	1	1000 1000 0000 0000	20	0	0101 1110 0001 1100	36	0	0011 1000 1010 0001
5	0	0100 0100 0000 0000	21	0	0010 1111 0000 1110	37	0	1011 1100 0101 0001
6	0	0010 0010 0000 0000	22	0	0001 0111 1000 0111	38	0	1111 1110 0010 1001
7	1	1001 0001 0000 0000	23	0	1010 1011 1100 0010	39	0	1101 1111 0001 0101
8	1	1100 1000 1000 0000	24	1	1101 0101 1110 0001	40	0	1100 1111 1000 1011
9	1	1110 0100 0100 0000	25	0	1100 1010 1111 0001	41	0	1100 0111 1100 0100
10	0	0111 0010 0010 0000	26	1	0100 0101 0111 1001	42	0	0110 0011 1110 0010
11	0	0011 1001 0001 0000	27	0	1000 0010 1011 1101	43	0	0011 0001 1111 0001
12	0	0001 1100 1000 1000	28	0	1110 0001 0101 1111	44	0	1011 1000 1111 1001
13	0	0000 1110 0100 0100	29	0	1101 0000 1010 1110	45	0	1111 1100 0111 1101
14	0	0000 0111 0010 0010	30	0	0110 1000 0101 0111	46	0	1101 1110 0011 1111
15	0	0000 0011 1001 0001	31	0	1001 0100 0010 1010	47	0	1100 1111 0001 1110

The computed CRC value is '1100\_1111\_0001\_1110'. The 16-bit CRC consists of two bytes, which this algorithm produces in reverse order. The correct ordering of these two bytes in the command frame is MSB first, LSB last (that is, '0001\_1110' followed by '1100\_1111' or in hex, 1E, CF). The intention is for these two bytes to transmit serially starting with the least-significant bit of each.

Take great care when implementing the CRC algorithm to ensure that the bit ordering convention is consistent in the entire frame including the CRC. The implementer should check several examples from this document against the data generated by the algorithm for use to ensure that the implementation is correct. The final command frame as it passes to a UART is:

	COMMAND FRAME BYTES
Command Frame Init	91
Device Address	03
Register Address	07
Data	05
CRC (MSB)	1E
CRC (LSB)	CF

The algorithm for checking a frame is similar. As an example, to check this frame, one possible implementation would be to simply calculate the CRC the first four bytes (excluding the CRC) and compare it with the received CRC value. Another option would be to take advantage of the cyclic nature of the CRC algorithm, passing all six bytes through, and then verifying that the result is 0. In this case, the initial zero padding of DIN with sixteen zeroes will not be necessary. The resulting calculation would progress as follows, resulting in a final CRC value of 0, indicating a successful check:



n	DINn	CRC15:0	n	DINn	CRC15:0	n	DINn	CRC15:0
0	1	1000_0000_0000_0000	16	1	0010_0001_1100_1001	32	0	0100_1010_0001_0101
1	0	0100_0000_0000_0000	17	1	0011_0000_1110_0101	33	1	0000_0101_0000_1011
2	0	0010_0000_0000_0000	18	1	0011_1000_0111_0011	34	1	0010_0010_1000_0100
3	0	0001_0000_0000_0000	19	0	1011_1100_0011_1000	45	1	1001_0001_0100_0010
4	1	1000_1000_0000_0000	20	0	0101_1110_0001_1100	36	1	1100_1000_1010_0001
5	0	0100_0100_0000_0000	21	0	0010_1111_0000_1110	37	0	1100_0100_0101_0001
6	0	0010_0010_0000_0000	22	0	0001_0111_1000_0111	38	0	1100_0010_0010_1001
7	1	1001_0001_0000_0000	23	0	1010_1011_1100_0010	39	0	1100_0001_0001_0101
8	1	1100_1000_1000_0000	24	1	1101_0101_1110_0001	40	1	0100_0000_1000_1011
9	1	1110_0100_0100_0000	25	0	1100_1010_1111_0001	41	1	0000_0000_0100_0100
10	0	0111_0010_0010_0000	26	1	0100_0101_0111_1001	42	1	1000_0000_0010_0010
11	0	0011_1001_0001_0000	27	0	1000_0010_1011_1101	43	1	1100_0000_0001_0001
12	0	0001_1100_1000_1000	28	0	1110_0001_0101_1111	44	0	1100_0000_0000_1001
13	0	0000_1110_0100_0100	29	0	1101_0000_1010_1110	45	0	1100_0000_0000_0101
14	0	0000_0111_0010_0010	30	0	0110_1000_0101_0111	46	1	0100_0000_0000_0011
15	0	0000_0011_1001_0001	31	0	1001_0100_0010_1010	47	1	0000_0000_0000_0000

There are many good sources for algorithms and efficient techniques for generating and checking CRCs available on the Internet. The following byte-oriented C language routine has been developed and verified as a reference. The only complication needed to take into account using this function is that the low byte of the CRC value returned is the CRC (MSB) and the high byte is the CRC (LSB).

```

uint16 crc_16_ibm(uint8 *buf, uint16 len) {
    uint16 crc = 0;
    uint16 j;

    while (len--) {
        crc ^= *buf++;

        for (j = 0; j < 8; j++)
            crc = (crc >> 1) ^ ((crc & 1) ? 0xa001 : 0);
    }
    return crc;
}

```

### 7.5.3 Transaction Frame Examples

To illustrate the various Command and Response formats, examples of representative transaction-frame types are presented in the following paragraphs. All numeric values are in hexadecimal unless otherwise noted. The CRC values in the examples are correct and the implementer can use them to verify the CRC algorithm. Unless specifically noted otherwise, all examples use 8-bit register addressing.

Additional communication examples with matched command and response frames are in the [bq76PL455A-Q1 Software Design Reference](#) (SLVA617).

Command Frames fall into two general categories:

1. Command frames that generate one or more response frames
2. Command frames that do not generate response frames

The REQ\_TYPE field in the Frame Initialization byte determines the category to which a command frame belongs. Category 1 contains the Single Device Write with Response, Group Write with Response, and Broadcast Write with Response request types. Category 2 contains the Single Device Write without Response, Group Write without Response, and Broadcast Write without Response request types.

Command frames that generate response frames, may generate more than one response frame. This depends on the specific command frame and the number of devices addressed by the command frame. In the case where more than one response frame is received in response to a single command frame, each response frame will be a complete frame containing the Frame Initialization, Data, and CRC bytes. A single device will not respond with more than a single-response frame in response to any single-command frame.



Special care should be taken when addressing the Command Register (address 2). When sending command frames that generate response frames to this register, the length of a response frame is dependent on the content of the Command Channel Select Register (address 3–6). When addressing multiple devices, the response from each device may vary in length depending on the configuration of the addressed device. Additionally, there may be a delay in the expected response(s) depending on the configuration information stored in the Voltage and Internal Temperature Sampling Period Register (address 62), AUX Sampling Period Register (address 63–66), and Test Sampling Period Register (address 67–68). All of the aforementioned registers affect the channel sampling period.

### 7.5.3.1 Single Device Write with Response Command Frame

Interpretation of the Data field in a Single Device Write with Response frame depends on the target register of the command.

If the target register is the Command Register (address 2), then the data bytes may contain the command, new content for the Command Channel Select Register, and new content for the Averaging Register. If the data for the Command Channel Register and Averaging Register are omitted from the Single Device Write with Response Command Frame, then the previously configured values in those registers will be used. If the data are included in the command frame, then these values will be written into the respective registers and used for the requested sampling.

If the target register is not the Command Register, then the interpretation of the data bytes will be as the number of bytes being requested from the bq76PL455A minus one, starting at the register address provided in the Register Address byte of the command frame.

The DATA\_SIZE field in the Frame Initialization byte should be written with the number of data bytes in the command frame.

#### 7.5.3.1.1 Single Device Write with Response to Command Register (Address 2)

The value of the DATA\_SIZE field in the Frame Initialization byte for this case is typically 001 (1 byte), 101 (5 bytes) or 110 (six bytes). These variations correspond to commands which:

1. Send only the sample command request and expect the bq76PL455A to use the preprogrammed sampling values in the registers that control sampling.
2. Send the sample command request and the value for the Channel Select Register (address 3–6), but expect the bq76PL455A to use the preprogrammed value in the Averaging Register (address 7). The data bytes from the command frame will overwrite the Channel Select Register.
3. Send the sample command request and the values for the Channel Select Register (address 3–6) and Averaging Register (address 7). The data bytes from the command frame will overwrite the respective register for both the Channel Select Register and the Averaging Register.

The size of the response frame in response to a command frame of this type is directly related to the number of channels selected by either the preprogrammed data in the Channel Select Register (address 3–6) or the data passed to the bq76PL455A in the command frame.

Three examples follow. All three examples target the device at Device Address 00, which is typically the address of a single device or the address of the lowest device in a stack of devices.

##### 7.5.3.1.1.1 Data Contains Command Only

For the purpose of this example, assume the following start conditions:

1. Content of Channel Select Register before command: 0FFF5500
2. Content of Averaging Register before command: 00

	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	001 (binary)		
Device Address	00							
Register Address	02							
Data (Command)	00							
CRC (MSB)	29							
CRC (LSB)	5C							

Notice that the DATA\_SIZE field in the Frame Initialization byte is 001. This means this Command Frame contains one data byte. This one data byte contains the Command for the Command Register (in this case 00). For more details regarding the Command Register, refer to the Command Register in [Register Details](#).

The expected response frame to this example command frame would contain 35 bytes: one Frame Initialization byte, 32 data bytes (two bytes for each of the sixteen-selected channels), and two-CRC bytes.

The content of the CHANNELS register and of the OVERSMPL register will remain unchanged.

#### 7.5.3.1.1.2 Data Contains Command and Channel Selection

For the purpose of this example ([Table 5](#)), assume the following start conditions:

1. Content of Channel Select Register before command: 0FFF5500
2. Content of Averaging Register before command: 00

**Table 5. Command and Channel Selection Example**

	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	101 (binary)		
Device Address	00							
Register Address	02							
Data (Command)	00							
Data (Channel Select MSB)	FF							
Data (Channel Select)	FF							
Data (Channel Select)	01							
Data (Channel Select LSB)	00							
CRC (MSB)	C8							
CRC (LSB)	09							

Notice that the DATA\_SIZE field in the Frame Initialization byte is 5 (b'101). This means that the Command Frame contains five data bytes. The first data byte contains the Command for the Command Register (in this case 00). The second through fifth data bytes contain the channel selection data, which the device writes to the Channel Select Register as part of this command. For more details on register usage, refer to [Register Details](#) for details.

The expected response frame to this example command frame would contain 37 bytes: one Frame Initialization byte, 34 data bytes (two bytes for each of the seventeen-selected channels), and two CRC bytes.

The content of the Channel Select Register will change. Resulting register content will be as follows:

1. Content of Channel Select Register after command: FFFF0100
2. Content of Averaging Register after command: 00

#### 7.5.3.1.1.3 Data Contains Command, Channel Selection, and Averaging Selection

For the purpose of this example, assume the following start conditions:

1. Content of Channel Select Register before command: 0FFF5500
2. Content of Averaging Register before command: 00

**Table 6. Command, Channel Selection, and Averaging Selection Example**

	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	110 (binary)		
Device Address	00							
Register Address	02							
Data (Command)	00							
Data (Channel Select MSB)	FF							
Data (Channel Select)	FF							
Data (Channel Select)	0F							

**Table 6. Command, Channel Selection, and Averaging Selection Example (continued)**

	7	6	5	4	3	2	1	0
Data (Channel Select LSB)	00							
Data (Averaging Select)	7B							
CRC (MSB)	3D							
CRC (LSB)	86							

Notice that the DATA\_SIZE field in the Frame Initialization byte is 6 (b'110). This means this Command Frame contains six data bytes. The first data byte contains the Command for the Command Register (in this case 00). The second through fifth data bytes contain the channel selection data, which the bq76PL455A device writes to the Channel Select Register as part of this command. The sixth data byte contains the averaging configuration data, which the device writes to the Averaging Register as part of this command. For more details on register usage, refer to [Register Details](#) for details.

The expected response frame to this example command frame would contain 43 bytes: one Frame Initialization byte, 40 data bytes (two bytes for each of the twenty selected channels), and two CRC bytes.

The content of the Channel Select Register and the Averaging Register will change. Resulting register content will be as follows:

1. Content of Channel Select Register after command: FFFF0F00
2. Content of Averaging Register after command: 7B

#### 7.5.3.1.2 Single Device Write with Response to Register(s) Other than Command Register

The value of the DATA\_SIZE field in the Framing Initialization byte for this case is typically 001 (1 byte). The interpretation of this value will be as the number of expected data bytes in the response frame minus one. For instance, if the expectation were to be to read the four bytes contained in the Channel Select Register, the data byte would contain 03 (four minus one).

Two examples follow. All examples in this section target the device at Device Address 00, which is typically the address of a single device or the address of the lowest device in a stack of devices.

##### 7.5.3.1.2.1 Requesting Four Bytes of Data from a Single Register

This command example requests four bytes of data, all from a single register. In the case of this example, the four bytes will come from the Channel Select Register at address 3–6. The most-significant byte of the four-byte register will be the first data byte in the response frame.

	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	001 (binary)		
Device Address	00							
Register Address	03							
Data (Desired Number of Bytes – 1)	03							
CRC (MSB)	68							
CRC (LSB)	CD							

Notice that the DATA\_SIZE field in the Frame Initialization byte is 001. This means this Command Frame contains one data byte. This data byte contains the desired number of response bytes minus one.

The response frame will contain seven bytes: one Frame Initialization byte, four data bytes, and two CRC bytes.

##### 7.5.3.1.2.2 Requesting Multiple Bytes across Register Boundaries

It is possible to request data from multiple registers across register boundaries. When performing this type of read, Reserved Register Addresses can also be in the block of registers being read. Reads of Reserved Register Addresses will always return zero and one must count these bytes in the requested number of data bytes. In this example, the request is for the data from three registers [the Channel Select Register (address 3–6), Averaging Register (address 7), and Device Address Register (address 10)]. These registers contain six bytes of data; however, two Reserved Register Addresses (addresses 8 and 9) lie between the Averaging Register (address 7) and the Device Address Register (address 10), so the request must be for eight bytes of data.

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	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	001 (binary)		
Device Address	01							
Register Address	03							
Data (Desired Number of Bytes - 1)	07							
CRC (MSB)	38							
CRC (LSB)	CE							

**NOTE**

The DATA\_SIZE field in the Frame Initialization byte is 1, indicating that this command frame contains a single data byte. This data byte indicates the number of desired bytes in the response (minus one).

The response frame will contain eleven bytes: one Frame Initialization byte, eight data bytes, and two CRC bytes.

**7.5.3.2 Single Device Write without Response Command Frame**

A Single Device Write without Response command is indicated when FRM\_TYPE = 1 and REQ\_TYPE = 1. In this example, the register address size is 8-bits (ADDR\_SIZE = 0) and the data length written is 1 byte (DATA\_SIZE). No Response Frame is expected to be returned.

The command in the example writes a single byte value to the Averaging Register (address 7).

For the purpose of this example, assume the following start conditions:

1. Content of Averaging Register before command: 00

	7	6	5	4	3	2	1	0
Command Frame Init	1	001 (binary)			0	001 (binary)		
Device Address	03							
Register Address	07							
Data (New Data for Target Register)	05							
CRC (MSB)	1E							
CRC (LSB)	CF							

The content of the Averaging Register will change. Resulting Averaging Register content will be: 05.

To write more than one byte to the bq76PL455A, the DATA\_SIZE field in the Frame Initialization byte should be updated and additional data bytes added to the command frame. A single command frame of this type can write up to eight, data bytes.

**7.5.3.3 Group Write With Response Command Frame**

There are several different ways to format the Group Write with Response command frame, and the interpretation of the data bytes will be different depending on the command frame configuration.

The Group Write with Response, which targets the Command register (address 2), has several different configurations. These configurations also differ from the two configurations of the Group Write with Response when it is targeted to a register other than the Command register. Primary examples of these different configurations are in the following sections.

It is important to note that devices in defined Groups **must** consist of devices with consecutive addresses. The device with the lowest address should be located closest to the host (that is, higher addresses should be located higher in the stack). Devices will respond to Group Write with Response command frames in order of decreasing address. If an address does not exist, the device will stop the responses. The recommendation is to have a group in which devices only have contiguous addresses. To establish Group IDs, program the Group ID Register (address 11) of all devices in a specific group to the same value.

### NOTE

For the following configuration examples, assume a daisy chain of four devices with addresses 00–03 in which devices at address 01 and address 02 belong to Group ID 01, and the devices at address 00 and address 03 belong to Group ID 00.

#### 7.5.3.3.1 Configuration 1: Group Write with Response to Command Register with Sampling Parameters Included in Command Frame

In response to the command frame in this example, each bq76PL455A in the specified group will write the new sample parameters into the CHANNELS and OVERSMPL registers, sample the channels identified in the data parameters, store the results, and send a response frame containing the sample data. In this example, the user expects two complete response frames, since there are two devices in the addressed group.

	7	6	5	4	3	2	1	0
Command Frame Init	1	010 (binary)			0	110 (binary)		
Group ID	01							
Register Address	02							
Data (Command)	02							
Data (Channel Select MSB)	FF							
Data (Channel Select)	FF							
Data (Channel Select)	55							
Data (Channel Select LSB)	00							
Data (Averaging Setting)	00							
CRC (MSB)	04							
CRC (LSB)	59							

For details on how to read the response, refer to [Register Details](#). A simplified overview of the meaning of the data bytes in this example is in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
A6	1 010 0 110	Command frame, Group Write with Response = REQ_TYPE, 8-bit Register Addressing, 6 data bytes = DATA_SIZE
01	00000001	Target is Group ID = 01
02	00000010	Target Register = 02 (Command Register)
02	000 00010	Upper three bits define Command sent to Command register, lower 5 bits is address of highest device in group to respond
FF	11111111	Select Channels 16 to 9
FF	11111111	Select Channels 8 to 1
55	01010101	Select AUX6, AUX4, AUX2 and AUX0
00	00000000	Do not select temperature or additional channels
00	00000000	No averaging
04	00000100	CRC
59	01011001	CRC

### 7.5.3.3.2 Configuration 2: Group Write with Response to Command Register without Sampling Parameters Included in Command Frame

#### NOTE

Sampling parameters come from values already stored in the CHANNELS and OVERSMPL registers.

In response to the sample command frame in this example, each bq76PL455A in the specified group will sample the channels identified by the values currently stored in the Command Channel Select register (address 3–6) and sample them using the averaging setting currently set in the Averaging register (address 7).

	7	6	5	4	3	2	1	0
Command Frame Init	1	010 (binary)			0	001 (binary)		
Group ID	01							
Register Address	02							
Data (Command)	02							
CRC (MSB)	F2							
CRC (LSB)	9D							

For details on how to interpret the response, refer to [Register Details](#). A simplified overview of the meaning of the data bytes in this example is in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
A1	1 010 0 001	Command frame, Group Write with Response = REQ_TYPE, 8-bit Register Addressing, 1 data byte = DATA_SIZE
01	00000001	Target is Group ID = 01
02	00000010	Target Register = 02 (Command Register)
02	000 00010	Upper three bits define Command sent to Command register, lower 5 bits is address of highest device in group to respond
F2	11110010	CRC
9D	10011101	CRC

### 7.5.3.3.3 Configuration 3: Group Write with Response to non-Command Register

#### NOTE

This configuration uses two bytes for addressing and response size.

The sample command frame in this example will read the data currently stored in the Command Channel Select (address 3–6) register. Interpretation of the data bytes is in the left-hand column of the following table. The DATA\_SIZE field in the Frame Initialization byte indicates the number of data bytes in the command frame.

	7	6	5	4	3	2	1	0
Command Frame Init	1	010 (binary)			0	010 (binary)		
Group ID	01							
Register Address	03							
Data (Address of Highest Device in Group to Respond)	02							
Data (Expected Number of Response Data Bytes – 1)	03							
CRC (MSB)	49							
CRC (LSB)	44							

For details on how to interpret the response, refer to [Register Details](#). A simplified overview of the meaning of the data bytes in this example is in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
A2	1 010 0 001	Command frame, Group Write with Response = REQ_TYPE, 8-bit Register Addressing, 2 data bytes = DATA_SIZE
01	00000001	Target is Group ID = 01
03	00000011	Target Register = 03 (Command Channel Select Register)
02	00000010	Address of highest device in target group
03	00000011	Number of Data Bytes – 1 expected in response (4 bytes in this example)
49	01001001	CRC
44	01000100	CRC

The command frame in this example will generate a response frame from each of the two devices targeted by the command frame. Each response frame will contain data stored in the Command Channel Select register of the responding bq76PL455A. The response frame from the bq76PL455A at the highest address in the addressed group will arrive first. If the stored data were FFFF8000 (hex) for the device at Device Address 02 in Group 01 and the data were FFFF0100 (hex) for the device at Device Address 01 in Group ID 01, then the response frames would be as in the following table.

	7	6	5	4	3	2	1	0
Response Frame Init	0	0000011 (binary)						
Data	FF							
Data	FF							
Data	80							
Data	00							
CRC (MSB)	25							
CRC (LSB)	E4							

	7	6	5	4	3	2	1	0
Response Frame Init	0	0000011 (binary)						
Data	FF							
Data	FF							
Data	01							
Data	00							
CRC (MSB)	45							
CRC (LSB)	B4							

The second of the two response frames will arrive immediately after the first response frame, so the response will typically appear to be one continuous response. Therefore, it is important to remember that each responding device will respond with a complete response frame with its own Frame Initialization byte, data bytes, and CRC bytes.

#### 7.5.3.3.4 Configuration 4: Group Write with Response to Non-Command Register

##### NOTE

This configuration uses one byte for addressing and response size.

As in the example for Configuration 3, the sample command frame in this example will read the value currently stored in the Command Channel Select (address 3–6) register, but the message to do so is one byte shorter. The expected response frames would be the same as in the example for Configuration 3.



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	7	6	5	4	3	2	1	0
Command Frame Init	1	010 (binary)			0	001 (binary)		
Group ID	01							
Register Address	03							
Data (Address of Highest Device in Group to Respond)	62							
CRC (MSB)	F3							
CRC (LSB)	25							

For details on how to interpret the data, refer to [Register Details](#). A simplified overview of the meaning of the data bytes in this example is in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
A1	1 010 0 001	Command frame, Group Write with Response = REQ_TYPE, 8-bit Register Addressing, 1 data byte = DATA_SIZE
01	00000001	Target is Group ID = 01
03	00000011	Target Register = 03 (Command Channel Select Register)
62	011 00010	Upper three bits are Number of Data Bytes – 1 expected in response, lower 5 bits is address of highest device in group to respond
F3	11110011	CRC (MSB)
25	00100101	CRC (LSB)

**NOTE**

Although not recommended, each of the configurations can also use 16-bit register addressing, which would add another byte for the MSB of the register address to the command frame.

**7.5.3.4 Group Write without Response Command Frame**

A Group Write without Response command is indicated when FRM\_TYPE = 1 and REQ\_TYPE = 3 (011 binary). In this example, the register address size is 8-bits (ADDR\_SIZE = 0) and the data length written is 1 byte (DATA\_SIZE). No Response Frame is expected to be returned.

In response to this example command frame, each bq76PL455A in the target group will write the value in the data byte to the target register (the Averaging Register in this example). For more information on the effect of this example command frame, see [Register Details](#).

	7	6	5	4	3	2	1	0
Command Frame Init	1	011 (binary)			0	001 (binary)		
Group ID	01							
Register Address	07							
Data	7B							
CRC (MSB)	34							
CRC (LSB)	EF							

**7.5.3.5 Broadcast Write with Response Command Frame**

As with the Single Write and Group Write with Response command frames, the interpretation of the Broadcast Write with Response command frame bytes will be different when the target register is the Command Register (address 2) compared to when the target is another register. Determination of response frame lengths when the command frame targets the Command Register will be by the content of the Channel Select Register of each targeted bq76PL455A device.

Broadcast Write command frames do not contain a Device Address/Group ID byte. This is the primary deviation from the examples already provided in the Group Write with Response section.



With the exception described previously, formation of the Broadcast Write with Response command frames can be in a similar fashion to the various configuration examples in the *Group Write with Response, Group\_Write\_With\_Response Command Frame*.

As with the Group Write with Response commands frames, Broadcast Write with Response command frames can utilize one of two formats to indicate the address of the highest device to respond and the number of bytes expected in response from each targeted device. One format uses one byte to specify both the address of the highest board in the response chain and the number of desired response bytes. The other format uses two bytes to specify the address of the highest responding device and the desired number of response bytes separately (first the address, then the number of bytes-1).

The two command frames that follow provide an example of each format.

An example of the two-byte method (to read the Communication Configuration register):

	7	6	5	4	3	2	1	0
Command Frame Init	1	110 (binary)			0	010 (binary)		
Register Address	10							
Data (Address of highest responder)	03							
Data (Number of response data bytes – 1)	01							
CRC (MSB)	F6							
CRC (LSB)	8D							

For further details on how to interpret the data, refer to [Register Details](#). A simplified overview of the meaning of the data bytes in this example is in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
E2	11100010	Command frame, Broadcast Write with Response = REQ_TYPE, 8-bit Register Addressing, 2 data bytes = DATA_SIZE
10	00010000	Target Register Address (Communication Configuration Register)
03	00000011	Address of highest (first) device to respond
01	00000001	Number of data bytes –1 expected in response (that is, 2 bytes)
F6	11110110	CRC (MSB)
8D	10001101	CRC (LSB)

An example of the one-byte method (to read the Communication Configuration register):

	7	6	5	4	3	2	1	0
Command Frame Init	1	110 (binary)			0	001 (binary)		
Register Address	10							
Data (Data Size and Address of highest responder)	22							
CRC (MSB)	DC							
CRC (LSB)	1F							

For further details on how to interpret the data, refer to [Register Details](#). A simplified overview of the meaning of the data bytes in this example is in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
E1	11100001	Command frame, Broadcast Write with Response = REQ_TYPE, 8-bit Register Addressing, 1 data byte = DATA_SIZE
10	00010000	Target Register Address (Communication Configuration Register)
22	001 00010	Upper three bits are Number of Data Bytes – 1 expected in response, lower 5 bits is address of highest device to respond
DD	11011101	CRC
EF	11101111	CRC

### 7.5.3.6 Broadcast Write without Response Command Frame

A Broadcast Write without Response command is indicated when FRM\_TYPE = 1 and REQ\_TYPE = 7 (111 binary).

In this example, the register address size is 8-bits (ADDR\_SIZE = 0) and the data length written is 1 byte (DATA\_SIZE). Note that since this command is for all devices, there is no Device Address/Group ID byte in the command frame.

No Response Frame is expected to be returned.

	7	6	5	4	3	2	1	0
Command Frame Init	1	111 (binary)			0	001 (binary)		
Register Address	C8							
Data	12							
CRC (MSB)	86							
CRC (LSB)	3E							

This example writes 12 (hex) into one of the Scratchpad Register bytes at address 200 (C8 hex) on all targeted devices. See [Register Details](#) for further information on the effects of changing register values.

### 7.5.4 Response Frame

A Response Frame is indicated when FRM\_TYPE = 0. Note that bits 6 through 0 in the Frame Initialization byte use a different format from the Command Frame format, as described in [Frame Initialization Byte](#).

In this example, the response data length is 3 bytes (RESP\_BYTES – 1 = 2). There is support for data lengths from 1 through 128 bytes. Since the protocol described here is for a single initiator (microcontroller) system, the initiator is always the intended target of a Response Frame.

If a command frame targets more than one device, responses go back to the initiator first from the device at the highest address in the targeted group, then the next highest address, and so forth until all devices in the targeted group have responded. Each device will respond with a complete response frame, which includes a Frame Initialization byte, one or more data bytes, and two CRC bytes.

If the command frame targets more than one device and the target register of that command frame is the Command Register, then there may be a delay in the responses. This delay is due to the time required for the targeted bq76PL455A devices to sample, store, and respond with their newly sampled data. The delay in the responses will be dependent on the sampling period and channel selection configuration of each targeted device.

	7	6	5	4	3	2	1	0
Response Frame Init	0 (binary)	0000010 (binary)						
Data	9B							
Data	8C							
Data	7D							
CRC (MSB)	D4							
CRC (LSB)	B6							

## 7.6 Register Maps

### 7.6.1 Conventions and Notations

The following conventions are in use throughout the document.

- Keywords that refer to specific software registers are in ALL CAPITALS.
- Each byte in a multi-byte register can be addressed individually. The format is big endian with the most-significant byte stored in the lowest physical address. Data are returned in lowest-to-highest address order.
- Locations marked "RESERVED" should not be written to, and always return 0.
- Bits marked "RESERVED" or "reserved" should be written as 0, unless otherwise specified.

## Register Maps (continued)

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### NOTE

Failure to comply with the preceding two statements may result in unexpected device behavior.

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### 7.6.1.1 Register Usage

All registers, except the Command Register (CMD), operate in the same manner. For all registers except CMD, reading will return the value stored in the addressed register, and writing will store a new value into the addressed register.

The Command Register (CMD) is a special register that accepts commands. A value written to CMD causes the bq76PL455A to carry out a specific action and this may include the generation of a response from the bq76PL455A. For example, a Synchronous Sample command written to CMD causes a response that contains the conversion values for any selected channels.

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### NOTE

New commands should not be written until the current command is complete and any requested response has been received in its entirety, or a timeout has occurred.

All unused bits in the registers should always be written as 0, unless otherwise noted.

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The register space is byte-addressable. Reads or writes can cover any number of bytes. Multi-byte registers (16-bit or 32-bit, and so forth) can read them as individual bytes, one at a time, or as a single register. The most-significant byte of multi-byte registers is stored at the lower address.

User firmware should not write to register addresses shown as "RESERVED" and addresses not shown in [Register Summary](#). Reserved Register Addresses will return zero if read, unless otherwise noted.

## Register Maps (continued)

### 7.6.2 Register Summary

**KEY:** **ADDR** = Address; **R** = Read; **W** = Write; **R/W** = Read/Write; **EE** = EEPROM; **NA** = value is volatile storage only and not included in the EEPROM; '-' indicates the location is reserved for future use; (hex value) indicates the default value programmed into the EEPROM location, that will be copied to the associated volatile register upon successful reset initialization; **CSUM** = Checksum: **Y** = value included in checksum calculation; **N** = value not included in calculation.

**Table 7. Register Summary**

ADDR HEX	ADDR DECIMAL	BITS	NAME	DESCRIPTION	DEFAULT (HEX)		R/W	CSUM <sup>(3)</sup>
					RAM <sup>(1)</sup>	EE <sup>(2)</sup>		
00–01	0–1	16	SREV	Silicon Revision	0806	N/A	R	N
02	2	8	CMD	Command	00	N/A	W	N
03–06	3–6	32	CHANNELS	Command channel select	0000 0000	FFFF 0000	R/W	Y
07	7	8	OVERSMPL	Command averaging (oversampling)	00	7B	R/W	Y
08–09	8–9	16	RESERVED	<i>Reserved for future use</i>	00	—	R/W	N
0A	10	8	ADDR	Device address	00	00	R/W	Y
0B	11	8	GROUP_ID	(Device) Group Identifier	00	00	R/W	Y
0C	12	8	DEV_CTRL	Device control	20	N/A	R/W	N
0D	13	8	NCHAN	Number of channels enabled for conversion	00	10	R/W	Y
0E	14	8	DEVCONFIG	Device configuration	00	10	R/W	Y
0F	15	8	PWRCONFIG	Power configuration	00	80	R/W	Y
10–11	16–17	16	COMCONFIG	Communications configuration	1000	1080	R/W	Y
12	18	8	TXHOLDOFF	UART Transmitter holdoff	00	00	R/W	Y
13	19	8	CBCONFIG	Cell balancing (equalization) configuration	00	00	R/W	Y
14–15	20–21	16	CBENBL	Cell balancing enables	0000	N/A	R/W	Y
16–1D	22–29	64	RESERVED	<i>Reserved for future use</i>	00	—	R/W	N
1E–1F	30–31	16	TSTCONFIG	Built-In Self-Test (BIST) configuration	0000	N/A	R/W	Y
20–21	32–33	16	TESTCTRL	BIST control	0000	N/A	R/W	N
22–24	34–36	24	TEST_ADC	ADC BIST control	0000	N/A	R/W	Y
25	37	8	TESTAUXPU	Test control—AUX pull-up resistors	00	N/A	R/W	Y
26–27	38–39	16	RESERVED	<i>Reserved for future use</i>	00	—	R/W	N
28	40	8	CTO	Communications time-out	00	DC	R/W	Y
29–2B	41–43	24	CTO_CNT	Communications time-out counter	0000	N/A	R/W	N
2C–31	44–49	40	RESERVED	<i>Reserved for future use</i>	0000	—	R/W	N
32	50	8			00	0	R/W	Y
33–36	51–54	32			0000	0000	R/W	Y
37	55	8			00	00	R/W	Y
38–3C	56–60	40	RESERVED	<i>Reserved for future use</i>	0000	—	R/W	N
3D	61	8	SMPL_DLY1	Initial sampling delay	00	0	R/W	Y
3E	62	8	CELL_SPER	Cell and die temperature measurement period	00	BC	R/W	Y
3F–42	63–66	32	AUX_SPER	AUX channels sampling period	0000 0000	4444 4444	R/W	Y
43–44	67–68	16	TEST_SPER	ADC test sampling period	0000	F999	R/W	Y
45–4F	69–79	88	RESERVED	<i>Reserved for future use</i>	00	—	R/W	N
50	80	8	SHDN_STS	Shutdown recovery status	00	N/A	R	N
51	81	8	STATUS	Device status	81 <sup>(4)</sup>	N/A	R/W	N
52–53	82–83	16	FAULT_SUM	Fault summary	0100 <sup>(4)</sup>	N/A	R/W	N
54–55	84–85	16	FAULT_UV	Undervoltage faults	0000 <sup>(4)</sup>	N/A	R/W	N
56–57	86–87	16	FAULT_OV	Overvoltage faults	0000 <sup>(4)</sup>	N/A	R/W	N
58–59	88–89	16	FAULT_AUX	AUX threshold exceeded faults	0000 <sup>(4)</sup>	N/A	R/W	N
5A–5B	90–91	16	FAULT_2UV	Comparator UV faults	0000 <sup>(4)</sup>	N/A	R/W	N

## Register Maps (continued)

**Table 7. Register Summary (continued)**

ADDR HEX	ADDR DECIMAL	BITS	NAME	DESCRIPTION	DEFAULT (HEX)		R/W	CSUM <sup>(3)</sup>
					RAM <sup>(1)</sup>	EE <sup>(2)</sup>		
5C–5D	92–93	16	FAULT_2OV	Comparator OV faults	0000 <sup>(4)</sup>	N/A	R/W	N
5E–5F	94–95	16	FAULT_COM	Communication faults	0000 <sup>(4)</sup>	N/A	R/W	N
60	96	8	FAULT_SYS	System fault	80 <sup>(4)</sup>	N/A	R/W	N
61–62	97–98	16	FAULT_DEV	Device fault	0000 <sup>(4)</sup>	N/A	R/W	N
63	99	8	FAULT_GPI	General purpose input (GPIO) fault	00 <sup>(4)</sup>	N/A	R/W	N
64–67	100–103	32	RESERVED	<i>Reserved for future use</i>	00	—	R/W	N
68–69	104–105	16	MASK_COMM	Communications FAULT mask register	0000	0000	R/W	Y
6A	106	8	MASK_SYS	System FAULT mask register	0	00	R/W	Y
6B–6C	107–108	16	MASK_DEV	Chip FAULT mask register	0000	0000	R/W	Y
6D	109	8	RESERVED	<i>Reserved for future use</i>	0	—	R/W	N
6E–6F	110–111	16	FO_CTRL	FAULT output control	0000	FFC0	R/W	Y
70–77	112–119	64	RESERVED	<i>Reserved for future use</i>	0	—	R/W	N
78	120	8	GPIO_DIR	GPIO direction control	00	00	R/W	Y
79	121	8	GPIO_OUT	GPIO output control	00	00	R/W	Y
7A	122	8	GPIO_PU	GPIO pull-up resistor control	00	00	R/W	Y
7B	123	8	GPIO_PD	GPIO pull-down resistor control	00	00	R/W	Y
7C	124	8	GPIO_IN	GPIO input value	00	N/A	R	N
7D	125	8	GP_FLT_IN	GPIO input 0/1 FAULT assertion state	00	00	R/W	Y
7.00E–81	126–129	32	RESERVED	<i>Reserved for future use</i>	00	—	R/W	N
82–85	130–133	32	MAGIC1	"Magic" value enables EEPROM write	0000 0000	N/A	W	N
86–8B	134–139	48	RESERVED	<i>Reserved for future use</i>	00	—	R/W	N
8C	140	8	COMP_UV	Comparator undervoltage threshold	00	00	R/W	Y
8D	141	8	COMP_OV	Comparator overvoltage threshold	00	FE	R/W	Y
8E–8F	142–143	16	CELL_UV	Cell undervoltage threshold	0000	0000	R/W	Y
90–91	144–145	16	CELL_OV	Cell overvoltage threshold	0000	FFFC	R/W	Y
92–93	146–147	16	AUX0_UV	AUX0 undervoltage threshold	0000	0000	R/W	Y
94–95	148–149	16	AUX0_OV	AUX0 overvoltage threshold	0000	FFFC	R/W	Y
96–97	150–151	16	AUX1_UV	AUX1 undervoltage threshold	0000	0000	R/W	Y
98–99	152–153	16	AUX1_OV	AUX1 overvoltage threshold	0000	FFFC	R/W	Y
9A–9B	154–155	16	AUX2_UV	AUX2 undervoltage threshold	0000	0000	R/W	Y
9C–9D	156–157	16	AUX2_OV	AUX2 overvoltage threshold	0000	FFFC	R/W	Y
9E–9F	158–159	16	AUX3_UV	AUX3 undervoltage threshold	0000	0000	R/W	Y
A0–A1	160–161	16	AUX3_OV	AUX3 overvoltage threshold	0000	FFFC	R/W	Y
A2–A3	162–163	16	AUX4_UV	AUX4 undervoltage threshold	0000	0000	R/W	Y
A4–A5	164–165	16	AUX4_OV	AUX4 overvoltage threshold	0000	FFFC	R/W	Y
A6–A7	166–167	16	AUX5_UV	AUX5 undervoltage threshold	0000	0000	R/W	Y
A8–A9	168–169	16	AUX5_OV	AUX5 overvoltage threshold	0000	FFFC	R/W	Y
AA–AB	170–171	16	AUX6_UV	AUX6 undervoltage threshold	0000	00000	R/W	Y
AC–AD	172–173	16	AUX6_OV	AUX6 overvoltage threshold	0000	FFFC	R/W	Y
AE–AF	174–175	16	AUX7_UV	AUX7 undervoltage threshold	0000	00000	R/W	Y
B0–B1	176–177	16	AUX7_OV	AUX7 overvoltage threshold	0000	FFFC	R/W	Y
B2–BD	178–189	96	RESERVED	<i>Reserved for future use</i>	0000	—	R/W	N
BE–C5	190–197	64	LOT_NUM	Device Lot Number	00...	Factory <sup>(5)</sup>	R	N
C6–C7	198–199	16	SER_NUM	Device Serial Number	00...	Factory <sup>(5)</sup>	R	N
C8–CF	200–207	64	SCRATCH	User-defined data	00...	00...	R/W	Y
D0–D1	208–209	16	RESERVED	<i>Reserved for future use</i>	00	—	R/W	N
D2	210	8	VSOFFSET	ADC voltage offset correction	00	00	R/W	Y

## Register Maps (continued)

**Table 7. Register Summary (continued)**

ADDR HEX	ADDR DECIMAL	BITS	NAME	DESCRIPTION	DEFAULT (HEX)		R/W	CSUM <sup>(3)</sup>
					RAM <sup>(1)</sup>	EE <sup>(2)</sup>		
D3	211	8	VSGAIN	ADC voltage gain correction	00	00	R/W	Y
D4-D5	212–213	16	AX0OFFSET	AUX0 ADC offset correction	0000	0000	R/W	Y
D6-D7	214–215	16	AX1OFFSET	AUX1 ADC offset correction	0000	0000	R/W	Y
D8-D9	216–217	16	AX2OFFSET	AUX2 ADC offset correction	0000	0000	R/W	Y
DA-DB	218–219	16	AX3OFFSET	AUX3 ADC offset correction	0000	0000	R/W	Y
DC-DD	220–221	16	AX4OFFSET	AUX4 ADC offset correction	0000	0000	R/W	Y
DE-DF	222–223	16	AX5OFFSET	AUX5 ADC offset correction	0000	0000	R/W	Y
E0-E1	224–225	16	AX6OFFSET	AUX6 ADC offset correction	0000	0000	R/W	Y
E2-E3	226–227	16	AX7OFFSET	AUX7 ADC offset correction	0000	0000	R/W	Y
E4-E5	228–229	16	RESERVED	<i>Reserved for future use</i>	00	—	R/W	N
E6-ED	230–237	64	TSTR_ECC	ECC Test Results	00...	N/A	R	N
EE-EF	238–239	16	RESERVED	<i>Reserved for future use</i>	0	—	R/W	N
F0-F3	240–243	32	CSUM	Saved checksum value	1234 5678	C9B0 12F7	R/W	N
F4-F7	244–247	32	CSUM_RSLT <sup>(6)</sup>	Checksum Readout	C9B0 12F7	N/A	R	N
F8-F9	248–249	16	TEST_CSUM	Checksum Test Result	0000	N/A	R	N
FA	250	8	EE_BURN	EEPROM Burn Count; up-counter	FA	Y	R	N
FB	251	8	RESERVED	<i>Reserved for future use</i>	00	—	R/W	N
FC-FF	252–255	32	MAGIC2	"Magic" value enables EEPROM write	0000 0000	N/A	W	N

(1) Initial value loaded at device RESET or POR.

(2) Value stored in EEPROM from factory may be overwritten by the user. This value is loaded after initial RESET or POR value (see note <sup>(1)</sup>) only if the ECC is valid or correctable for the block.

(3) CSUM: This register is included ('Y') or not included ('N') in the USER checksum calculation.

(4) Value shown after wakeup and only the FAULT\_SYS[SYS\_RESET] fault conditions exist.

(5) Factory programmed values will vary from device to device.

(6) This register value is set indirectly by the contents of all register values included in the checksum. The value updates after any register change for registers included in the checksum.

**Table 8. Registers in Alphabetical Order**

NAME	DESCRIPTION	ADDR HEX	ADDR DECIMAL
ADDR	Device address	0A	10
AUX_SPER	AUX channels sampling period	3F–42	63–66
AUX0_OV	AUX0 overvoltage threshold	94–95	148–149
AUX0_UV	AUX0 undervoltage threshold	92–93	146–147
AUX1_OV	AUX1 overvoltage threshold	98–99	152–153
AUX1_UV	AUX1 undervoltage threshold	96–97	150–151
AUX2_OV	AUX2 overvoltage threshold	9C–9D	156–157
AUX2_UV	AUX2 undervoltage threshold	9A–9B	154–155
AUX3_OV	AUX3 overvoltage threshold	A0–A1	160–161
AUX3_UV	AUX3 undervoltage threshold	9E–9F	158–159
AUX4_OV	AUX4 overvoltage threshold	A4–A5	164–165
AUX4_UV	AUX4 undervoltage threshold	A2–A3	162–163
AUX5_OV	AUX5 overvoltage threshold	A8–A9	168–169
AUX5_UV	AUX5 undervoltage threshold	A6–A7	166–167
AUX6_OV	AUX6 overvoltage threshold	AC–AD	172–173
AUX6_UV	AUX6 undervoltage threshold	AA–AB	170–171

**Table 8. Registers in Alphabetical Order (continued)**

NAME	DESCRIPTION	ADDR HEX	ADDR DECIMAL
AUX7_OV	AUX7 overvoltage threshold	B0–B1	176–177
AUX7_UV	AUX7 undervoltage threshold	AE–AF	174–175
AX0OFFSET	AUX0 ADC offset correction	D4–D5	212–213
AX1OFFSET	AUX1 ADC offset correction	D6–D7	214–215
AX2OFFSET	AUX2 ADC offset correction	D8–D9	216–217
AX3OFFSET	AUX3 ADC offset correction	DA–DB	218–219
AX4OFFSET	AUX4 ADC offset correction	DC–DD	220–221
AX5OFFSET	AUX5 ADC offset correction	DE–DF	222–223
AX6OFFSET	AUX6 ADC offset correction	E0–E1	224–225
AX7OFFSET	AUX7 ADC offset correction	E2–E3	226–227
CBCONFIG	Cell balancing (equalization) configuration	13	19
CBENBL	Cell balancing enables	14–15	20–21
CELL_OV	Cell overvoltage threshold	90–91	144–145
CELL_SPER	Cell and die temperature measurement period	3E	62
CELL_UV	Cell undervoltage threshold	8E–8F	142–143
CHANNELS	Command channel select	03–06	3–6
CMD	Command	02	2
COMCONFIG	Communications configuration	10–11	16–17
COMP_OV	Comparator overvoltage threshold	8D	141
COMP_UV	Comparator undervoltage threshold	8C	140
CSUM	Saved checksum value	F0–F3	240–243
CSUM_RSLT	Checksum Readout	F4–F7	244–247
CTO	Communications time-out	28	40
CTO_CNT	Communications time-out counter	29–2B	41–43
DEV_CTRL	Device control	0C	12
DEVCONFIG	Device configuration	0E	14
EE_BURN	EEPROM Burn Count; up-counter	FA	250
FAULT_AUX	AUX threshold exceeded faults	58–59	88–89
FAULT_COM	Communication faults	5E–5F	94–95
FAULT_2OV	Comparator OV faults	5C–5D	92–93
FAULT_2UV	Comparator UV faults	5A–5B	90–91
FAULT_DEV	Device fault	61–62	97–98
FAULT_GPI	General purpose input (GPIO) fault	63	99
FAULT_OV	Overvoltage faults	56–57	86–87
FAULT_SUM	Fault summary	52–53	82–83
FAULT_SYS	System fault	60	96
FAULT_UV	Undervoltage faults	54–55	84–85
FO_CTRL	FAULT output control	6E–6F	110–111
GP_FLT_IN	GPIO input 0/1 FAULT assertion state	7D	125
GPIO_DIR	GPIO direction control	78	120
GPIO_IN	GPIO input value	7C	124
GPIO_OUT	GPIO output control	79	121
GPIO_PD	GPIO pull-down resistor control	7B	123
GPIO_PU	GPIO pull-up resistor control	7A	122
GROUP_ID	(Device) Group Identifier	0B	11
LOT_NUM	Die Lot Identifier	BE–C5	190–197
MAGIC1	"Magic" value enables EEPROM write	82–85	130–133



**Table 8. Registers in Alphabetical Order (continued)**

NAME	DESCRIPTION	ADDR HEX	ADDR DECIMAL
MAGIC2	"Magic" value enables EEPROM write	FC–FF	252–255
MASK_COMM	Communications FAULT mask register	68–69	104–105
MASK_DEV	Chip FAULT mask register	6B–6C	107–108
MASK_SYS	System FAULT mask register	6A	106
NCHAN	Number of channels enabled for conversion	0D	13
OVERSMPL	Command averaging (oversampling)	07	7
PWRCONFIG	Power configuration	0F	15
RESERVED	<i>Reserved for future use</i>	08–09	9–Aug
RESERVED	<i>Reserved for future use</i>	16–1D	22–29
RESERVED	<i>Reserved for future use</i>	26–27	38–39
RESERVED	<i>Reserved for future use</i>	2C–31	44–49
RESERVED	<i>Reserved for future use</i>	32	50
RESERVED	<i>Reserved for future use</i>	33–36	51–54
RESERVED	<i>Reserved for future use</i>	37	55
RESERVED	<i>Reserved for future use</i>	38–3C	56–60
RESERVED	<i>Reserved for future use</i>	45–4F	69–79
RESERVED	<i>Reserved for future use</i>	64–67	100–103
RESERVED	<i>Reserved for future use</i>	6D	109
RESERVED	<i>Reserved for future use</i>	70–77	112–119
RESERVED	<i>Reserved for future use</i>	7.00E–81	126–129
RESERVED	<i>Reserved for future use</i>	86–8B	134–139
RESERVED	<i>Reserved for future use</i>	B2–BD	178–189
RESERVED	<i>Reserved for future use</i>	D0–D1	208–209
RESERVED	<i>Reserved for future use</i>	E4–E5	228–229
RESERVED	<i>Reserved for future use</i>	EE–EF	238–239
RESERVED	<i>Reserved for future use</i>	FB	251
SCRATCH	User-defined data	C8–CF	200–207
SER_NUM	Device serial number	C6–C7	198–199
SHDN_STS	Shutdown recovery status	50	80
SMPL_DLY1	Initial sampling delay	3D	61
SREV	Silicon Revision	00–01	0–1
STATUS	Device status	51	81
TEST_ADC	ADC BIST control	22–24	34–36
TEST_CSUM	Checksum Test Result	F8–F9	248–249
TEST_SPER	ADC test sampling period	43–44	67–68
TESTAUXPU	Test control—AUX pull-up resistors	25	37
TESTCTRL	BIST control	20–21	32–33
TSTCONFIG	Built-In Self-Test (BIST) configuration	1E–1F	30–31
TSTR_ECC	ECC Test Results	E6–ED	230–237
TXHOLDOFF	UART Transmitter holdoff	12	18
VSGAIN	ADC voltage gain correction	D3	211
VSOFFSET	ADC voltage offset correction	D2	210



### 7.6.3 Register Details

#### NOTE

The terms "Write without Response", "Write", and "write" are equivalent and synonymous. The words "Read" and "read" are equivalent to "Write with Response".

#### 7.6.3.1 SREV 0x00-01 (0-1) Device Version

This register provides the digital and analog die revisions used in the bq76PL455A device.

BIT	NAME	DESCRIPTION
[15:8]	DDIE_VER	Digital die version number (byte address 0)
[7:0]	ADIE_VER	Analog die version number (byte address 1)

#### 7.6.3.2 CMD 0x02 (2) Command

Write\_With\_Response requests directly targeted to this register cause the specified command to execute and the corresponding results to return a response. The number of bytes returned will be based on the bits selected in the CHANNELS register. Some bits in the CHANNELS register have more than one value returned, refer to their descriptions under the CHANNELS register.

#### NOTE

This transaction will return results from the command, not a read of register values.

It is not possible to read the last value written to this register. Indirect reads of this register produce an undefined value for this register.

A command sent to this register without writing the CHANNELS or OVERSMPL registers in the same frame uses the values currently in those registers. If a command writes the CHANNELS or OVERSMPL registers in the same frame then sends the command to the register, the new register values will overwrite the current register values and the execution of the command uses the new values.

Requested values return MSB first in the order that they exist in the CHANNELS register, starting with the MSB (Cell 16, Cell 15 ...). No values return for bits not selected in the CHANNELS register.

BIT	NAME	DESCRIPTION
[7:6]	Reserved	Write these bits as 0.
[4:0]	resp_addr	If set by a Broadcast_Write_With_Response or Group_Write_With_Response request, devices will respond in successive order. These bits set the address of the highest device in the group/set to respond. This value has no effect for other transaction types.

#### 7.6.3.3 CHANNELS 0x03–06 (3–6) Channel Select

When the indicated bit is set, the named channel is included when a CMD (COMMAND) is executed in the Command register.

BIT	NAME	DESCRIPTION
[31:16]	CMD_VSEL	This bitmask determines which battery cell voltages are used when a COMMAND is executed. CMD_VSEL[0] (bit 16) corresponds to cell 1, bit 31 corresponds to cell 16. For each bit in this field: 0 = Do not include this cell voltage. 1 = Include this cell voltage.
[15:8]	CMD_ASEL	This bitmask determines which auxiliary channels are used when a COMMAND is executed. CMD_ASEL[0] (bit 8) corresponds to AUX0. For each bit in this field: 0 = Do not include this AUX channel. 1 = include this AUX channel.
[7]	CMD_GTSEL	Digital die temperature. Usually used as part of self-testing.

BIT	NAME	DESCRIPTION
[6]	CMD_HTSEL	Analog die temperature. Usually used as part of self-testing.
[5]	CMD_V18SEL	VDD18 internal digital supply. Usually used as part of self-testing.
[4]	RSVD	Reserved — Always write a 0.
[3]	RSVD	Reserved — Always write a 0.
[2]	CMD_REFSEL	4.5-V analog die reference (window comparator ref) is included when a COMMAND is executed. This bit selects both the 4.5-V reference and the ground output from the reference MUX. Sampling and reporting will be 4.5 V and then ground. This command is generally used for self-testing purposes.
[1]	CMD_MODULESEL	Sum-of-cells (VMODULE) monitor is included when a COMMAND is executed. Two conversions are performed to get this value, but only the average of the two is stored and reported. TSTCONFIG[MODULE_MON_EN] is used to enable the MODULE measurement. When TSTCONFIG[MODULE_MON_EN] = 0, but CMD_MODULESEL = 1, then ground will be measured. This selection is generally used for self-testing purposes.
[0]	CMD_VMMONSEL	VM (negative supply charge pump) voltage monitor. TST_CONFIG[VM_MON_EN] is used to enable the measurement. This selection is generally used for self-testing purposes.

#### 7.6.3.4 OVERSMPL 0x07 (7) Command Oversampling

BIT	NAME	DESCRIPTION
[7]	CMD_OVS_CYCLE	This bit only applies to voltage and AUX averaging (oversampling).
		<p>= 0      Average channels by sampling multiple times on the same channel before changing channel. The initial sample period for the first sample on each channel is made per the respective ADC_PERIOD_VOL and ADC_PERIOD_AUXx time period settings, and then each subsequent average occurs at the respective CMD_OVS_HPER and CMD_OVS_GPER period settings.</p> <p>= 1      Average channels by cycling through all channels one sample per channel before resampling. All voltage averages are completed before any AUX sampling begins and then all AUX are completed before anything else. The settling time before voltage sampling is set by ADC_PERIOD_VOL and the settling time before AUX sampling is set by ADC_PERIOD_AUXx.</p>
[6:5]	CMD_OVS_HPER	<p>= 3      CMD_OVS_HPER sets the averaging period for the:</p> <ul style="list-style-type: none"> <li>Internal temperature measurement of the analog die</li> <li>4.5-V voltage reference of the analog die</li> <li>VM monitor</li> <li>Sum-of-cells (VMODULE) monitor</li> </ul> <p>When CMD_OVS_CYCLE = 0, this value also sets the period for the averaging on all the cell voltage channels.</p> <p>These bits must be set to 3 (0b11), which selects 12.6 μs as the average period. Other settings are Reserved and should not be used.</p>
[4:3]	CMD_OVS_GPER	<p>CMD_OVS_GPER sets the averaging period for:</p> <ul style="list-style-type: none"> <li>Internal temperature measurement of the digital die. Note that although CMD_OVS_GPER bits set the timing for the internal temperature measurement of the digital die, averaging is not used for this measurement.</li> <li>VDD18</li> </ul> <p>When CMD_OVS_CYCLE = 0, this value also sets the period for the averaging on all the auxiliary channels.</p> <p>= 0      4.13 μs  = 1      5.96 μs  = 2      8.02 μs  = 3      12.6 μs: <i>This setting is recommended for best accuracy in most designs. See the <a href="#">Application and Implementation</a> section for detailed information on using other settings.</i></p>

BIT	NAME	DESCRIPTION
[2:0]	CMD_OVSMP	<p>These bits set the number of times each ADC converted value will be averaged before being stored. Each converted signal will be sampled the requested number of times, averaged, and the results convergent rounded to 16 bits.</p> <p>= 0            Single sample (no averaging)  = 1            2 samples are averaged.  = 2            4 samples are averaged.  = 3            8 samples are averaged.  = 4            16 samples are averaged.  = 5            32 samples are averaged.  = 6–7        <i>Reserved, do not use this value.</i></p>

### 7.6.3.5 ADDR 0x0A (10) Device Address

BIT	NAME	DESCRIPTION
[7:5]	RSVD	Reserved — always write as zero.
[4:0]	DEV_ADDR	These bits set the device address that the device will respond. These bits can only be written when AUTO_ADDRESS is set to 1. Otherwise, writes to these bits are ignored. The address may also be stored and loaded from EEPROM or using GPIO bits. See text for details.

### 7.6.3.6 GROUP\_ID 0x0B (11) Group ID

BIT	NAME	DESCRIPTION
[7:4]	RSVD	Reserved — always write as zero.
[3:0]	GROUP_ID	These bits set the lower 4 bits of the group identifier that the device will respond to for Group Broadcast requests. The upper 4 bits of the group identifier are fixed at 0 and cannot be changed.

### 7.6.3.7 DEV\_CTRL 0x0C (12) Device Control

BIT	NAME	DESCRIPTION
[7]	SOFT_RESET	Writing a '1' will return the device to its reset state, causing it to rerun its initialization sequence. This bit is self-clearing and will always return '0' when read.
[6]	PWRDN	Writing a '1' will cause the device to shut down. This is usually broadcast to the entire stack of ICs to shut down all of the bq76PL455A devices at the same time.
[5]	STACK_WAKE	<p>Writing a '1' will cause a wakeup tone to be sent from the high-side communication interface to the next device up the stack.</p> <p>Note that setting this bit blocks communication to devices higher in the stack until the wakeup tone sequence is complete. The time it takes to complete the stack wake sequence is dependent on the state and number of devices in the stack.</p> <p>This bit is self-clearing and will return '1' while a wakeup tone is in process, and '0' after it has completed.</p>
[4]	WRITE_EEPROM	<p>Writing a '1' while MAGIC1 is set to 0x8C2DB194 and MAGIC2 is set to 0xA375E60F causes the EEPROM to save (be programmed with) the current register values.</p> <p>This bit is self-clearing and will return '1' while the programming cycle is in progress, and '0' after the programming cycle is complete. This bit should not be written while a programming cycle is in progress.</p> <p>Normal EEPROM burns require COMM_PD_PER &gt;= 3. For COMM_PD_PER settings smaller than this, the user should have the device perform the following steps:</p> <ol style="list-style-type: none"> <li>1. Set CCNT_RST_OFF = 1</li> <li>2. Set COMM_TIM_CNT = 0x1000</li> <li>3. Burn as normal</li> </ol> <p><b>Do not write to registers while a programming cycle is in progress.</b>  <b>Do not shut down the device while a programming cycle is in progress.</b></p>
[3]	AUTO_ADDRESS	<p>If ADDR_SEL = 0, writing a '1' will cause the device to sample the GPIO pins and store the resulting value in DEV_ADDR.</p> <p>If ADDR_SEL = 1, writing a '1' will cause the device to enter auto addressing mode.</p> <p>When ADDR_SEL = 1, this bit is self-clearing and will be set to '0' after the next frame is received, even if that frame does not set DEV_ADDR.</p> <p>When ADDR_SEL = 0 this bit is self-clearing and will always read 0.</p>

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BIT	NAME	DESCRIPTION
[2:0]	RSVD	Reserved — always write as zero

**7.6.3.8 NCHAN 0x0D (13) Number of Channels**

BIT	NAME	DESCRIPTION
[7:5]	RSVD	Reserved — always write as zero.
[4:0]	NUM_CHAN	<p>This register sets the number of VSENSE channels (battery inputs) that will be used by the device. Unused channels are dropped consecutively starting from channel 16.</p> <p>The idle channel (the channel the MUX "rests" on between sample intervals) is set to this value.</p> <p>A setting of 0 is not recommended. If 0 is set, the idle channel = VSENSE1.</p> <p>This value masks cell overvoltage and undervoltage faults for unused channels and turns off the comparators associated with the channel.</p> <p>Values greater than 16 are reserved and should not be used.</p>

**7.6.3.9 DEVCONFIG 0x0E (14) Device Configuration**

BIT	NAME	DESCRIPTION
[7:6]	Reserved	These bits must always be set to 0.
[5]	REG_DISABLE	<p>0 = Internal regulator (NPN drive for VP/VDIG) is enabled. This is the normal operating mode.</p> <p>1 = Internal regulator (NPN drive) is disabled. In this case, the bq76PL455A VP, VDIG, and VIO <b>must</b> be externally supplied. REG_DISABLE = 1 is typically used only for some system diagnostic tests.</p> <p>Regardless of the state of this bit, the regulator will always be enabled while FAULT_SYS[SYS_RESET] = 1.</p>
[4]	ADDR_SEL	<p>0 = Address will be set using the GPIO inputs.</p> <p>1 = Address will be set using auto addressing.</p> <p><i>Note: Changing this bit will not change the current device address.</i></p>
[3:2]	COMP_CONFIG	<p>0 = Overvoltage (OV) and undervoltage (UV) comparators are enabled.</p> <p>1 = OV comparators are enabled, UV comparators are disabled.</p> <p>2 = Comparators are disabled.</p> <p>3 = Reserved</p>
[1]	COMP_HYST_EN	<p>0 = Comparator hysteresis is disabled.</p> <p>1 = Comparator hysteresis is enabled.</p>
[0]	UNLATCHED_FAULT	<p>0 = Faults are latched and write fault register to clear.</p> <p>1 = Faults are unlatched and clear automatically.</p> <p>This setting only applies to some fault registers. See individual fault register descriptions for details.</p> <p><i>The UNLATCHED_FAULT bit should only be changed while no fault bits are set (= 1). The latched/unlatched status of fault bits is undefined when the UNLATCHED_FAULT bit is changed while a fault bit = 1.</i></p>

**7.6.3.10 PWRCONFIG (0x0F) (15) Power Configuration**

BIT	NAME	DESCRIPTION
[7]	AFE_PCTL	<p>It is strongly recommended this bit be set to 1.</p> <p>Cell voltage sampling will be delayed by 100 <math>\mu</math>s every time sampling is requested, regardless of whether or not the AFE was already powered up. This provides time for the AFE to power up and ensures that the sampling synchronization is maintained between multiple devices.</p> <p>Changes to this register may not take effect until after the next AFE sample is taken.</p>
[6:0]	RSVD	Reserved — always write as zero.

**7.6.3.11 COMCONFIG 0x10–11 (16–17) Communications Configuration**

BIT	NAME	DESCRIPTION
[15:14]	RSVD	Reserved — always write/read as zero.

BIT	NAME	DESCRIPTION
[13:12]	BAUD	0 = 125 Kbaud 1 = 250 Kbaud 2 = 500 Kbaud 3 = 1 Mbaud This register will be reset to 250 Kbaud by a communication reset.
[11:8]	RSVD	Reserved — always write/read as zero.
[7]	UART_EN	0 = Disable single-ended transmitter and FAULT_N outputs. When disabled, TX will drive high and FAULT_N will drive low. Signals do not tri-state. 1 = Enable single-ended transmitter interface
[6]	COMM_HIGH_EN	0 = Disable high-side differential receiver interface 1 = Enable high-side differential receiver interface
[5]	DIFF_COMM_EN	0 = Disable differential low-side transmission interface 1 = Enable differential low-side transmission interface
[4]	FAULT_HIGH_EN	0 = Disable high-side fault differential receiver interface 1 = Enable high-side fault differential receiver interface
[3]	DIFF_FAULT_EN	0 = Disable differential fault output heartbeat 1 = Enable differential fault output heartbeat
[2:0]	RSVD	Reserved—Always write/read as zero.

### 7.6.3.12 TXHOLDOFF 0x12 (18) UART Transmitter Holdoff

BIT	NAME	DESCRIPTION
[7:0]	TX_HOLDOFF	This sets how many bit periods after a received stop bit the transmitter needs to wait before it starts to transmit response data.

### 7.6.3.13 CBCONFIG 0x13 (19) Balance Configuration

BIT	NAME	DESCRIPTION
[7:4]	BAL_TIME	<p>This sets the time that balancing will be enabled before it is automatically disabled. This is separate from the communication timeout counter and is not reset by communication. The counter is reset any time the BALANCE_EN register is written with a non-zero value.</p> <p>0 = Until stopped (timer disabled)  1 = 1 second  2 = 1 minute  3 = 2 minutes  4 = 5 minutes  5 = 10 minutes  6 = 15 minutes  7 = 20 minutes  8 = 30 minutes  9 = 60 minutes  10–15 = Reserved</p>
[3]	BAL_CONTINUE	<p>This controls how CBENBL[BALANCE_EN] bits are handled when faults occur.</p> <p>0 = CBENBL is set to 0 when any fault bit is set, except CUST_CKSUM_ERR, which is ignored.  1 = CBENBL is not changed if a fault occurs.</p>
[2:0]	RSVD	Reserved — always write/read as zero.

### 7.6.3.14 CBENBL 0x14–15 (20–21) Balancing Enable

BIT	NAME	DESCRIPTION
[15:0]	BALANCE_EN	<p>When EQ_SQUEEZE_EN = 0, these bits control the channels which are balancing. When EQ_SQUEEZE_EN = 1, these bits control the squeeze resistors used in open-wire-detection (OWD). BALANCE_EN[0] controls pin EQ1 for balancing cell1, bit1 controls EQ2, and so forth.</p> <p>For each bit:</p> <p>0 = Balancing (or squeeze) is disabled on this channel.  1 = Balancing (or squeeze) is enabled on this channel.</p> <p>If BAL_CONTINUE = 0, all bits in this register will be set to '0' and writes will be ignored if any fault bit (except CUST_CKSUM_ERR) is set. CUST_CKSUM_ERR is ignored.</p> <p>If BAL_CONTINUE = 1, fault bits have no effect on this register.</p>

### 7.6.3.15 TSTCONFIG 0x1E–1F (30–31) Test Configuration

BIT	NAME	DESCRIPTION
[15:12]	RSVD	Reserved — always write/read as zero.
[11:8]	LDO_TEST	These bits directly control the VDD18 LDO test. Set to 0 for normal operation. For additional information, contact a representative at Texas Instruments.
[7]	CCNT_RST_OFF	<p>When this bit is set, the communication counter does not reset when a valid communications packet is received, allowing the communications timeout counters to be tested.</p> <p>Do not change COMM_PD_PER while this bit is set:</p> <ul style="list-style-type: none"> <li>If COMM_PD_PER is inadvertently set to a value less than COMM_TIM_CNT while this bit is set, the communications timeout may be missed and not occur for up to 70 min after loss of communications.</li> <li>If COMM_PD_PER is inadvertently written while this bit is set, writing a new value to COMM_TIM_CNT (new value before the timeout should occur) will avoid the issue.</li> </ul>
[6]	VDIG_TEST	<p>This bit is used to cause the device to enter SHUTDOWN when the VDIG<sub>DDIEPOR</sub> is tripped as part of a suite of self-test functions.</p> <p>Note: Once set, subsequently clearing this bit will not disable this control even though the bit will read 0. It will not be disabled until the device enters shutdown.</p>
[5]	RSVD	Reserved — always write as zero.

BIT	NAME	DESCRIPTION
[4]	EQ_SQUEEZE_EN <sup>(1)</sup>	This bit is used to control the internal resistors connected across the VSENSE inputs, and changes the behavior of the CBENBL register. In the event of a broken wire, applying the resistor should cause any stored charge on the VSENSEn capacitor to bleed off. This bit is normally used for system testing purposes. When using this feature, CBCONFIG[BAL_CONTINUE] is typically set to '1'.
[3]	RSVD	Reserved — always write as zero
[2]	VM_MON_EN	0 = Disable VM (–5 V charge pump) monitor so the monitor ground can be measured using CMD_VMMONSEL. 1 = Enable VM monitor so it can be measured using CMD_VMMONSEL. This bit is normally used for self-testing purposes.
[1]	RSVD	Reserved — always write as zero.
[0]	MODULE_MON_EN	0 = Disable V <sub>MODULE</sub> monitor so the monitor ground can be measured using CMD_MODULESEL. 1 = Enable V <sub>MODULE</sub> monitor so it can be measured using CMD_MODULESEL. This bit is normally used for self-testing purposes.

(1) Please see Section [Window Comparator Special Considerations](#) for additional considerations for the use of this function.

### 7.6.3.16 TESTCTRL 0x20–21 (32–33) Test Control

#### CAUTION

Do NOT run more than one test simultaneously.

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero.
[7:5]	ECC_TEST	0 = Do nothing. 1 = Load USER space register correctable error to ECC_TEST_RSLT(x). 2 = Load USER space register uncorrectable error to ECC_TEST_RSLT(x). 3 = Load TI space register correctable error ECC_TEST_RSLT(x). 4 = Load TI space register uncorrectable error to ECC_TEST_RSLT(x). 5–7 = Reserved This bit is normally used for self-testing purposes.
[4]	ADC_FCAL_TEST	This test can be used to confirm the ADC is functioning properly. Test pass or fail is reported in register FAULT_DEV[ADC_CAL_ERR] (0x61[4]). 0 = Do nothing. 1 = Perform a full calibration test of the ADC. This bit is self-clearing and will return '1' while the test is running and '0' when it is complete. <i>Note: If written to '1' when ADC_PCAL_TEST is set, the device will stop the partial calibration and start a full calibration. The ADC_PCAL_TEST bit will be cleared.</i>
[3]	ADC_PCAL_TEST	This test can be used to confirm the ADC is functioning properly by running an abbreviated calibration cycle and comparing the results to those stored during TI factory testing. The original results are not overwritten. 0 = Do nothing 1 = Perform a partial calibration test of the ADC. This bit is self-clearing and will return '1' while the test is running and '0' when it is complete. <i>Note: If written to '1' when ADC_FCAL_TEST is set, the device will ignore the command and the ADC_PCAL_TEST bit will be cleared.</i>
[2]	GTSD_TRIP	This bit directly forces the thermal shutdown of the digital die to trip. Setting this bit to 1 will cause the device to reset: 0 = Normal operation 1 = Simulate over temperature (triggers thermal shutdown) This bit is normally used for self-testing purposes.
[1]	HTSD_TRIP	This bit directly forces the thermal shutdown of the analog die to trip. Setting this bit to 1 will cause the device to reset: 0 = Normal operation 1 = Simulate over temperature (triggers thermal shutdown) This bit is normally used for self-testing purposes.

BIT	NAME	DESCRIPTION
[0]	NPN_OC_TRIP	0 = Normal operation, no NPN protection check is triggered 1 = Simulate NPN protection check (triggers power-down) Setting this bit will cause the device to reset. This bit is normally used for self-testing purposes.

### 7.6.3.17 TEST\_ADC 0x22–24 (34–36) ADC Output Test

BIT	NAME	DESCRIPTION
[23]	ADC_OUTTST_EN	When this bit is set, the ADC conversion will be run, but the ADC_TEST_OUT value will be substituted for the ADC output value. This test is normally used for self-testing purposes.
[22:20]	RSVD	Reserved — always write as zero.
[19:14]	RSVD	Reserved — always read/write as zero.
[13:0]	ADC_TEST_OUT	These 14 bits in two's complement format set the false ADC output value that will be used when enabled. The default value of 0x0000 represents middle range (nominally 2.5000 V). The maximum positive value (nominally 4.9997 V) is 0x1FFF and the maximum negative value is 0x2000 (nominally 0.0000 V). It should be noted that channel trim values will still be applied to the value programmed here.

### 7.6.3.18 TESTAUXPU 0x25 (37) AUX Pull-up Test Control

BIT	NAME	DESCRIPTION
[7:0]	AUX_PULLUP_EN	These bits enable pull-ups on the AUX inputs for self-test or system configuration purposes. Bit zero corresponds to AUX0. Setting a bit (1) enables the resistor. Clearing the bit (0) disables the resistor.

### 7.6.3.19 CTO 0x28 (40) Communication Timeout

BIT	NAME	DESCRIPTION
[7:4]	COMM_PD_PER	This register sets the period at which the system will automatically power-down if no valid communication frames have been received.  0 = Communication power-down disabled 1 = 0.1 second 2 = 0.5 second 3 = 1 second 4 = 2 seconds 5 = 5 seconds 6 = 10 seconds 7 = 30 seconds 8 = 1 minute 9 = 2 minutes 10 = 5 minutes 11 = 10 minutes 12 = 30 minutes 13 = 1 hour 14–15 = Reserved  <i>Note: This setting should be greater than the COMM_TMOUTPER setting (below), if it is necessary to trigger a fault, and code has the time to address it before the device enters SHUTDOWN.</i>



BIT	NAME	DESCRIPTION
[3:0]	COMM_TMOUTPER	<p>This register sets the period after which the system will set the FAULT_SYS[COMM_TIMEOUT] fault if no valid communication frames have been received.</p> <p>0 = Communication timeout fault disabled  1 = 0.1 second  2 = 0.5 second  3 = 1 second  4 = 2 seconds  5 = 5 seconds  6 = 10 seconds  7 = 30 seconds  8 = 1 minutes  9 = 2 minutes  10 = 5 minutes  11 = 10 minutes  12 = 30 minutes  13 = 1 hour  14–15 = Reserved</p> <p><i>Note: This setting should be less than the COMM_PD_PER setting, if it is necessary to trigger a fault, and code has the time to address it before the device enters SHUTDOWN as a part of testing.</i></p>

### 7.6.3.20 CTO\_CNT 0x29–2B (41–43) Communication Timeout Counter

BIT	NAME	DESCRIPTION
[23:0]	COMM_TIM_CNT	<p>This register sets and reports the current value of the communication timeout up-counter running from a 4-kHz clock source. This is the counter used for both COMM_PD_PER and COMM_TMOUTPER. Writing these bits sets the current value of the communication timeout counter. Reads of this register are only useful when CCNT_RST_OFF is set.</p>

### 7.6.3.21 SMPL\_SLY1 0x3D (61) Initial Sampling Delay

BIT	NAME	DESCRIPTION
[7]	RSVD	Reserved — always write/read as zero.
[6:4]	INIT_VOL_DLY	<p>This value specifies the delay from changing the MUX to the first cell voltage until the channel is sampled. This delay is applied only once per sample request, even if oversampling is used.</p> <p>0 = no delay (<i>Recommended</i><sup>(1)</sup>)*  1 = 2 <math>\mu</math>s  2 = 5 <math>\mu</math>s  3 = 10 <math>\mu</math>s  4 = 20 <math>\mu</math>s  5 = 50 <math>\mu</math>s  6 = 100 <math>\mu</math>s  7 = 200 <math>\mu</math>s</p> <p>This value is useful when all the cell voltages should return values that are nearly the same, as it allows one settling delay and shorter channel-to-channel delays.</p> <p>See the <a href="#">Application and Implementation</a> section for using non-zero settings in accordance with specific design criteria requirements.</p>
[3]	RSVD	Reserved — always write/read as zero
[2:0]	INIT_AUX_DLY	<p>This value specifies the delay from changing the MUX to the first auxiliary channel until the channel is sampled. This delay is applied only once per sample request, even if oversampling is used.</p> <p>0 = no delay (<i>Recommended</i><sup>(1)</sup>)*  1 = 2 <math>\mu</math>s  2 = 5 <math>\mu</math>s  3 = 10 <math>\mu</math>s  4 = 20 <math>\mu</math>s  5 = 50 <math>\mu</math>s  6 = 100 <math>\mu</math>s  7 = 200 <math>\mu</math>s</p> <p>This value is useful when all the AUX voltages should return values that are nearly the same, as it allows one settling delay and shorter channel-to-channel delays.</p> <p>See the <a href="#">Application and Implementation</a> section for using non-zero settings in accordance with specific design criteria requirements.</p>

(1) *Recommended setting: 0x00*

### 7.6.3.22 Cell\_CSPER 0x3E (62) Cell Voltage and Internal Temperature Sampling Interval

BIT	NAME	DESCRIPTION
[7:4]	ADC_PERIOD_VOL	This value sets the ADC sampling interval that will be used for the cell voltages.
[3:0]	ADC_PERIOD_HTEMP	This value sets the ADC sampling interval that will be used for the analog die internal temperature channel. See <a href="#">Table 9</a> for settings.

**Table 9. ADC Sample Intervals, Registers 62–68**

SAMPLING <sup>(1)</sup>		NOTE
PERIOD <sup>(1)</sup> $\mu$ s	ADC_PERIOD_*	
4.13	0	Not Recommended for Analog Die Channels
5.96	1	
8.02	2	
10.0	3	
12.6	4	OK
14.9	5	OK
17.4	6	OK
19.9	7	OK
24.9	8	OK
30.0	9	OK
40.1	A	OK
60.0	B	OK
100	C	OK
200	D	OK
500	E	OK
1000	F	OK

(1) Sampling interval and averaging mode will affect device accuracy.

### 7.6.3.23 AUX\_SPER 0x3F–42 (63–66) AUX Sampling Period

BIT	NAME	DESCRIPTION
[31:28]	ADC_PERIOD_AUX0	This value sets the ADC sampling interval that will be used for the specified AUX channel. See <a href="#">Table 9</a> for settings.
[27:24]	ADC_PERIOD_AUX1	
[23:20]	ADC_PERIOD_AUX2	
[19:16]	ADC_PERIOD_AUX3	
[15:12]	ADC_PERIOD_AUX4	
[11:8]	ADC_PERIOD_AUX5	
[7:4]	ADC_PERIOD_AUX6	
[3:0]	ADC_PERIOD_AUX7	

### 7.6.3.24 TEST\_SPER 0x43–44 (67–68) Test Sampling Periods

BIT	NAME	DESCRIPTION
[15:12]	ADC_PERIOD_MOD	This value sets the ADC sampling interval that will be used for the Module monitor. See <a href="#">Table 9</a> for settings.
[11:8]	RSVD	Reserved — to maintain compatibility with default configuration, the user should program these bits to "1001" (binary).
[7:4]	ADC_PERIOD_REF	This value sets the ADC sampling interval that will be used for the 4.5-V ANALOG reference. See <a href="#">Table 9</a> for settings.
[3:0]	ADC_PERIOD_VM	This value sets the ADC sampling interval for the VM monitor to use. See <a href="#">Table 9</a> for settings.

### 7.6.3.25 SHDN\_STS 0x50 (80) Shutdown Recovery Status

The SHDN\_STS register is for design debug only. The application software must not use information in this register for system actions.

BIT	NAME	DESCRIPTION
[7]	GCL_PD_STAT	This bit is set after a control logic power down event. It indicates that shutdown was requested by the controller. This is caused by writing the DEV_CTRL[PWRDN] = 1 bit or the communication power down timeout expiring.
[6]	GTSD_PD_STAT	This bit indicates that shutdown was caused by the Digital TSD (Thermal Shut Down) or by VIO being held low long enough to cause shutdown.
[5]	V5VAO_PD_STAT	This bit is set by a falling V5VAO reaching the V5VAO POR voltage V5VAO <sub>SD</sub> . This usually indicates that voltage from the TOP pin was removed and reapplied.
[4]	ANALOG_PD_STAT	This bit is set due to the analog die requesting shutdown. See the details for bits 0:1 (below) for the specific cause. In proper operation, if this bit is set either NPN_PD_STAT bit [1] or HTSD_PD_STAT, bit [0] should also be set.
[3:2]	RSVD	Reserved — always read as zero.
[1]	NPN_PD_STAT	This bit is set any time the (VP regulator circuit) external NPN took too long to get VP into proper operating range. This bit is only valid when ANALOG_PD_STAT is set; otherwise, it should be ignored.
[0]	HTSD_PD_STAT	This bit is set when the Analog die TSD occurs. This bit is only valid when ANALOG_PD_STAT is set; otherwise, it should be ignored.

### 7.6.3.26 STATUS 0x51 (81) Device Status

BIT	NAME	DESCRIPTION
[7]	FAULT_CONDITION	Write '1': No effect Write '0': No effect Read '1': A fault bit is currently set in one or more of the fault registers. This does not include bits in this register even if they do affect the fault output.
[6]	STACK_FAULT	Write '1': No effect Write '0': No effect Read '1': A fault is currently detected on the differential fault input. The state of this bit is always included in the fault output. This fault is masked if COMCONFIG[FAULT_HIGH_EN] == 0. This fault is self-clearing when the fault condition goes away.
[5]	STACK_FAULT_DET	Write '1': Reset the bit to zero. Write '0': No effect Read '1': A fault was detected on the differential fault input. This is a latched version of STACK_FAULT and indicates that some stack fault has been seen since the last time this bit was reset. The state of this bit does not affect the fault output. It is provided for informational purposes and for debugging transient faults. This fault is masked if COMCONFIG[FAULT_HIGH_EN] == 0.
[4]	COMM_CLEAR	Write '1': Reset the bit to zero. Write '0': No effect Read '1': A communication clear has been detected. The state of this bit does not affect the fault output.
[3]	COMM_RESET	Write '1': Reset the bit to zero. Write '0': No effect Read '1': A communication reset has been detected. The state of this bit does not affect the fault output.

BIT	NAME	DESCRIPTION
[1]	NEW_DATA	<p>This read-only bit indicates ADC conversion data are available when set. Writing to the bit has no effect.</p> <p>The bit is reset by reading <i>any</i> conversion result (sample) data.</p> <p>This can be used to tell if some new data have been collected since the last COMMAND to report sample data. This only indicates if some sample has been collected since the last report. It does not track what channel was reported or collected. This bit will not be set by the automatic internal temperature sampling or initialization sampling.</p>
[0]	SYS_INIT	<p>Write '1': Stop waiting for VM and continue with initialization. Write '0': No effect Read '0': System initialization is complete. Read '1': System initialization is in progress.</p> <p>This can be useful to speed up the wakeup sequence. Device accuracy may be impaired and is not specified until VM is in the correct range.</p> <p>This is useful when waking the device quickly for self-testing purposes or performing tests that will cause shutdown or reset. Setting this bit allows code to perform other functions while waiting for VM to ramp up.</p>

### 7.6.3.27 FAULT\_SUM 0x52–53 (82–83) Fault Summary

BIT	NAME	DESCRIPTION
[15]	UV_FAULT_SUM	<p>For each of these bits: Write '1': Reset all fault conditions of this type. Write '0': No effect Read '1': One or more of the individual fault bits of this type are currently set. These bits always reflect the state of the underlying bits in the other fault registers, which may be latched or not, depending on the setting of the DEVCONFIG[UNLATCHED_FAULT] bit.</p>
[14]	OV_FAULT_SUM	
[13]	AUXUV_FAULT_SUM	
[12]	AUXOV_FAULT_SUM	
[11]	CMPUV_FAULT_SUM	
[10]	CMPOV_FAULT_SUM	
[9]	COMM_FAULT_SUM	
[8]	SYS_FAULT_SUM	
[7]	CHIP_FAULT_SUM	
[6]	GPI_FAULT_SUM	
[5:0]	RSVD	Reserved — always read as zero.

### 7.6.3.28 FAULT\_UV 0x54–55 (84–85) Cell Undervoltage Fault

BIT	NAME	DESCRIPTION
[15:0]	UV_FAULT	<p>For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': The stored result for the corresponding battery channel is less than UV_THRES_CELL. UV_FAULT[0] corresponds to cell 1. If UNLATCHED_FAULT is set, this register is self-clearing.</p>

### 7.6.3.29 FAULT\_OV 0x56–57 (86–87) Cell Overvoltage Fault

BIT	NAME	DESCRIPTION
[15:0]	OV_FAULT	<p>For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': The stored result for the corresponding battery channel is greater than OV_THRES_CELL. OV_FAULT[0] corresponds to cell 1. If UNLATCHED_FAULT is set, this register is self-clearing.</p>

### 7.6.3.30 FAULT\_AUX 0x58–59 (88–89) Auxiliary Under/Over-Threshold Fault

BIT	NAME	DESCRIPTION
[15:8]	AUX_UV_FAULT	For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': The stored result for the corresponding auxiliary channel is less than UV_THRES_AUX*. AUX_UV_FAULT[0] corresponds to AUX0. If UNLATCHED_FAULT is set, this register is self-clearing.
[7:0]	AUX_OV_FAULT	For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': The stored result for the corresponding auxiliary channel is greater than OV_THRES_AUX*. AUX_OV_FAULT[0] corresponds to AUX0. If UNLATCHED_FAULT is set, this register is self-clearing.

### 7.6.3.31 FAULT\_2UV 0x5A–5B (90–91) Comparator Undervoltage Fault

BIT	NAME	DESCRIPTION
[15:0]	CMPUV_FAULT	For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': Corresponding battery cell comparator has detected an undervoltage condition. CMPUV_FAULT[0] corresponds to cell 1.  When UNLATCHED_FAULT is set, these comparator faults only automatically clear if no other Analog die based fault exists. This is true even for faults that are masked.  Analog die faults include FAULT_SYS[0:3] or any bit in registers FAULT_2UV or FAULT_2OV.

### 7.6.3.32 FAULT\_2OV 0x5C–5D (92–93) Comparator Overvoltage Fault

BIT	NAME	DESCRIPTION
[15:0]	CMPOV_FAULT	For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': Corresponding battery cell comparator has detected an overvoltage condition. CMPOV_FAULT[0] corresponds to cell 1.  When UNLATCHED_FAULT is set, these comparator faults only automatically clear if no other Analog die based fault exists. This is true even for faults that are masked.  Analog die faults include FAULT_SYS[0:3] or any bit in registers FAULT_2UV or FAULT_2OV.

### 7.6.3.33 FAULT\_COM 0x5E–5F (94–95) Communications Fault

BIT	NAME	DESCRIPTION
[15]	COMP_ERR_H	Write '1': Reset the fault condition. Write '0': No effect Read '1': A bit on the high-side interface failed to compare with its complement. This is notification only; the frame is processed by the communications interface logic.
[14]	COMP_ERR_L	Write '1': Reset the fault condition. Write '0': No effect Read '1': A bit on the low-side interface failed to compare with its complement. This is notification only; the frame is processed by the communications interface logic.
[13]	COMP_FLT_H	Write '1': Reset the fault condition. Write '0': No effect Read '1': A frame on the high-side interface (COMMH) was stopped due to two or more complement errors (COMP_ERR_H).
[12]	COMP_FLT_L	Write '1': Reset the fault condition. Write '0': No effect Read '1': A frame on the low-side interface (COMML) was stopped due to two or more complement errors (COMP_ERR_L).

BIT	NAME	DESCRIPTION
[11]	EDGE_ERR_H	Write '1': Reset the fault condition. Write '0': No effect Read '1': A falling edge was not detected on the high-side interface by the 4 <sup>th</sup> bit.
[10]	EDGE_ERR_L	Write '1': Reset the fault condition. Write '0': No effect Read '1': A falling edge was not detected on the low-side interface by the 4 <sup>th</sup> bit.
[9]	ABORT_H	Write '1': Reset the fault condition. Write '0': No effect Read '1': A framing bit with value "1" was detected on the high-side differential interface.  A data byte was stopped and ignored. If this occurs on the high-side interface, it is always due to a communication problem. Sending COMM_RESET or COMM_CLEAR to the UART interface on the bottom chip will cause this fault on the low-side interface.  When it occurs on the high side, it may have caused this chip to fail to return its frame in a broadcast or group response (although the microcontroller should already have detected this before this bit was read).
[8]	ABORT_L <sup>(1)</sup>	Write '1': Reset the fault condition. Write '0': No effect Read '1': A framing bit with value "1" was detected on the low-side differential interface.  A data byte was stopped and ignored. ABORT_L also reads "1" on devices in a stack when a COMM_RESET or COMM_CLEAR is sent to the UART interface on the base device of a stack.
[7]	CRC_FAULT_H	Write '1': Reset the fault condition. Write '0': No effect Read '1': A CRC fault has been detected on the high-side interface. The frame was discarded. If it occurs on the high side, it may have caused this chip to fail to return its frame in a broadcast or group response.
[6]	CRC_FAULT_L	Write '1': Reset the fault condition. Write '0': No effect Read '1': A CRC fault has been detected on the low-side interface (either single-ended UART or differential VBUS). The frame was discarded.
[5]	FRAME_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': A framing error has been detected. This indicates that the chip received a start of frame on the differential communications interface before it had completed the prior frame.
[4]	RSVD	Reserved — always read as zero
[3]	STOP_ERR <sup>(1)</sup>	Write '1': Reset the fault condition. Write '0': No effect Read '1': The UART receiver detected an invalid stop bit on the single-ended low-side interface.  This error only appears on chips using the UART interface. COMM_CLEAR and COMM_RESET will also cause this fault.  This error is specific to the UART interface.
[2:1]	RSVD	Reserved — always read as zero
[0]	STK_FAULT_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': Stack fault input (FAULTH±) is too noisy or is running at the wrong frequency.  <i>Note: The STK_FAULT_ERR flag may not be clearable under some conditions. If a STK_FAULT_ERR is detected, and then no more edges appear on the high-side fault pins (as would be the case if the chip above had a fault condition), it may be impossible to clear the STK_FAULT_ERR flag. Once proper signaling resumes on the high-side fault pin, it will again be possible to clear this fault.</i>  <i>Masked STK_FAULT_ERR is not cleared during initialization. As a result, there is a approximately 5-μs window at startup where, if the high-side fault receiver detects more than four falling edges, the STK_FAULT_ERR will be set even though it is masked.</i>

- (1) COMM\_CLEAR causes STOP\_ERR and COMM\_CLEAR on base device and ABORT\_L on the chips higher in the stack. COMP\_ERR\_L, COMP\_FLT\_L, and EDGE\_ERR\_L faults do not occur on the base device in a stack configuration. See [Protocol Description](#) section for more details.

### 7.6.3.34 FAULT\_SYS 0x60 (96) System Fault

BIT	NAME	DESCRIPTION
[7]	SYS_RESET	Write '1': Reset the bit to zero. Write '0': No effect Read '1': A system reset has been detected.
[6]	COMM_TIMEOUT	Write '1': Reset the fault condition. Write '0': No effect Read '1': Communications timeout has been detected.
[5]	VDIG_WAKE_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': VDIG supply was already high on wakeup. This could happen if the NPN transistor were leaking and preventing VDIG from going away when VP/VDIG shuts down. It could also occur if the chip is reset (in which case the VDIG supply remained on) or if it was shut down too briefly to allow the supply time to ramp down. This bit is provided to allow detection of leakage current into the supply during shutdown.  This bit is checked only set by the device during the device initialization sequence. Once cleared, it will not set again until the block is reset.
[4]	INT_TEMP_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': Overtemperature condition in the digital die If UNLATCHED_FAULT is set, this bit is self-clearing.
[3]	VDIG_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': VDIG supply failure detected in the analog die.
[2]	VM_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': VM supply failure detected in analog die.
[1]	VP_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': VP supply failure detected in analog die.
[0]	VP_CLAMP	Write '1': Reset the fault condition. Write '0': No effect Read '1': NPNB pin is monitored and clamped to keep the NPNB pin from going over voltage.

### 7.6.3.35 FAULT\_DEV 0x61–62 (97–98) Chip Fault

BIT	NAME	DESCRIPTION
[15]	USER_CKSUM_ERR	Write '1': No effect Write '0': No effect Read '1': A checksum error was detected in the registers. This fault is self-clearing when the condition goes away.
[14]	FACT_CKSUM_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': A checksum error was detected in the factory registers.
[13]	ANALOG_FAULT_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': The analog die is reporting an error, but it cannot tell what the error is (no error condition has been detected). This may be caused by a single event upset, or possibly the device has failed. If this occurs consistently, the device should be removed from service.
[12]	HREF_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': Analog die 4.5-V reference measurement was out of range.



BIT	NAME	DESCRIPTION
[11]	HREF_GND_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': Analog-die reference ground measurement was out of range.
[10:5]	RSVD	Reserved — always read as zero
[4]	ADC_CAL_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': An ADC test (ADC_FCAL_TEST or ADC_PCAL_TEST) failed.
[3]	USER_ECC_COR	Write '1': Reset the fault condition. Write '0': No effect Read '1': A ECC fault was corrected while loading user space from EEPROM.
[2]	USER_ECC_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': An uncorrectable ECC fault was detected while loading from EEPROM. Registers in the block (not all registers) have been loaded with their default values.
[1]	FACT_ECC_COR	Write '1': Reset the fault condition. Write '0': No effect Read '1': A ECC fault was corrected while loading factory space from EEPROM.
[0]	FACT_ECC_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': An uncorrectable ECC fault was detected while loading from factory registers. Registers in the block (not all registers) have been loaded with their default values. The device is operating abnormally and has probably failed. Functionality, behavior, and results are suspect and should not be relied upon.

### 7.6.3.36 FAULT\_GPI 0x63 (99) GPI Fault

BIT	NAME	DESCRIPTION
[7:6]	RSVD	Reserved — always read as zero.
[5:0]	GPI_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': A GPIO input, configured as a fault input in GPI_FAULT_CONFIG, has signaled a fault condition. If UNLATCHED_FAULT is set, this register is self-clearing.

### 7.6.3.37 MASK\_COMM 0x68–69 (104–105) Communications Fault Masks

BIT	NAME	DESCRIPTION
[15]	COMP_ERR_H_MSK	For each of these bits: 0 = Do not mask this fault. 1 = Mask this fault.
[14]	COMP_ERR_L_MSK	
[13]	COMP_FLT_H_MSK	
[12]	COMP_FLT_L_MSK	
[11]	EDGE_ERR_H_MSK	
[10]	EDGE_ERR_L_MSK	
[9]	ABORT_H_MSK	
[8]	ABORT_L_MSK	
[7]	CRC_FAULT_H_MSK	
[6]	CRC_FAULT_L_MSK	
[5]	FRAM_ERR_MSK	
[4]	RSVD	Reserved — always write/read as zero
[3]	STOP_ERR_MSK	0 = Do not mask this fault. 1 = Mask this fault.

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BIT	NAME	DESCRIPTION
[2:1]	RSVD	Reserved — always write/read as zero
[0]	STK_FAULT_ERR_MSK	0 = Do not mask this fault. 1 = Mask this fault. <i>Masked STK_FAULT_ERR is not cleared during initialization. As a result, there is an approximately 5-μs window at startup where, if the high-side fault receiver detects more than four falling edges, STK_FAULT_ERR will be set even though it is masked.</i>

**7.6.3.38 MASK\_SYS 0x6A (106) System Fault Masks**

BIT	NAME	DESCRIPTION
[7]	SYS_RESET_MSK <sup>(1)</sup>	For each of these bits: 0 = Do not mask this fault. 1 = Mask this fault.
[6]	COMM_TIMEOUTMSK	
[5]	RSVD	Reserved — always write/read as zero
[4]	INT_TEMP_FAULT_MSK	For each of these bits: 0 = Do not mask this fault. 1 = Mask this fault.
[3]	VDIG_FAULT_MSK	
[2]	VM_FAULT_MSK	
[1]	VP_FAULT_MSK	
[0]	VP_CLAMP_MSK	

(1) If the SYS\_RESET\_MSK is set to 1, this setting should be burned to EEPROM in order to provide useful information.

**7.6.3.39 MASK\_DEV 0x6B–6C (107–108) Chip Fault Masks**

BIT	NAME	DESCRIPTION
[15]	USER_CKSUM_MSK	For each of these bits: 0 = Do not mask this fault. 1 = Mask this fault.
[14]	FACT_CKSUM_MSK	
[13]	ANALOG_FERR_MSK	
[12:0]	RSVD	Reserved — always write/read as zero

**7.6.3.40 FO\_CTRL 0x6E–6F (110–111) Fault Output Control**

BIT	NAME	DESCRIPTION
[15]	UV_FAULT_OUT	For each of these bits: 0 = Do not include these faults in the fault output. 1 = Include these faults in the fault output.
[14]	OV_FAULT_OUT	
[13]	AUXUV_FAULT_OUT	
[12]	AUXOV_FAULT_OUT	
[11]	CMPUV_FAULT_OUT	
[10]	CMPOV_FAULT_OUT	
[9]	COMM_FAULT_OUT	
[8]	SYS_FAULT_OUT	
[7]	CHIP_FAULT_OUT	
[6]	GPI_FAULT_OUT	
[5:0]	RSVD	Reserved — always write/read as zero

### 7.6.3.41 GPIO\_DIR 0x78 (120) General Purpose IO Direction

BIT	NAME	DESCRIPTION
[7:6]	RSVD	Reserved — always write/read as zero
[5:0]	GPO_EN	This bitmask enables the GPIO pins to behave as GPI or GPO: 0: Input 1: Output GPO_EN[0] corresponds to GPIO0.

### 7.6.3.42 GPIO\_OUT 0x79 (121) General Purpose Output

BIT	NAME	DESCRIPTION
[7:6]	RSVD	Reserved — always write/read as zero
[5:0]	GPO	This bitmask sets the output state for each GPIO pin when the corresponding bit of GPO_EN = 1. GPO[0] corresponds to GPIO0. 0: the GPIO output is 0. 1: the GPIO output is 1.

### 7.6.3.43 GPIO\_PU 0x7A (122) General Purpose Pull-Up

BIT	NAME	DESCRIPTION
[7:6]	RSVD	Reserved — always write/read as zero
[5:0]	GPO_PU	Setting any bit to 1 turns the respective GPIO pull-up on. <b>Note: Care should be taken not to turn on a bit at same time as the corresponding GPO_PD bit in register GPIO_PD.</b>

### 7.6.3.44 GPIO\_PD 0x7B (123) General Purpose Pull-Down

BIT	NAME	DESCRIPTION
[7:6]	RSVD	Reserved — always write/read as zero
[5:0]	GPO_PD	Setting any bit to 1 turns the respective GPIO pull-down on. <b>Note: Care should be taken not to turn on a bit at same time as the corresponding GPO_PU bit in register GPIO_PU.</b>

### 7.6.3.45 GPIO\_IN 0x7C (124) General Purpose Input

[7:6]	RSVD	Reserved — always read as zero
[5:0]	GPI	Reports the current value of the GPIO pin. GPI[0] corresponds to GPIO0.

### 7.6.3.46 GP\_FLT\_IN 0x7D (125) General Purpose Fault Input

BIT	NAME	DESCRIPTION
[7]	RSVD	Reserved — always read as zero
[6]	GPI_FAULT_SENSE	0 = GPIO fault inputs will create a fault if low. 1 = GPIO fault inputs will create a fault if high.
[5:0]	GPI_FAULT_CONFIG	This bitmask sets which of the GPIO pins are treated as fault inputs. Note that this setting does not prevent the I/O pin from being driven by the device. This feature may be used as a part of self-test.

### 7.6.3.47 MAGIC1 0x82–85 (130–133) Magic1

BIT	NAME	DESCRIPTION
[31:0]	MAGIC1	Magic value to enable EEPROM programming. This value must be written in a single frame. Reads always return zero.

**7.6.3.48 COMP\_UV 0x8C (140) Comparator Undervoltage Threshold**

BIT	NAME	DESCRIPTION
[7:1]	CMP_UV_THRES	These bits set the comparator undervoltage-threshold value in 25-mV steps. The range is determined by the CMP_TST_SHF_UV bit.
[0]	CMP_TST_SHF_UV	This bit sets the operating range for the undervoltage comparators. 0 = Normal range of 0.7 V to 3.875 V 1 = Shifted range of 2.0 V to 5.175 V (used for self-test purposes)

**7.6.3.49 COMP\_OV 0x8D (141) Comparator Overvoltage Threshold**

BIT	NAME	DESCRIPTION
[7:1]	CMP_OV_THRES	These bits set the comparator overvoltage-threshold value in 25-mV steps. The range is determined by the CMP_TST_SHF_OV bit.
[0]	CMP_TST_SHF_OV	This bit sets the operating range for the undervoltage comparators. 0 = Normal range of 2.0 V to 5.175 V 1 = Shifted range of 0.7 V to 3.875 V (used for self-test purposes).

**7.6.3.50 CELL\_UV 0x8E–8F (142–143) Cell Undervoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_CELL	This register sets the upper 14 bits of the 16-bit undervoltage threshold value that will be used for all of the ADC cell voltage measurements. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.51 CELL\_OV 0x90–91 (144–145) Cell Overvoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_CELL	This register sets the overvoltage threshold value that will be used for all of the ADC cell voltage measurements. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.52 AUX0\_UV 0x92–93 (146–147) AUX0 Undervoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX0	This register contains the undervoltage threshold that will be used for the AUX0 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.53 AUX0\_OV 0x94–95 (148–149) AUX0 Overvoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX0	This register contains the overvoltage threshold that will be used for the AUX0 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.54 AUX1\_UV 0x96–97 (150–151) AUX1 Undervoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX1	This register contains the undervoltage threshold that will be used for the AUX1 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.55 AUX1\_OV 0x98–99 (152–153) AUX1 Overvoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX1	This register contains the overvoltage threshold that will be used for the AUX1 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.56 AUX2\_UV 0x9A–9B (154–155) AUX2 Undervoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX2	This register contains the undervoltage threshold that will be used for the AUX2 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.57 AUX2\_OV 0x9C–9D (156–157) AUX2 Overvoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX2	This register contains the overvoltage threshold that will be used for the AUX2 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.58 AUX3\_UV 0x9E–9F (158–159) AUX3 Undervoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX3	This register contains the undervoltage threshold that will be used for the AUX3 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.59 AUX3\_OV 0xA0–A1 (160–161) AUX3 Overvoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX3	This register contains the overvoltage threshold that will be used for the AUX3 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.60 AUX4\_UV 0xA2–A3 (162–163) AUX4 Undervoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX4	This register contains the undervoltage threshold that will be used for the AUX4 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.61 AUX4\_OV 0xA4–A5 (164–165) AUX4 Overvoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX4	This register contains the overvoltage threshold that will be used for the AUX4 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.62 AUX5\_UV 0xA6–A7 (166–167) AUX5 Undervoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX5	This register contains the undervoltage threshold that will be used for the AUX5 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.63 AUX5\_OV 0xA8–A9 (168–169) AUX5 Overvoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX5	This register contains the overvoltage threshold that will be used for the AUX5 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.64 AUX6\_UV 0xAA–AB (170–171) AUX6 Undervoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX6	This register contains the undervoltage threshold that will be used for the AUX6 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.65 AUX6\_OV 0xAC–AD (172–173) AUX6 Overvoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX6	This register contains the overvoltage threshold that will be used for the AUX6 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.66 AUX7\_UV 0xAE–AFB (174–175) AUX7 Undervoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX7	This register contains the undervoltage threshold that will be used for the AUX7 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.67 AUX7\_OV 0xB0–B1 (176–177) AUX7 Overvoltage Threshold**

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX7	This register contains the overvoltage threshold that will be used for the AUX7 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

**7.6.3.68 LOT\_NUM 0xBE–C5 (190–197) Device Lot Number**

BIT	NAME	DESCRIPTION
[63:0]	LOT_NUM(x)	Device lot number

**7.6.3.69 SER\_NUM 0xC6–C7 (198–199) Device Serial Number**

BIT	NAME	DESCRIPTION
[15:0]	SERIAL_NUM	Device serial number

**7.6.3.70 SCRATCH 0xC8–CF (200–207) Scratch Registers**

BIT	NAME	DESCRIPTION
[63:0]	SCRATCH(x)	This register contains user-defined data (for example, post-assembly calibration coefficients) that can be written and read by the host microcontroller.

### 7.6.3.71 VSOFFSET 0xD2 (210) Cell Offset Correction

BIT	NAME	DESCRIPTION
[7:0]	CCOFFSET	User offset-adjustment register for VSENSE cell voltage channels. This 2's complement value will be added to all cell voltage channels. The range is approximately –9.77 mV to 9.69 mV in 255 steps. The offset is approximately equal to $(5\text{ V} \times \text{CCOFFSET} / 2^{16})$ . It can be used to compensate for offsets induced by the user design or PCB mounting.

### 7.6.3.72 VSGAIN 0xD3 (211) Cell Gain Correction

BIT	NAME	DESCRIPTION
[7:0]	CCGAIN	User gain-adjustment register for VSENSE cell voltage channels. This is a 2's complement value where positive values represent a gain > 1.0 and negative values represent a gain < 1.0, and is applied to all cell voltage channels.  The range is approximately –9.77 mV to 9.69 mV full scale in 255 steps. The gain correction is approximately equal to $(\text{input value} \times (1 + \text{CCGAIN} / 2^{16}))$ . It can be used to compensate for gain error induced by the user design (such as larger values of input resistor) or PCB mounting.

### 7.6.3.73 AX0OFFSET 0xD4–D5 (212–213) AUX0 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET0	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to $(5\text{ V} \times \text{AUXCOFFSET0} / 2^{16})$ . See Section <a href="#">AUX Channel Post-Assembly Calibration Adjustment</a> for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

### 7.6.3.74 AX1OFFSET 0xD6–D7 (214–215) AUX1 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET1	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to $(5\text{ V} \times \text{AUXCOFFSET1} / 2^{16})$ . See Section <a href="#">AUX Channel Post-Assembly Calibration Adjustment</a> for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

### 7.6.3.75 AX2OFFSET 0xD8–D9 (216–217) AUX2 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET2	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to $(5\text{ V} \times \text{AUXCOFFSET2} / 2^{16})$ . See Section <a href="#">AUX Channel Post-Assembly Calibration Adjustment</a> for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

### 7.6.3.76 AX3OFFSET 0xDA–DB (218–219) AUX3 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET3	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to $(5\text{ V} \times \text{AUXCOFFSET3} / 2^{16})$ . See Section <a href="#">AUX Channel Post-Assembly Calibration Adjustment</a> for details. It can be used to compensate for offsets induced by the user design or PCB mounting.



**7.6.3.77 AX4OFFSET 0xDC–DD (220–221) AUX4 Offset Correction**

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET4	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to $(5\text{ V} \times \text{AUXCOFFSET4} / 2^{16})$ . See Section <a href="#">AUX Channel Post-Assembly Calibration Adjustment</a> for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

**7.6.3.78 AX5OFFSET 0xDE–DF (222–223) AUX5 Offset Correction**

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET5	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to $(5\text{ V} \times \text{AUXCOFFSET5} / 2^{16})$ . See text for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

**7.6.3.79 AX6OFFSET 0xE0–E1 (224–225) AUX6 Offset Correction**

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET6	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to $(5\text{ V} \times \text{AUXCOFFSET6} / 2^{16})$ . See text for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

**7.6.3.80 AX7OFFSET 0xE2–E3 (226–227) AUX7 Offset Correction**

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET7	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to $(5\text{ V} \times \text{AUXCOFFSET7} / 2^{16})$ . See text for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

**7.6.3.81 TSTR\_ECC 0xE6–ED (230–237) ECC Test Result[1:0]**

BIT	NAME	DESCRIPTION
[31:0]	ECC_TEST_RSLT(x)	These values display the test result from running an ECC test using the TEST_CTRL[ECC_TEST] bits. Expected output for Correctable User ECC Test 0x18C3 FF8A 68A9 8069. Expected output for Correctable Factory ECC Test 0xCC72 D182 80BA 9767. Expected output for non-correctable User and Factory ECC tests is 0x0000 0000 0000 0000.

**7.6.3.82 CSUM 0xF0–F3 (240–243) Checksum**

BIT	NAME	DESCRIPTION
[31:0]	USER_CKSUM	This register contains the programmed checksum for the registers. See Table 7, column "CS" for included registers. The FAULT_DEV[USER_CKSUM_ERR] flag will be set when this value does not match the internally calculated value shown in <a href="#">CSUM_RSLT 0xF4–F7(244–247) Checksum Readout</a> .

**7.6.3.83 CSUM\_RSLT 0xF4–F7(244–247) Checksum Readout**

BIT	NAME	DESCRIPTION
[31:0]	USER_CKSUM_RD	This register contains the current internally calculated checksum for the registers.



### 7.6.3.84 TEST\_CSUM 0xF8–F9 (248–249) Checksum Test Result

BIT	NAME	DESCRIPTION
[15:0]	CKSUM_TEST	This register contains the most recent test result, from either a User or TI space checksum test. TESTCTRL[CKSUM_TEST_RUN] triggers the test for which the results will appear in the CKSUM_TEST register. Expected results are provided in the CKSUM_TEST_RUN bit description.

### 7.6.3.85 EE\_BURN 0xFA (250) EEPROM Burn Count

BIT	NAME	DESCRIPTION
[7:0]	EE_BURN_CNT	This register contains the EEPROM burn count. It is incremented every time the EEPROM is programmed.

### 7.6.3.86 MAGIC2 0xFC–FF (252–255) Magic2

BIT	NAME	DESCRIPTION
[31:0]	MAGIC2	Magic value to enable EEPROM programming. This value must be written in a single frame. Reads always return zero.

## 8 Application and Implementation

### NOTE

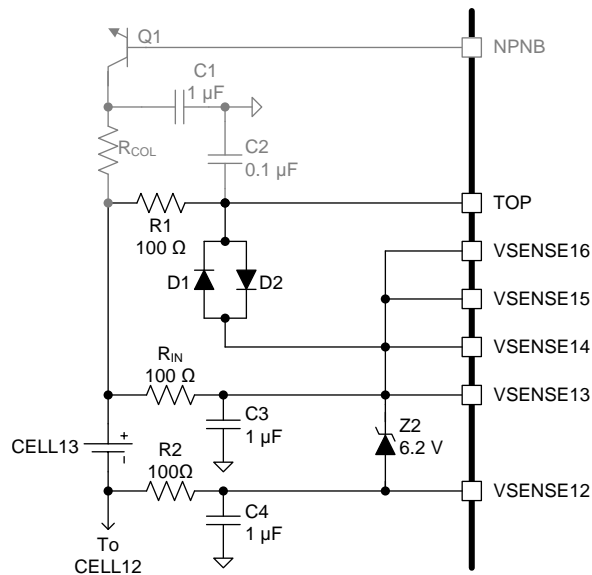
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Special Pin Considerations

##### 8.1.1.1 Unused VSENSE Inputs (Designs with Less Than 16 Cells)

VSENSE inputs start with VSENSE0 and continue to VSENSE16. Inputs must be used in ascending order, with all unused inputs connected together with the input to the highest used VSENSE\_ input. For example, in a 13-cell design, inputs VSENSE14, VSENSE15, and VSENSE16 are not used. These VSENSE inputs must be connected together with VSENSE13 for proper operation. The highest used VSENSE, which is connected to a cell through the resistor of the input low-pass filter. As an example, VSENSE13 is connected to cell 13 through a 100-Ω resistor; pins VSENSE14, VSENSE15, and VSENSE16 are then connected to pin VSENSE13. A 100-Ω resistor is used here as an example only, all inputs should use the same resistor as chosen by the designer to meet filter requirements for their circuit implementation. Figure 25 illustrates the proper connection for unused VSENSE inputs.



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**Figure 25. Example Connection for Less than 16 Cells (Some Components Omitted for Clarity)**

##### 8.1.1.2 Unused AUX Inputs

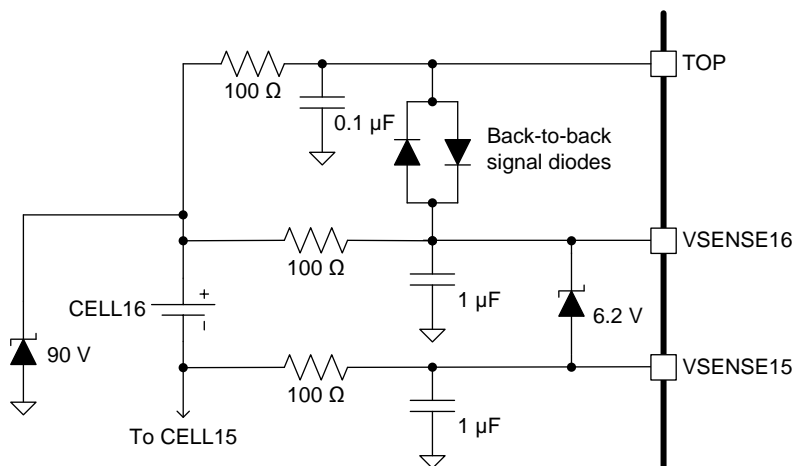
Unused AUX inputs can be allowed to float, be tied to VSS, or pulled up to VP/VDIG through a nominal 10-kΩ to 1-MΩ resistor. To pull up the AUX input to VP, enable the TESTAUXPU register, which uses an internally supplied resistor.

## Application Information (continued)

### 8.1.1.3 TOP and VSENSE16 Pins

To ensure that the voltage between TOP and VSENSE16 does not violate the [Absolute Maximum Ratings](#) and [Recommended Operating Conditions](#) during hot-plug or other unusual conditions, connect the VSENSE16 input (and any unused SENSE inputs) to the TOP pin using two back-to-back signal diodes. Select diodes with a high enough current rating to withstand the continuous currents during a wire disconnect and the inrush currents during hot plug. Use diodes that have a higher  $V_f$ , such as an ultra-fast or fast diode. Low  $V_f$  diodes, such as Schottkey diodes, must not be used because noise on the TOP pin may couple onto the VSENSE16 pin (or highest-sense line used).

The TOP input must also include a low-pass filter using a 0.1- $\mu$ F capacitor and a 100- $\Omega$  to 300- $\Omega$  resistor to avoid voltage stress during cell connection (hot-plug). [Figure 26](#) illustrates the correct VSENSE-TOP connection. Additionally, connect a transient suppression diode (TVS) to TOP to clamp the voltage to below 88 V and prevent an overvoltage condition on TOP during hot-plug and other transient events.



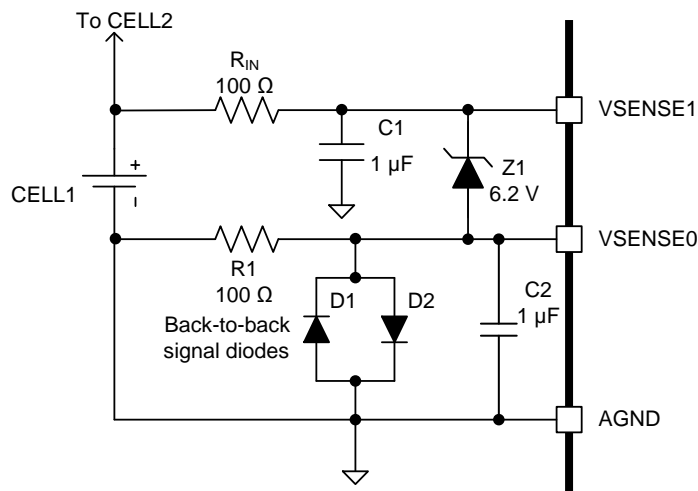
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**Figure 26. Connecting the TOP and VSENSE16 Pins**

### 8.1.1.4 AGND1 and VSENSE0 Pins

To ensure that the voltage between VSENSE0 and AGND1 does not violate the [Absolute Maximum Ratings](#) and [Recommended Operating Conditions](#) during hot-plug or other unusual conditions, connect the VSENSE0 input to the AGND1 pin using two back-to-back signal diodes. Select diodes with high enough current rating to withstand the continuous currents during a wire disconnect and the inrush currents during hot plug. Use diodes that have a higher  $V_f$ , such as an ultra-fast or fast diode. Low  $V_f$  diodes, such as Schottkey diodes, must not be used because noise on AGND may couple onto the VSENSE0 input. Additionally, connect a 1- $\mu$ F capacitor between VSENSE0 and AGND1. [Figure 27](#) illustrates the correct VSENSE0-to-AGND1 connection.

## Application Information (continued)

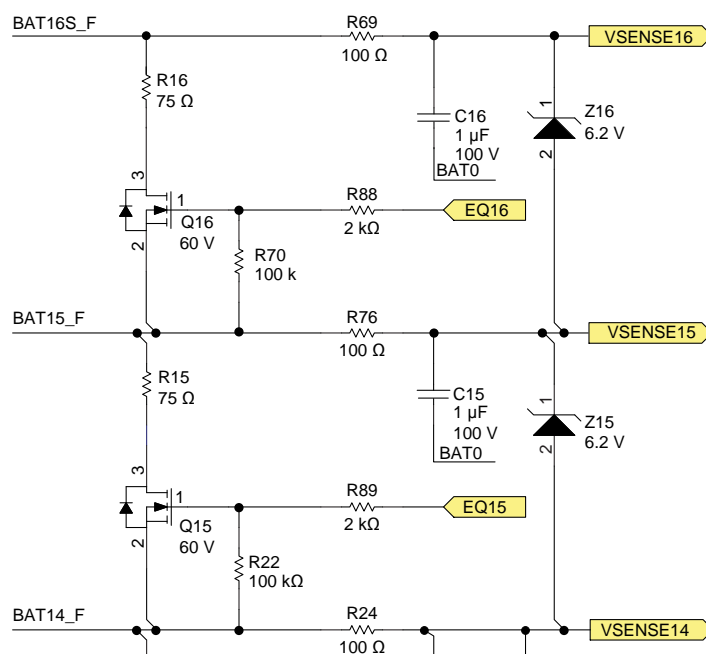


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**Figure 27. Connecting the AGND1 and VSENSE0 Pins**

### 8.1.1.5 VSENSE to VSENSE Connections

To ensure that the voltage between the VSENSE\_ inputs (VSENSE0 to VSENSE1, VSENSE1 to VSENSE2, and so forth) does not violate the [Absolute Maximum Ratings](#) and [Recommended Operating Conditions](#) during hot-plug or other unusual conditions, zener diodes must be connected between the VSENSE input pins, as close as possible to the inputs. One zener across every input is advised. The zener diodes provide overvoltage protection and a path for inrush current during a hotplug event. [Figure 28](#) illustrates the correct VSENSE-to-VSENSE connection.



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BAT0S is the sense point to the negative terminal of CELL1. BAT0 is the power plane for the negative terminal of the cell stack.

**Figure 28. Cell Voltage Sense Circuit**

## Application Information (continued)

Select zener diodes that meet the following conditions:

1. The bq76PL455 inputs are protected from input voltage transients greater than 5.5 V. Any transients greater than 5.5 V must be clamped to less than 6.5 V for an accumulative time duration not to exceed 0.1% of the device 10-year lifetime.
2. The zener maximum reverse current ( $I_Z$ ) at normal battery-cell voltage levels are as low as possible to keep the quiescent system-current draw low. Additionally, any leakage through the zener diode affects the total channel accuracy measurements as it adds to the voltage drop across the filter resistor.
3. The zener must be capable of withstanding instantaneous or continuous currents that the bq76PL455A experiences during fault events. These events can include cable connect/disconnect, inrush, or reverse battery voltage. Depending on the fault and the direction of current flow, the maximum power dissipation for the zener diode must not be exceeded to stay within maximum operating conditions.

Additionally, a series resistor and bypass capacitor are required for each of the VSENSE inputs. The series resistor (R132 and R138 in [Figure 28](#)) serves two functions:

1. They protect the AFE inputs from in-rush currents during hot plug-in. This requirement limits the input series R to a minimum of 100  $\Omega$ . Keep this resistance as low as possible to minimize input voltage offset, which is also subject to drift over temperature. These requirements limit the maximum value to 1 k $\Omega$ . Error due to input bias currents, on the front end of the AFE, is directly proportional to the value of the resistors. The voltage measurement error can be calculated as:

$$\text{voltage measurement error} = 2 \times R \times I_{\text{SENSE}} \quad (10)$$

2. The resistor and capacitor (R132 and C61 in [Figure 28](#)) provide an RC filter for high-frequency noise on the AFE inputs. The tuning of this filter cutoff is adjustable and depends on the expected frequency of noise in the system. Select a minimum 0.1- $\mu$ F capacitor connected from the VSENSE input to the battery pack GND (BAT0 in [Figure 28](#)). Calculate the cutoff frequency using [Equation 11](#):

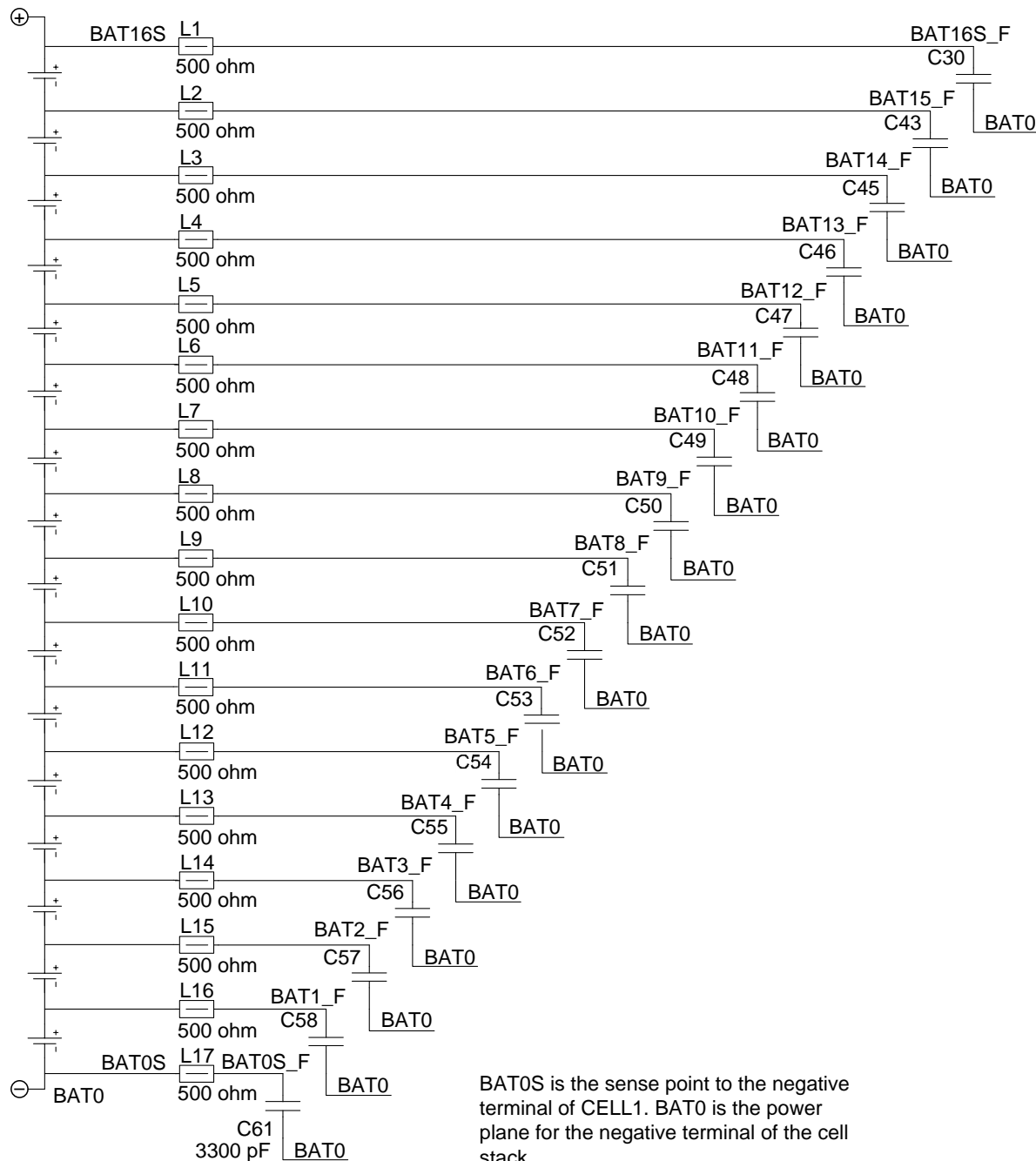
$$f_c = \frac{1}{2\pi R1C1} \text{ Hz} \quad (11)$$

3. Ensure that the RC-filter components are as close to the device as possible. The capacitor location is extremely important and must be given priority for optimum performance.
4. For applications that require a very low filter cutoff frequency, connect a differential capacitor between the VSENSE lines to provide the bulk of the AFE input filtering. The bias voltage on these differential capacitors are the same (or very close), therefore, anti-aliasing is improved.

Additional components are necessary to improve EMC performance of bq76PL455A in applications with electrically noisy environments.

- Use ferrite beads or small inductors in series with the cell inputs between the cell output and the series resistor to the VSENSE input. The bead and small capacitor must be located near each other.
- Add a 0.0033- $\mu$ F capacitor from each cell input to the battery pack (BAT0 in [Figure 29](#)). Adjust the value of capacitance to satisfy the PCB layout and field conditions for the application.

## Application Information (continued)



**Figure 29. EMC Filter on Cell Inputs**

The AUX\_ inputs are single ended, which makes them vulnerable to noisy environments. In order to achieve more accurate results in extremely noisy environments, it is recommended to use the AUX\_ inputs to form a pseudo-differential measurement. One example is shown in . In this example, AUX1 is used to measure the high side of the connection, while AUX0 is used to measure the low-side of the connection. The AUX0 measurement is then subtracted from the AUX1 measurement in order to get a differential measurement that is more accurate.

## Application Information (continued)

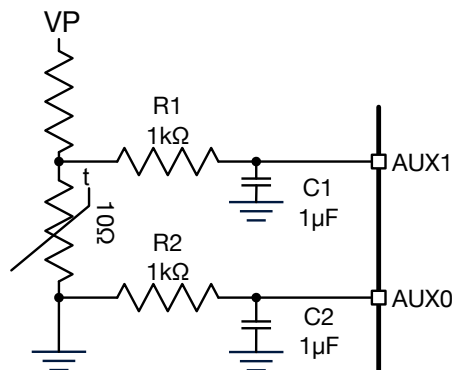


Figure 30. Differential AUX\_ Example

### 8.1.1.6 AUX\_Connections

VAUX connections require a series resistor and bypass capacitor for filtering to ensure best results. Connect a 1-kΩ resistor from the measure point to the VAUX input and bypass VAUX to GND with a 1-μF capacitor. See [Figure 31](#) for connection example.

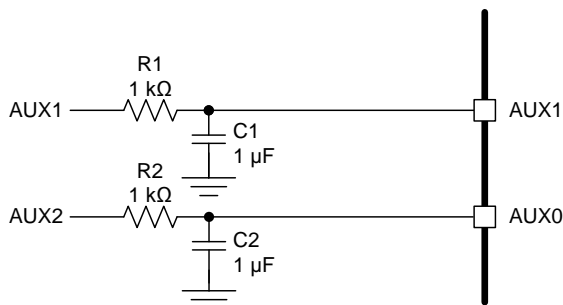


Figure 31. AUX\_ Filter Components

## 8.1.2 Communication Buses

### 8.1.2.1 Single-Ended Communication (UART)

Communication with the bq76PL455A from a host controller is performed utilizing a UART communication protocol. The UART interface requires the following configuration:

1. COMML- is connected by 100-kΩ pull-down to DGND.
2. COMML+ is connected by 100-kΩ pull-up to V5VAO.
3. FAULT\_N has a 50k pull-down to make sure a faults are generated when VIO is not present. The pull-down on the FAULT\_N notifies the host controller in the case of an inadvertent shutdowns.
4. TX and RX are pulled-up to VIO through a 100-kΩ resistor. Do not leave TX and RX unconnected. The TX must be pulled high to prevent triggering an invalid communications frame during the idle state when TX is high. When using a serial cable to connect to the host controller, connect the TX pull-up on the host side and the RX pull-up on the bq76PL455A side.

### 8.1.2.2 Daisy-Chain Communication Differential Communications

For applications that require multiple bq76PL455A devices, a back-side differential communication bus is provided that allows the host controller to interface with up to 16 devices, while utilizing only one UART interface. In this configuration, the bq76PL455A devices are daisy-chained. For the devices that are higher in the stack (not using the UART interface, differential communications only), the following is the required configuration.

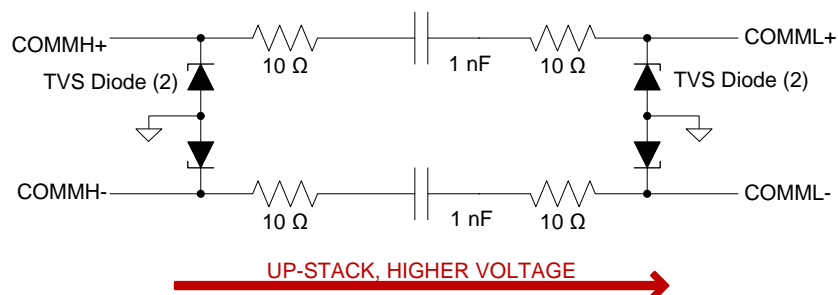


## Application Information (continued)

1. FAULT\_N has a 50-k $\Omega$  pull-down resistor to make sure a fault is generated when VIO is not present.
2. TX and RX should be pulled-up to VIO through a 100-k $\Omega$  resistor. Do not leave TX and RX unconnected.

### 8.1.2.2.1 Stacked Devices on Same PCB

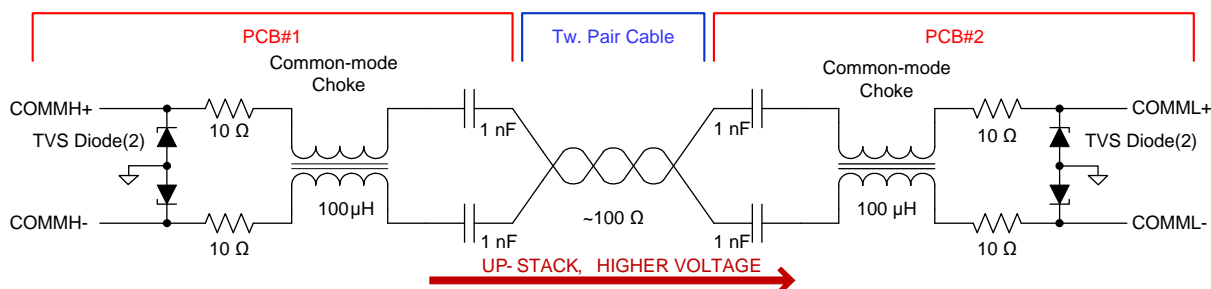
When multiple, daisy-chained bq76PL455A devices are located on the same PCB, use the circuit in [Figure 32](#) to ensure best performance of the backside communication.



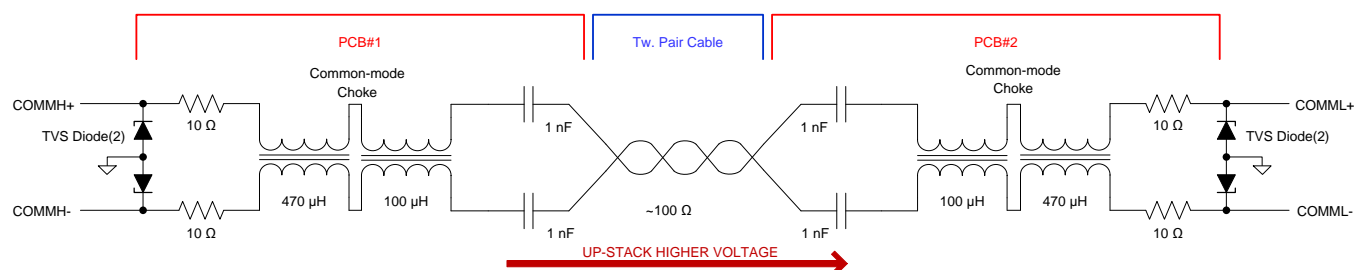
**Figure 32. Components Required for Daisy-Chain Communication between Devices on Same PCB**

### 8.1.2.2.2 Stacked Devices Separated by Cables

Many applications require multiple, daisy-chained bq76PL455A devices that are separated by cables. The cable introduces additional challenges to the application. The recommended circuit is as defined in [Figure 33](#) and [Figure 34](#).



**Figure 33. Components Required for Daisy-Chain Communication between PCBs**



**Figure 34. Components Required for Daisy-Chain Communication between PCBs in Noisy Environments**

### 8.1.2.2.3 Daisy-Chain Communication Cables

Select and design the communication cables such that the total sum of capacitance on any COMML $\pm$ , COMMH $\pm$  or FAULT\_N $\pm$  lines (between ICs) is no greater than 140 pF to support the maximum number of stacked ICs.

The capacitance of the cable is calculated using [Equation 12](#):

## Application Information (continued)

$$\text{unshielded twisted pair cable } C = \frac{2.2\epsilon}{\log\left(\frac{1.3D}{f \times d}\right)}$$

where

- C = mutual capacitance, pF/ft
- $\epsilon$  = insulation dielectric constant (for example: PVC = 5)
- f = stranding factor (for example: 1 strand = 1, 7 strands = 0.939, 19 strands = 0.97, 37 strands = 0.98)
- D = diameter over the insulation, inches
- d = diameter of the conductor, inches

(12)

The unshielded twisted cable used for bench testing (Alpha Wire 3050 series, Digi-Key part number +A2015W-1000-ND) has the following specifications:

$\epsilon = 5$  (PVC)

f = 0.939 (7 strand)

D = 0.056"

d = 0.024" (0.056" – 2 x 0.016" insulation thickness)

conductor DCR = 25  $\Omega$ /1000 ft

∴ (therefore) resulting in capacitance of  $\approx 21.6$  pF/ft.

The best choice of differential cable is an automotive-grade, unshielded, twisted cable designed for CAN, such as the [Waytek SAE J1939/15 CAN](#) data bus cable. The capacitance for this cable is approximately 17 pF/ft.

The input capacitance presented by the common-mode filter (see [Common-Mode Filter](#)) must also be included in the total capacitance budget. Only one TVS diode is used as they are connected to both sides of the differential pair. The allowable cable length is calculated using [Equation 13](#):

$$\text{allowable cable length in ft} = \frac{140\text{pF} - 2 \times \text{common mode filter} - 1 \times \text{TVS diode capacitance}}{\text{cable capacitance/ft}} \quad (13)$$

### 8.1.2.2.4 TVS Diodes

TVS diodes are required on the differential I/Os for protection of the communication interface signals during hot-plug events and also for absorption of high-voltage transients in operation. Select the TVS diodes for the lowest possible capacitance as any capacitance on the lines affects the rise-time of the communication signal. The NXP PESD5V0U1UA is used on the reference design, which has a maximum  $C_d$  of 2.6 pF.

### 8.1.2.2.5 Resistance

The total resistance of each COMML $\pm$ , COMMH $\pm$  or FAULT\_N $\pm$  lines must be less than 20  $\Omega$  (10  $\Omega$  on each end of the signal connection between bq76PL455A devices). This series resistance is required to limit in-rush current in a hot-plug event.

### 8.1.2.2.6 Common-Mode Filter

TI recommends to use a 50–100  $\mu$ H common-mode filter minimum for proper operation. To achieve the best performance in noisy environments, use dual common-mode filters (100  $\mu$ H and 470  $\mu$ H).

For single common-mode filter applications, the TDK 51- $\mu$ H, 2.8-k $\Omega$  choke (part number ACT45B-510-2P-TL003) is recommended. This device has an input capacitance of approximately 18 pF.

For dual common-mode filter applications, the TDK 100- $\mu$ H, 5.8-k $\Omega$  choke (part number ACT45B-101-2P-TL003) and Wurth 470- $\mu$ H, 2.2-k $\Omega$  (part number 744242471) are recommended. The total capacitance is approximately 40 pF.

## Application Information (continued)

### 8.1.2.2.7 Isolation Capacitor

The differential signal lines are isolated between ICs by a DC blocking capacitor. The capacitor must be rated with a high enough voltage to provide standoff margin in the event of a fault in the system that exposes the device to a local hazardous voltage. Selecting a capacitor rated at a minimum of 2 times the stack the voltage is the recommended practice. One capacitor is sufficient for the normal operation of the device. However, two capacitors are used (one at each end of the cable or PCB wiring) for an additional safety factor. In these applications, the capacitor must be doubled from the typical requirement to maintain the required capacitance in the signal path. Connect a minimum of 1 nF, with  $\pm 10\%$  or better tolerance and the appropriate voltage rating for the application. In noisy environments, 2 nF is recommended.

### 8.1.2.2.8 Unused Differential Communications Pins

Unused stack communications pins (COMMH+/-, COMML+/-, FAULTH+/-, FAULTL+/-) have internal terminations; no external pull-up or pull-down resistors are required on these pins, if not used. If not used, leave the unused pins unconnected. The COMMH drivers cannot be disabled.

## 8.1.3 ADC

### 8.1.3.1 Idle (Parking) Channel Errors

Between acquisition cycles, the multiplexer idles on the highest VSENSE channel enabled for conversion by the CHANNELS register for sampling first on the next cycle.

Parking introduces a very small error to the idle channel due to the input impedance of the device causing a small IR drop through the external resistor, which is part of the LP filter. The error is increased when using VSENSE series resistors greater than 100  $\Omega$ . Setting the AFE\_CTL bit = 1 in this application provides the greatest error improvement. When AFE\_PCTL is set, every time cell voltage sampling requests occur, cell voltage sampling delays by 100  $\mu$ s, regardless of the power status of the AFE. This maintains sampling synchronization between multiple chips. Changes to this bit do not take effect until after the next AFE sample occurs.

### 8.1.3.2 VSENSE Channel Post-Assembly Calibration Adjustment

Use of post-assembly calibration adjustment can improve device accuracy further after exposure to soldering and/or bake cycles in the manufacturing process. ADC gain and offset-correction factors are programmable in the bq76PL455A to allow for post-assembly calibration. The total range of adjustment limitation for both factors is from -9.77 mV to 9.69 mV.

Application of these gain and offset corrections is global to all VSENSE channels. The AUX channels do not receive these corrections. Application of the corrections is to the raw ADC values after application of the factory-stored offset and gain corrections.

Perform the correction procedures at room temperature (RT) using a stable, high-accuracy DC source and / or voltmeter. The registers contain signed 2's complement values. A zero value in either register indicates no correction. Measurement of two voltage points, VIN1 and VIN2, occurs for each correction. The expected minimum and maximum values for the cell can be used; however, ensure the lowest VIN<sub>MIN</sub> value is greater than or equal to 2.0 V and the highest VIN<sub>MAX</sub> is less than or equal to 4.5 V.

For best results in most designs, both VIN1 and VIN2 use the average voltage measured by each channel VSENSE1–16 after correcting for any errors in the stimulus (source) voltages at each input.

#### 8.1.3.2.1 Gain Error Correction

Gain Error Correction: -9.77 mV to 9.69 mV in 255 steps (8 bits) in register VSGAIN

Procedure:

1. Apply voltage VIN1, read back from ADC VOUT1, and record both.
2. Apply voltage VIN2, read back from ADC VOUT2, and record both.
3. Calculate slope  $m = (VOUT2 - VOUT1) / (VIN2 - VIN1)$ .
4. Find the gain error correction (GEC) at 5 V in 16-bit LSB (5 V is used regardless of VINx value).

## Application Information (continued)

$$GEC = \left( \frac{1}{m} - 1 \right) * \frac{5}{\left( \frac{5}{2^{16}} \right)} = \left( \left( \frac{1}{m} \right) - 1 \right) * 2^{16} \quad (14)$$

### NOTE

The final GEC should be an 8-bit 2's-complement value in the range –128 to +127 after discarding the upper 8 bits of the 16-bit value. Values exceeding this are suspect and probably indicate an error. If using such a value, saturate (–128 or +127) the resulting 8-bit value and correct the sign as necessary.

This gain adjustment is input dependent—A correction of 9 mV at full-scale input, results in a correction of 4.5 mV at half-scale input.

5. Write the 8-bit value to the VSGAIN register.
6. Perform the steps in [Offset Error Correction](#).

### 8.1.3.2.2 Offset Error Correction

Offset Error Correction: –9.77 mV to 9.69 mV in 255 steps (8 bits) in register VSOFFSET

Procedure: (Use m, VIN1, and VOUT1 from the [Gain Error Correction](#) procedure.)

1. Find the offset error correction (OEC).

$$OEC = \frac{VIN1 - \left( \frac{1}{m} \right) * VOUT1}{\frac{5}{2^{16}}} = \left( VIN1 - \left( \frac{1}{m} \right) * VOUT1 \right) * \frac{2^{16}}{5} \quad (15)$$

### NOTE

The final OEC should be an 8-bit 2's-complement value in the range –128 to +127 after discarding the upper 8-bits of the 16-bit value. Values exceeding this are suspect and probably indicate an error. If such a value must be used, the resulting 8-bit value should be saturated (–128 or +127) and sign corrected as necessary.

2. Write the 8-bit value to the VSOFFSET register.
3. Save the new values to EEPROM by setting DEV\_CTRL[WRITE\_EEPROM], after setting the appropriate values for MAGIC1 and MAGIC2. The EEPROM checksum will also require re-calculation and saving due to this (or any) change.

### 8.1.3.3 AUX Channel Post-Assembly Calibration Adjustment

Using post-assembly calibration adjustment can also improve the AUX channel accuracy further after exposure to soldering and/or bake cycles in the manufacturing process. The process is similar to the steps for the VSENSE channel correction, with three differences:

- AUX channels only have offset correction, there is no gain correction.
- Each AUX channel has an individual offset correction register, rather than a single global correction.
- The correction range has an extension from –39.06 mV to 38.99 mV in 1023 steps (10 bits).

Perform the correction procedures at room temperature (RT) using a stable, high-accuracy DC source and / or voltmeter. The registers contain 10-bit, signed, 2's-complement values. A zero value in any register indicates no correction. Each correction measures two voltage points. The procedure can use the expected minimum and maximum values for the cell. However, the lowest VIN<sub>MIN</sub> value should be greater than or equal to 2.0 V and the highest VIN<sub>MAX</sub> should be less than or equal to 4.5 V.

## Application Information (continued)

Although the bq76PL455A does not provide AUX gain error correction, the host microcontroller can perform the required correction using the slope value calculated as part of the GEC for the VSENSE channels. The procedure can use the value stored in VSGAIN or a different value stored separately in one of the SCRATCH registers of the bq76PL455A. If the procedure uses a value stored in the bq76PL455A, this permits the value to follow the device in distributed systems. Optionally, the microcontroller memory can store the value. Because gain error corrections are primarily correcting for VREF errors, a single-gain error correction for the AUX channels is sufficient.

**AUX Offset Error Correction:** –39.06 mV to 38.99 mV in 1023 steps (10 bits) in registers AX0OFFSET through AX7OFFSET, one 16-bit register per AUX input channel.

Procedure: (use *m* from the [VSENSE Gain Error Correction](#) procedure, or recalculate separately using any AUX channel, as desired)

1. Apply voltage VINn, read back from ADC VOUTn, where 'n' is the AUX channel number. Record both values.
2. Find the AUX offset correction (AOC). This is the same formula used for the VSENSE offset correction (OEC,) but a larger adjustment range is possible.

$$AOC_n = \frac{VIN_n - \left(\frac{1}{m}\right) * VOUT_n}{\frac{5}{2^{16}}} = \left(VIN_n - \left(\frac{1}{m}\right) * VOUT_n\right) * \frac{2^{16}}{5} \quad (16)$$

### NOTE

The final AOC should be a 10-bit 2's-complement value in the range –512 to +511 after discarding the upper 6-bits of the 16-bit value. Values exceeding this are suspect and probably indicate an error. If such a value must be used, the resulting 10-bit value should be saturated (–512 or +511) and sign corrected as necessary.

3. Write the 10-bit value to the 16-b AXnOFFSET register, where *n* is the AUX channel number.
4. Repeat steps 1–3 for each AUX channel 0–7.
5. Save the new values to EEPROM by setting DEV\_CTRL[WRITE\_EEPROM], after setting the appropriate values for MAGIC1 and MAGIC2. The EEPROM checksum will also require re-calculation and saving due to this (or any) change.

## 8.1.4 Device Addressing

### 8.1.4.1 Using a Stored Address

As part of the reset process, the EEPROM restores the value in ADDR. If DEVCONFIG[ADDR\_SEL] == 0, this value is overridden by the value sampled from the GPIOs.

### 8.1.4.2 GPIO Addressing

When DEVCONFIG[ADDR\_SEL] == 0, the device uses the address sampled from GPIO[4:0] to set ADDR. The address is sampled as part of the reset process or by setting DEV\_CTRL[AUTO\_ADDRESS].

### 8.1.4.3 Auto Addressing

Prior to using the Auto-Addressing function in a stack, all devices must be awake and ready for communication. The steps necessary for this state are detailed elsewhere in this document, but typically require a few milliseconds per device.

Very simple *stacks* consisting of a single device may use address 0x00 (or any other valid address) for the device. The first device in stacks of more than one device may also use Address 0x00.

## Application Information (continued)

When `DEVCONFIG[ADDR_SEL] == 1` and `DEV_CTRL[AUTO_ADDRESS] == 1`, then the device enters automatic addressing mode. In this mode, the device turns off the high-side communications transmitters for one frame (so the next frame received is not driven out the high-side differential interface) and enables writes to `ADDR[DEV_ADDR]`. The expectation is that the next frame will set the address of the part. Normally, the address is not writeable, so the device can use a Broadcast write transaction and will only affect the one part waiting for an address. After receiving the frame, writes to `ADDR[DEV_ADDR]` are again disabled and the high-side transmitter is re-enabled.

To auto-address the stack of bq76PL455A devices, the microcontroller should:

1. Broadcast write `DEV_CTRL[AUTO_ADDRESS] = 1`
2. Broadcast write consecutive addresses to `ADDR[DEV_ADDR]` until all parts have been assigned a valid address.

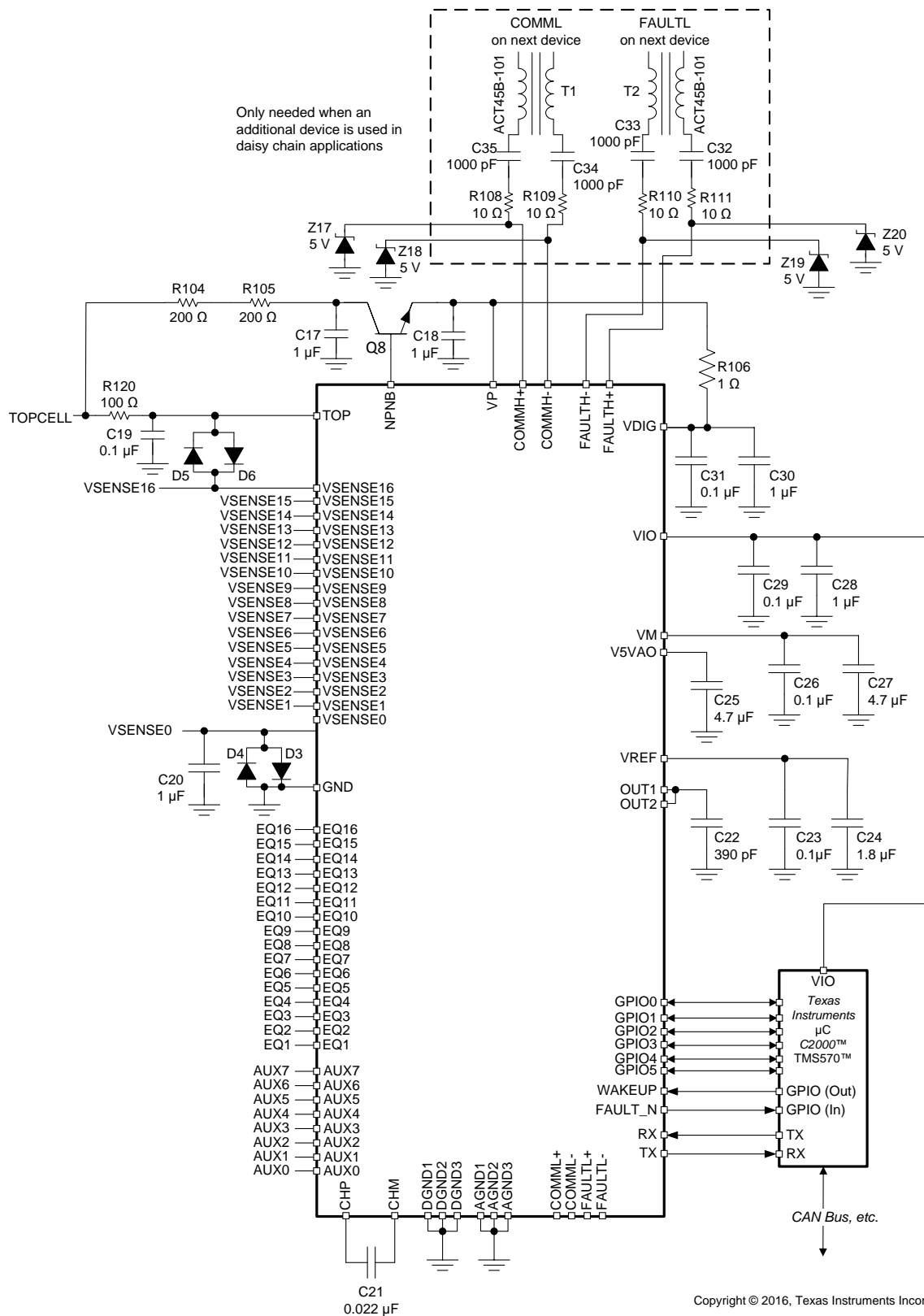
Good practice dictates that all devices be checked by reading back their address registers, at a minimum, to establish that the addressing functions worked properly. Subsequent reading and writing depend on correctly addressed devices in the stack or executing any user-initiated tests, such as the checksum test.

### 8.1.5 Balancing

If the part is configured to disable balancing on a fault condition and any fault occurs while balancing is occurring (`CBCONFIG[BAL_CONTINUE] = 1` && `CBENBL`  $\neq$  0), there is a window approximately 2  $\mu$ s where writes to the part are blocked immediately after the fault occurs. If the user attempts a write in this window, the write will not occur. In general, the user should verify that any commands have been properly processed.

### Figure 35. Cell Connections

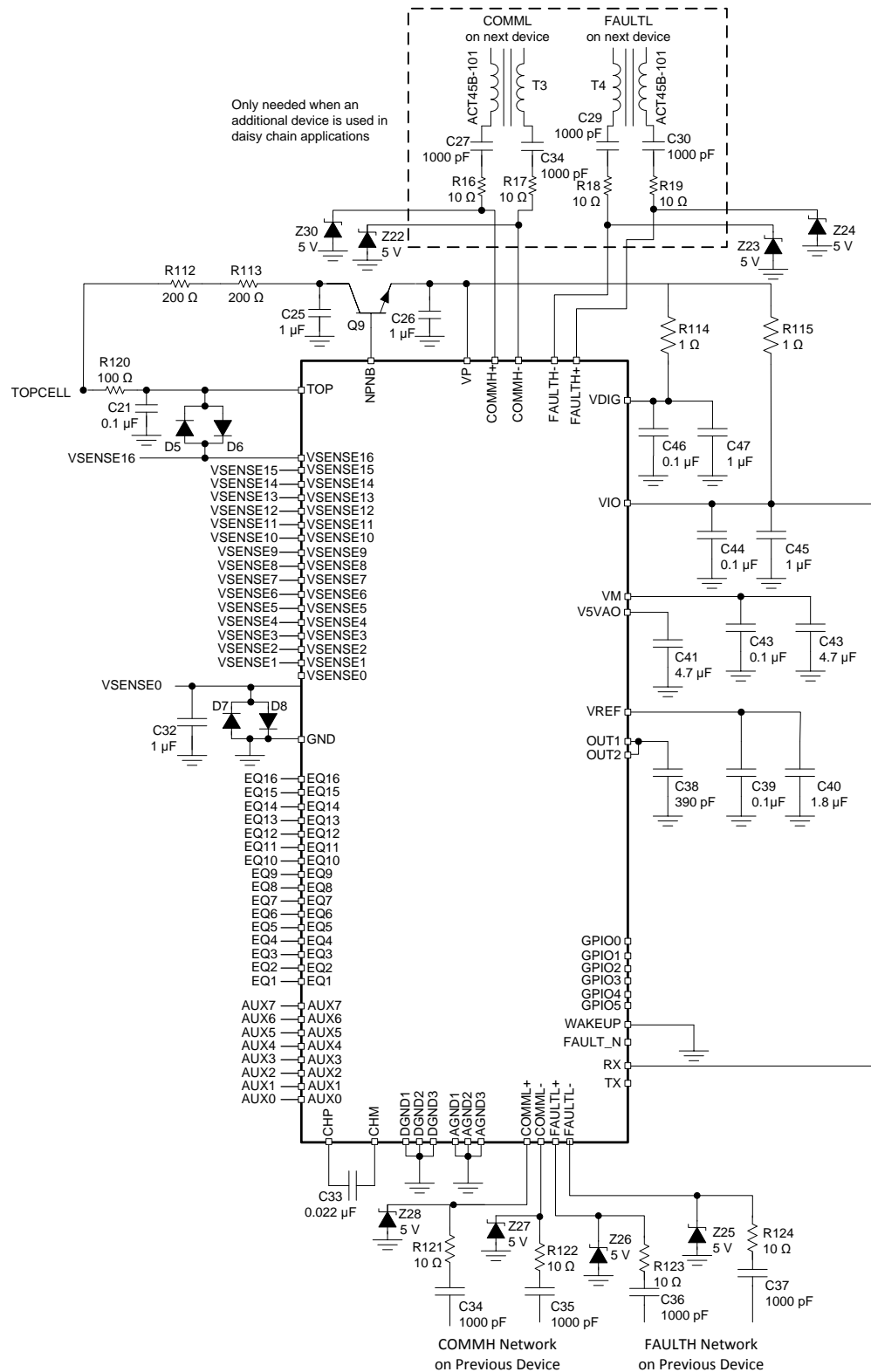
## Typical Application (continued)



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Figure 36. Main Device



**Typical Application (continued)**


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**Figure 37. Additional Device**

## Typical Application (continued)

### 8.2.1 Design Requirements

In order to extract the best performance from the bq76PL455A, it is imperative to take care with the choice of external components and the design of the PCB to which the device and the associated components are mounted.

### 8.2.2 Detailed Design Procedure

The following sections have a more detailed discussion of design considerations that should be made.

#### 8.2.2.1 Voltage Reference

A decoupling capacitor (sum of C60 and C39 in schematic in or ) of no greater than 2  $\mu$ F, with minimum temperature stability rating of X7R (COG/NPO provide better performance).

#### 8.2.2.2 OUT1 Capacitor Selection

To determine the value of the OUT1 capacitor, use the averaging mode, sampling period, and averaging sample interval.

##### 8.2.2.2.1 For OVERSMPL[CMD\_OVS\_CYCLE] = 0

When OVERSMPL[CMD\_OVS\_CYCLE] = 0, each channel is sampled n times before proceeding to the next channel. This bit only affects the VSENSE and AUX channels. The typical recommended OUT1 capacitor value is 390 pF, type C0G/NP0 or better.

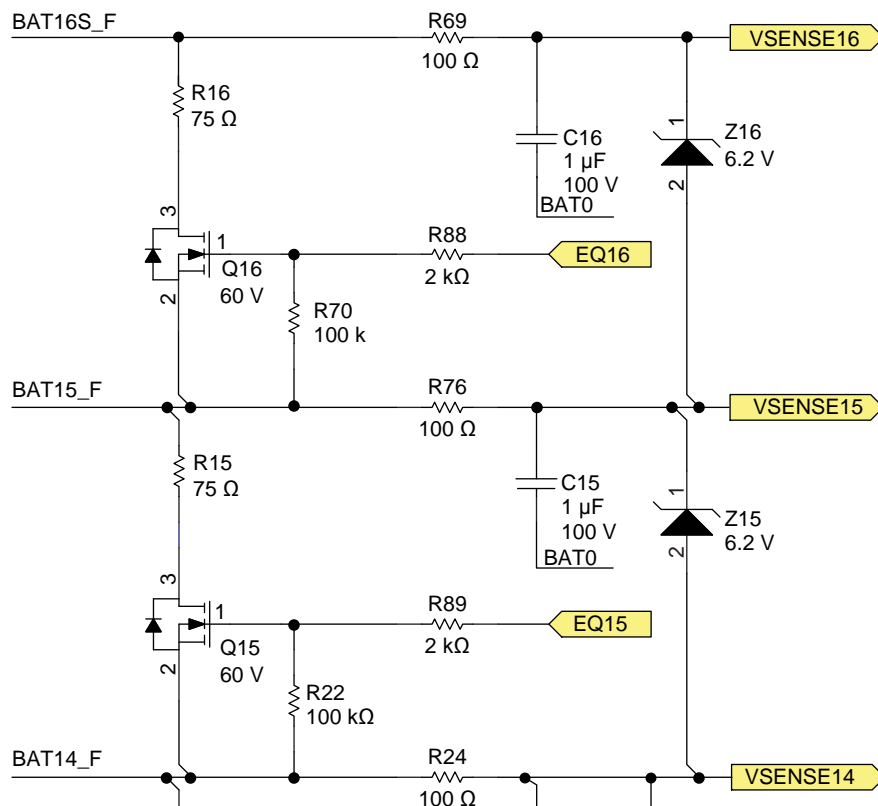
##### 8.2.2.2.2 For OVERSMPL[CMD\_OVS\_CYCLE] = 1

When OVERSMPL[CMD\_OVS\_CYCLE] = 1, all channels are sampled in order, then the cycle repeats until the number of additional oversamples has been taken. This bit only affects the VSENSE and AUX channels. For a brief discussion of proper OUT1 capacitor selection and the default configuration, please see *Out Filter Selection* section in [bq76PL455EVM and GUI User's Guide](#) (SLUUAT2).

#### 8.2.2.3 Passive Cell Balancing Circuit

[Figure 38](#) shows the balancing circuit for two cells in the stack. All cells require this circuit for passive balancing.

## Typical Application (continued)



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**Figure 38. Cell Balancing Circuit**

### 8.2.2.4 Balance FET

Select the Balance FET (Q15 and Q16) based on the following criteria:

1. The  $V_{DS}$  must be selected based on derating requirements determined by the stack voltage.
2.  $V_{GS}$  must be as large as possible and preferably have ESD protection from gate to source. This protects the part during hot plug.
3. The  $V_{GS}$  threshold is of concern only if the discharge resistors are going to be turned on at low-battery voltages.

The 2V7002K is recommended because of its 60  $V_{DS}$ ,  $\pm 20 V_{GS}$ , and the gate is ESD protected with an internal zener diode.

$R_{DS}$  value is of little consideration with the discharge currents for this application.

Power dissipation of the FET will be a function of discharge current selected and the resistance value of FET at that worst-case condition, usually at hot temperature.  $I^2R$  will be the power dissipated. Take care in selecting size if using very small packages.

The  $V_{GS}$  resistor (R77 and R85) ensures that the gate of the FET is turned off and does not float into a linear or on state causing excessive leakage currents on that cell in case of FET failure or PCB open.

A series resistor between the EQ pin and the FET gate limits current going into the FET during hot plug or other transient events.

## Typical Application (continued)

### 8.2.2.5 Balance Resistor

The balance resistor (R15 and R16) sets the required balance current. If used, the resistors in series with the cell connections (top and bottom, in front of the zener diode) must be included in this calculation. These resistors must be sized appropriately to handle the thermal dissipation of continuous cell balancing.

### 8.2.2.6 WAKEUP Pin

The WAKEUP pin input requires a pull-down to ensure it is not left unconnected and cause an unintended wakeup (active high).

## 8.3 Initialization Set Up

### 8.3.1 Factory Configuration Summary

When the bq76PL455A leaves the factory, its EEPROM memory holds a configuration suitable for many applications, but may need some adjustment for your design.

From the factory (see [Register Summary](#)):

1. The address is set to 0x00.
2. All digital and communications faults are enabled.
3. All analog faults (OV, UV) are disabled (masked).
4. Any fault that occurs and is not masked will control the FAULT\_N and FAULTL± outputs.
5. Sampling is set for 8-sample averaging, 60 µs for the first sample, and 12.6 µs for the other samples (7). This setup requires a 390-pF capacitor on pin OUT1.
6. All sixteen VSENSE inputs and no AUX channels are enabled for conversions.
7. No user-settable gain or offset corrections are applied to the VSENSE or AUX ADC channels – these allow post-assembly or end-of-line corrections to ADC results.
8. The UART interface is enabled at 250 Kbaud.
9. GPIO pins are all programmed as inputs, no pull-up or pull-down resistor is enabled, leaving the inputs floating. The pins should be reprogrammed to become outputs, or inputs with a pull-up/down enabled if none are provided externally. The pins should not be allowed to remain as floating inputs, because unpredictable operation is possible accompanied by excess current draw.

## Initialization Set Up (continued)

### 8.3.2 Device Setup/User Configuration Summary

An abbreviated version of starting up a stack of devices is described. Many more details are available in the [bq76PL455A-Q1 Software Design Reference](#) (SLVA617), including validated communications sequences.

1. Set an address for each device in the stack, using GPIO pins or Auto-Addressing.
  - (a) Make sure all devices are awake and are ready to receive the Auto-Address Enable command.
  - (b) Turn on the downstream communications drivers on all devices in the chain.
  - (c) Place all devices into Auto-Address learn mode.
  - (d) Send out new addresses to all possible bq76PL455A device addresses, in incrementing order starting at zero.
  - (e) Read back the value stored in the Device Address register from each newly addressed device, starting at address zero and proceeding sequentially. The last bq76PL455A to respond successfully is the last device in the serial chain. Steps d and e may be shortened if the range of possible devices is known in advance. Limit the number addressed to the expected quantity.
  - (f) Turn off the high-side communications receiver on the last (top-most) device in the chain.
  - (g) Turn off the single-ended transmitter on all but the lowest device in the chain.
  - (h) Starting at the top of the stack of devices, clear all existing faults. It is important to start clearing faults from the top of the stack to prevent faults from *higher* units from re-enabling faults as they propagate down the stack.
2. Configure the AFE (Channel Selections and Fault Thresholds)

Prior to reading voltages from daisy-chain networked devices, the AFE on each of the stacked devices should be properly configured to scan the desired channels at the desired timing. Once each device has been properly configured, reading voltages from each device can begin.

The following listed steps should be performed as a group for each stacked device, starting from the top device, continuing through, and ending with the bottom-most device of the stack. Generally, this configuration is done in advance during factory initialization and test and the desired configuration parameters are stored in EEPROM on each device.

- (a) Configure GPIO pins as required by your design
  - (b) Configure the initial sampling delay
  - (c) Configure voltage and internal sample intervals/periods
  - (d) Configure the oversampling rate
  - (e) Select number of cells and desired channels to sample
  - (f) Set overvoltage and undervoltage thresholds
  - (g) Check and clear faults, which may have occurred because of the configuration.
3. Reading Voltages from Daisy-Chain Networked Devices

When bq76PL455A devices are networked, wherein each device monitors a section of a stack of cells, it is important to try to capture the voltages of each sub-stack as synchronously as possible. This *snapshot* can be obtained if all devices in the stack are sampling in parallel.

#### Summary of Steps for Reading Voltages from Daisy-Chain Networked Devices

Broadcast a Sample and Send command to all devices in the network: this causes all devices to start sampling in parallel, and, once the sampling is complete, the devices will respond in sequence, starting at the highest address with the sampled data. Alternatively, the following two-step process could be employed to similar effect:

- (a) Broadcast a trigger to all devices in the network to start sampling the selected cell and auxiliary channels and temperature.
- (b) Query each device individually in sequence for the data collected during the last *snapshot* read.

## 9 Power Supply Recommendations

The bq76PL455A is powered from the same cells it monitors. The bq76PL455A generates the additional VP and VDIG supplies used in operation from this input. For best performance, use the following guidelines for component selection.

### 9.1 NPN LDO Supply

VP1 is the input for the external LDO supply for the bq76PL455A. Figure 39 shows the typical circuit.

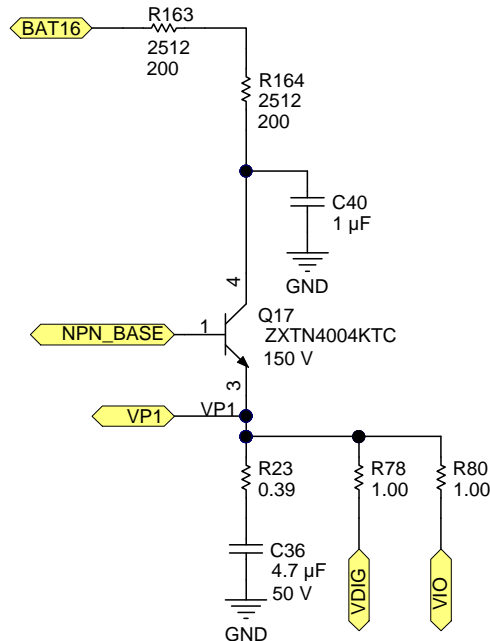


Figure 39. Power Supply Schematic

Select the NPN Transistor based on the following criteria:

1. Collector-Emitter Breakdown Voltage ( $BV_{CEO}$ ) > 100 V (or the module voltage plus any derating)
2. DC gain ( $\beta$  or approximately equal to  $h_{fe}$  (AC gain)) > 100 at the expected load current
3. Collector-base capacitance < 35 pF at typical base-voltage range
4. Power handling > 500 mW (this assumes a 1-k $\Omega$  resistance in series with the collector)
5. Current handling > 100 mA

The series resistors R163 and R164 in Figure 39 serve several purposes:

1. Limit the current in the event of a fault
2. Shift some constant power dissipation in the regulator away from the transistor onto the resistor
3. Combine with the input capacitor on the transistor collector to serve as a filter

To calculate the required resistance, use Equation 17:

$$R_{MAX} = \frac{(V_{MODULE(min)} - (V_{P_{MAX}} + V_{CE(SAT)}))}{31mA + I_{LOAD}}$$

where

- $V_{CE(SAT)}$  =  $V_{CE}$  min at  $V_{BE(on)}$ , from transistor datasheet.
- 31mA is the bq79PL455A maximum inrush current at startup.
- $I_{LOAD}$  is the expected current for any non-bq76PL455A external loads applied to the VP pin.

(17)

## NPN LDO Supply (continued)

Allowing for the lowest possible module voltage ( $V_{BAT\ min}$ ) of 12 V, using  $V_P\ max = 5.5\ V$ ,  $V_{CE\_SAT} = 0.25\ V$  (from transistor datasheet) and maximum load current (bq76PL455A  $I_{ACTIVE\ max}$  + any additional load connected to VP)  $\approx 7\ mA$ , results in  $R\ max \approx 1.464\ k\Omega$ .

The R78 and R80 series resistors in the VDIG and VIO supplies (respectively) isolate large load capacitance from the voltage regulator to help with loop stability.

Connect a filter on the VP supply (R23 and C36) for stability. Use  $R23 = 390\ m\Omega$  and  $C36 = 4.7\ \mu F$ .

### 9.1.1 External Supply

The bq76PL455A also supports using an external supply for VDIG and VIO. Connect the external supply to these inputs and disable the internal regulator by setting  $REG\_DISABLE = 1$  in DEVCONFIG register (address 14).

### 9.1.2 Handling of Supplies in Shutdown Mode

If the NPN circuit is not used (external supply), VP and VDIG should be turned off immediately after entering SHUTDOWN mode. Removing the VP and VDIG supplies places the device in SHUTDOWN mode.

While in SHUTDOWN mode, VIO and any other external supply indirectly connected to the communication, fault, GPIO and AUX inputs must be turned off or disabled to avoid back powering the device through internal ESD structures. The bq76PL455A immediately enters reset when VIO is removed.

### 9.1.3 AFE Output RC Filter

The bq76PL455A AFE output requires an RC-filter circuit comprised of a 1-k $\Omega$  series resistor (internal to the device) and an external capacitor on OUT1 (C44). OUT1 and OUT2 must be connected together externally. The simple first-order RC filter provides a limited amount of noise filtering before the signal is converted by the integrated ADC. Each input channel is converted sequentially according to the channel conversion time. For example:  $ADC\_PERIOD\_VOL$ , programmed in register 62, see [Register Maps](#), and the OUT1 and OUT2 voltage must change quickly and settle to the new measured channel value within this time. The RC filter, while reducing noise, slows the settling speed of the OUT1 and OUT2 voltage to the ADC and must be selected as a tradeoff between noise cancellation and accuracy degradation. Selecting too much capacitance prevents OUT1 from settling to the required accuracy within the programmed-channel conversion period.

Ideally, to maximize measurement accuracy, the AFE output must settle to within  $< 1/2$  of the ADC LSB. The worst case condition is one where the AFE output has to move the full range that is possible in the system. For example, when an extreme imbalance condition exists or if there is a broken cell sense connection, the swing may exceed 4.2 V. In typical conditions, where cell-to-cell variation is within 100 mV, the AFE output does not need the extreme settling time when the new channel is selected. Select the capacitor value based on the maximum channel-to-channel voltage transition and the actual available settling time, which is dependent on the conversion period of the programmed channel and oversampling mode, if oversampling is programmed.

A value of 390 pF provides best accuracy with a 60- $\mu S$  ADC conversion period and 8x oversampling (on the same channel before changing channels –  $CMD\_OVS\_CYCLE = 0$ ).

For help in selecting C44 for other sampling periods and modes or when it is desired to sample a mixture of channel types (for example: temperature, internal test voltages as well as external cells), please contact Texas Instruments through your FAE.

## 10 Layout

### 10.1 Layout Guidelines

Since the bq76PL455A measures small changes in voltage, care must be taken in the layout of signals to and from the device to avoid coupling noise onto sensitive inputs. The layout of ground and power connections, as well as communication signals should also be made carefully.

#### 10.1.1 Grounding

The bq76PL455A has three analog ground pins: AGND1, AGND2, and AGND3. AGND1 is a general-purpose analog ground associated with the integrated linear regulator controller VP, while AGND2 and AGND3 are quiet analog grounds for the 2.5-V reference, ADC, AFE, and Secondary Protector (window comparators) circuitry. The bq76PL455A device also has three DGND pins for the digital core and one CGND pin for the differential communications I/Os.

Creation of a good ground plane in the layout is crucial to getting optimal performance from the part. A good ground plane on a dedicated layer will improve measurement accuracy, reduce noise, and provide the necessary ESD, EMI, and EMC performance. There is a strong recommendation to have a minimum of four layers in the PCB, with one fully dedicated as an unbroken VSS plane (except thermal reliefs). Avoid placing tracks on this layer to maintain the unbroken integrity of the plane structure.

All seven device grounds should connect to the ground plane with as short as possible track sections to minimize the effects of stray inductance on noise performance.

If more than one bq76PL455A is included on a single PCB assembly, each will require its own plane in the area surrounding the device. This is required because each device has its own VSS reference, often separated by more than 60 V from VSS-to-VSS of adjacent ICs in the stack. These can exist on the same physical layer, with correct separation to meet creepage and clearance requirements.

Although the plane is employed as a solid GND reference with all grounds connected to it, good layout practice still requires locating any decoupling capacitors as close to the pin they are associated with as possible. This reduces inductance and keeps the loop area as small as possible, which in turn keeps the capacitors as effective as possible in reducing noise.

In this document, the reference term for combined grounds connected to the ground plane is *ground* or GND.

#### 10.1.2 Differential Communications

The bq76PL455A uses two differential communications links to transmit signals between ICs in a stack. Employing differential links provides superior noise immunity. The base device then translates the differential signals back to a single-ended signal.

It is important to maintain the signal integrity of each differential pair to maximize immunity to interfering signals from external sources.

1. Keep wires and PCB traces as short as possible. Do not exceed datasheet recommendations.
2. For any single-signal pair between two nodes (ICs), individual wires and traces should have the same length.
3. Unshielded, twisted-pair wiring is required for any cable runs.
4. Run PCB traces in parallel, on the same layer, without any other traces or planes in between. Long runs should avoid *noisy* traces and/or be stitched at intervals similar to twisted-pair wire.
5. Use high-quality capacitors for voltage isolation between ICs and place in close physical proximity to each other as part of the parallel-track layout.

### 10.2 Layout Example

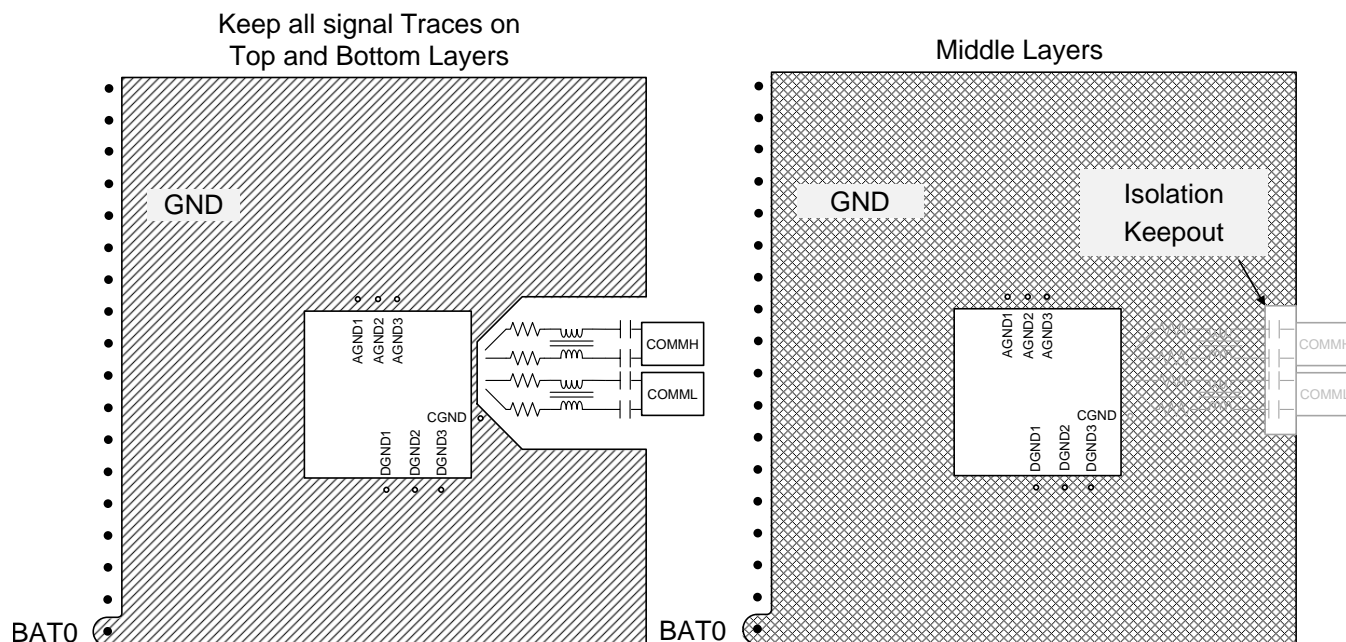
To ensure the best possible accuracy performance, TI recommends to follow some basic layout guidelines for the bq76PL455A to provide best EMI and BCI performance. The isolation caps must be placed close to the edge of the board. The Common Mode Chokes must be close to the daisy-chain cable connector to provide a high-impedance path to common-mode noise as it enters the board. Place the series resistors and TVS diodes next to the bq76PL455A.



## Layout Example (continued)

An unbroken ground plane layer as part of a four or more layer board is recommended, with all AGND, DGND, and CGND connections made directly to the plane. The common GND planes are star connected directly to BAT0. There should also be a keep-out area on plane area adjacent to the isolation capacitors if daisy-chain communication is implemented. The following is a list of grounds.

- AGND1 – Power section (noisy GND)
- AGND2 – GND for Front end output
- AGND3 – GND for ADC input
- DGND1, DGND2, DGND3 – Digital GND
- CGND – Communications digital GND



**Figure 40. Simplified Layout Guideline**

## 10.3 Board Construction and Accuracy

The accuracy numbers provided in are based on the following board stack. Results may vary with board thickness, layout, solder profile, and so forth.

## Board Construction and Accuracy (continued)

Layers	6	Board Size	12 x 18	SIG
Material	FR4 370	Quantity	1	PLN
Req. Thickness (imp mils)	125.0000 (+/- 12.5)	Calculated Thickness	125.6000	BLANK
Lot #	Layer #	Solder Mask	LPI Mask	Thickness
		Plating	1 oz	1.2000
TOP	1	FOIL	1/2 oz	0.7000
		Pre-Preg		5.8000
GND	2		1 oz	1.2000
		Core	31 mils, FR4 370	31.0000
VCC	3		1 oz	1.2000
		Pre-Preg		5.8000
			0 oz	0.0000
		Core	31 mils, FR4 370	31.0000
			0 oz	0.0000
		Pre-Preg		5.8000
New 80 V PLANE	4		1 oz	1.2000
		Core	31 mils, FR4 370	31.0000
Copy of GND Layer 2	5		1 oz	1.2000
		Pre-Preg		5.8000
BOTTOM	6	FOIL	1/2 oz	0.7000
		Plating	1 oz	1.2000
		Solder Mask	LPI Mask	0.4000

**Figure 41. Board Stack for Board Level Accuracy Measurements**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

An evaluation module (EVM), with an associated PC-based Graphical User Interface (GUI) program, is available. Please see [Related Documentation](#) for the reference numbers for the evaluation module and its associated interface software.

#### 11.1.2 Device-Specific Terminology

<b>AFE</b>	Analog front-end. A set of analog signal-conditioning circuitry that uses operational amplifiers and filters to provide a configurable and flexible-electronics functional block, which is needed to interface a variety of sensors to a microcontroller or an analog-to-digital converter.
<b>Battery</b>	A collection of series and parallel connected cells with a single set of high voltage (+) and (–) outputs, which power the vehicle.
<b>BIST</b>	Built-in-Self-Test. A feature of the part allowing testing of critical and other blocks for correct operation. Testing is user controlled and may include external components. Built-In Self Tests can be used optionally as a diagnostic check of defined internal functions of the bq76PL455A-Q1.
<b>BMS</b>	Battery Monitor System (or battery management system), a system of bq76PL455A-Q1s connected together and then to a microcontroller (μC) for measuring, monitoring, and controlling a stacked series of cells forming a battery pack.
<b>Cell</b>	An individual cell or group of cells connected in parallel. Cells are connected to VSENSE inputs and connected in series to form modules and stacks of cells to form a battery.
<b>Daisy-Chain</b>	A series-connected string of monitoring devices, that is, bq76PL455A-Q1 devices communicating to a base device by passing the communications signals through DC blocking devices and the bq76PL455A-Q1 integrated circuits (ICs) in the string. In the case of the bq76PL455A-Q1, a suitably rated capacitor is used as the DC block. A differential communications link is used to form the daisy-chain of the bq76PL455A-Q1. “Daisy-chain” usually refers to just the communications links, but is sometimes used to refer to the collection of devices and cells.
<b>Differential-Signaling</b>	Differential signaling sends a digital signal and its complement simultaneously over a pair of wires. The receiver is sensitive to the difference of the two signals, not the absolute amplitude of either signal by itself. The wire pair is usually twisted so that any interfering signal affects both equally as a common-mode signal. The result is that differential signaling offers much higher common-mode rejection ratios (CMRR) than single-ended signals and results in much better noise rejection.
<b>LPF</b>	Low Pass Filter made up of one or more R/C combinations where the resistor is in series with the signal and the capacitor is on the load side and connected to “ground”. Each R/C element contributes one time constant or tau.
<b>Module</b>	A collection of cells connected in series monitored by one bq76PL455A-Q1. This is typically 16 cells, but may be fewer as needed. Modules may be connected in series to form stacks and complete battery packs. The bq76PL455A-Q1s are also typically connected in a series daisy-chain to facilitate communications to a microcontroller.
<b>Stack</b>	A collection of modules of cells. Stack and battery are synonymous in most applications.
<b>V<sub>CELL</sub></b>	The voltage from one cell or group of parallel connected cells, which is measured across two VSENSE pins, for example, VSENSEn and VSENSEn-1.
<b>V<sub>MODULE</sub></b>	The voltage from a collection of series connected cells forming a module. The voltage is measured by the device from the TOP pin to GND.
<b>V<sub>STACK</sub></b>	The voltage from a collection of series connected cells forming a stack or battery pack. This is often a high voltage. The voltage is not measured directly by the bq76PL455A-Q1, but may be calculated by adding all of the individual cell voltages in the stack or by adding together all of the V <sub>MODULE</sub> voltages in the stack. These should produce approximately the same value.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation, see the following:

- [bq76PL455A-Q1 Software Design Reference](#) (SLVA617)
- [bq76PL455EVM and GUI User Guide](#) (SLUUBA7)
- [Semiconductor and IC Package Thermal Metrics](#) (SPRA953)
- *JEDEC Standard JESD51-2A, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- *JEDEC Standard JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- *JEDEC Standard JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions - Junction-to-Board*

## 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data are subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

For packaging and ordering information, please contact your TI representative.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ76PL455APFCR	ACTIVE	TQFP	PFC	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	76PL455APFC	<a href="#">Samples</a>
BQ76PL455APFCT	ACTIVE	TQFP	PFC	80	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	76PL455APFC	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF BQ76PL455A :**

- Automotive: [BQ76PL455A-Q1](#)

**NOTE:** Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ76PL455APFCR	TQFP	PFC	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
BQ76PL455APFCT	TQFP	PFC	80	250	180.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2

## TAPE AND REEL BOX DIMENSIONS

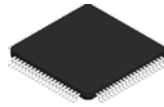


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ76PL455APFCR	TQFP	PFC	80	1000	350.0	350.0	43.0
BQ76PL455APFCT	TQFP	PFC	80	250	213.0	191.0	55.0



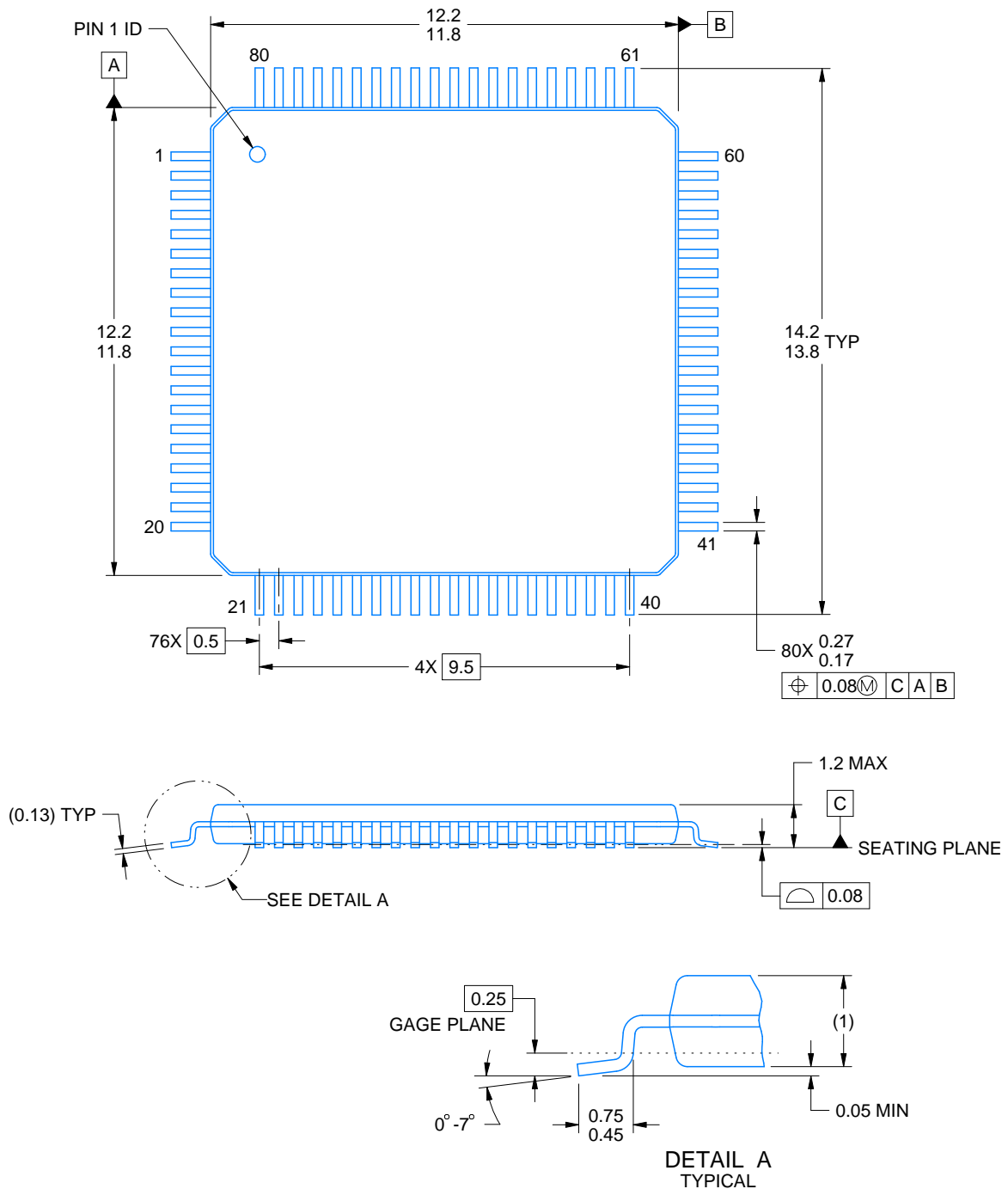
**PFC0080A**



## PACKAGE OUTLINE

**TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



4215165/B 06/2017

### NOTES:

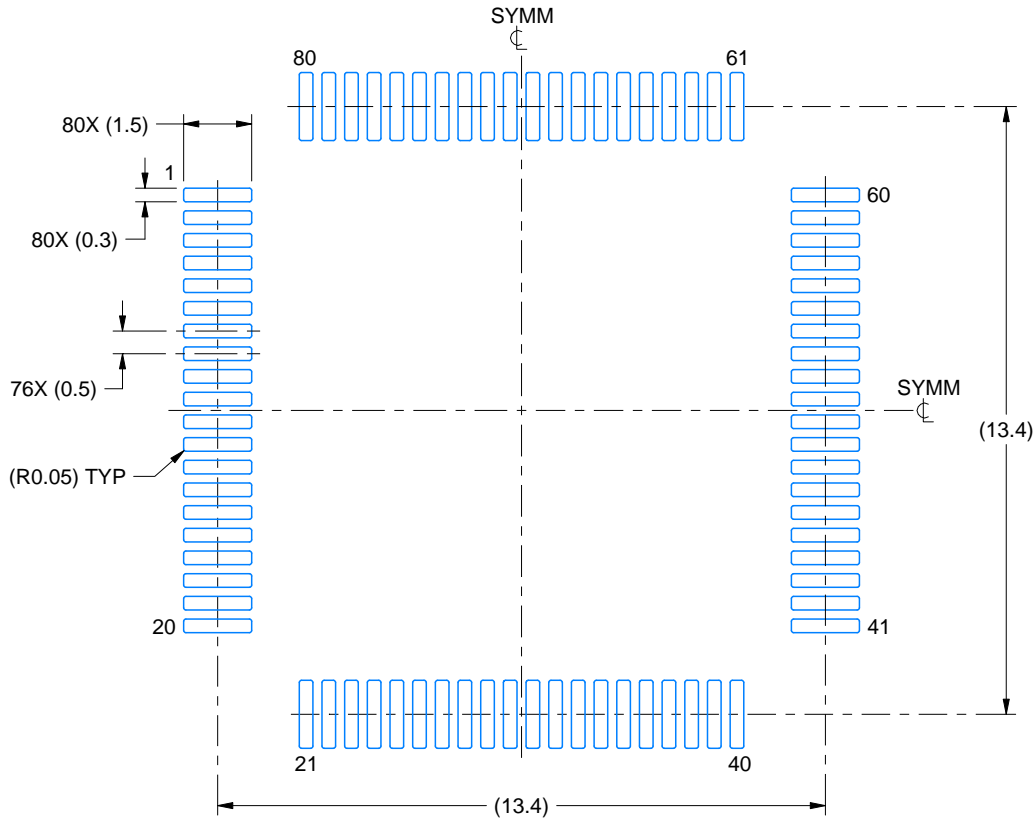
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

# EXAMPLE BOARD LAYOUT

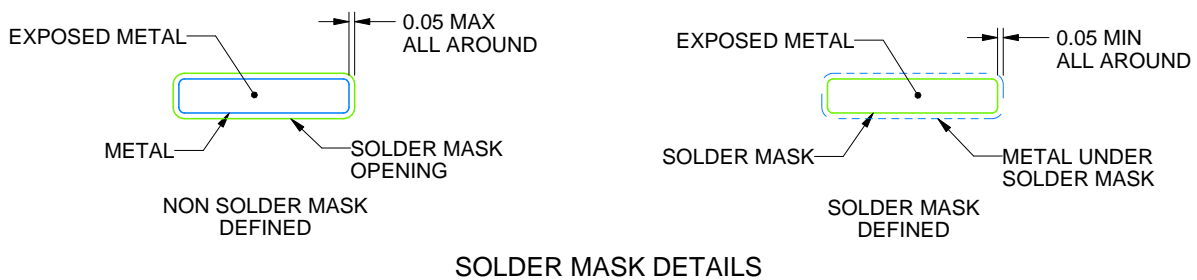
PFC0080A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

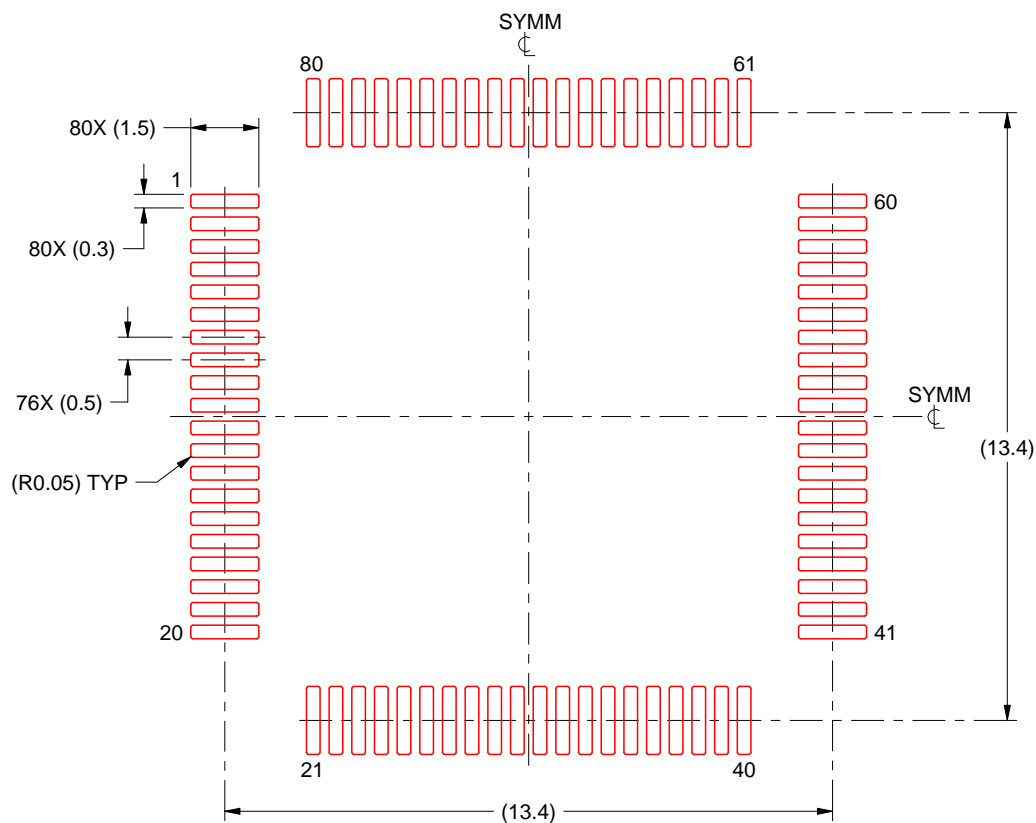
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).

# EXAMPLE STENCIL DESIGN

PFC0080A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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