Panasonic

AN49503A

Battery Monitoring IC for Industry

Features

AN49503A is a battery monitoring IC with protection function. With high resolution ADC built-in, AN49503A is capable to measure battery cell voltage and current level accurately.
Through SPI serial interface, microcontroller unit (MCU) is able to read the status and measured result by AN49503A. The ALARM pins alert the MCU with the abnormal condition such as over voltage (OV), under voltage (UV), over current (OC) and short circuit (SC).
AN49503A can support an application with up to 16 batteries cells in series or a maximum voltage of 85V, it is suitable for application with high input voltage such as E-bike, UPS etc.

- Maximum support 16 battery cells in series
- 10mV measurement accuracy with 14 bits voltage ADC for cell voltage, and 5 channels analog input measurement
- Built-in 16 bits low speed current measurement ADC (Coulomb Counter) and high speed current measurement ADC
- Low–side shunt sense resistor for current measurement and monitoring
- 2 interrupt pins ADIRQ1, ADIRQ2 for voltage measurement and current measurement
- Operation mode - Active, Standby and Shutdown Mode
- SPI serial communication interface up to 1MHz clock with CRC code correction and watchdog timer
- Built-in ALARM pins for overvoltage, undervoltage, overcurrent and short circuit detection and protection feature
- Built-in cell balancing MOSFET, with support of external cell balance MOSFET operation
- 6 channels General GPIO and 2 channels high voltage output
- High-side Charge (CHG) & Discharge (DIS) N-ch FET driver with built-in charge pump and FETOFF control pin
- 50mA 5V LDO
- Package : LQFP080-P-1414FZ

Application

Pedelec, e-Bike, UPS, Server Backup System, Power Tool, Energy Storage Systems etc

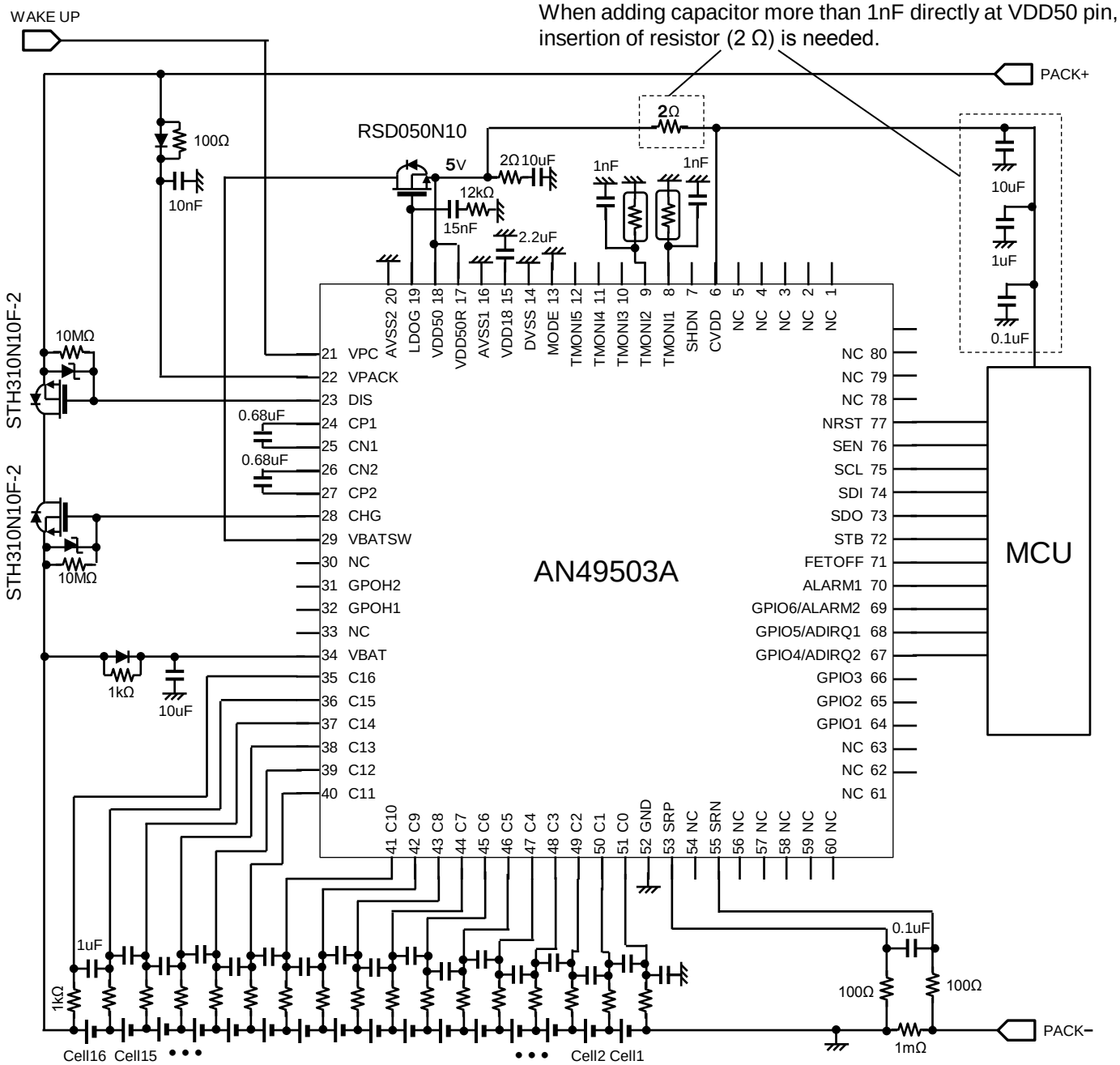
Contents

Chapter 1 Overview

1.1 Recommended Circuit

When connecting a circuit to VDD50, please be careful about below.

- Adding capacitor more than 1nF to VDD50 pin directly is prohibited.
- When needing capacitor more than 1nF, please use through 2Ω resistor.
  Please design as the total capacitor is from 6uF to 16uF.



Note: The recommended circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. Customer is fully responsible for the incorporation of the above illustrated application circuit in the production.

1.2 Electrical Characteristics

1.2.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{VBAT}	-0.3 ~ 99	V	*1
	V_{CVDD}	-0.3 ~ 6.5	V	*1
Operating junction temperature	T_j	-40 ~ 125	°C	*2
Storage temperature	T_{stg}	-55 ~ 125	°C	*2
Input Voltage Range	C16	-0.3 ~ VBAT+1.2	V	*3
	Cn (n=1~15)	-0.3 ~ VBAT+0.3	V	*3
	C0	-0.3 ~ 6.5	V	
	SEN, SCL, SDI, FETOFF STB, GPIOn (n=1~6)	-0.3 ~ V_{CVDD}+0.3	V	*4
	TMONIn (n=1~5),	-0.3 ~ V_{VDD50}+0.3	V	*4
	SRP.SRN	-0.5 ~ 2.0	V	
	VPC	-0.3 ~ 99	V	
	SHDN	-0.3 ~ 6.5	V	
Output Voltage Range	ALARM1,SDO,NRST	-0.3 ~ V_{CVDD}+0.3	V	
	VDD50	-0.3 ~ 6.5	V	
	GPOHn (n=1~2)	-0.3 ~ 99	V	
Output Current Range	ALARM1,SDO,NRST	-6.0 ~ +6.0	mA	*5
	GPIOn (n=1~6)	(-12.0 ~ +12.0)		*6
Allowable Voltage Between Pins	C_n - C_{n-1} (n=1~16)	-0.3 ~ 11	V	

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
Do not apply external currents and voltages to any pin not specifically mentioned.
*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 °C
*3 : (VBAT+0.3) & (VBAT+1.2) shall not over 99V.
*4 : (VCVDD + 0.3), (VVDD50 + 0.3) must not exceed 6.5V.
*5: + Polarity is the direction that flows from the pin to the outside, - polarity is the direction that flows from the outside to the pin.
*6: This is the rated current at the I / O output drivability setting 2mA. The value of () is the rated current when increasing the I / O output drivability by register settings.

1.2.2 POWER DISSIPATION RATING

Package	θj-a	θj-c	P_D(Ta=25℃)	P_D(Ta=105℃)
LQFP080-P-1414FZ	55.5 °C/W	7.2 °C/W	1.80 W	0.36 W

Note) For the actual usage, please refer to the P_D-T_a characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

1.2.3 RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	V_{VBAT}	12.5	59.2	85	V	
	V_{CVDD}	3.0	5.0	5.5	V	
Input Voltage Range	C_n - C_{n-1} (n=1～16)	0	—	5.0	V	
	SEN, SCL, SDI	0	—	V_{CVDD}	V	
	TMONIn (n=1～5)	0	—	5.0	V	
	GPIOn (n=1～6)	0	—	V_{CVDD}	V	
	SRP,SRN	-0.18	—	0.18	V	
	VPC	0	—	85	V	
	SHDN	0	—	V_{VDD50}	V	
Operating Ambient Temperature	Ta_{opr}	–40	25	105	℃	

1.2.4 ELECTRICAL CHARACTERISTICS

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SUPPLY CURRENT							
VBAT Active Mode	I_{BAT1}		—	3.1	3.9	mA	
VBAT Standby Mode	I_{BAT2}	5VLDO:Low Power, Coulomb Counter:off FDRV:Intermittent Communication:off	—	0.15	0.30	mA	
VBAT Shutdown Mode	I_{BAT3}		0	—	1	μA	
5VLDO							
VDD50 Output Voltage	V_{VDD}		4.75	5.0	5.25	V	
VDD50 Drive Current	I_{VDD1}	Normal mode	0	—	50	mA	
VDD50 Drive Current	I_{VDD2}	Low Power mode	0	—	5	mA	
CELL BALANCING CONTROL OUTPUT (CBn)							
Output Impedance	Z_{CB}	⊿Cn = 3.0V ～ 5.0V	—	12.5	20	Ω	

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
CELL VOLTAGE MONITOR							
Input Voltage Range	ΔCn	C_n - C_{n-1} (n=1～16)	0	—	5	V	
Voltage Resolution	V_{RES}	14bits	-—	0.3	—	mV	*1
Voltage Accuracy	V_{ACC_VC}	ΔCn = 2.0V ～ 4.3 V Ta = –30℃ ～ 65℃	–10	—	10	mV	
Conversion Time	t_{conv}	time/cell	—	50	—	μs	*1
Cell Measurement Input Current	I_{IN}	Active mode	–5	—	5	μA	
Input Leakage Current	I_{LK}	Shutdown mode	–1	—	1	μA	
OVER / UNDER VOLTAGE DETECTOR (OV / UV)							
OV detection threshold step	V_{ACC_OV}	2.0～4.5V@6bit	—	50	—	mV	*1
UV detection threshold step	V_{ACC_UV}	0.5～3.0V@6bit	—	50	—	mV	*1
VPACK CELL VOLTAGE MONITOR							
Input Voltage Range	V_{IN}		0	—	85	V	
Voltage Resolution	V_{RES}	14bits	—	6.1	—	mV	*1
Voltage Accuracy	V_{ACC_VPACK}	V_{VPACK} = 12.5V ～ 72V T_a = –30℃ ～ 65℃	–1	—	1	V	
TMONI1-5 VOLTAGE MONITOR							
Input Voltage Range	V_{IN}		0	—	5	V	
Voltage Resolution	V_{RES}	14bits	—	0.3	—	mV	*1
Voltage Accuracy	V_{ACC_VC}	VIN = 0.4～4.7 Not use Pull-up Resistance T_a = –30℃ ～ 65℃	–10	—	10	mV	
Input Pull-up Resistance	R_{PU}		7	10	13	kΩ	
Input Pull-up Resistance Temperature coefficient	RT_{PU}	T_a = –30℃ ～ 65℃	–1.0	—	1.0	%	*3
THERMAL SHUTDOWN							
Shutdown Threshold	T_{SD2}	Tj	150	175	200	°C	*2 *3

*1 : It is a design center value.
*2 : When thermal shutdown occurs, all circuitry is shutdown.
Following wake up (to active mode) sequence in order to restart.
*3 : It is design value. The inspection is not done.

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
LOW SPEED CURRENT MONITOR (SRP,SRN)							
Input Voltage Range	V_{IN}		-180	—	180	mV	
Voltage Resolution	V_{RES}	16bits	—	5.493	—	μV	*1
Voltage Accuracy1	V_{ACC_IMONI}	VIN = 100mV	-1000	—	1000	μV	
Voltage Accuracy2	V_{ACC_IMONI}	VIN = 10mV	-150	—	150	μV	*2
Voltage Accuracy3	V_{ACC_IMONI}	VIN = 1mV	-25	—	25	μV	*2
HIGH SPEED CURRENT MONITOR (SRP,SRN)							
Input Voltage Range	V_{IN}		-180	—	180	mV	
Voltage Resolution	V_{RES}	15bits	—	10.99	—	μV	*1
Voltage Accuracy1	V_{ACC_IMONI}	VIN = 100mV	-1000	—	1000	μV	
Voltage Accuracy2	V_{ACC_IMONI}	VIN = 10mV	-150	—	150	μV	*2
Voltage Accuracy3	V_{ACC_IMONI}	VIN = 1mV	-50	—	50	μV	*2
CURRENT PROTECTION (SRP,SRN)							
Over Current in Charge Detection Accuracy1	V_{CP_OCC}	Detection Threshold 10mV	-5	—	5	mV	*2
Over Current in Charge Detection Accuracy2	V_{CP_OCC}	Detection Threshold from 20mV to 100mV	–10	—	10	mV	*2
Over Current in Charge Detection Accuracy3	V_{CP_OCC}	Detection Threshold from 100mV to 200mV	–10	—	10	%	*2
Over Current in Discharge Detection Accuracy1	V_{CP_OCD}	Detection Threshold from 25mV to 100mV	–10	—	10	mV	*2
Over Current in Discharge Detection Accuracy2	V_{CP_OCD}	Detection Threshold from 100mV to 800mV	–10	—	10	%	*2
Short Circuit in Discharge Detection Accuracy1	V_{CP_SCD}	Detection Threshold from 50mV to 100mV	–10	—	10	mV	*2
Short Circuit in Discharge Detection Accuracy2	V_{CP_SCD}	Detection Threshold from 100mV to 800mV	–10	—	10	%	*2

*1 : It is a design center value.
*2 : It is a design verification value. The inspection is not done.

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
GENERAL PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage “H”	V_{IH}		V_{CVDD} ×0.8	—	V_{CVDD}	V	
Input Voltage “L”	V_{IL}		0	—	V_{CVDD} ×0.2	V	
Output Voltage “H”	V_{OH}	I_{OH} = –1mA	V_{CVDD} –0.6	—	V_{CVDD} +0.3	V	
Output Voltage “L”	V_{OL}	I_{OL} = +1mA	–0.3	—	0.4	V	
GENERAL PURPOSE HV OUTPUT (GPO)							
Output Voltage “L”	V_{OL}	I_{OL} = +1mA	–0.3	—	7.0	V	
DIGITAL INPUT(1) VPC							
Input Voltage “H”	V_{IH}		4.0	—	—	V	
Input Voltage “L”	V_{IL}		—	—	0.3	V	
Pull-down resistance	R_{IL}		6	28	55	MΩ	
DIGITAL INPUT(2) SHDN							
Input Voltage “H”	V_{IH}		3.0	—	—	V	
Input Voltage “L”	V_{IL}		—	—	0.1	V	
Pull-down resistance	R_{IL}		200	820	1500	kΩ	
DIGITAL INPUT(3) SDI,SCL,SEN,FETOFF,STB							
Input Voltage “H”	V_{IH}		V_{CVDD} ×0.8	—	V_{CVDD}	V	
Input Voltage “L”	V_{IL}		0	—	V_{CVDD} ×0.2	V	
Input Leakage Current	I_{LK}		-1	0	1	μA	
DIGITAL OUTPUT(1) ALARM1,SDO							
Output Voltage “H”	V_{OH}	I_{OH} = –1mA	V_{CVDD} –0.6	—	V_{CVDD} +0.3	V	
Output Voltage “L”	V_{OL}	I_{OL} = +1mA	–0.3	—	0.4	V	
DIGITAL OUTPUT(2) NRST							
Output voltage “L”	V_{OL}	I_{OL} = 0 mA	–0.3	—	0.5	V	
Pull-up resistance	R_{IL}	—	50	100	200	kΩ	

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
CVDD UV							
UV detection voltage	V_{IL_UV}	—	—	2.45	—	V	*1 *2
UV release voltage	V_{IH_UV}	—	—	2.80	—	V	*1
Hysteresis voltage	V_{HYS_UV}		—	0.35	—	V	*1
VDD50 UVLO							
UVLO detection voltage	V_{IL_UVLO}		—	4.00	—	V	*1 *3
Nch. FET DRIVER							
Drive voltage (DIS=“H”)	V_{ON_DIS}	V_{ON_DIS} = V_{DIS} – V_{VPACK} VGS connect 10MΩ	9	11	13	V	
Drive voltage (CHG="H”)	V_{ON_CHG}	V_{ON_CHG} = V_{CHG} – V_{VBAT} VGS connect 10MΩ	9	11	13	V	
Drive voltage (DIS=“L”)	V_{OFF_DIS}	V_{OFF_DIS} = V_{DIS} – V_{VPACK} VGS connect 10MΩ	—	—	0.2	V	
Drive voltage (CHG=“L”)	V_{OFF_CHG}	V_{OFF_CHG} = V_{CHG} – V_{VBAT} VGS connect 10MΩ	—	—	0.2	V	
Rise time (DIS=“L” to ”H”)	tr	V_{DIS} = 10% to 90% C_L = 47nF	—	0.8	1.6	ms	
Rise time (CHG=“L” to ”H”)	tr	V_{CHG} = 10% to 90% C_L = 47nF	—	0.8	1.6	ms	
Fall time (DIS =“H” to ”L”)	tf	V_{DIS} = 90% to 10% C_L = 47nF	—	0.5	1.0	ms	
Fall time (CHG=“H” to ”L”)	tf	V_{CHG} = 90% to 10% C_L = 47nF	—	0.5	1.0	ms	

*1 : It is a design center value.
*2 : When detecting the CVDD UV,CVDD_UV flag (CVDD_STAT: bp2) is set to "0".
*3 : When detecting the VDD50 UVLO, it will be switched to the Shutdown mode. (if VPC pin is "L“)

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI Interface Timing (SEN, SDI, SCL, SDO)							
SCL Frequency	f_{SCL}	—	—	—	1	MHz	
SCL Duty Cycle	t_{DUTY}	—	45	50	55	%	
SEN Rising to SCL Rising	t_{SEN_LD}	—	100	—	—	ns	
SCL Falling to SEN Falling	t_{SEN_LG}	—	100	—	—	ns	
SEN "L" Width	t_{SEN_LO}	—	500	—	—	ns	
SDI Setup Time	t_{SDI_SU}	SDI valid to SCL falling	100	—	—	ns	
SDI Hold Time	t_{SDI_HD}	SCL falling to SDI valid	100	—	—	ns	
SDO Valid Time	t_{SDO_VD}	SCL rising to SDO valid C_L ≦ 50 pF	—	—	400	ns	
SDO Disable Time	t_{SDO_DIS}	SEN falling to SDO disable	—	—	400	ns	

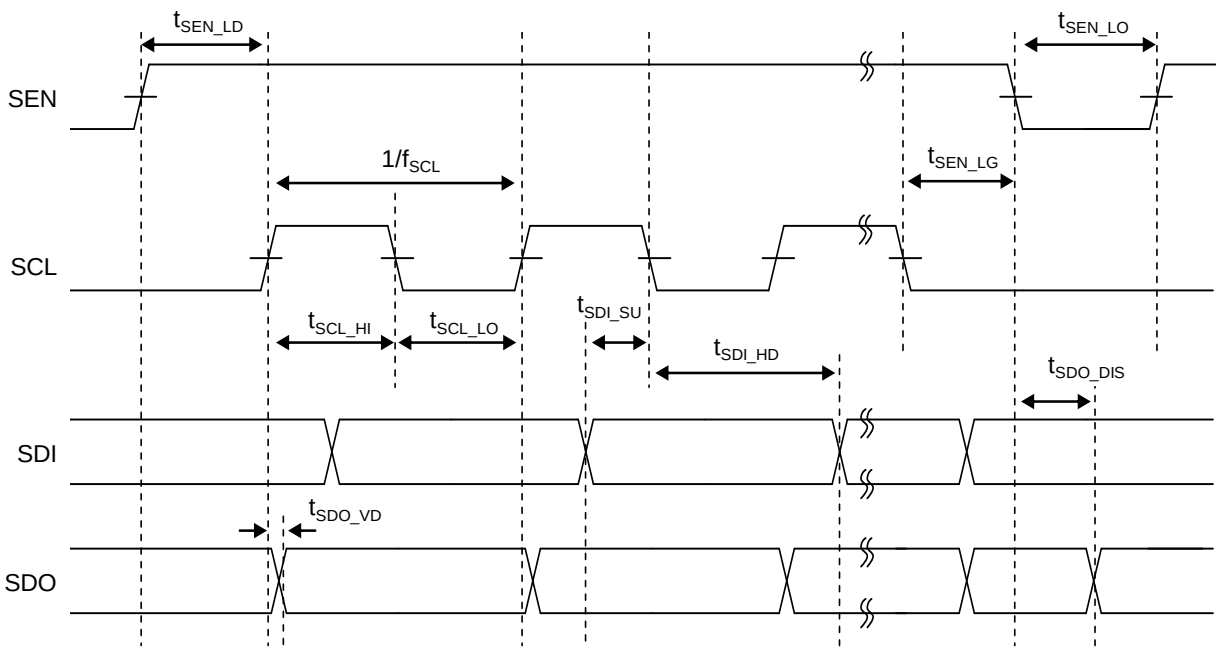
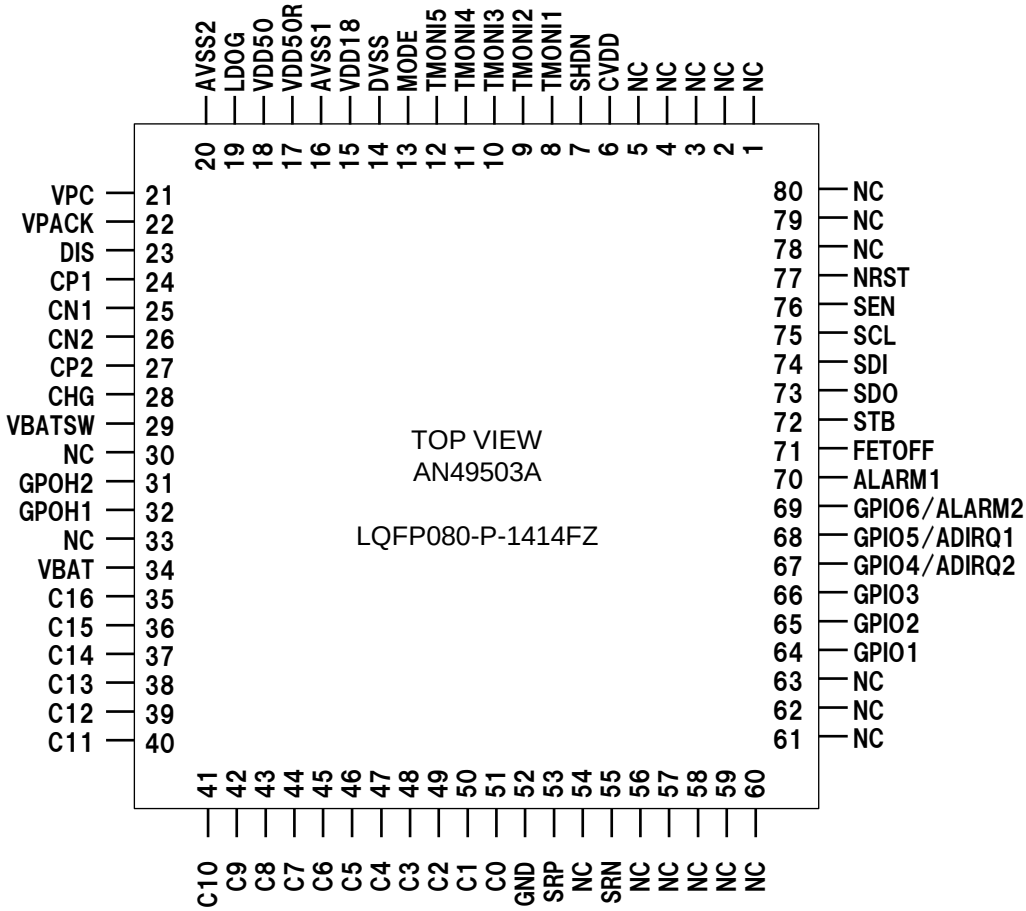


Fig.2.4.1 SPI Timing

1.3 PIN CONFIGURATION



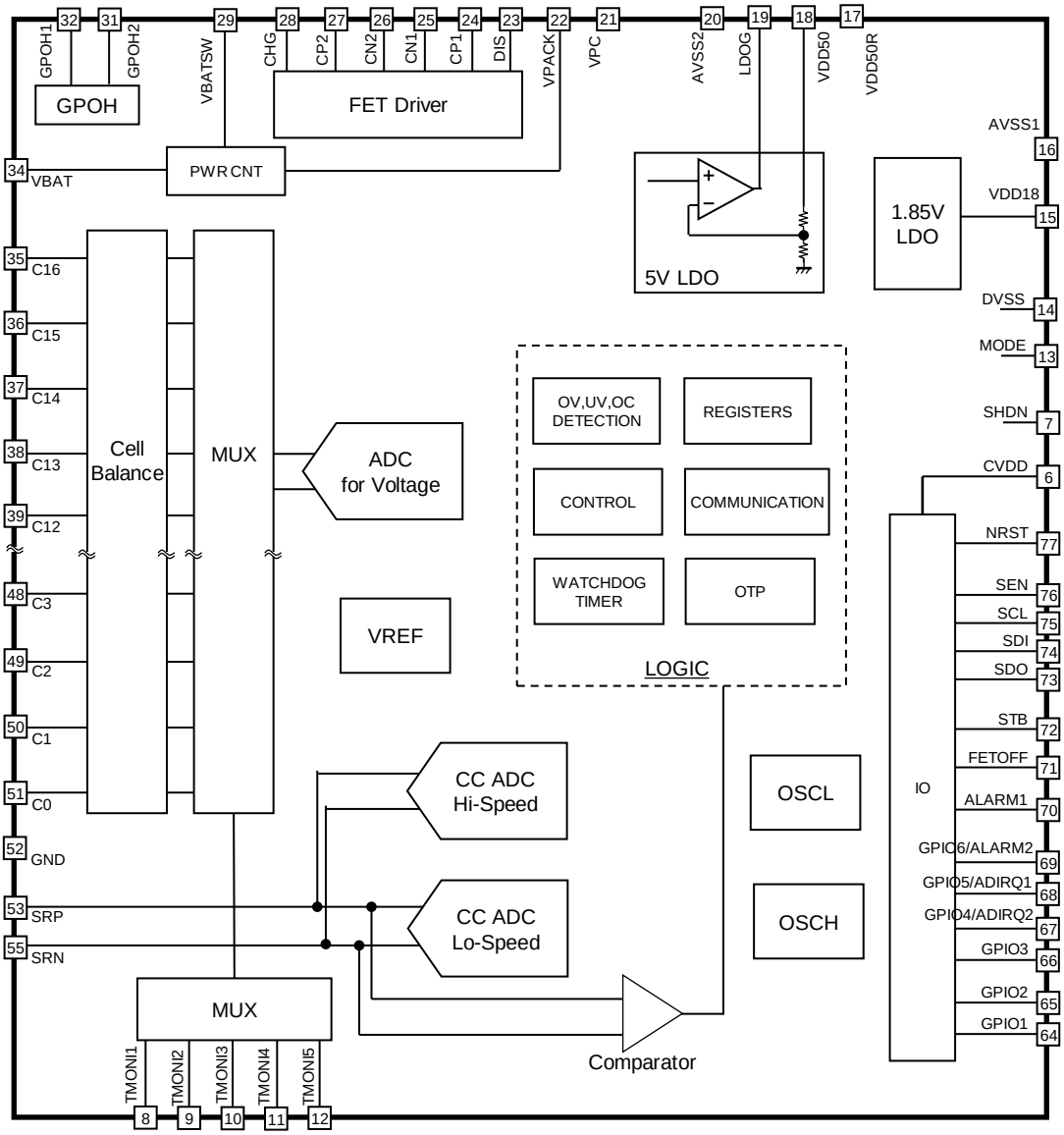
1.4 PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	NC	-	N.C. Pin
2	NC	-	N.C. Pin
3	NC	-	N.C. Pin
4	NC	-	N.C. Pin
5	NC	-	N.C. Pin
6	CVDD	I(Supply)	Digital Voltage Supply
7	SHDN	I	Shutdown Control “L”: Active mode / “H”: Shutdown mode
8	TMONI1	I	Analog Input Pin 1
9	TMONI2	I	Analog Input Pin 2
10	TMONI3	I	Analog Input Pin 3
11	TMONI4	I	Analog Input Pin 4
12	TMONI5	I	Analog Input Pin 5
13	MODE	I	Test Mode Pin for Manufacturer Use Only (Connect to DVSS always)
14	DVSS	GND	Digital Ground
15	VDD18	O	1.85V LDO Output Pin for Internal Use
16	AVSS1	GND	Analog Ground
17	VDD50R	I	(To be connected to VDD50 pin)
18	VDD50	O	5V Output Pin
19	LDOG	O	Gate Control Pin for 5V LDO NMOS Gate Pin
20	AVSS2	GND	Analog Ground
21	VPC	I	Wake Up Signal Pin “H” Wake Up, Please be always fixed to "L" after Wake Up.
22	VPACK	I(Power Supply)	Positive Pin for Battery Pack
23	DIS	O	Discharge NMOSFET Gate Drive Pin
24	CP1	O	Charge Pump Capacitor Pin (Positive Pin for VPACK)
25	CN1	O	Charge Pump Capacitor Pin (Negative Pin for VPACK)
26	CN2	O	Charge Pump Capacitor Pin (Negative Pin for VBAT)
27	CP2	O	Charge Pump Capacitor Pin (Positive Pin for VBAT)
28	CHG	O	Charge NMOSFET Gate Drive Pin
29	VBATSW	O	Power Pin for 5V LDO NMOS Drain Pin
30	NC	-	N.C. Pin

Pin No.	Pin name	Type	Description
31	GPOH2	O	High Voltage General Purpose Output Pin 2 (Open Drain)
32	GPOH1	O	High Voltage General Purpose Output Pin 1 (Open Drain)
33	NC	-	N.C. Pin
34	VBAT	I(Power Supply)	Battery Top Most Pin
35	C16	I	Cell 16 Input Pin (+ve)
36	C15	I	Cell 15 Input Pin (+ve) / Cell 16 Input Pin (-ve)
37	C14	I	Cell 14 Input Pin (+ve) / Cell 15 Input Pin (-ve)
38	C13	I	Cell 13 Input Pin (+ve) / Cell 14 Input Pin (-ve)
39	C12	I	Cell 12 Input Pin (+ve) / Cell 13 Input Pin (-ve)
40	C11	I	Cell 11 Input Pin (+ve) / Cell 12 Input Pin (-ve)
41	C10	I	Cell 10 Input Pin (+ve) / Cell 11 Input Pin (-ve)
42	C9	I	Cell 9 Input Pin (+ve) / Cell 10 Input Pin (-ve)
43	C8	I	Cell 8 Input Pin (+ve) / Cell 9 Input Pin (-ve)
44	C7	I	Cell 7 Input Pin (+ve) / Cell 8 Input Pin (-ve)
45	C6	I	Cell 6 Input Pin (+ve) / Cell 7 Input Pin (-ve)
46	C5	I	Cell 5 Input Pin (+ve) / Cell 6 Input Pin (-ve)
47	C4	I	Cell 4 Input Pin (+ve) / Cell 5 Input Pin (-ve)
48	C3	I	Cell 3 Input Pin (+ve) / Cell 4 Input Pin (-ve)
49	C2	I	Cell 2 Input Pin (+ve) / Cell 3 Input Pin (-ve)
50	C1	I	Cell 1 Input Pin (+ve) / Cell 2 Input Pin (-ve)
51	C0	I	Cell 1 Input Pin (-ve)
52	GND	GND	Analog Ground
53	SRP	I	Shunt Resistor Positive Pin
54	NC	-	N.C. Pin
55	SRN	I	Shunt Resistor Negative Pin
56	NC	-	N.C. Pin
57	NC	-	N.C. Pin
58	NC	-	N.C. Pin
59	NC	-	N.C. Pin
60	NC	-	N.C. Pin

Pin No.	Pin name	Type	Description
61	NC	-	N.C. Pin
62	NC	-	N.C. Pin
63	NC	-	N.C. Pin
64	GPIO1	I/O	General Purpose I/O Pin 1
65	GPIO2	I/O	General Purpose I/O Pin 2
66	GPIO3	I/O	General Purpose I/O Pin 3
67	GPIO4/ADIRQ2	I/O	General Purpose I/O Pin 4 / ADIRQ2 Pin
68	GPIO5/ADIRQ1	I/O	General Purpose I/O Pin 5 / ADIRQ1 Pin
69	GPIO6/ALARM2	I/O	General Purpose I/O Pin 6 / ALARM2 Pin
70	ALARM1	O	ALARM1 Pin
71	FETOFF	I	CHG/DIS FET Control Pin - “L” Normal / “H” FET Forced OFF
72	STB	I	Standby Mode Control Pin - “L” Active mode / “H” Standby mode
73	SDO	O	SPI Interface Pin – Data Out (Open Drain)
74	SDI	I	SPI Interface Pin – Data In
75	SCL	I	SPI Interface Pin – Clock
76	SEN	I	SPI Interface Pin – Enable
77	NRST	O	Power Reset Output Pin（Open Drain）
78	NC	-	N.C. Pin
79	NC	-	N.C. Pin
80	NC	-	N.C. Pin

1.5 FUNCTIONAL BLOCK DIAGRAM



Chapter 2 Battery Connection

The minimum required VBAT pin voltage is 12.5V to guarantee normal operation.

For application using less than 16 cells, all unused cells Cn pins should be connected as shown in figure below, user shall use cells connect to C16, C15, C1 and C2 pins first and follow by battery from lower cell.

Battery cells connection sequence:
Connect the GND pin followed by VBAT pin. After that, it should be connected from the lower cell in turn.
GND -> VBAT -> Cell between C0-C1 -> Cell between C1-C2 -> ▪▪▪

Figures below show example connection for 15 battery cells and 4 battery cells, please note, it is possible to be connected for 4 battery cells only when the minimum VBAT is higher then 12.5V.

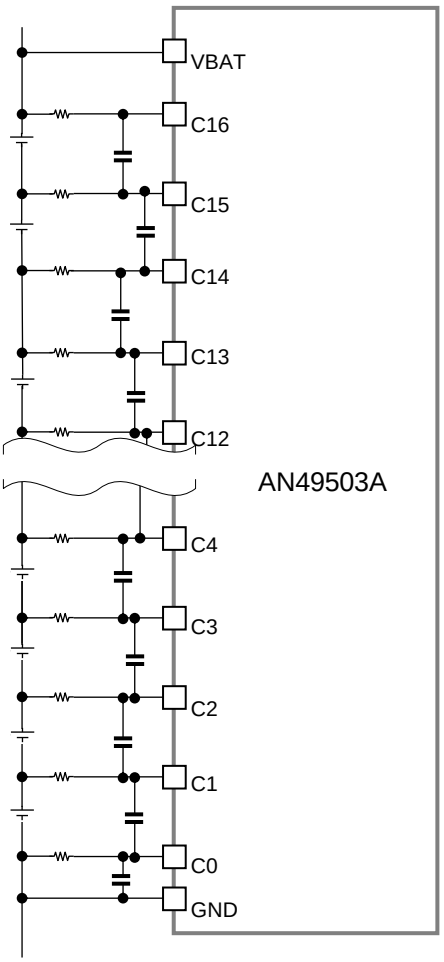


Fig.2.1.1 AN49503A Cell Connection example with 15 cell connected

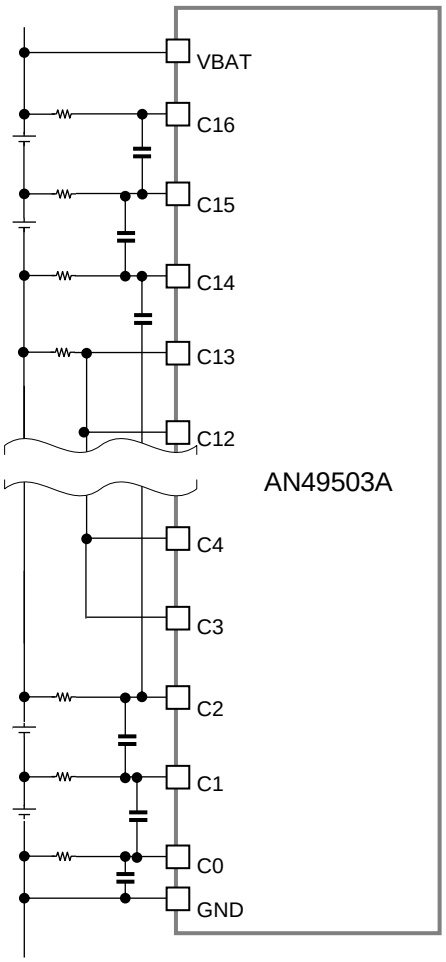


Fig.2.1.2 AN49503A Cell Connection Example with only 4 cell connected

Chapter 3 Operation Mode

3.1 Overview of Operation Mode

AN49503A supports Active Mode, Standby Mode and Shutdown Mode as operation mode.
The operating mode can be determined by *ST_ACT* flag, *ST_STBY* flag, *ST_SDWN* flag (MODE_STAT:bp2-0).

3.1.1 Active Mode

In Active Mode only, voltage and high speed (HS) current measurement can be performed. Low speed current measurement can be performed in both Active Mode as well as Standby Mode.

From shut down mode, VPACK or VBAT pins voltage higher than 12.5V and VPC pin at “H” condition, AN49503A will enter Active Mode. After wake up, SDO pin will change from “L” to “H” indicating the SPI communication is ready. After wake up, VPC pin must be fixed to "L".
When watchdog timer is set to enabled, AN49503A will shutdown when no communication between MCU and the IC is made in set duration (initial value:1 minute) and VPC pin is “L”. For watchdog timer, refer to Chapter 13.6.

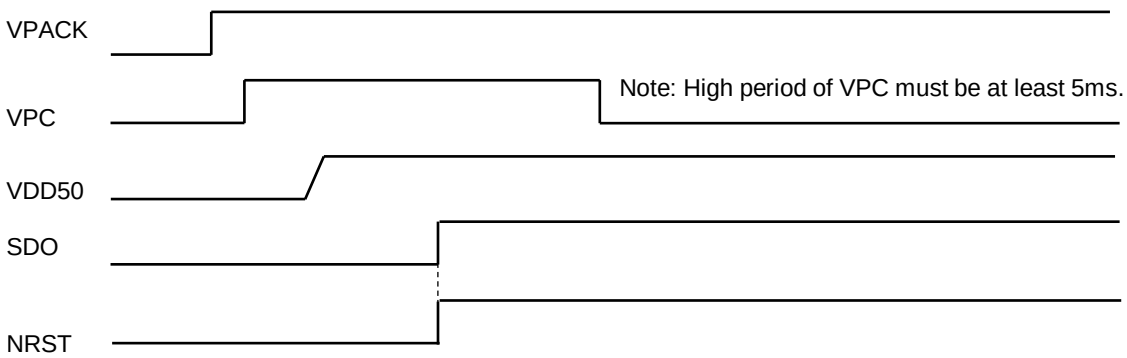


Fig. 3.1.1 Wake up waveform

3.1.2 Standby Mode

By entering Standby Mode, it can reduce current consumption. Voltage and high speed (HS) current measurement will not be performed. Low speed current measurement, however, can be set to perform. From Active Mode, IC enter Standby Mode by setting STB pin to “H” (at least1.3ms). When STB pin is set to “L”, AN49503A will resume to Active Mode.

At Standby Mode, by setting *LP50EN* flag（SPICTL:bp4）to “1”, 5VLDO could be set to operate at Low Power Mode which reduce current consumption. For 5VLDO operation, refer to Chapter 4.

SPI communication is available in the initial state of Standby mode. By setting *COM_STP* flag（SPICTL:bp0）to “1”, SPI communication is turned OFF for further power reduction, *COM_STP* flag (SPICTL: bp0) will be auto reset to “0”.
To resume SPI communication, input “H” to SEN pin for more than 1ms. After a further 1ms wait, register access will be available.

At Standby Mode, it is possible to automatically switch back to Active Mode and measure the cell voltage. When AN49503A enters Standby Mode with OV/UV detection enabled and *STB_MONEN* flag（PWR_CTL:bp9）and *ADC_CONT* flag（PWR_CTL:bp8）set to 1, if no SPI communication is done within 1s, it will automatically switch back to Active Mode for cell voltage measurement and it will switch back to Standby Mode automatically when this operation is done.

3.1.3 Shutdown Mode

All circuit stopped functioning, the current consumption is minimized at Shutdown Mode.

The IC can be shutdown by setting SHDN pin to “H” (at least 1ms.) or by setting *MSET_SHDN* flag（PWR_CTL:bp7) to “1” with VPC pin at “L”.

When Watchdog Timer, Thermal Shutdown or VDD50 UVLO detected, AN49503A enter to Shutdown Mode automatically while VPC pin is "L“.

Table.3.1.1 Condition of moving to Shutdown Mode (VPC pin “L”)

Mode	SHDN pin ”H”	*MSET_SHDN* flag "1"	Watchdog Timer	Thermal Shutdown	VDD50 UVLO
Active Mode	Available	Available	Available	Available	Available
Standby Mode Communication ON	Available	Available	Available	Available	Available
Standby Mode Communication OFF	Available	Not available	Not available	Available	Available

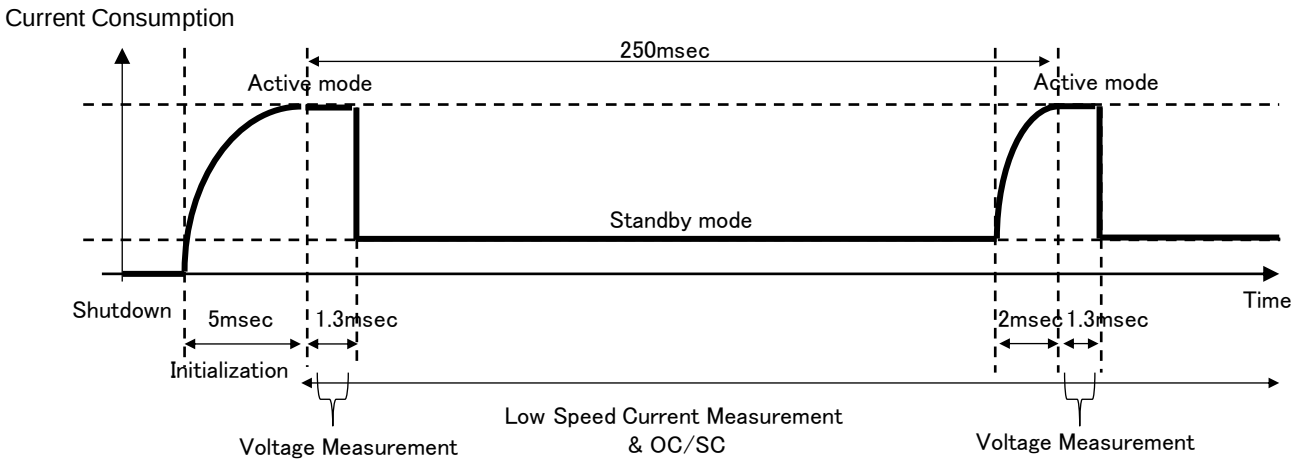
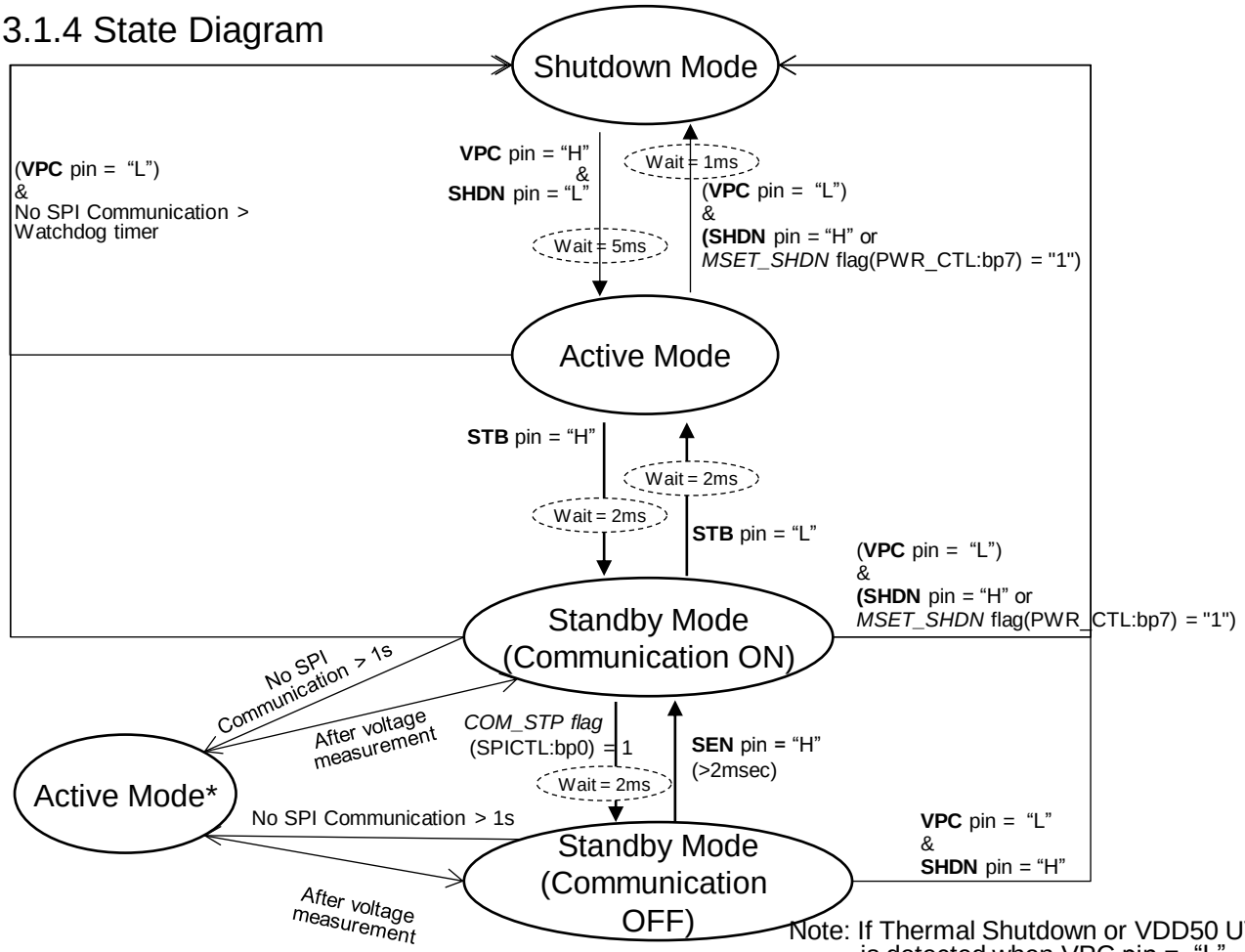


Fig. 3.1.2 Example of operation on intermittent operation (Active Mode -> Standby Mode and repeating)

- For AN49503A, it is possible to reduce the current consumption by operating the IC in intermittent operation, MCU control the IC to operate switching form Active Mode to Standby Mode and repeating.
- It requires minimum of 5ms for initialization wake up from Shutdown Mode before IC start voltage measurement.
- It requires minimum of 2ms for initialization when return to Active Mode from Standby mode before start voltage measurement.

3.1.4 State Diagram



Note: If Thermal Shutdown or VDD50 UVLO is detected when VPC pin = "L", the state will be changed to the Shutdown Mode no matter whichever state it is.

Fig.3.1. 3 State Diagram

Table.3.1.2 Operation Mode Summary

Mode	5VLDO drivability	Cell Voltage Measurement	Coulomb Counter (CC)	DIS, CHG FET ON/OFF	Cell Balance	SPI I/F	ALARM
Active	50mA	ON	ON/OFF	ON/OFF	ON/OFF*2	ON	ON/OFF (OV/UV/OC/SC)
Standby	5mA/ 50mA	OFF	ON/OFF	ON/OFF *1	ON/OFF	ON/OFF	ON/OFF (OC/SC)
Shutdown	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Note: The LDO drivability, coulomb counter (CC), FET control, cell balance control can be set by respective register.

*1 DIS and CHG FET setting is kept when operation mode change from Active Mode to Standby Mode, FET control is available in Standby Mode (Communication ON) except when register FDRV_STBY = "1". During Standby Mode (Communication OFF), it can only be turned OFF by FETOFF pin.
*2 Cell balance can be turned ON during Active Mode, however it could cause wrong abnormal detection, user shall not enable UV/OV detection at the same time.

3.2 Control Registers

3.2.1 Operation Mode control register

Table.3.2.1 shows the registers that control operation mode.

Table.3.2.1 Operation Mode Control Register

Register	Address	Function	Page
PWR_CTL	0x01	Operation Mode・FET Driver Operation Control register	99
SPICTL	0x18	Communication・VDD50 LDO Power Mode Control register	116
MODE_STAT	0x22	Operation Mode Status register	123

Chapter 4 5V LDO

4.1 5V LDO

AN49503A has built-in with a 5V LDO controller, with a external NMOS, it generate a 5V regulated output which can drive up to 50mA load current.

At Active Mode, the LDO operates at Normal Mode which can drive load up to 50mA while at Standby Mode, it could be set to operate at Low Power Mode which drive up to 5mA with *LP50EN* flag (SPICTL:bp4) set to “1”. This flag has no effect at Active Mode, it only take effect when it enters Standby Mode.

It requires minimum of 2ms to stabilize circuit when LDO MODE is switching.

When detecting the VDD50 UVLO, it will be switched to the Shutdown mode. (if VPC pin is "L“)

Table.4.1.1 5V LDO

Function Mode	STB Pin	*LP50EN* flag (SPICTL:bp4)	LDO MODE	Drive load
Active Mode	L	0/1	Normal	50mA
Standby Mode	H	0	Normal	50mA
Standby Mode	H	1	Low Power	5mA

4.2 Control Registers

4.2.1 Registers

Table.4.2.1 shows the registers that control 5V LDO.

Table.4.2.1 5V LDO Control Registers

Register	Address	Function	Page
SPICTL	0x18	Communication・VDD50 LDO Power Mode Control register	116

Chapter 5 CHG / DIS FET Control

5.1 Description of CHG/DIS FET Control

AN49503A has built-in charge pump circuit to drive high side NMOS FET switches. The two NMOS FETs are controlled by connecting CHG and DIS pins to gate pin of the NMOS FETs as shown, this control can be done in both Active and Standby Mode.
Under ALARM condition, the NMOS FETs could be set to be response to the ALARM condition.
For more information, refer to Chapter 11 Monitoring and Protection.

The turning ON of NMOS FETs are controlled by setting flags *FDRV_CHG_FET* (PWR_CTL : bp1) and *FDRV_DIS_FET* (PWR_CTL : bp0) to 1 respectively. When it is turned ON, the VGS voltage of NMOS FET is 11V typically. The VGS voltage can be set by flag FDRV_LEVEL (FDRV_CTL : bp4-2).

While the NMOS FETs can be turned OFF by setting the flags *FDRV_CHG_FET* (PWR_CTL : bp1) and *FDRV_DIS_FET* (PWR_CTL : bp0) to “0”, it can also be turned OFF through setting FETOFF pin to “H”.

During Standby Mode, with flag *FDRV_STBY* (FDRV_CTL : bp8) set to “1”, internal circuit of the charge pump circuit will operate intermittently for further power reduction while no change in FET ON/OFF state. When user wants to change FET state, user shall first change register *FDRV_STBY* to “0” before changing *FDRV_CHG_FET* and *FDRV_DIS_FET* setting.

If the load capacitance of CHG pin and DIS pin shown in Fig.5.1.1 is 47nF, rise time of the control signal of the external MOSFET is 800us (Typ.) and fall time is 500us (Typ.).

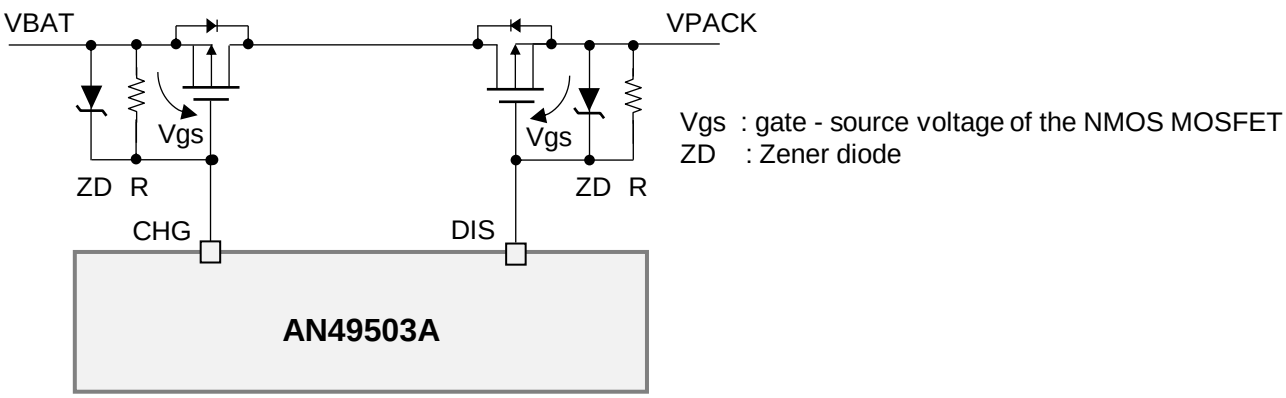


Fig.5.1.1 CHG / DIS FET circuit

5.2 Control Registers

5.2.1 CHG/DIS FET Control Registers

Table.5.2.1 shows the flags that control CHG / DIS FET.

Table.5.2.1 CHG/DIS FET Control Registers

Register	Address	Function	Page
PWR_CTL	0x01	CHG / DIS FET ON/OFF control register	99
FDRV_CTL	0x03	External FET drive voltage control register	101

Chapter 6 General Purpose High Voltage Output (GPOH1/2)

6.1 Description of General Purpose High Voltage Output

AN49503A has built-in with two high voltage open drain GPOH pins (GPOH1/GPOH2) . The two pins can sustain voltage up to VBAT level. When used, pull up resistors of more than 100kΩ are needed.

These pins could be used to drive high side PMOS FET and set to response to ALARM condition.
Refer to Chapter 11 Monitoring and Protection.

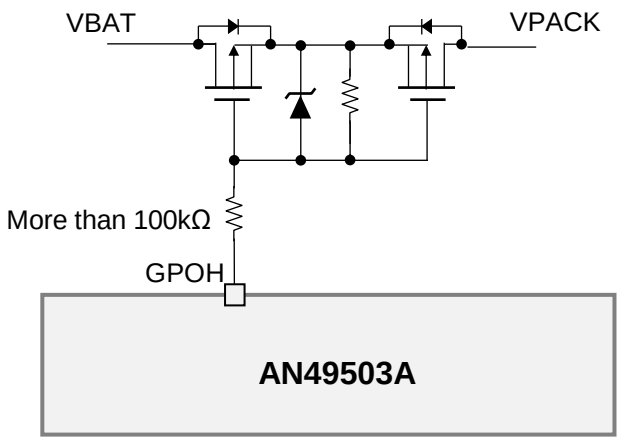


Fig.6.1.1 Circuit example using GPOH1/2

6.2 Control Registers

6.2.1 Registers

Table.6.2.1 shows the registers that control GPOH pins.

Table.6.2.1 GPOH Control Registers

Register	Address	Function	Page
GPOH_CTL	0x1B	GPOH control register	119
FDRVSTAT	0x55	FET Driver status register	133

6.3 Operation at the time of ALARM occurrence

AN49503A is possible to control the GPOH1 / 2 pins in accordance with the state of the ALARM.
Refer to Chapter 11 Monitoring and Protection.

Table.6.3.1 GPOH Pins control at the time of the alarm (when flag *GPOH_FET* = “1”)

	Detecting abnormality	GPOH1	GPOH2
Abnormal	OV/UV OCC/OCD SCD	Control by flag *GPOH1_ALM_ST*	Control by flag *GPOH2_ALM_ST*
Normal	-	Control by flag *GPOH1_EN*	Control by flag *GPOH2_EN*

6.4 GPOH state flag

The status of GPOH1/2 can be checked by a state flag.

Table.6.4.1 GPOH Pin state flag

GPOH	State flag
GPOH1	*GPOH1_ST* flag (FDRVSTAT : bp0)
GPOH2	*GPOH2_ST* flag (FDRVSTAT : bp1)

Chapter 7 General Purpose Input Output (GPIO1~6)

7.1 Description of General Purpose Input Output

AN49503A has built-in with six low voltage (CVDD) GPIO pins (GPIO1~6) .
Power of GPIO is supplied from CVDD.
Refer table below for possible configuration for each pin.

Table.7.1.1 GPIO Pins Configuration

Pin	Pin Configuration	Internal Pull Down Resistor	Other Function
GPIO1	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	Analog Input/ GPOH1Data Output
GPIO2	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	Analog Input/ GPOH2Data Output
GPIO3	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	High Speed Oscillator Clock Divided Output
GPIO4	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	ADIRQ2/ Low Speed Oscillator Clock Divided Output
GPIO5	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	ADIRQ1/ Active mode state Output
GPIO6	Input / Output (Push pull or N-ch open drain) set by register	Pull Down Resistor set by register	ALARM2/ Standby mode state Output

Note:
When GPIO pin is configured as output, it shall not be set with pull down resistor. (ie. flag *GPIO[n]_PD* = “1”)
When GPIO pin is configured as Analog Input , flag *GPIO[n]_IE* shall be set to “0”.
By outputting GPOH data, GPIO1/GPIO2 can be used to drive a low-side NMOS FET (responding to the ALARM condition).

7.2 Control Registers

7.2.1 Registers

Table.7.2.1 shows the registers that control GPIO.

Table.7.2.1 GPIO Control Registers

Register	Address	Function	Page
GPIO_CTL1	0x0C	GPIO control register 1	109
GPIO_CTL2	0x0D	GPIO control register 2	109
GPIO_CTL3	0x0E	GPIO control register 3	110
GPIO_CTL4	0x0F	GPIO control register 4	109
GPIOSEL	0x17	GPIO output control register	115

7.3 GPIO Pins Input and Output Configuration

7.3.1 GPIO Pins Input and Output Configuration

Each GPIO Pins can be set as the various configurations by control register.

Table.7.3.1 GPIO pin setting Register

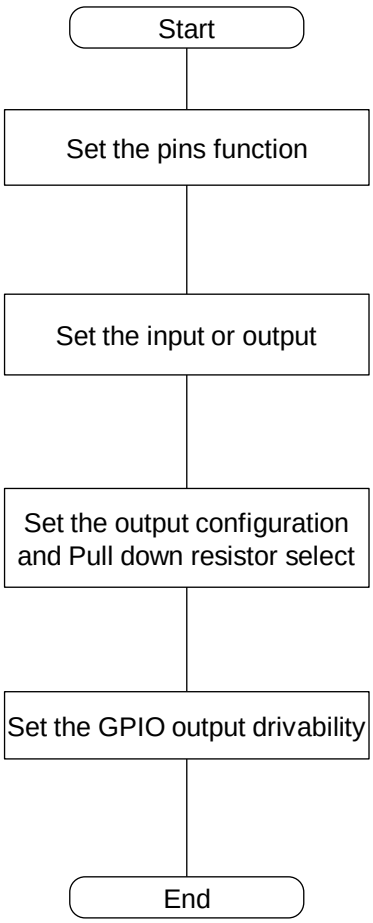
Flag	Pin Configuration	Description
GPIO*_NOE	Output Enable	1:Disabled（default）
GPIO*_IE	Input Enable	0:Disable(default)
GPIO*_OD	Output Configuration	0:Push Pull(default)
GPIO*_PD	Pull-Down Register	0:No（default）
ST_GPIO*	Input Data	0:LO (VSS) （default）
GPIO*_OUT	Output Data	0:LO （default）
GPIO*_CHDRV	Output Drivability	0:2mA （default）
GPIO*SEL[1:0]	Function	—
OSC2_DIV	Low Speed Clock Divider (when output from GPIO4)	10:1/64 (4.096kHz) (Default)

Note:
When GPIO1/2 pin is configured as GPOH1/2 , GPIO1_OD and GPIO2_OD should be set to “0”.
It is required to change other registers accordingly when setting GPIO[n]SEL.
e.g. GPIO6 is set to ALARM2,
User shall set:
GPIO6SEL : 01 (ALARM 2)
GPIO6_NOE: 0 (Output enable)
GPIO6_IE: 0 (Input disable)
And set GPIO6_CHDRV, GPIO6_PD and GPIO6_OD accordingly depend on need.

When GPIO pin is configured as output , GPIO[n]_PD shall not be set to “1” at the same time.
When GPIO pin is configured as Analog Input , GPIO[n]_IE shall not be set to “1” at the same time.

7.3.2 Setup Example

GPIO Pins use the following settings
GPIO1 : Analog Input
GPIO2 : GPIO2 Pin , Output Configuration Push Pull , Output Drivability 2mA
GPIO3 : GPIO3 Pin , Output Configuration N-ch Open Drain , Output Drivability 4mA
GPIO4 : Low Speed Oscillator Clock Divided Output , Clock Divider 8.192kHz
GPIO5 : ADIRQ1
GPIO6 : GPIO3 Pin , Input , Pull down resistor ON
with a description of each step is shown below.



・Set the Pins function
Set the GPIO*SEL[1:0] flag of GPIOSEL register.
GPIO6SEL[1:0] = 00、GPIO5SEL[1:0] = 01、GPIO4SEL[1:0] = 11
GPIO3SEL[1:0] = 00、GPIO2SEL[1:0] = 00、GPIO1SEL[1:0] = 10
OSC2_DIV flag(GPIOSEL:bp13-12) set to “01” to 8.192 kHz.

・Set the input or output
GPIO*_NOE flag(GPIO_CTL1:bp13-8) set to ”100001” to GPIO2-5 output.
Set the GPIO*_IE flag(GPIO_CTL1:bp5-0) set to ”100000” to GPIO1 input.

・Set the Output configuration and Pull down resistor select
Set the GPIO*_OD flag(GPIO_CTL2:bp13-8) set to ”000100” to GPIO3 N-ch open drain.
Set the GPIO*_PD flag(GPIO_CTL2:bp5-0) set to ”100000” to GPIO6 pull down resistor ON.

・Set the GPIO Output drivability
Set the GPIO*_CHDRV flag(GPIO_CTL4:bp5-0) set to ”000100” to GPIO3 output drivability 4mA.

※ When the R/WL register control, please implement the LOCK register settings.

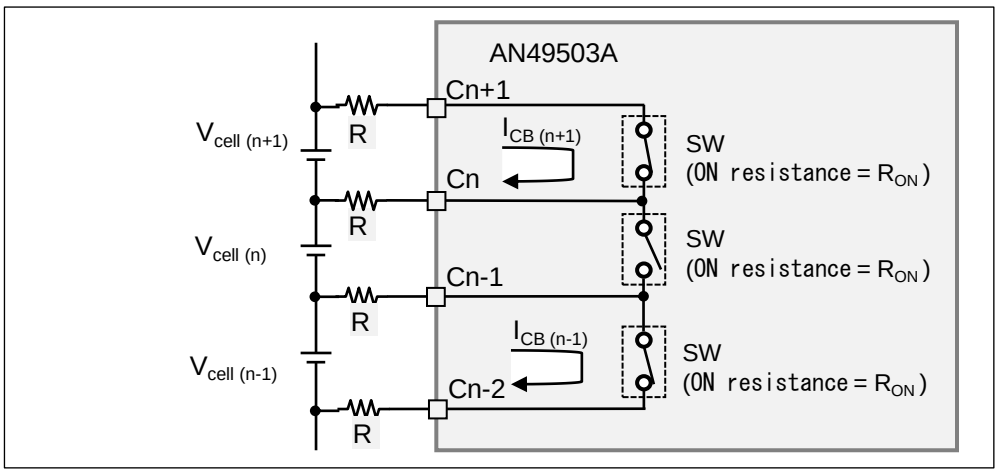
Chapter 8 Cell Balance

8.1 Description of Cell Balance

AN49503A has Cell balance function. This function can be turned ON during Active Mode, and Standby Mode , and can be done by using an external MOSFET or the built-in MOSFET.

Please note the following points.
・When using cell balance, user shall set 5V LDO to normal operation.(See Chapter 4 5V LDO)
・Adjacent cell (Vcell (n+1) and Vcell(n) shown in Fig.8.1.1) should not be operated in cell balance at the same time.
・When cell balance is turned ON, the OV/UV detection will not operate correctly. Therefore, user shall turn OFF OV/UV detection when using cell balance.
(See Chapter 11 Monitoring and Protection)
・In using the cell balance function , the power consumption of the IC increase. Then user shall do the thermal design with enough margin for the actual usage. Please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions.
(See 1.4.2 POWER DISSIPATION RATING)

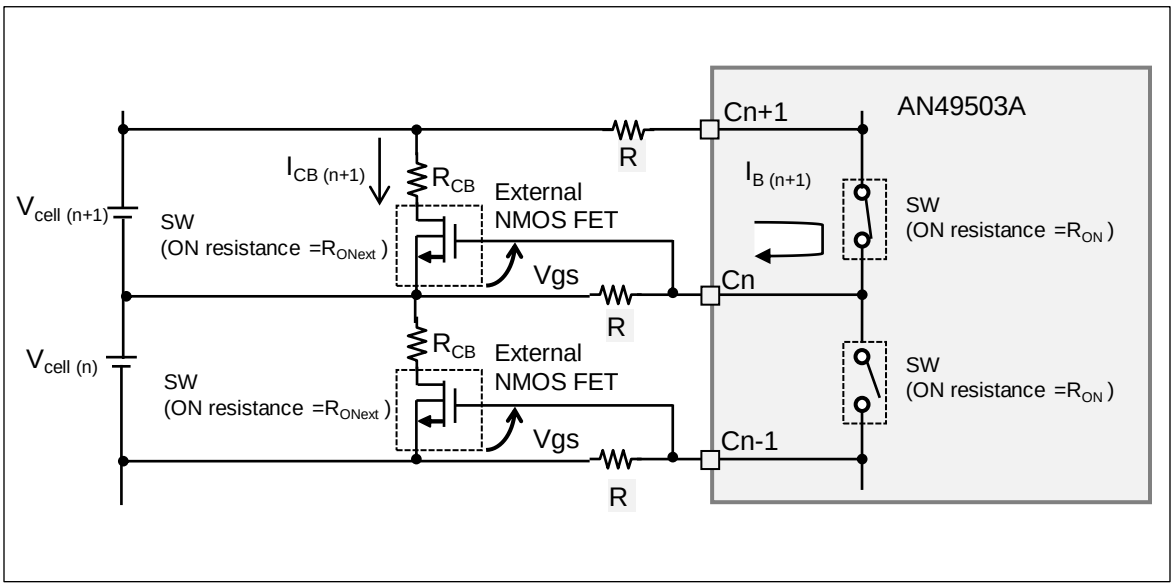
[How to design cell balance with built-in MOSFET (See Fig.8.1.1)]
・ Cell balance can be done by turning ON the SW made of built-in MOSFET.
・ ON resistance of built-in MOSFET (SW) is Max.20Ω.
・ When only one cell is to be in cell balance , user shall set the external resistor (R) value so that current flowing through the built-in MOSFET ($I_{CB\,(n)}$) does not exceed 50mA.
・ When cell balance is to be performed for multi-cells simultaneously, user shall set the external resistor (R) value so that each current flowing through the built-in MOSFET ($I_{CB\,(n+1)}$, $I_{CB\,(n-1)}$) does not exceed 25mA. If more discharge current flowing through the built-in MOSFET is required for each case (one cell: >50mA, multi-cells: >25mA), it is recommended to use external FET for cell balance shown in Fig.8.1.2 .



SW: SW made of built-in MOSFET R_{ON}: ON resistance of built-in MOSFET(Max.20Ω)
$I_{CB(n+1)} = V_{cell(n+1)} / (2R + R_{ON})$ $I_{CB(n-1)} = V_{cell(n-1)} / (2R + R_{ON})$
Fig.8.1.1 Circuit example in using the built-in MOSFET

[How to design cell balance with external NMOS FET (See Fig.8.1.2)]

- Cell balance can be done by turning ON the external NMOS FET with the Vgs , the Vgs is generated by the discharge current ($I_{B\,(n)}$) when the built-in MOSFET SW is ON and the external resistor (R) .
- ON resistance of built-in MOSFET (SW) is Max.20Ω.
- When only one cell is to be in cell balance , user shall set the external resistor (R) value so that current flowing through the built-in MOSFET ($I_{CB\,(n)}$) does not exceed 50mA.
- When cell balance is to be performed for multi-cells simultaneously, user shall set the external resistor (R) value so that each current flowing through the built-in MOSFET ($I_{CB\,(n+1)}$, $I_{CB\,(n-1)}$) does not exceed 25mA.
- Cell balance current in the external MOSFET ($I_{CB\,(n)}$) can be obtained by the cell voltage ($V_{cell\,(n)}$) and the resistance value (R_{CB} + R_{ONext})



SW : SW made of built-in MOSFET
R_{ON} : ON resistance of built-in MOSFET(Max.20Ω)
Vgs : Gate – Source Voltage of external NMOS FET
R_{ONext} : ON resistance of external NMOS FET

$I_{B(n+1)} = V_{cell(n+1)} / (2R + R_{ON})$
$Vgs = R \times I_{B(n+1)}$
$= V_{cell(n+1)} / 2 \quad (R_{ON} \ll R)$
$I_{CB(n+1)} = V_{cell(n+1)} / (R_{CB} + R_{ONext})$

Fig.8.1.2 Circuit example in using the external MOSFET

8.2 Control Registers

8.2.1 Registers

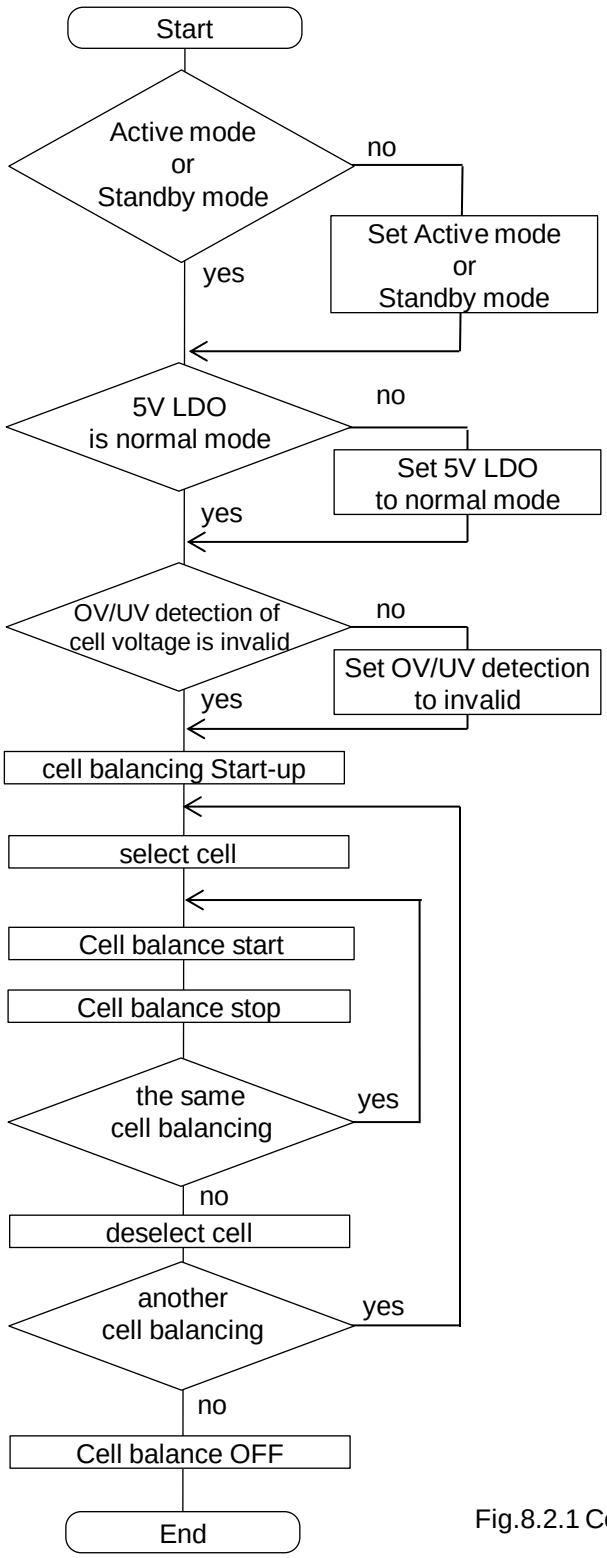
Table.8.2.1 shows the registers that control Cell Balance.

Table.8.2.1 Cell Balance Control Registers

Register	Address	Function	Page
OP_MODE	0x0A	Cell Balance ON/OFF control register	107
CB_CTL	0x14	Cell Balance Operation control register	113
CBSEL	0x15	Select Cell control register	114
CBSTAT	0x56	Cell balance operation status register	134

8.2.2 Cell Balance Flow

It shows the setting procedure for using cell balance function below.



■Prior confirmation
Set to Active mode or Standby mode, and set the 5V LDO to normal mode.
Disable OV/UV detection of cell voltage.

■Cell balancing Start-up
Set *CB_PD* flag (CB_CTL:bp0) to “0” to turn ON cell balance circuit.

■Select cell
Set *DI_CBSEL* flag (CBSEL:bp15-0) to “1” for cell to be cell balanced.
DI_CBSELn is corresponding to VCELL (n)
(e.g. if *DI_CBSEL[1]* is selected, $V_{CELL\ (1)}$ (between C1-C0) is cell balanced.)
Please do not select adjacent cells at the same time.

■Cell balance start
Set *CB_SET* flag (OP_MODE:bp8) to ”1” to start cell balancing operation.

■ Cell balance stop
Set *CB_SET* flag (OP_MODE:bp8) to “0” to stop cell balancing operation.

■Deselect cell
Set *DI_CBSEL* flag (CBSEL:bp15-0) to “0” to deselect cell.

■another cell balancing
When doing another cell balancing ,repeat step from “select cell “ to “deselect cell”.

■Cell balance OFF
Set *CB_PD* flag (CB_CTL:bp0) to “1” to turn OFF cell balance circuit.

※ Accessibility of some register flags above are R/WL, LOCK register needed to be set accordingly.

Fig.8.2.1 Cell Balance Flow

Chapter 9 Voltage Measurement

9.1.1 Voltage Measurement

Several voltage data is measured by the built-in 14 bits ADC only in Active Mode*. Figure.9.1.1 below shows the sequence of data measured by ADC. The voltage measurement is done in the following sequence, GPIO1 / 2 pin, VPACK, TMONI1~5 pin, VDD50, Cell Voltage.

The measurement cycle time, including the Reset period, is about 1.3ms (50us / cell × 26).

The voltage measurement can be set to continuous measurement or 1shot measurement with respective registers which will be explained in this chapter.

* Including Active Mode during Standby Mode when no SPI communication more than 1s at certain registers setting as explained in Chapter 3.1.2

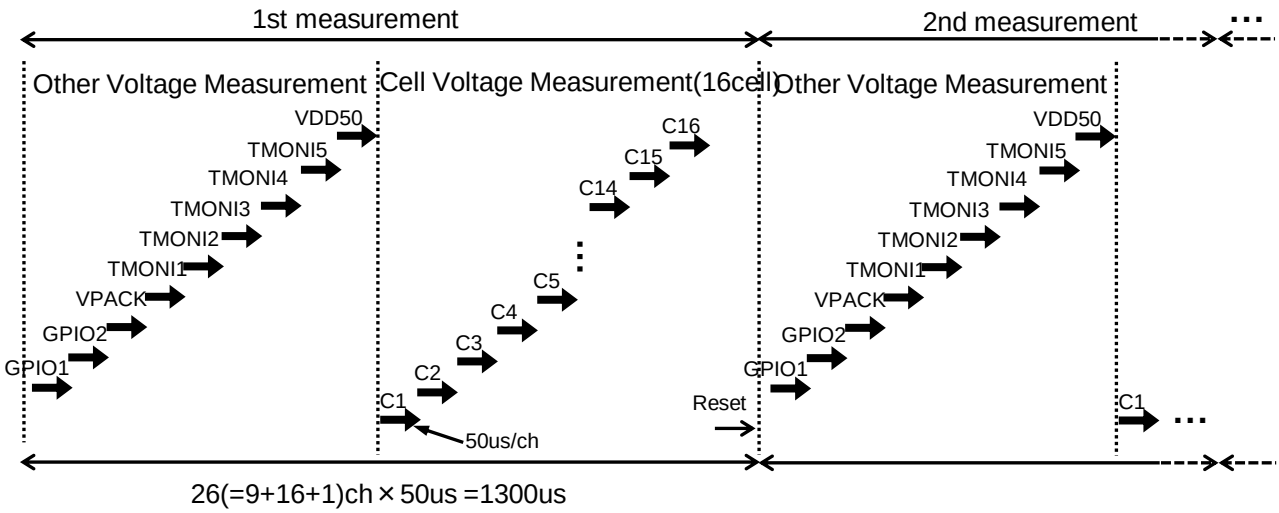


Fig.9.1.1 measurement sequence（continuous measurement)

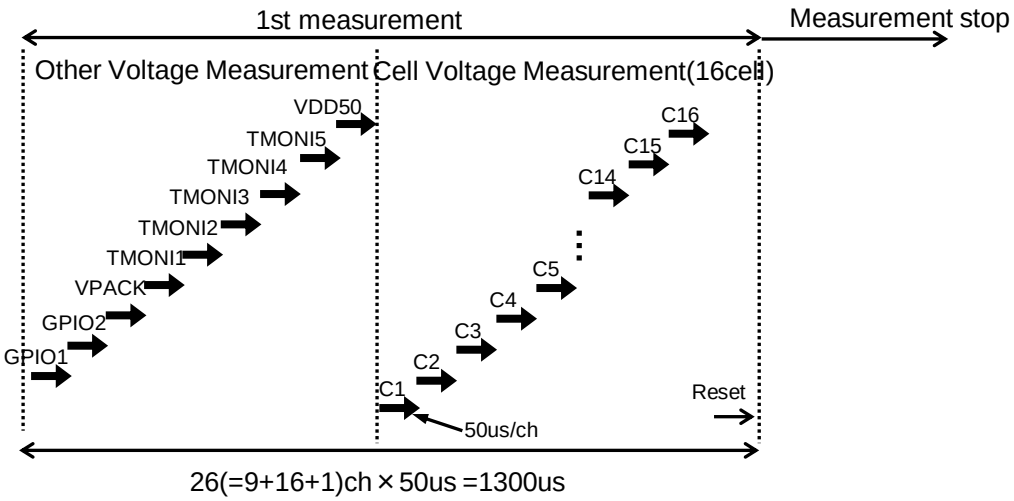


Fig.9.1.2 measurement sequence（1shot measurement)

The block diagram of the ADC for voltage measurement is shown in Fig.9.1.3. Cell voltage measurement is measured the voltage of both cell ends (in the case of Cell16, C16 and C15),
TMONI pin, GPIO pin, VPACK voltage and VDD50 voltage measurement is measured the voltage between the pin and GND.

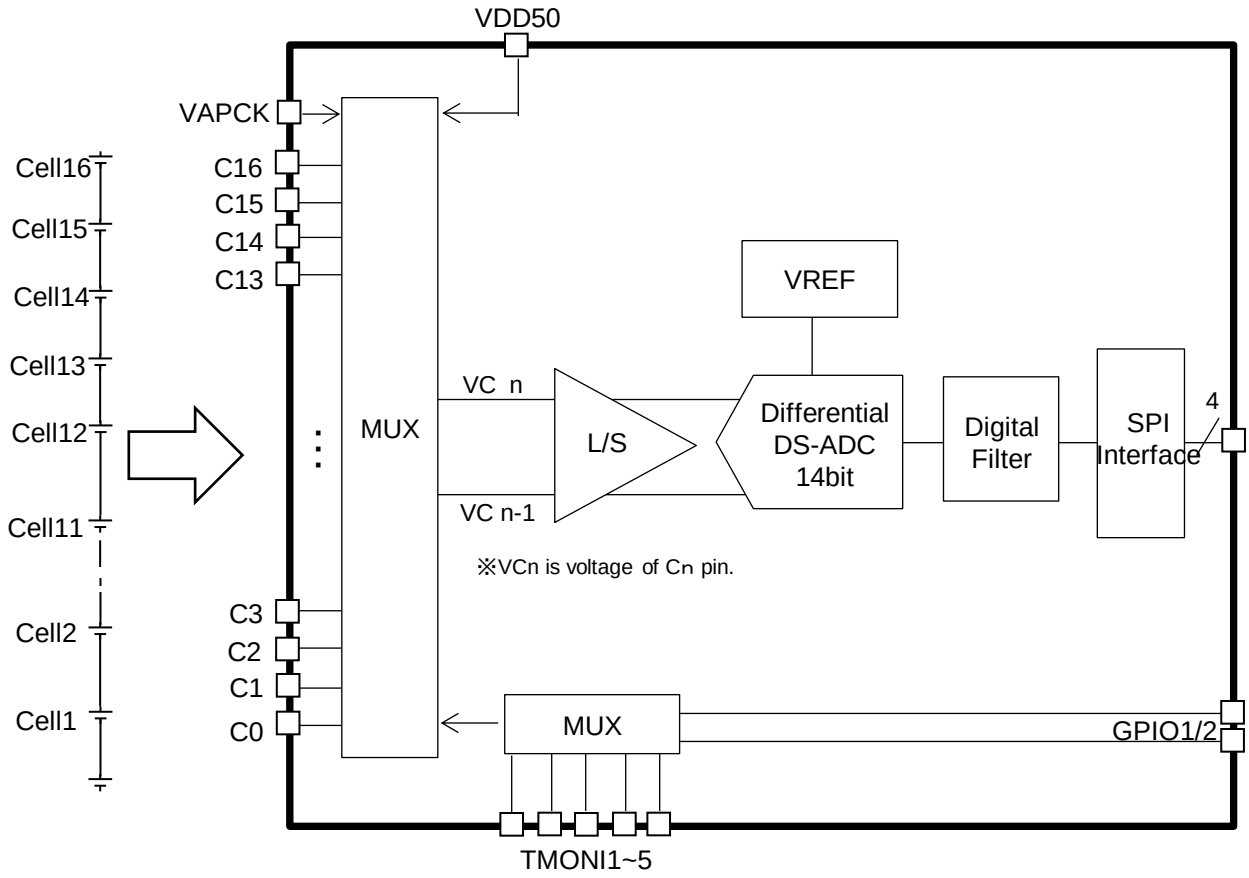


Fig.9.1.3 block diagram of the ADC for voltage measurement

9.1.2 Voltage Measurement and Timing

Voltage measurement is operated during active mode only. There are two measurement operation, continuous measurement (when ADC_CONT flag (PWR_CTL:bp8) = “1”) and 1shot operation (when ADC_CONT flag (PWR_CTL:bp8) = “0”). During continuous measurement, the voltage measurement cycle is repeating. While 1shot measurement is done once when ADC_TRG flag (OP_MODE:bp4) is set to “1”. This flag is automatically cleared to “0” after measurement.

When each measurement cycle is completed, ADIRQ1 pin will be triggered to “H” and register VAD_DONE flag (STAT:bp0) will be set to “1”. The measured data has to be latched to data register 0x33~0x4B by setting ADV_LATCH flag (OP_MODE:bp0) to “1”, ADIRQ1 pin will be reset to “L” and ADV_LATCH flag (OP_MODE:bp0) become “0” after completion. VAD_DONE flag (STAT:bp0) is cleared by write “1” to it.

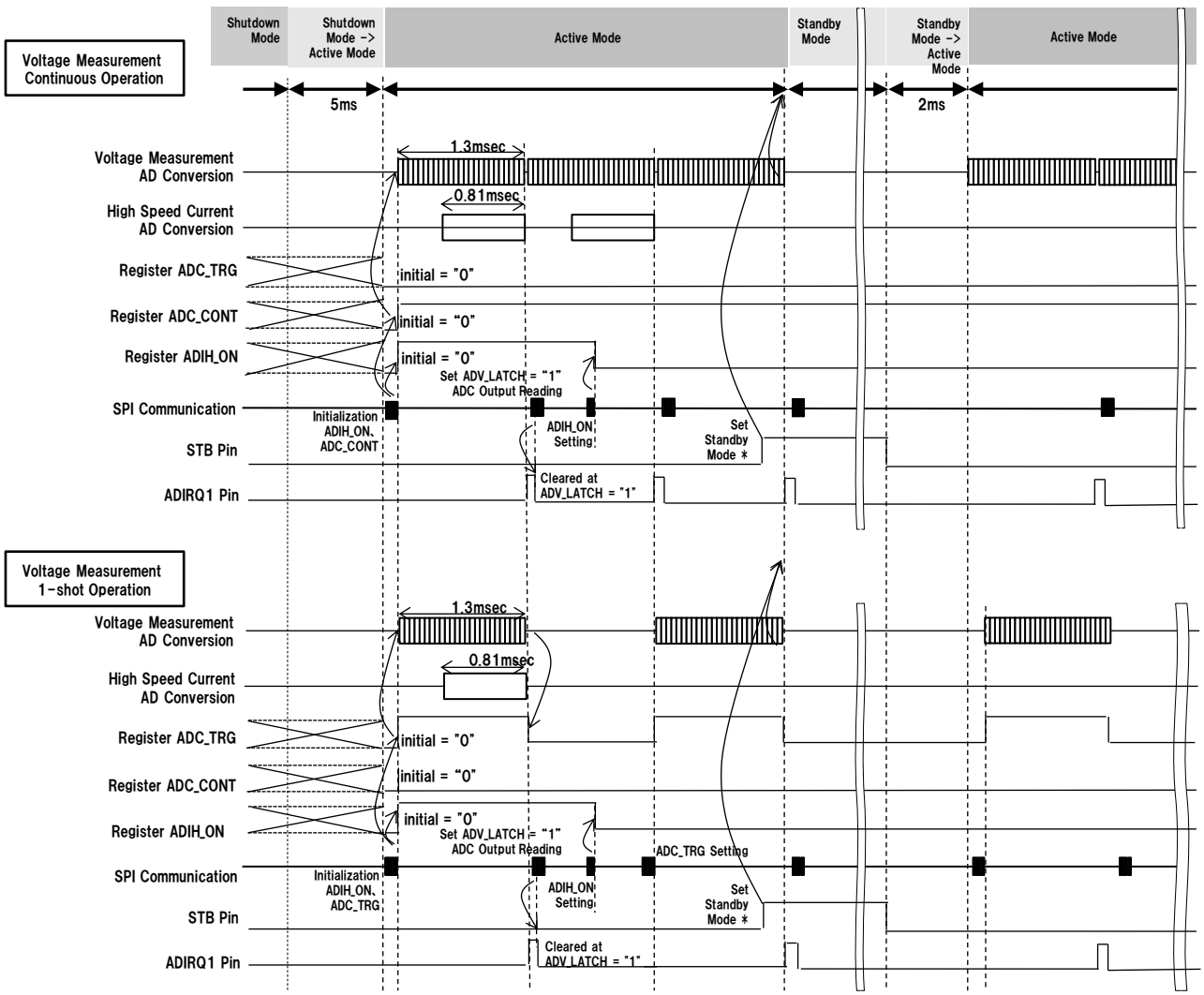


Fig.9.1.4 Example of Voltage and Current Measurement Timing Diagram

9.2 Control Registers

9.2.1 Registers

Table.9.2.1 and Table.9.2.2 shows the registers that control Voltage Measurement.

Table.9.2.1 Voltage Measurement Control Registers1

Register	Address	Function	Page
PWR_CTL	0x01	Mode of Operation・FET Driver Operation Control register	99
CVSEL	0x04	Respective cell voltage measurement ON/OFF setting register	102
GVSEL	0x05	Other voltage measurement ON/OFF setting register	103
OP_MODE	0x0A	ADC Operation register	107
GPIO_CTL1	0x0C	GPIO control 1 register	109
GPIO_CTL2	0x0D	GPIO control 2 register	109
GPIO_CTL3	0x0E	GPIO control 3 register	110
GPIO_CTL4	0x0F	GPIO control 4 register	109
GPIOSEL	0x17	GPIO output control register	115
ADCTL1	0x19	ADC control register1	117
FUSE_RADR	0x2E	FUSE Read address setting register	124
FUSE_DATA	0x2F	FUSE read data register	124
STAT	0x30	ADC/ALARM Status register	125
CV01_AD	0x33	Voltage measurement result for cell 1 register	127
CV02_AD	0x34	Voltage measurement result for cell 2 register	127
CV03_AD	0x35	Voltage measurement result for cell 3 register	127
CV04_AD	0x36	Voltage measurement result for cell 4 register	127
CV05_AD	0x37	Voltage measurement result for cell 5 register	127
CV06_AD	0x38	Voltage measurement result for cell 6 register	127
CV07_AD	0x39	Voltage measurement result for cell 7 register	127
CV08_AD	0x3A	Voltage measurement result for cell 8 register	127
CV09_AD	0x3B	Voltage measurement result for cell 9 register	127
CV10_AD	0x3C	Voltage measurement result for cell 10 register	127
CV11_AD	0x3D	Voltage measurement result for cell 11 register	127
CV12_AD	0x3E	Voltage measurement result for cell 12 register	127
CV13_AD	0x3F	Voltage measurement result for cell 13 register	127
CV14_AD	0x40	Voltage measurement result for cell 14 register	127

Table.9.2.2 Voltage Measurement Control Registers2

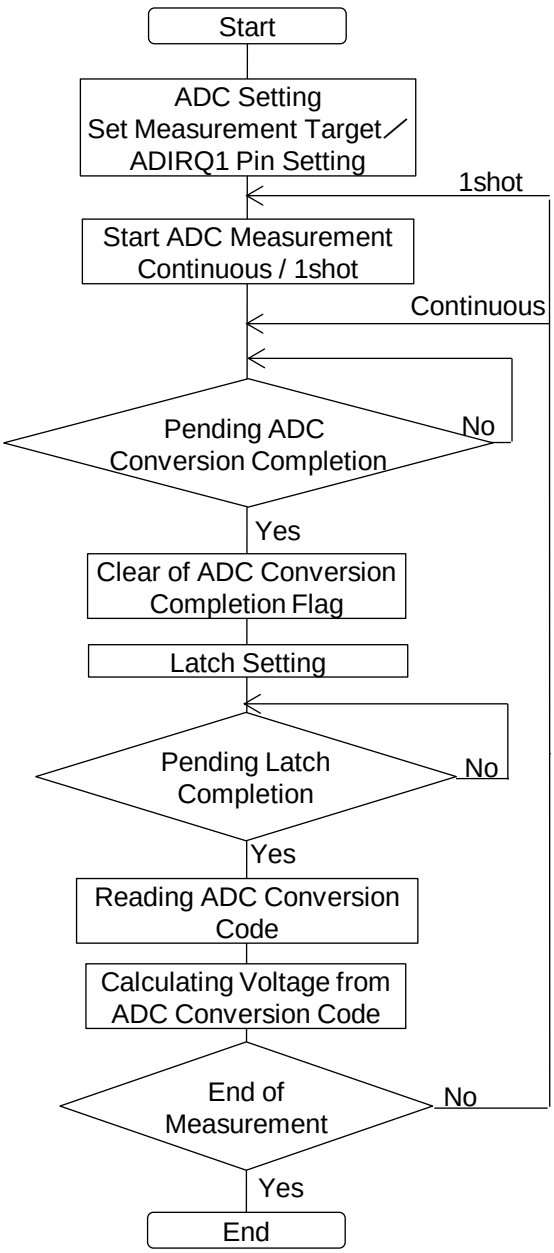
Register	Address	Function	Page
CV15_AD	0x41	Voltage measurement result for cell 15 register	127
CV16_AD	0x42	Voltage measurement result for cell 16 register	127
VPACK_AD	0x43	Voltage measurement result for VPACK register	127
TMONI1_AD	0x44	Voltage measurement result for TMONI1 register	128
TMONI2_AD	0x45	Voltage measurement result for TMONI2 register	128
TMONI3_AD	0x46	Voltage measurement result for TMONI3 register	128
TMONI4_AD	0x47	Voltage measurement result for TMONI4 register	128
TMONI5_AD	0x48	Voltage measurement result for TMONI5 register	128
VDD50_AD	0x49	Voltage measurement result for VDD50 register	129
GPIO1_AD	0x4A	Voltage measurement result for GPIO1 register	129
GPIO2_AD	0x4B	Voltage measurement result for GPIO2 register	129

9.3 Cell Voltage Measurement

Voltage across each cell (C1, C2 … C16) will be measured during voltage measurement cycle.

9.3.1 Cell Voltage Measurement Setting Procedure

Cell Voltage use the following settings
・Set Measurement Target: Cell 1~16
・ADIQR1 Pin Setting



■ADC Setting
Set the CV[n]SEL flag (CVSEL:bp15-0) to 0xFFFF to set measurement target.
Set the GPIO5SEL flag (GPIOSEL:bp9-8) to “01” for ADIRQ1 output.
Set the GPIO5_NOE flag (GPIO_CTL1:bp12) to “0” setting GPIO5 as output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (PWR_CTL:bp8) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (OP_MODE:bp4) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 pin : ADIRQ1 -> “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (STAT:bp0), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (STAT:bp0) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (OP_MODE:bp0) to “1”, latch Voltage measurement result for CVn_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (OP_MODE:bp0) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read CVn_AD register (0x33-0x42)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from Cell voltage conversion table.9.3.1.

※ When the R/WL register control, please implement the LOCK register settings.

9.3 Cell Voltage Measurement

9.3.2 Cell Voltage Conversion Table

The full range and resolution of cell voltage measurement is shown below and listed in Table.9.3.1.

- Maximum input voltage:4.999695V = 5.0V × (2^{14}-1) /2^{14}
- Minimum Input Voltage:0V
- Resolution:0.000305V = 5.0V/2^{14}

Table.9.3.1 Cell Voltage Conversion Table

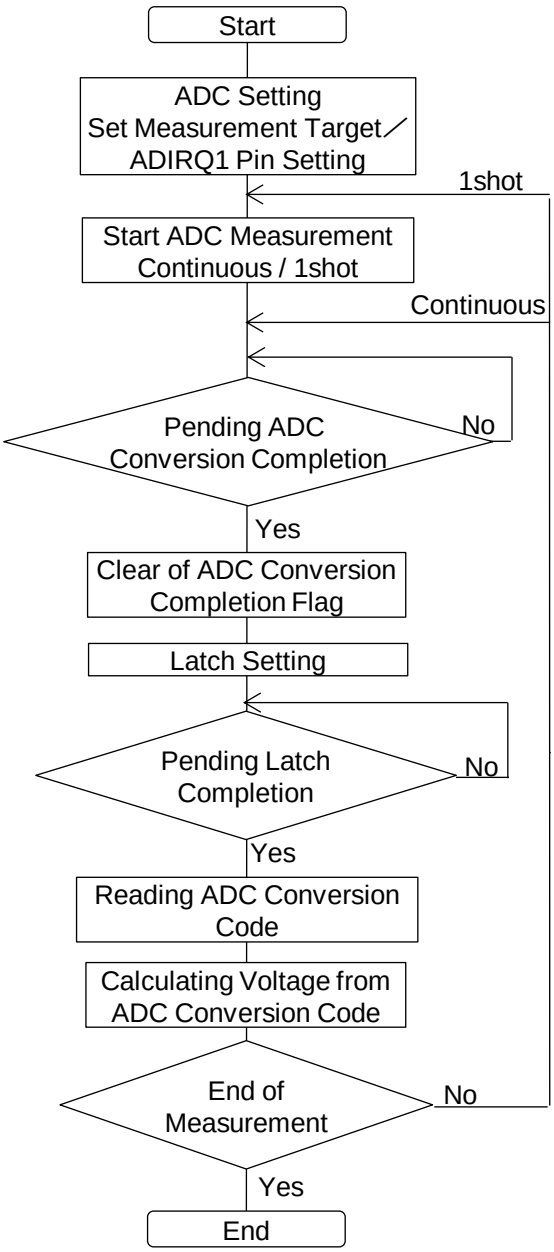
Analog level [V] (typ)	Digital output (CV01_AD[13:0] ～ CV16_AD[13:0])														
	Code	MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.4 VPACK Voltage Measurement

Voltage at VPACK pin is measured during voltage measurement cycle.

9.4.1 VPACK Voltage Measurement Setting Procedure

VAPCK Voltage use the following settings
- Set Measurement Target:VAPCK
- ADIQR1 Pin Setting



■ADC Setting
Set the GVSEL flag (GVSEL:bp0) to “1” to set measurement target.
Set the GPIO5SEL flag (GPIOSEL:bp9-8) to “01” to ADIRQ1 output.
Set the GPIO5_NOE flag (GPIO_CTL1:bp12) to “0” to GPIO5 output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (PWR_CTL:bp8) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (OP_MODE:bp4) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 pin : ADIRQ1 -> “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (STAT:bp0), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (STAT:bp0) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (OP_MODE:bp0) to “1”, latch Voltage measurement result for VPACK_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (OP_MODE:bp0) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read VAPCK_AD register (0x43)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from VPACK voltage conversion table.9.4.1.

※ When the R/WL register control, please implement the LOCK register settings.

9.4 VPACK Voltage Measurement

9.4.2 VPACK Voltage Conversion Table

The full range and resolution of VPACK measurement is shown below and listed in Table.9.4.1.

- Maximum input voltage:99.993896V = 100.0V × $(2^{14}-1)/2^{14}$
- Minimum Input Voltage: 0V
- Resolution:0.0060104V = 100.0V/2^{14}

Table.9.4.1 VPACK Voltage Conversion Table

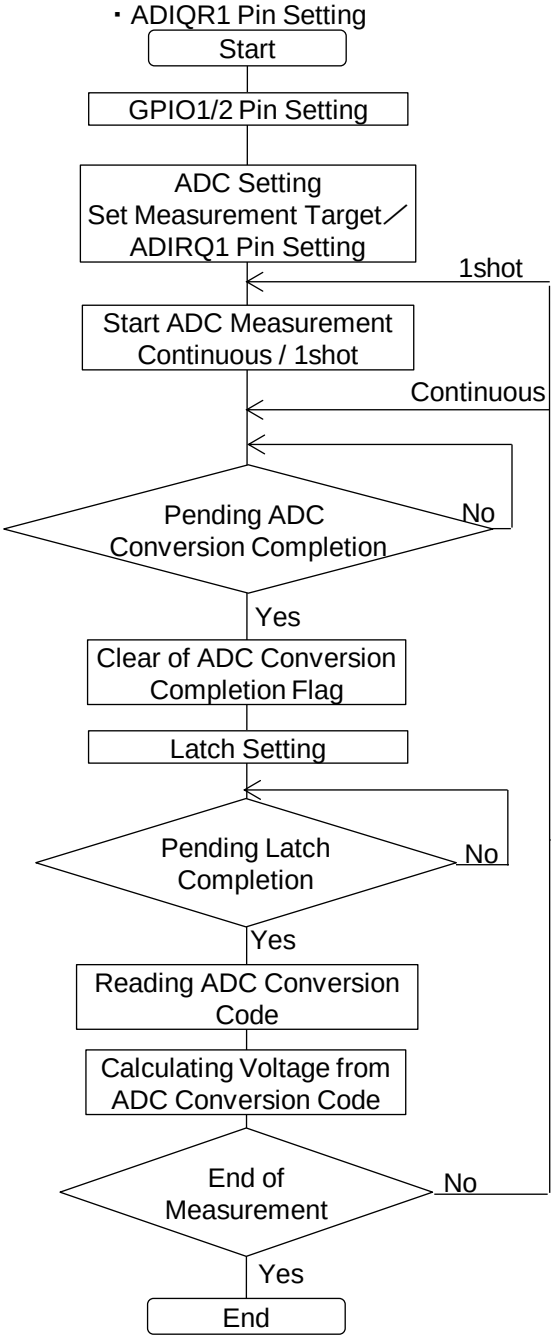
Analog level [V] (typ)	Code	Digital output (VPACK_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
99.993896	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
50.006104	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
50.000000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
49.993896	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.006104	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.5 GPIO1/2 Voltage Measurement

GPIO1/2 pins can be set as analog input and the voltage will be measured during voltage measurement cycle.

9.5.1 GPIO1/2 Voltage Measurement Setting Procedure

GPIO1/2 Voltage use the following settings
- Set Measurement Target:GPIO1,2
- ADIQR1 Pin Setting



■GPIO1/2 Pin Setting
Set GPIO1/2 Pin as Table 9.5.1.

■ADC Setting
Set the GVSEL flag (GVSEL:bp8-7) to “11” to set measurement target.
Set the GPIO5SEL flag (GPIOSEL:bp9-8) to “01” to ADIRQ1 output.
Set the GPIO5_NOE flag (GPIO_CTL1:bp12) to “0” to GPIO5 output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (PWR_CTL:bp8) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (OP_MODE:bp4) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 pin : ADIRQ1 -> “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (STAT:bp0), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (STAT:bp0) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (OP_MODE:bp0) to “1”, latch Voltage measurement result for GPIO1/2_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (OP_MODE:bp0) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read GPIO1/2_AD register (0x4A-0x4B)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from GPIO1/2 voltage conversion table.9.5.2.

※ When the R/WL register control, please implement the LOCK register settings.

Table.9.5.1 GPIO1 pin setting of GPIO Voltage Measurement

Address	bp	Flag	Pin Configuration	Description
0x0C	8	GPIO1_NOE	Output Enable	1:Disabled（default）
0x0C	0	GPIO1_IE	Input Enable	1:Enabled
0x0D	8	GPIO1_OD	Output Configuration	0:Push Pull(default)
0x0D	0	GPIO1_PD	Pull-Down Register	0:No（default）
0x0E	8	ST_GPIO1	Input Data	0:LO (VSS) （default）
0x0E	0	GPIO1_OUT	Output Data	0:LO （default）
0x0F	0	GPIO1_CHDRV	Output Drivability	0:2mA （default）
0x17	1-0	GPIO1SEL[1:0]	Function	10:Analog Input

9.5 GPIO1/2 Voltage Conversion Table

9.5.2 GPIO1/2 Voltage Conversion Table

The full range and resolution of GPIO1/2 voltage measurement is shown below and listed in table below.

・Maximum input voltage:4.999695V = 5.0V × (2^{14}-1)/2^{14}

・Minimum Input Voltage:0V

・Resolution:0.000305V = 5.0V/2^{14}

Table.9.5.2 GPIO1/2 Voltage Conversion Table

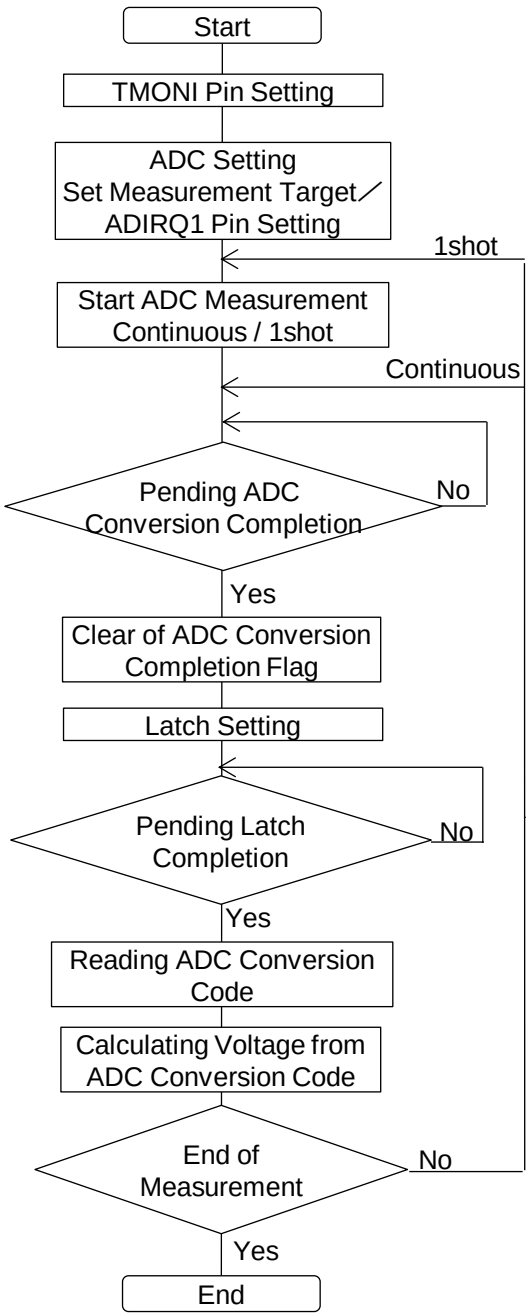
Analog level [V] (typ)	Code	Digital output (GPIO1_AD[13:0] / GPIO2_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.6 TMONI1~5 Voltage Measurement

TMONI1~5 pins are designed as temperature measurement input. To used these pins, connect thermistor externally to GND and set registers accordingly as below.

9.6.1 TMONI1~5 Voltage Measurement Setting Procedure

TMONI Voltage use the following settings
・Set Measurement Target:TMONI1~5
・ADIQR1 Pin Setting



■TMONI Pin Setting
Set PULLUP_SEL flag (GPIO_CTL4:bp12-8) to “11111” to add the pull-up resistance in ADC measurement. Pull-up resistor only connected during voltage measurement for respective pin.

■ADC Setting
Set the GVSEL flag (GVSEL:bp5-1) to “11111” to set measurement target.
Set the GPIO5SEL flag (GPIOSEL:bp9-8) to “01” to ADIRQ1 output.
Set the GPIO5_NOE flag (GPIO_CTL1:bp12) to “0” to GPIO5 output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (PWR_CTL:bp8) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (OP_MODE:bp4) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 pin : ADIRQ1 -> “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (STAT:bp0), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (STAT:bp0) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (OP_MODE:bp0) to “1”, latch Voltage measurement result for TMONIn_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (OP_MODE:bp0) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read TMONIn_AD register (0x44-0x48)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from TMONI voltage conversion table.9.6.1.

※ When the R/WL register control, please implement the LOCK register settings.

9.6 TMONI1~5 Voltage Measurement

9.6.2 TMONI1~5 Voltage Conversion Table

The full range and resolution of TMONI voltage measurement is shown below and listed in table below.

・Maximum input voltage:4.999695V = 5.0V × $(2^{14}-1)/2^{14}$

・Minimum Input Voltage:0V

・Resolution:0.000305V = $5.0V/2^{14}$

Table.9.6.1 TMONI Voltage Conversion Table

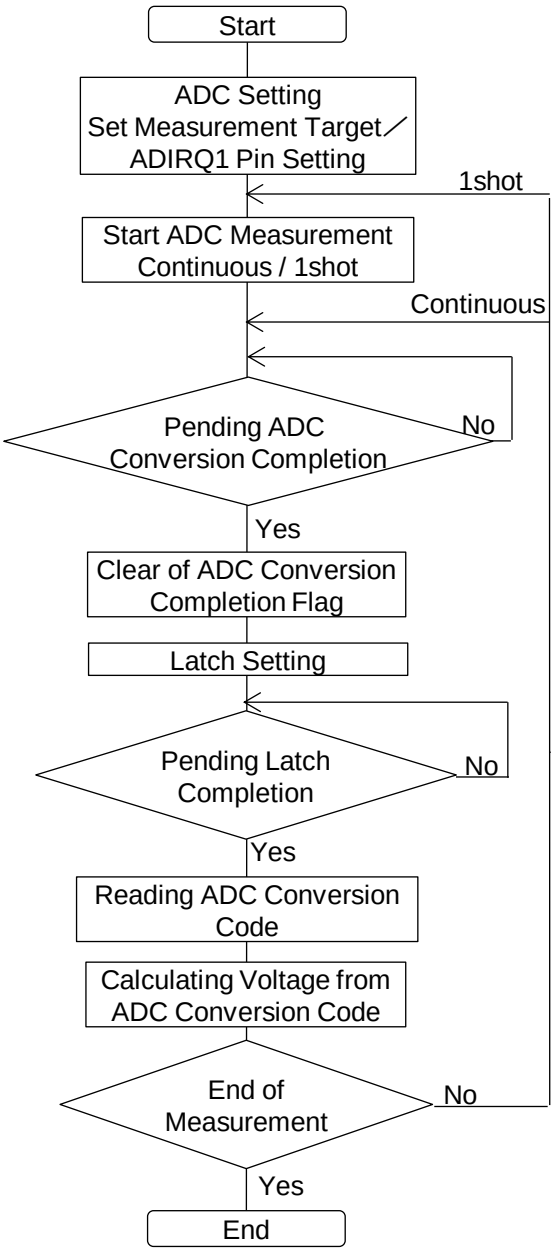
Analog level [V] (typ)	Code	Digital output (TMONI1_AD[13:0]～TMONI5_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.7 VDD50 Voltage Measurement

VDD50 is measured during voltage measurement cycle. As VDD50 is used as supply voltage for internal pull up resistor for TMONI1~5 pins, VDD50 voltage affect the TMONI1~5 pin voltage measurement.

9.7.1 VDD50 Voltage Measurement Setting Procedure

VDD50 Voltage use the following settings
・Set Measurement Target:VDD50



■ADC Setting
Set the GVSEL flag (GVSEL:bp6) to “1” to set measurement target.
Set the GPIO5SEL flag (GPIOSEL:bp9-8) to “01” to ADIRQ1 output.
Set the GPIO5_NOE flag (GPIO_CTL1:bp12) to “0” to GPIO5 output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (PWR_CTL:bp8) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (OP_MODE:bp4) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 pin : ADIRQ1 -> “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (STAT:bp0), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (STAT:bp0) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (OP_MODE:bp0) to “1”, latch Voltage measurement result for VDD50_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (OP_MODE:bp0) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read VDD50_AD register (0x49)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from VDD50 voltage conversion table.9.7.1.

※ When the R/WL register control, please implement the LOCK register settings.

9.7 VDD50 Voltage Measurement

9.7.2 VDD50 Voltage Conversion Table

The full range and resolution of VDD50 voltage measurement is shown below and listed in table below.

・Maximum input voltage:7.499542V = 7.5V × (2^{14}-1)/2^{14}

・Minimum Input Voltage:0V

・Resolution:0.000458V = 7.5V/2^{14}

Table.9.7.1 VDD50 Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (VDD50_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7.499542	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
3.750458	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
3.750000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
3.749542	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1

9.8 Temperature Measurement with TMONI1~5 pins

9.8.1 Temperature Measurement Procedure with TMONI1~5 pins

TMONI1~5 is designed for temperature measurement, with external thermistor connected from each pin to ground. For each pin, there is an internal pull up resistor of 10kΩ to VDD50 connected with a switch. User may choose to use the internal pull up resistor or external pull up resistor by register.

Due to the process tolerance, the internal pull up resistors may be deviated from the typical value, the actual resistor values are measured during the production test and stored in FUSE_DATA registers, user should use these registers data in temperature calculation. These are explained in more details from the following section. By connecting the pull-up resistor and a thermistor externally in series, it is possible to measure the resistance of the thermistor externally.

The connection example at TMONI1~5 with thermistor and internal pull up resistor is given in Fig 9.8.1.

The temperature could be derived from the TMONI1~5 reading, VDD50 with the consideration of thermistor characteristic, and pull up resistor.

The capacitor at TMONI1~5 should not exceed 1nF.

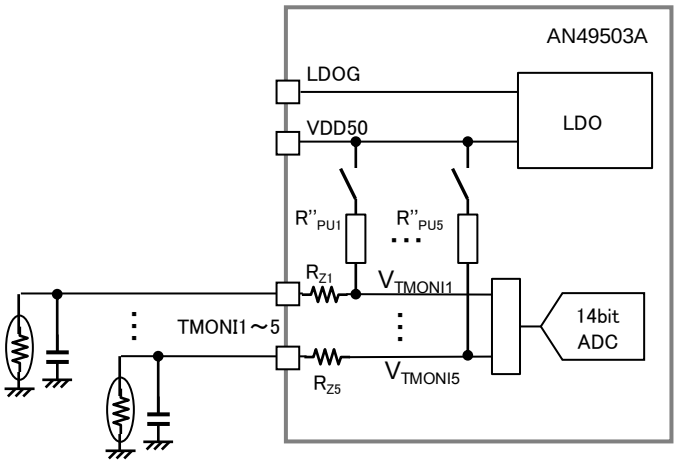


Fig.9.8.1 Thermistor Connection (Internal pull up resistor

The temperature calculation procedure by TMONI pin is shown in Fig9.8.2 .

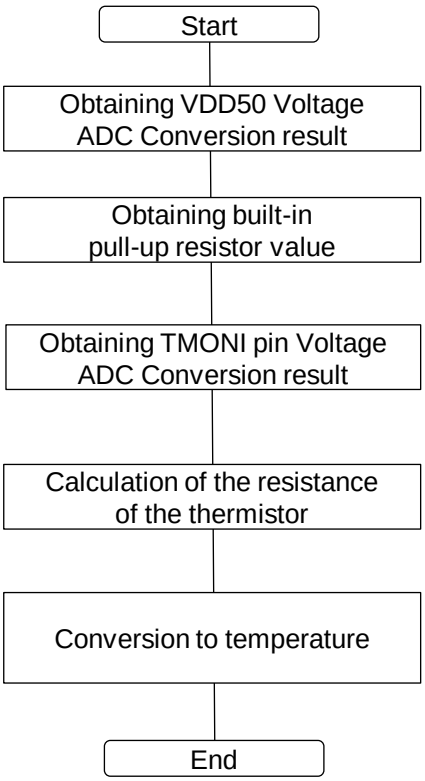


Fig.9.8.2
Temperature Measurement Procedure with TMONI1~5 pins

■Obtaining VDD50 Voltage
Obtain the VDD50 voltage [V_{VDD50}] by the ADC conversion as explained in 9.7.

■Obtaining internal pull-up resistor value
Obtain internal pull-up resistor [R_{PU}] = [R''_{PU}] + [R_Z] , by reading the pre-measured data from the built-FUSE register, and converted into the resistance value following steps in 9.8.2.

■Obtaining TMONI pin Voltage
Obtain voltage at each TMONI1~5 [V_{TMONI}] pins as explained in 9.6.

■Calculation of the resistance of the thermistor
Effective resistance of the thermistor [R_S][kohm] can be calculated as
$[R_S] = V_{TMONI} / (V_{VDD50} - V_{TMONI}) \times (R_{PU} - R_{Z[n]}) - R_{Z[n]}$

Table.9.8.4 $R_{Z[n]}$ of TMONI Pins

	TMONI1	TMONI2	TMONI3	TMONI4	TMONI5
$R_{Z[n]}$ [kohm]	0.155	0.150	0.135	0.120	0.100

■Conversion to temperature
From the effective resistance of thermistor [R_S], the temperature can be obtained from the temperature characteristic of the thermistor, an example of the thermistor is shown in Fig.9.8.3.

※ When the R/WL register control, please implement the LOCK register settings.

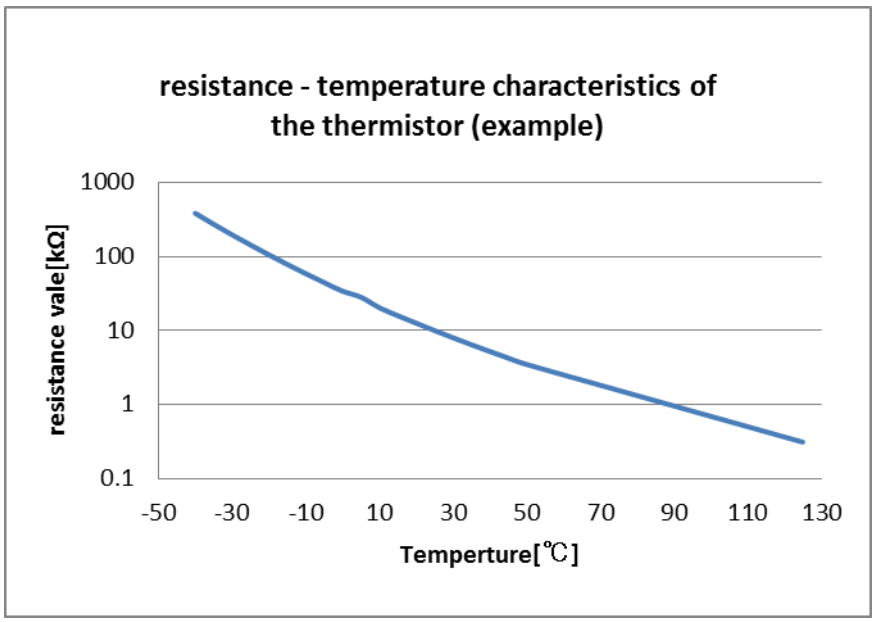


Fig.9.8.3 resistance - temperature characteristics of the thermistor (example)

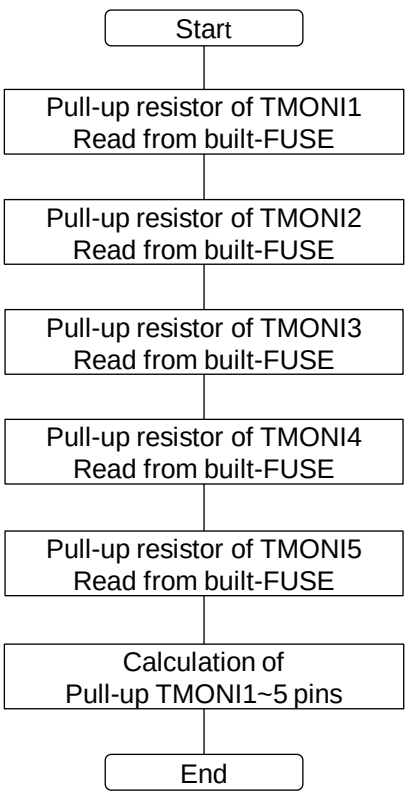
9.8 Temperature Measurement with TMONI1~5 pins

9.8.2 Internal pull-up resistor of TMONI pin calculation procedure

The information for pre-measured pull up resistor of TMONI1~5 is stored in the built-FUSE, it can be used to calculate the resistance value. The address map of the built-FUSE is shown in Table.9.8.1. Internal pull-up resistor value of TMONI1 pin is absolute value, Internal pull-up resistor value of TMONI2 ~ 5 pins are stored as the difference from TMONI1 pin resistor.
The procedure to calculate the TMONI1 ~ 5 internal pull-up resistor value is shown in Fig.9.8.4.

Table.9.8.1 Built-FUSE address map

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x2B	Pull-up resistor of TMONI1 (absolute) [9:5]															
0x2C	Pull-up resistor of TMONI1 (absolute) [4:0]															
0x2E	Pull-up resistor of TMONI3 (difference) [7:0]								Pull-up resistor of TMONI2 (difference) [7:0]							
0x2F	Pull-up resistor of TMONI5 (difference) [7:0]								Pull-up resistor of TMONI4 (difference) [7:0]							



■Pull-up resistor of TMONI1
Set 0x2B to FUSE_RADR flag (FUSE_RADR:bp7-0).
Read FUSE_DATA flag (FUSE_DATA:bp15-11).
Set 0x2C to FUSE_RADR flag (FUSE_RADR:bp7-0).
Read FUSE_DATA flag (FUSE_DATA:bp15-11)

■Pull-up resistor of TMONI2
Set 0x2E to FUSE_RADR flag (FUSE_RADR:bp7-0).
FUSE_DATA flag (FUSE_DATA:bp7-0).

■Pull-up resistor of TMONI3
Set 0x2E to FUSE_RADR flag (FUSE_RADR:bp7-0).
Read FUSE_DATA flag (FUSE_DATA:bp15-8).

■Pull-up resistor of TMONI4
Set 0x2F to FUSE_RADR flag (FUSE_RADR:bp7-0).
Read FUSE_DATA flag (FUSE_DATA:bp7-0).

■ Pull-up resistor of TMONI5
Set 0x2F to FUSE_RADR flag (FUSE_RADR:bp7-0).
Read FUSE_DATA flag (FUSE_DATA:bp15-8).

■Calculation of Pull-up TMONI1~5 pins
TMONI1 is calculated resistance in accordance with TNMONI1 pin pull-up resistor conversion table.9.8.2, TMONI2 is calculated resistance in accordance with TMNONI2 pin pull-up resistor conversion table.9.8.3. TMONI3 ~ 5 pins are the same calculation formula as TMONI2 pin.

※ When the R/WL register control, please implement the LOCK register settings.

Fig.9.8.4 Internal pull-up resistor of TMONI pin calculation procedure

■TMONI1 pin

Refer to the table below to obtain pull up resistance from data read (from previous page)

・Max:12.99414 kΩ = 6 kΩ × $(2^9 - 1) / 2^{10}$ + 10kΩ

・Min:7 kΩ

・Resolution:5.86 Ω = 6 kΩ / 2^{10}

(2's complement data)

■TMONI2 pin

For TMONI2 pin, the differences from TMONI1 pin is determined from the table below using data read (from previous page)

・Max:0.74414 kΩ = 1.5 kΩ × $(2^7 - 1) / 2^8$

・Min:-0.75 kΩ

・Resolution:5.86 Ω = 1.5 kΩ / 2^8

(2's complement data)

TMONI2's resistance is calculated by = differences read in this step + TMONI1 resistance

■TMONI3/4/5 pins

TMONI3~TMONI5 resistance can be determined similarly as for TMONI2, with the data read changes accordingly:

Table.9.8.2 TMONI1 pin pull up resistance conversion

resistance [kΩ] (typ)	Fuse Digital output (0x2B[15:11] / 0x2C[15:11])										
	Code	MSB									LSB
		0x2B					0x2C				
		b15	b14	b13	b12	b11	b15	b14	b13	b12	b11
12.99414	0x1FF	0	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・
10.00586	0x001	0	0	0	0	0	0	0	0	0	1
10	0x000	0	0	0	0	0	0	0	0	0	0
9.99414	0x3FF	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・
7.00586	0x201	1	0	0	0	0	0	0	0	0	1
7	0x200	1	0	0	0	0	0	0	0	0	0

Table.9.8.3 TMONI2 pin pull up resistance conversion

resistance (difference from TMONI1) [kΩ] (typ)	Code	Fuse Digital output (0x2E[7:0])							
		MSB							LSB
		b7	b6	b5	b4	b3	b2	b1	b0
0.74414	0x7F	0	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・
0.00586	0x01	0	0	0	0	0	0	0	1
0	0x00	0	0	0	0	0	0	0	0
-0.00586	0xFF	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・
-0.74414	0x81	1	0	0	0	0	0	0	1
-0.75	0x80	1	0	0	0	0	0	0	0

Chapter 10 SRP/SRN Current Measurement (High Speed / Low Speed)

10.1.1 SRP/SRN Current Measurement (High Speed / Low Speed)

This IC measures the voltage across the shunt resistor connected between SRP / SRN pins with ADC. For current measurement, different ADCs from voltage measurement are used as shown in 1.7. Current across the shunt resistor can be calculated by dividing the measured voltage with shunt resistor value used.

There are two current measurement modes, High Speed current measurement and Low Speed current measurement which using two different ADCs. High Speed current measurement mode measured current in synchronize with the voltage measurement with a short measurement time. While Low Speed current measurement mode that integrate the measured current, which can be used such as Coulomb Counter,

It is possible to be selected depending on the application.

The measured voltage is output as 16-bit data.

High Speed current measurement can operate only during the Active mode.

Low Speed current measurements can operate in Active mode and Standby mode.

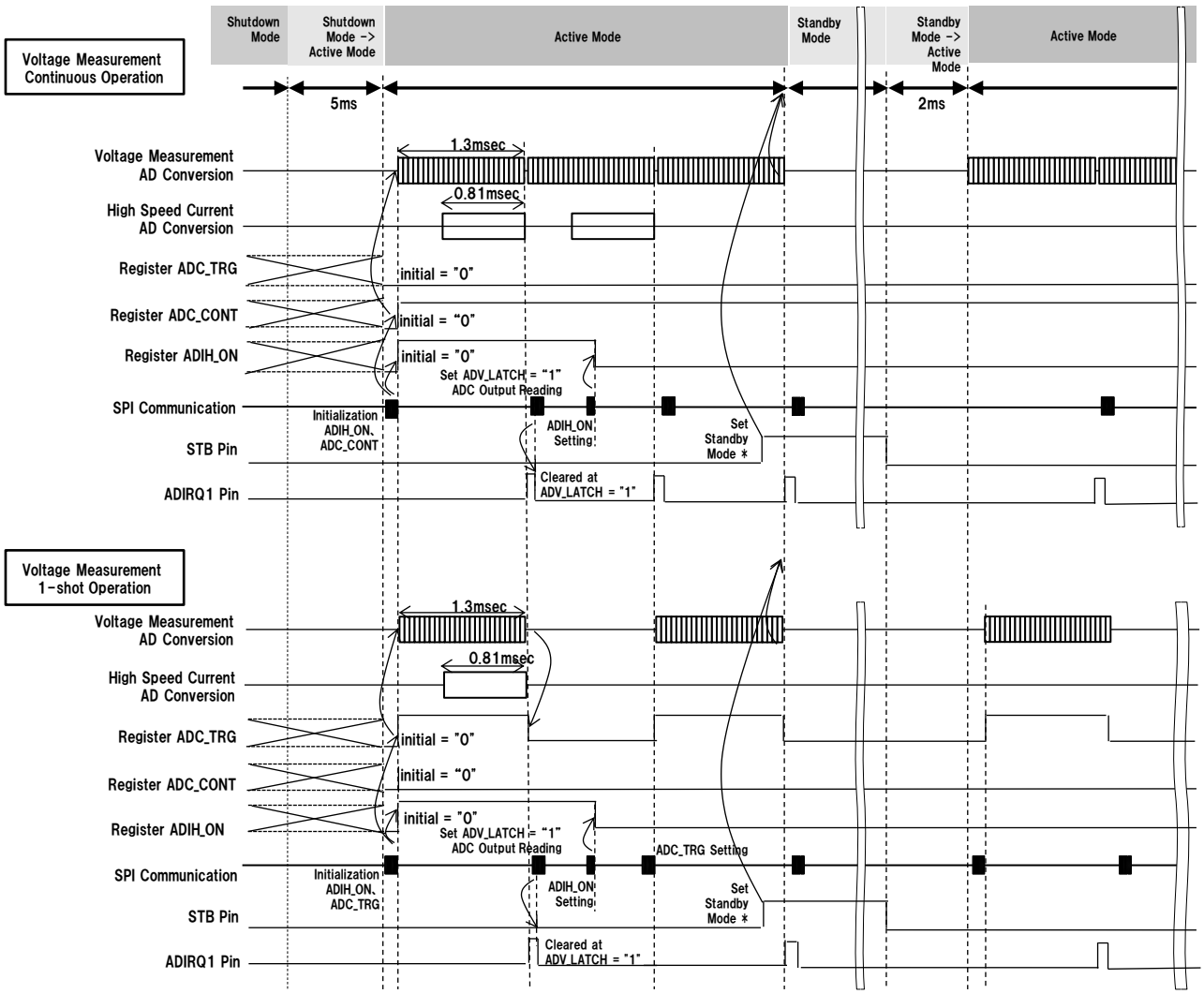
Conversion time of the ADC for High Speed current measurement mode is about 0.81ms while conversion time for Low Speed current measurement mode is about 250ms.

10.1.2 High Speed (HS) Current Measurement Timing

HS current measurement only operates during active mode which can be set by ADIH_ON flag (ADCTL2:bp0) and ADSWHY_EN flag (ADCTL2:bp13) to “1”. HS current measurement will start at next cell voltage measurement. The current is measured at the same time cell voltage is being measured, which is about 0.81ms for each measurement.

When current measurement completed, IADH_DONE flag (STAT:bp1) will be set to “1”, and the measured data is latched to CVIH_AD flag (CVIH_AD:bp15-0) when ADIH_LATCH flag (OP_MODE:bp1) is set to “1”, this flag is cleared to “0” after completion. IADH_DONE flag (STAT:bp1) is cleared by write “1” to it.

Fig.10.1.1 Example of Voltage and Current Measurement Timing Diagram

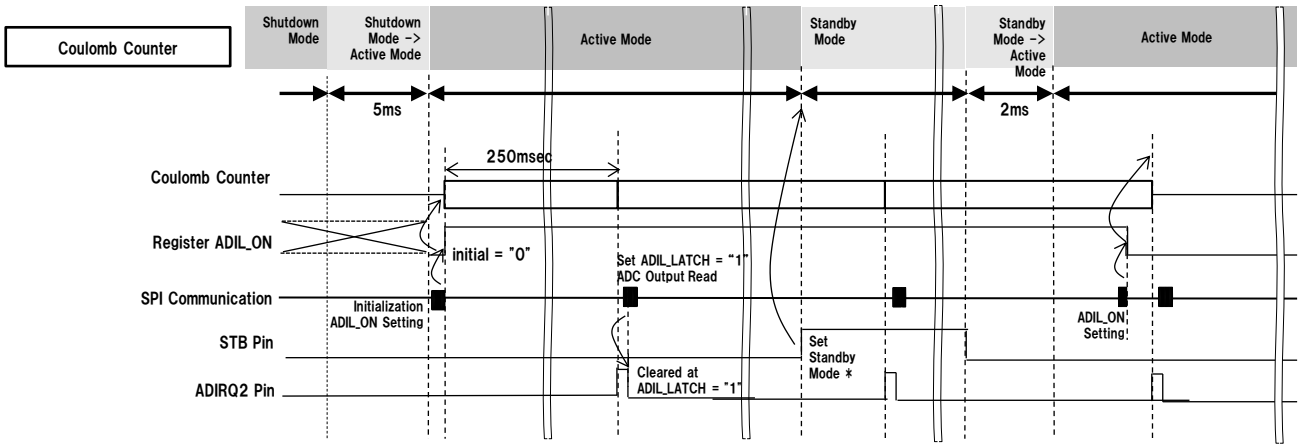


10.1.3 Low Speed (LS) Current Measurement Timing

Coulomb Counter can be operated during Active Mode and Standby Mode. The measurement starts when ADIL_ON flag (ADCTL2:bp1) and ADSWSD_EN flag (ADCTL2:bp12) set to “1” and accumulating the current for a period of 250ms.

When each measurement cycle completed, ADIRQ2 pin will be triggered to “H” and IADS_DONE flag (STAT:bp2) will be set to “1”. The measured data will be updated to CVIL_AD flag (CVIL_AD:bp15-0) when ADIL_LATCH flag (OP_MODE:bp2) is set to “1”. ADIRQ2 pin is cleared when ADIL_LATCH flag (OP_MODE:bp2) is set to “1”. This flag is cleared to “0” after completion. IADS_DONE flag (STAT:bp2) is cleared by write “1” to it.

Fig.10.1.2 Example Coulomb Counter Timing Diagram



* Standby Mode started after voltage conversion cycle complete
Note : The timing diagram of SPI Communication is not to the scale.

10.2 Control Registers

10.2.1 Registers

Table.10.2.1 shows the registers that control Current Measurement.

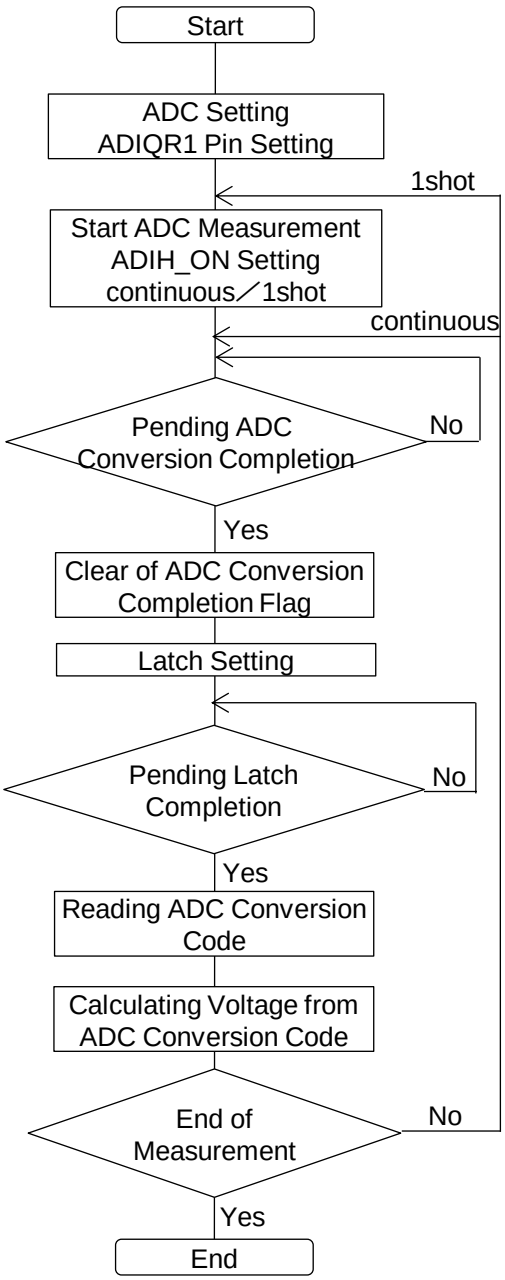
Table.10.2.1 Current Measurement Control Registers

Register	Address	Function	Page
PWR_CTL	0x01	Mode of Operation・FET Driver Operation Control register	99
OP_MODE	0x0A	ADC Operation register	107
GPIO_CTL1	0x0C	GPIO control 1 register	109
GPIOSEL	0x17	GPIO output control register	115
ADCTL1	0x19	ADC control register1	117
ADCTL2	0x1A	ADC control register2	118
STAT	0x30	ADC/ALARM Status register	125
CVIH_AD	0x4C	High speed current ADC measurement result register	130
CVIL_AD	0x4D	Low speed current ADC measurement result register	130

10.3 SRP/SRN Current Measurement Setting Procedure

10.3.1 SRP/SRN Current (High Speed) Measurement Setting Procedure

HS Current use the following setting.



■ADC Setting
Set the GPIO5SEL flag (GPIOSEL:bp9-8) to “01” to ADIRQ1 output.
Set the GPIO5_NOE flag (GPIO_CTL1:bp12) to “0” to GPIO5 output.

■Start ADC Measurement
ADIH_ON Setting : Set ADSWHY_EN flag (ADCTL2:bp13) and ADIH_ON flag (ADCTL2:bp0) to “1”, start measurement in synchronize with the voltage measurement.

Continuous Measurement : Set the ADC_CONT flag (PWR_CTL:bp8) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (OP_MODE:bp4) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 pin : ADIRQ1 -> “H” when measurement complete.
Using flag polling : Read IADH_DONE flag (STAT:bp1), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write IADH_DONE flag (STAT:bp1) to “1” to clear this flag.

■Latch Setting
When write ADIH_LATCH flag (OP_MODE:bp1) to “1”, latch Voltage measurement result for HS current register.
※If it is cleared ADIRQ1 pin (OP_MODE: bp0), write ADV_LATCH flag (OP_MODE:bp0) to "1". It uses an interrupt of voltage ADC.

■Pending Latch Completion
Polling until ADIH_LATCH flag (OP_MODE:bp1) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read CVIH_AD register (0x4C)

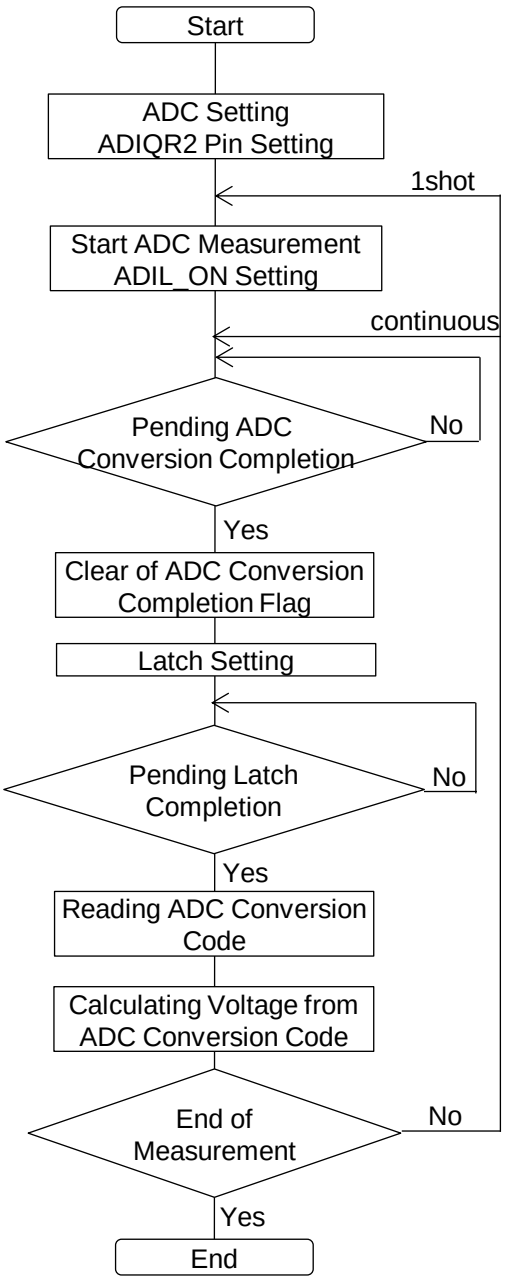
■Calculating Voltage from ADC Conversion Code
Calculate the voltage from SRP/SRN current conversion table.10.3.1.

※ When the R/WL register control, please implement the LOCK register settings.

10.3 SRP/SRN Current Measurement Setting Procedure

10.3.2 SRP/SRN Current (Low Speed) Measurement Setting Procedure

LS Current use the following setting.



■ADC Setting
Set the GPIO4SEL flag (GPIOSEL:bp7-6) to “01” to ADIRQ2 output.
Set the GPIO4_NOE flag (GPIO_CTL1:bp11) to “0” to GPIO4 output.

■Start ADC Measurement
ADIL_ON Setting : Set ADSWSD_EN flag (ADCTL2:bp12) and ADIL_ON flag (ADCTL2:bp1) to “1”, start measurement.

■Pending ADC Conversion Completion
When using interrupt ADIRQ2 pin : ADIRQ2 -> “H” when measurement complete.
Using flag polling : Read IADS_DONE flag (STAT:bp2), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write IADS_DONE flag (STAT:bp2) to “1” to clear this flag.

■Latch Setting
When write ADIL_LATCH flag (OP_MODE:bp2) to “1”, latch Voltage measurement result for LS current register.

■Pending Latch Completion
Polling until ADIL_LATCH flag (OP_MODE:bp2) become “0” or ADIRQ2 pin become “L”. Or wait for 48us.

■Reading ADC Conversion Code
Read CVIL_AD register (0x4D)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from SRP/SRN current conversion table.10.3.1.

※ When the R/WL register control, please implement the LOCK register settings.

10.3 SRP/SRN Current Measurement Setting Procedure

10.3.3 SRP/SRN Current Measurement Conversion Table

The full range and resolution of current measurement (High Speed / Low Speed) is shown below and listed in table below.

・Maximum input voltage:+179.994507 mV

$= 360\ mV \times (2^{15} - 1) / 2^{16}$

・Minimum input voltage:-180 mV

・Resolution:0.005493 mV = 360 mV / 2^{16}

Table.10.3.1 SRP/SRN Current Measurement Conversion Table

Analog level [mV] (typ)	Digital output (CVIL_AD[15:0] / CVIH_AD[15:0])																
	Code	MSB															LSB
		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
179.994507	0x7FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.005493	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-0.005493	0xFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
-179.994507	0x8001	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
-180	0x8000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

From the voltage between the SRP-SRN pins which has been calculated in the above,
it is calculate the of the current flowing between the SRP-SRN pins.
The voltage between the SRP-SRN pins is V_{SRPN}.
Current = V_{SRPN} ÷ shunt resistor

Chapter 11 Monitoring and Protection

11.1 Function Description

The abnormal cell voltage (Over Voltage / Under voltage) and abnormal current can be detected by this IC, and FET can be set to turn OFF automatically according to abnormal status and register setting, which will be explained in this chapter.
Over Voltage / Under Voltage can be only detected in Active Mode. In Standby Mode, it operate differently. Refer to 11.3.1 for more details on cell voltage abnormality.
Over Current in Charge (OCC), Over Current in Discharge(OCD), Short Circuit in Discharge(SCD) can be detected in Active Mode and Standby Mode and is explained in 11.3.2.
Under Voltage for CVDD can be detected in Active mode and Standby mode and is explained in 11.3.3.

Table.11.1.1 Abnormality status list

Abnormality status	Abnormality source	Active mode	Standby mode
OV : Over Voltage	Cell voltage	YES	NA
UV : Under Voltage	Cell voltage	YES	NA
OCC : Over Current in Charge	SRP/SRN differential voltage	YES	YES
OCD : Over Current in Discharge	SRP/SRN differential voltage	YES	YES
SCD : Short Circuit in Discharge	SRP/SRN differential voltage	YES	YES
CVDD UV : Under Voltage in CVDD	CVDD voltage	YES	YES

Note: there is no extra protection for CVDD UV detection

Alarm condition will be triggered when the detected abnormal condition remains longer than delay time, and will be released when the release condition is met as shown in Table 11.1.2.
The current alarm should be released by external control (register access from MCU). The voltage alarm can be released automatically when the release condition met, i.e the voltage get a relief more than hysteresis value. The setting for alarm detection consist of threshold value, delay time and hysteresis value.

Table.11.1.2 Abnormality detection setting list

Abnormality status		MIN	MAX	STEP	BITS	Release Condition
Over Voltage (OV)	Threshold	2.0V/3.5V	4.5V	50mV	6/5	automatically or External Control
	Delay time	1000ms	4000ms	1000ms	2	
	Hysteresis Value	100mV	450 mV	50mV	3	
Under Voltage (UV)	Threshold	0.5V	3.0V	50mV	6	
	Delay time	1000ms	4000ms	1000ms	2	
	Hysteresis Value	100mV	450 mV	50mV	3	
Over Current in Charge (OCC)	Threshold	10mV	200mV	10 mV	5	External Control
	Delay time	1ms	16ms	1ms	4	
Over Current in Discharge (OCD)	Threshold	25mV	800mV	25mV	5	
	Delay time	1ms	16ms	1ms	4	
Short Circuit in Discharge (SCD)	Threshold	50 mV	800 mV	50mV	4	
	Delay time	50 us	1600 us	50 us	5	

When Alarm is triggered, the ALARM1/2 pin will be set to inform the abnormal status, two kinds of high-side FET control and digital output, which is used for such as Low side N-ch MOSFET or Relay etc, are provided. The operation is explained in details from 11.4 onward.

Table.11.1.3 Protection control list

Control Pin	Usage
ALARM1	To inform MCU (ALARM1 for all alarm status is available)
ALARM2	
CHG	High Side N-ch MOSFET
DIS	
GPOH1	High Side P-ch MOSFET
GPOH2	
GPIO1	Digital Output Note: High voltage is CVDD Level.
GPIO2	

Fig.11.1.1 describes a follow chart for protection setting and control

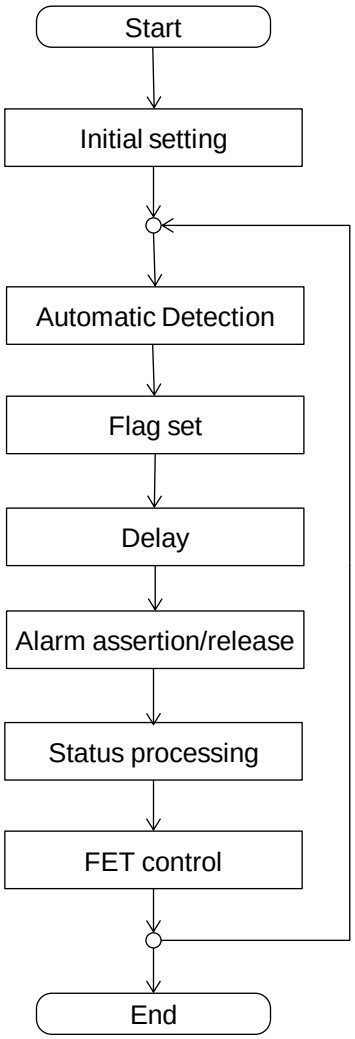


Fig.11.1.1 Protection setting Flow

■Initial setting
Enable or disable
Threshold value, delay time, hysteresis value.
Protection methods for detected alarm

■Automatic Detection
Detect voltage abnormal by using measured voltage from ADC
Detect current abnormal by using analog comparator

■Flag set
Voltage Flag
OVn_F flag (OVSTAT:bp15-0)
UVn_F flag (UVSTAT:bp15-0)
OVn_LF flag (OVL_STAT:bp15-0)
UVn_LF flag (UVL_STAT:bp15-0)
Current Flag
COND_SCD flag (MODE_STAT:bp5)
COND_OCD flag (MODE_STAT:bp4)
COND_OCC flag (MODE_STAT:bp3)

Status
ST_OV(STAT:bp9)
ST_UV(STAT:bp8)

■delay
if there is a abnormality or back to normal

■Alarm occurence/release
Output ALARM1/2
“L”: Alarm asserted
“H”: Alarm released
Status
ST_SCD(STAT:bp6)
ST_OCD(STAT:bp5)
ST_OCC(STAT:bp4)

■Status Processing
Decide if change FET Control according to Alarm status and setting.

■FET control
Output FET control

※ When the R/WL register control, please implement the LOCK register settings.

11.2 Protection control register

11.2.1 Protection control register list

Protection control register is listed as Table.11.2.1.

Table.11.2.1 Protection control register list

Register Name	address	Description	Page
PWR_CTL	0x01	Operation Mode and FET driver mode setting register	99
FDRV_CTL	0x03	FET driver setting register	101
OUVCTL1	0x06	OV/UV setting register	104
OUVCTL2	0x07	OV/UV setting register2	105
UVMSK	0x08	UV detection setting register	106
OVMSK	0x09	OV detection register	106
LOCK	0x0B	Write protected register Lock/Unlock setting register	108
ALARM_CTL1	0x11	Alarm control register1	111
ALARM_CTL2	0x12	Alarm control register2	112
ALARM_CTL3	0x13	Alarm control register3	112
GPIOSEL	0x17	GPIO Output control register	115
GPOH_CTL	0x1B	General purpose high-voltage output pin setting	119
MODE_STAT	0x22	Mode and status register	123
STAT	0x30	ADC/ALARM status register	125
OVSTAT	0x31	OV status register	126
UVSTAT	0x32	UV status register	126
OVL_STAT	0x52	OV detection flag register	131
UVL_STAT	0x53	UV detection flag register	131
CVDD_STAT	0x54	CVDD status register	132
FDRVSTAT	0x55	FET driver status register	133

11.3 Abnormality Detection

11.3.1 Cell Voltage Abnormality

Cell voltage abnormality consists of over charge (OV: Over Voltage) and over discharge (UV: Under Voltage), and is detected by using measured value from ADC.

The cell OV and UV detection can be enabled by setting OVMSKn flag (OVMSK:bp15-0) and UVMSKn flag (UVMSK:bp15-0) to “0” and disabled by setting these flag to “1”.

The setting for OV/UV abnormality detection consist of threshold limit, delay time and hysteresis value. The delay timer will start once the voltage is beyond the set threshold, and release threshold will be different by hysteresis value set. The delay timer will be reset when the voltage meets the release condition. The registers to set threshold value, delay time and hysteresis value is summarized on Table 11.3.3.

If abnormality is detected, respective flag (OVn_F flag (OVSTAT:bp15-0), OVn_LF flag (OVL_STAT:bp15-0), UVn_F flag (UVSTAT:bp15-0), UVn_LF flag (UVL_STAT:bp15-0) and ST_OV flag (STAT:bp9)) will be set to “1” immediately. OVn_F, UVn_F and ST_OV flag will be automatically cleared when released condition met. OVn_LF and UVn_LF flag are used for history check, and is cleared only by writing “0000” to the register.

The reaction of Alarm pin and control output to cell voltage abnormality is explained from 11.4 onward.

During Standby Mode, as voltage ADC is not operating by default, OV/UV detection is performed differently. By setting STB_MONEN flag (PWR_CTL:bp9) and ADC_CONT flag (PWR_CTL:bp8) to "1", if there is not SPI communication at Standby Mode, this IC will enter Active Mode automatically every 1 second to perform the voltage measurement once.

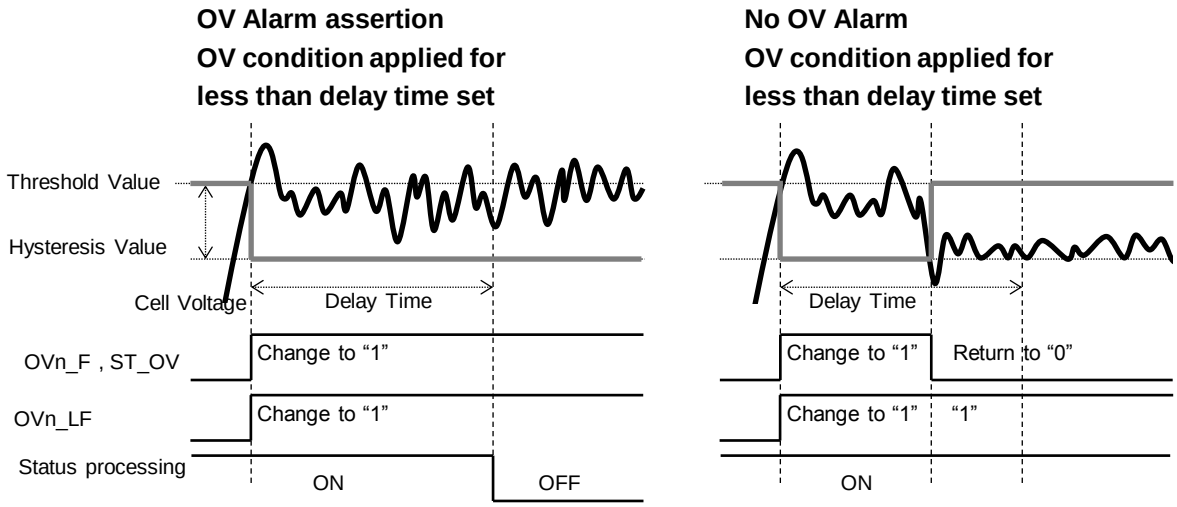


Fig.11.3.1 Example: OV Alarm occurrence & Control timing

Table.11.3.1 Register for interval measurement in Standby mode

Item	register	flag	0	1
Automatic measurement in Standby mode	PWR_CTL	STB_MONEN	Do nothing	Do interval measurement(every 1 second) when there is no SPI communication
	PWR_CTL	ADC_CONT	Do nothing	Continuous measurement mode

Note: Please set ADC_CONT to “1” when setting STB_MONEN to “1”.

Table.11.3.2 OV/UV enable register

Item	register	flag	0	1
OV/UV Mask	OVMSK	OVMSKn	Detection Enable	Detection Disable
	UVMSK	UVMSKn	Detection Enable	Detection Disable

Table.11.3.3 OV/UV setting register1

Item		register	flag	MIN	MAX	STEP	BITS
Over Voltage (OV)	Threshold	OUVCTL1	OVTH	2.0V/3.5V	4.5V	50mV	6/5
	Delay time	OUVCTL2	OV_DLY	1000ms	4000ms	1000ms	2
	Hysteresis	OUVCTL2	OV_HYS	100mV	450 mV	50mV	3
Under Voltage (UV)	Threshold	OUVCTL1	UVTH	0.5V	3.0V	50mV	6
	Delay time	OUVCTL2	UV_DLY	1000ms	4000ms	1000ms	2
	Hysteresis	OUVCTL2	UV_HYS	100mV	450 mV	50mV	3

Note: The lower limit for OVTH can be restricted to 2.0V by setting OVHLMT flag (OUVCTL2:bp15) to “0”.

Table.11.3.4 OV/UV setting register2

Item		register	flag	0	1
Over Voltage (OV)	Detection Mask	OVMSK	OVMSK	Detection Enable	Detection Disable
	abnormality happening	OVSTAT	OVn_F	normal	Happening
	abnormality history	OVL_STAT	OVn_LF	normal	abnormality happened
	status	STAT	ST_OV	normal	Happening
Under Voltage (UV)	Detection Mask	UVMSK	UVMSK	Detection Enable	Detection Disable
	abnormality happening	UVSTAT	UVn_F	normal	Happening
	abnormality history	UVL_STAT	UVn_LF	normal	abnormality happened
	status	STAT	ST_UV	normal	Happening

Table.11.3.5 OV Threshold Setting value

Threshold [V] (typ)	Setting value (OVTH[5:0])						
	Code	MSB					LSB
		b5	b4	b3	b2	b1	b0
4.500	0x34	1	1	0	1	0	0
4.450	0x33	1	1	0	0	1	1
・	・		・	・	・	・	・
3.550	0x21	1	0	0	0	0	1
3.500	0x20	1	0	0	0	0	0
3.450	0x1F	0	1	1	1	1	1
・	・		・	・	・	・	・
2.050	0x03	0	0	0	0	1	1
2.000	0x02	0	0	0	0	1	0

Note: OVTH[5] will be fixed to “1” when
OVHLMT flag (OUVCTL2:bp15) flag is set to “1”.

Table.11.3.6 UV Threshold Setting value

Threshold [V] (typ)	Setting value (UVTH[5:0])						
	Code	MSB					LSB
		b5	b4	b3	b2	b1	b0
3.000	0x32	1	1	0	0	1	0
2.950	0x31	1	1	0	0	0	1
・	・		・	・	・	・	・
0.550	0x01	0	0	0	0	0	1
0.500	0x00	0	0	0	0	0	0

11.3 Abnormality Detection

11.3.2 Current Abnormality Detection

Current abnormality detection consists of Over Current in charge detection (OCC), Over Current in Discharge (OCD) and Short Current in Discharge(SCD).
Current abnormality is detected by monitoring the differential voltage between SRP and SRN with analog comparator. Analog comparator will work both in Active mode and Standby mode.

Set the following register to "1" for enable and “0” for disable detection:
EN_CP flag (ALARM_CTL1:bp0), EN_OCC flag (ALARM_CTL1:bp1), EN_OCD flag (ALARM_CTL1:bp2), EN_SCD flag (ALARM_CTL1:bp3)

The setting for OCC/OCD/SCD abnormality detection consist of threshold value and delay time and is summarized on Table 11.3.8. There is no hysteresis value for current abnormality detection.

Delay timer will start to count once the current is beyond the threshold and will be cleared once the current goes under the threshold value.

When current abnormality is detected, COND_OCC flag (MODE_STAT:bp3), COND_OCD flag (MODE_STAT:bp4), COND_SCD flag (MODE_STAT:bp5) will be set to "1".
And when alarm is asserted after delay time, ST_OCC flag (STAT:bp4), ST_OCD flag (STAT:bp5), ST_SCD flag (STAT:bp6) will be set to "1".

The reaction of Alarm pin and control output to current abnormality is explained from 11.4 onward.

The flag (COND_OCC/COND_OCD/COND_SCD) will be clear automatically when current goes to normal.
The status (ST_OCC/ST_OCD/ST_SCD) will not be clear automatically, and writing "1" to the corresponding register to clear if it is needed.

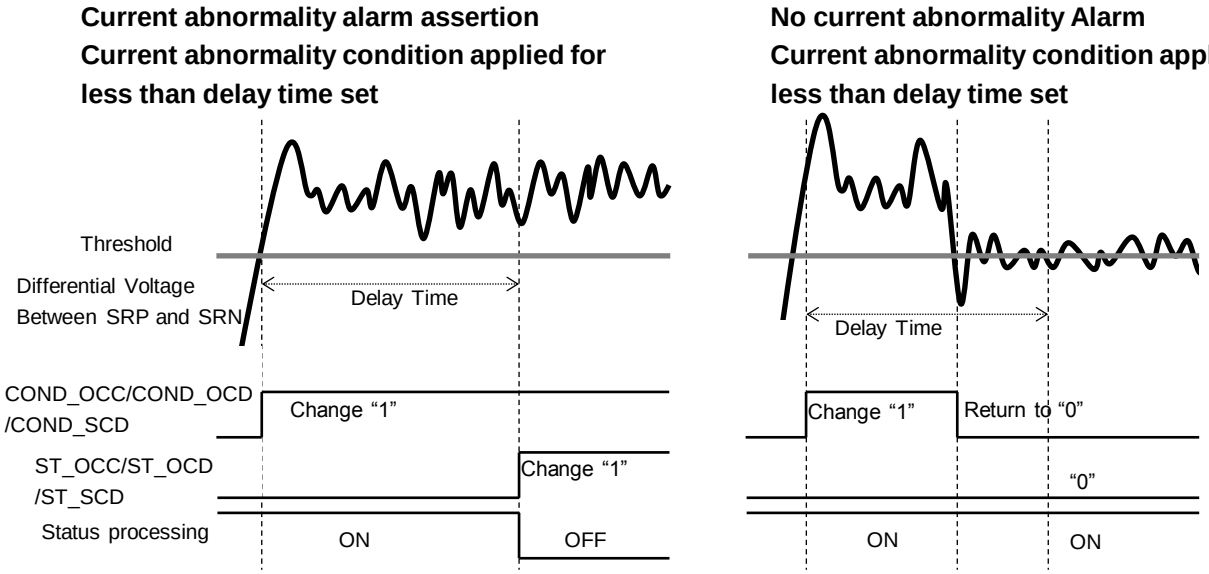


Fig.11.3.2 Example Current Alarm assertion & Control timing

Table.11.3.7 OCC/OCD/SCD enable register

Item	register	flag	0	1
All enable	ALARM_CTL1	EN_CP	Disable	Enable
OCC enable		EN_OCC	Disable	Enable
OCD enable		EN_OCD	Disable	Enable
SCD enable		EN_SCD	Disable	Enable

Table.11.3.8 OCC/OCD/SCD setting register 1

Item		register	flag	MIN	MAX	STEP	BITS
OCC	Threshold	ALARM_CTL2	OCC_D	10mV	200mV	10mV	5
	Delay time	ALARM_CTL3	OCC_DLY	1ms	16ms	1ms	4
OCD	Threshold	ALARM_CTL2	OCD_D	25mV	800mV	25mV	5
	Delay time	ALARM_CTL3	OCD_DLY	1ms	16ms	1ms	4
SCD	Threshold	ALARM_CTL2	SCD_D	50mV	800mV	50mV	4
	Delay time	ALARM_CTL3	SCD_DLY	50us	1600us	50us	5

Table.11.3.9 OCC/OCD/SCD setting register 2

Item		register	flag	0	1
OCC	abnormality happening	MODE_STAT	COND_OCC	normal	Happening
	alarm happening	STAT	ST_OCC	normal	Alarm happened
OCD	abnormality happening	MODE_STAT	COND_OCD	normal	Happening
	alarm happening	STAT	ST_OCD	normal	Alarm happened
SCD	abnormality happening	MODE_STAT	COND_SCD	normal	Happening
	alarm happening	STAT	ST_SCD	normal	Alarm happened

Table.11.3.10 OCC detection threshold

Threshold [mV]	Setting value (OCC_D[4:0])						
	Code	MSB					LSB
		b4	b3	b2	b1	b0	
200	0x13	1	0	0	1	1	
190	0x12	1	0	0	1	0	
・	・	・	・	・	・	・	
20	0x01	0	0	0	0	1	
10	0x00	0	0	0	0	0	

Table.11.3.11 OCD Threshold Setting value

Threshold [mV]	Setting value (OCD_D[4:0])						
	Code	MSB					LSB
		b4	b3	b2	b1	b0	
800	0x1F	1	1	1	1	1	
775	0x1E	1	1	1	1	0	
・	・	・	・	・	・	・	
50	0x01	0	0	0	0	1	
25	0x00	0	0	0	0	0	

Table.11.3.12 SCD Threshold Setting value

Threshold [mV]	Setting value (SCD_D[3:0])				
	Code	MSB			LSB
		b3	b2	b1	B0
800	0x0F	1	1	1	1
750	0x0E	1	1	1	0
・	・	・	・	・	・
100	0x01	0	0	0	1
50	0x00	0	0	0	0

11.3.3 CVDD Under voltage detection

CVDD under voltage abnormality (CVDD_UV) can be detected by using analog comparator.
Analog comparator works both in active mode and standby mode.
This abnormality gives you a reference that the communication may goes to wrong and there is no automatic FET control with this abnormality.

Threshold value, hysteresis value for CVDD_UV abnormality detection is fixed.
The delay timer will start once the voltage is under the set threshold, and threshold will increased with hysteresis value. The delay timer will be reset when the voltage is bigger than the new threshold.

CVDD_UV flag (CVDD_STAT:bp2) will be set to "1" when CVDD_UV abnormality is detected, and automatically cleared when voltage goes to normal.

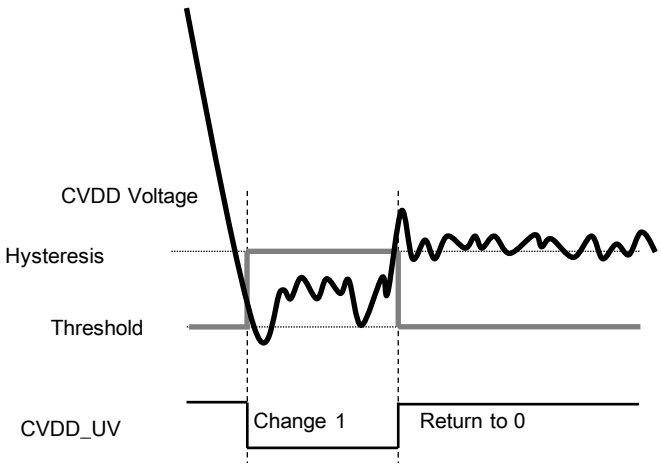


Fig.11.3.3 CVDD UV detection

Table.11.3.13 CVDD UV value

Item		Value (Fixed)
CVDD (UV)	Threshold	2.45V
	Hysteresis	0.35V

Table.11.3.14 CVDD UV detection register

Item		register	flag	0	1
CVDD Under Voltage (UV)	abnormality happening	CVDD_STAT	CVDD_UV	Happening	normal

11.4 ALARM1/2 Pin

These pins are used to inform the alarm assertion.
One-pin mode (ALARM1) and two-pin mode (pin ALARM1 and pin ALARM2) are available.
ALARMSEL flag (ALARM_CTL1:bp15) is used to select pin mode.
ALARM pin will goes “L” when the alarm is asserted.

ALARM1/2 will return to H when Alarm is released.
Voltage alarm can be released automatically.
Current alarm is released by write “1” to ST_OCC/ST_OCD/ST_SCD flag register.

Table.11.4.1 Alarm assertion Vs. ALRAM1/2 output

	Alarm	ALARMSEL=0	ALARMSEL=1	
		ALARM1	ALARM1	ALARM2
Abnormal	OV/UV OCC/OCD	"L"	"H"	"L"
	SCD	"L"	"L"	"H"
Normal	-	"H"	"H"	"H"

11.5 status processing

When alarm is asserted, the reaction of output control is set by the status processing flags.
Enable or disable the protection output, release mode can be selected.
Return method of current abnormality is only the external control.
It is cleared, when set the FDRV_ALM_CLR flag(FDRV_CTL:bp13) to "1".

Table.11.5.1 status processing flag

register	flag	description
FDRV_CTL bp15	FDRV_ALM_SD	Enable protection output when alarm is asserted 1:Enable protection output 0:Disable protection output（status remain）
FDRV_CTL bp14	FDRV_ALM_RCV	protection output Clear Condition 1:Manual Clear (By write 1 to FDRV_ALM_CLR) 0:Automatically
FDRV_CTL bp13	FDRV_ALM_CLR	Manual Clear 1:Clear （no less than 1 clock) 0:Do nothing

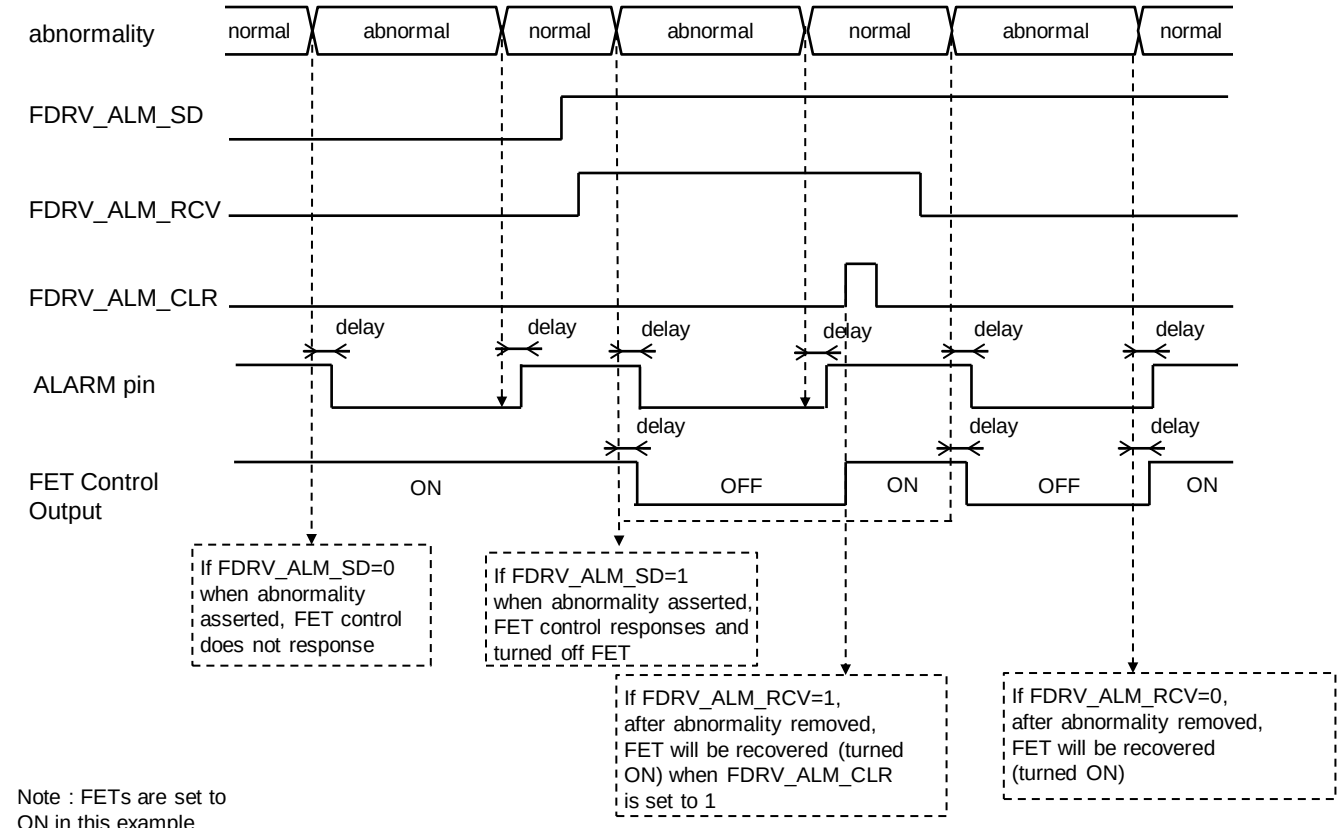


Fig.11.5.1 status processing timing for OV/UV

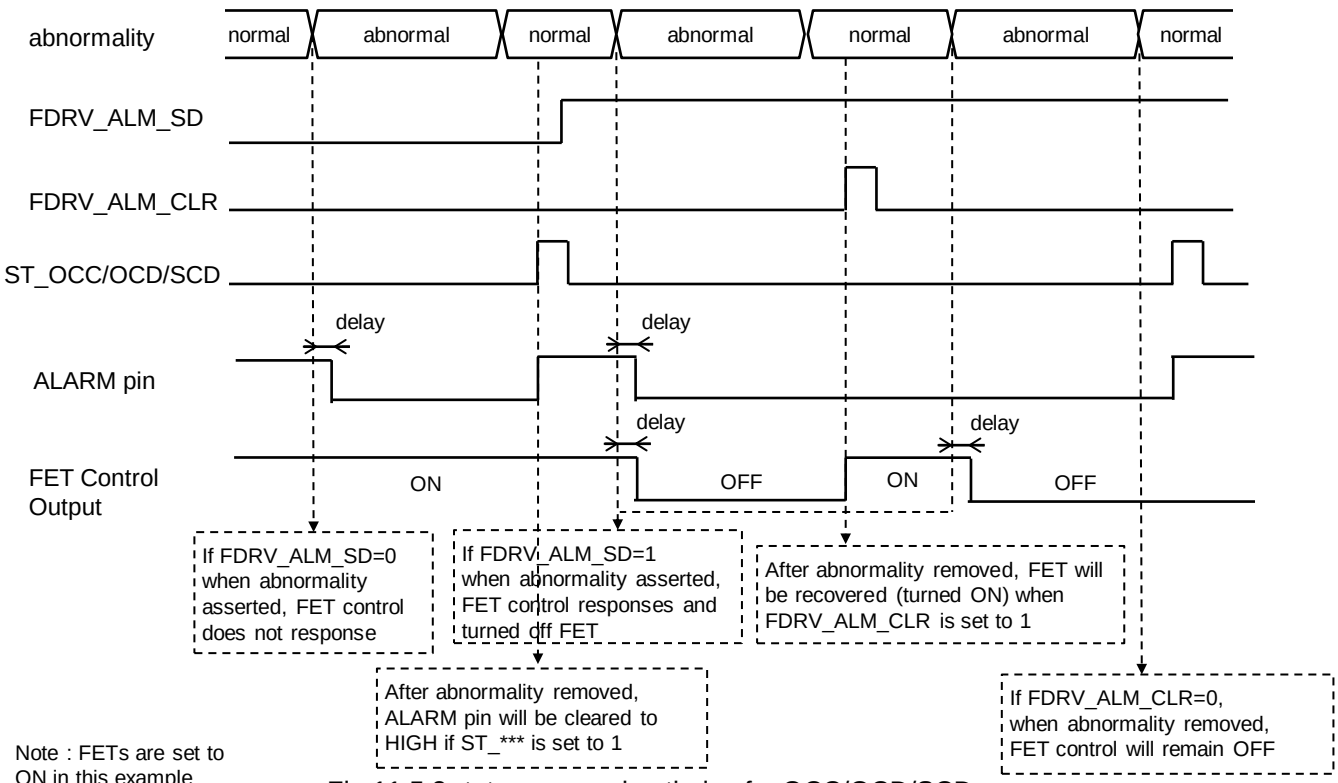


Fig.11.5.2 status processing timing for OCC/OCD/SCD

11.6 Control Output

11.6.1 CHG/DIS pin output

This protection function is for usage of High side N-ch MOSFET.
CHG/DIS pin is controlled according to FDRV_CHG_FET flag (PWR_CTL:bp1) and FDRV_DIS_FET flag (PWR_CTL:bp0) in normal condition, and when alarm is asserted it will be switched to the value described as the following list.
FDRV_OUVCTL flag (FDRV_CTL:bp1) is used to select CHG/DIS pin output when alarm is asserted.

If FET driver is in intermittent operation, Changes of CHG/DIS (On to OFF or OFF to On) will need very long time, so please shift to normal mode if you want change the CHG/DIS. But, when the protection control, it automatically return from the intermittent operation to the normal mode.

Table.11.6.1 Alarm assertion Vs. CHG/DIS pin

	Alarm type	FDRV_OUVCTL=0 (default)		FDRV_OUVCTL=1	
		CHG	DIS	CHG	DIS
Abnormal	UV	-	OFF	OFF	OFF
	OV	OFF	-	OFF	OFF
	OCC	OFF	-	OFF	-
	OCD/SCD	-	OFF	-	OFF

11.6.2 GPOH1/2 pin output

This protection function is for usage of High side P-ch MOSFET.
GPOH1/2 pin is controlled according to GPOH1_EN flag (GPOH_CTL:bp0), GPOH2_EN flag (GPOH_CTL:bp1) in normal condition, and when alarm is asserted it will be switched to the value set by GPOH1_ALM_ST flag (GPOH_CTL:bp4), CPOH2_ALM_ST flag (GPOH_CTL:bp5) described as the following list.
GPOH_FET flag (GPOH_CTL:bp2) should be set to “1” to enable protection output for GPOH1/2.

Table.11.6.2 Alarm assertion Vs. GPOH1/2

	Alarm type	GPOH1	GPOH2
Abnormal	OV/UV OCC/OCD SCD	According to GPOH1_ALM_ST	According to GPOH2_ALM_ST
Normal	-	According to GPOH1_EN	According to GPOH2_EN

11.6.3 GPIO1/2 pin output

Setting Register for GPIO1/2 is the same with GPOH1/2.
GPIO output is enabled by Setting GPIO1SEL flag (GPIOSEL:bp1-0) to “11” and GPIO2SEL flag (GPIOSEL:bp3-2) to “11”.
When alarm is triggered it will be switched to the value described as the following list.

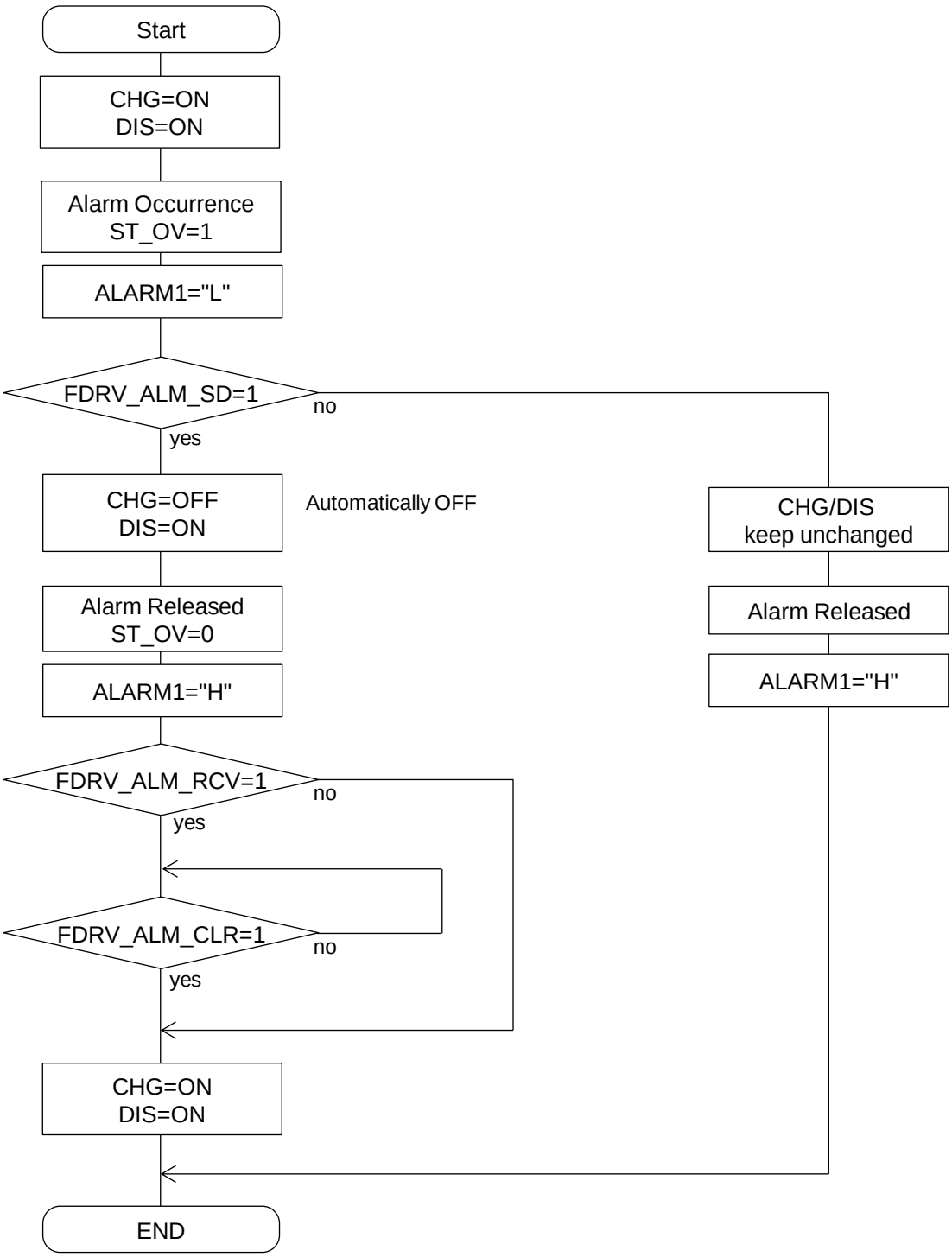
Table.11.6.3 Alarm assertion Vs. GPIO1/2 pin

	Alarm type	GPIO1	GPIO2
Abnormal	OV/UV OCC/OCD SCD	According to GPOH1_ALM_ST flag	According to GPOH2_ALM_ST flag
normal	-	According to GPOH1_EN flag	According to GPOH2_EN flag

11.7 Example for Control Output when Alarm Occurred

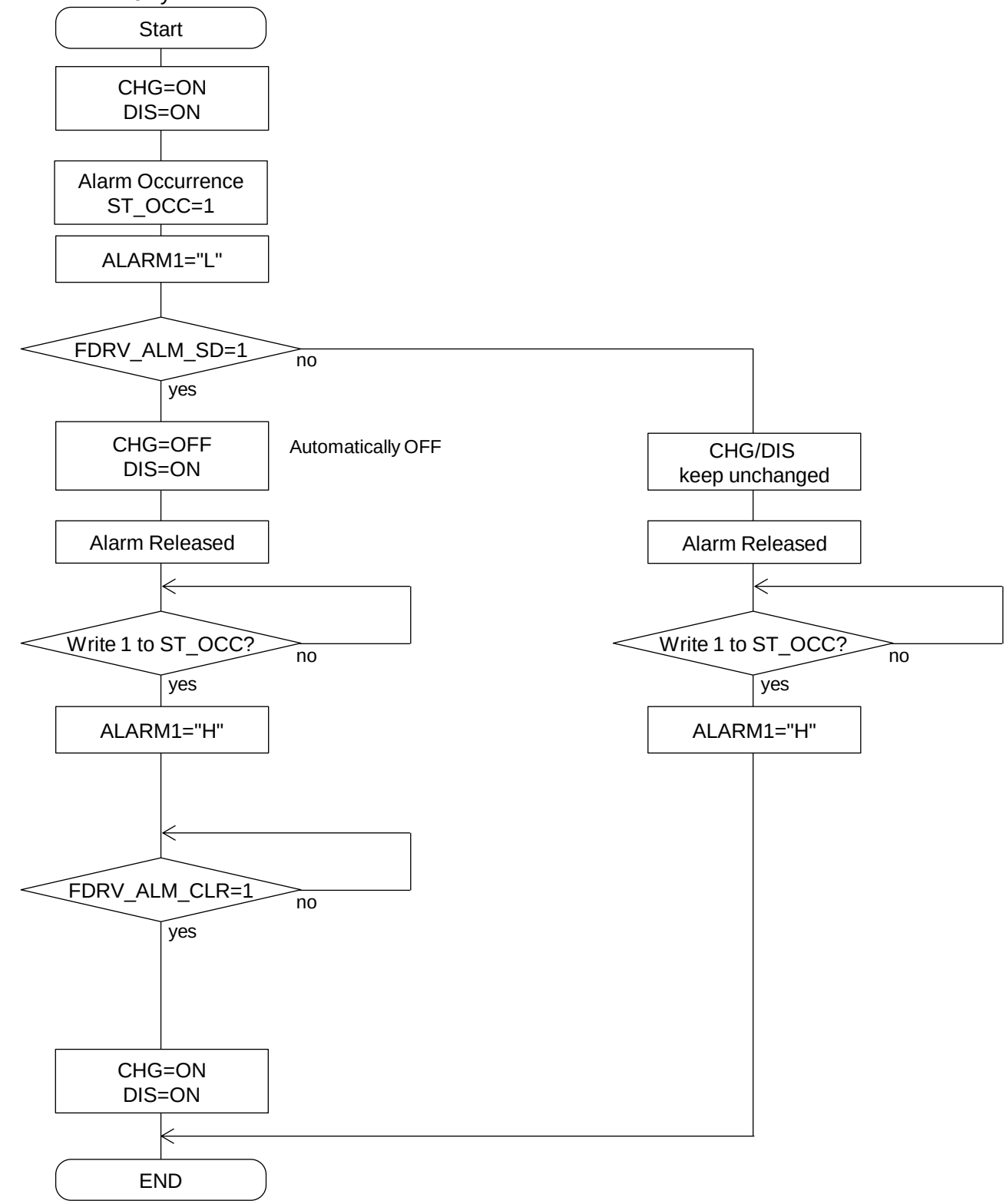
11.7.1 CHG/DIS control flow when OV Alarm Occurred

Ex. ALARM1 only



11.7.2 CHG/DIS Control Flow when OCC Alarm Occurred

Ex. ALARM1 only



Chapter 12 Open Detection

12.1 Description of Open Detection

AN49503A has built-in with open detection function.
This function can be turned ON during Active Mode, and Standby Mode .

Each pins has the current source shown in Fig.12.1.1 .
C0 , C1 pins have the current source (Typ.40μA) pushing to the outside of the IC from the pin.
C2 ~ C16 pins have the current sink (Typ.37μA) pulling into the IC from the pin.
By using these current sources when the open detect function is ON , user can judge whether the wires are open or not by comparing the cell voltages before and after this function.
User can select the pin for detecting by the flag and select multiple detection at the same time.

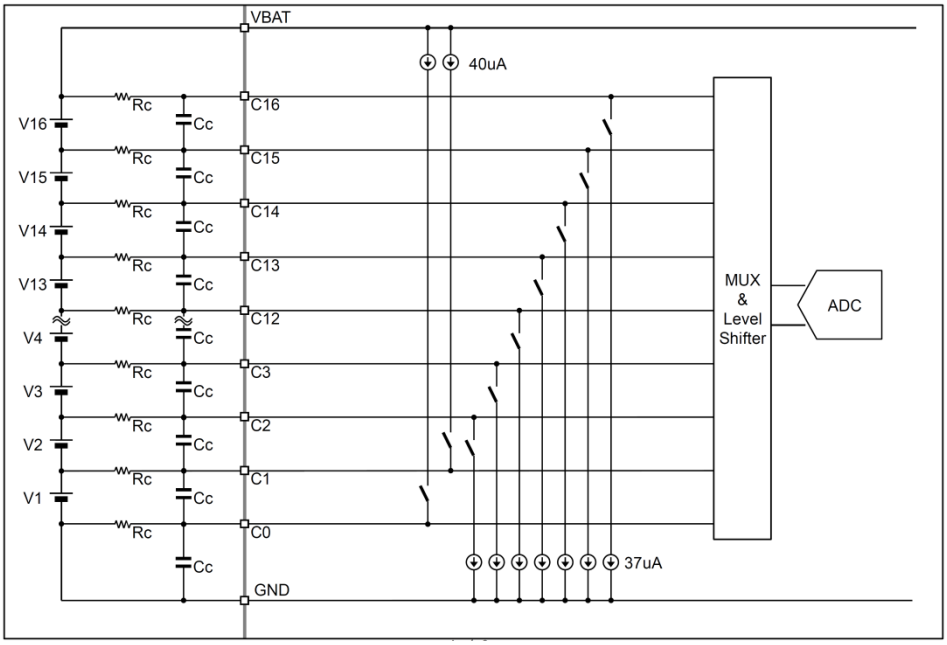


Fig.12.1.1 Open Detection circuit

Open Detection at C0,C1 pins

First, you shall obtain the cell voltage immediately before the open detection function.

If open detection function is done when wire is normal, the voltage of C2 pin decreases and the voltage of C0 , C1 pins shown in Fig.12.1.2(a) increase.

The decrease of voltage at C2 pin is obtained from the multiplication the sink current and the resistance (Rc) at C2 pin.

The increase voltage of C1 and C0 pins are obtained from the multiplication the source current and the resistance (Rc) at C1 and C0 pins.

If C1 pin is open shown in Fig.12.12(b), the voltage of C1 pin increases rather than normal condition by the pushing current and then V1 increase.

If C0 pin is open shown in Fig.12.12(c), the voltage of C0 pin increases rather than normal condition by the pushing current and then V1 decrease.

Then, you shall obtain the cell voltage again after the response time (latency) obtained from the following equation 12-1. If the difference between the two measured cell voltage before and after open detection ON is more than 100mV, it considered that the wire is open.

$$\text{the response time[ms]} = 100 \times Cc[\mu F] \quad (12\text{-}1)$$

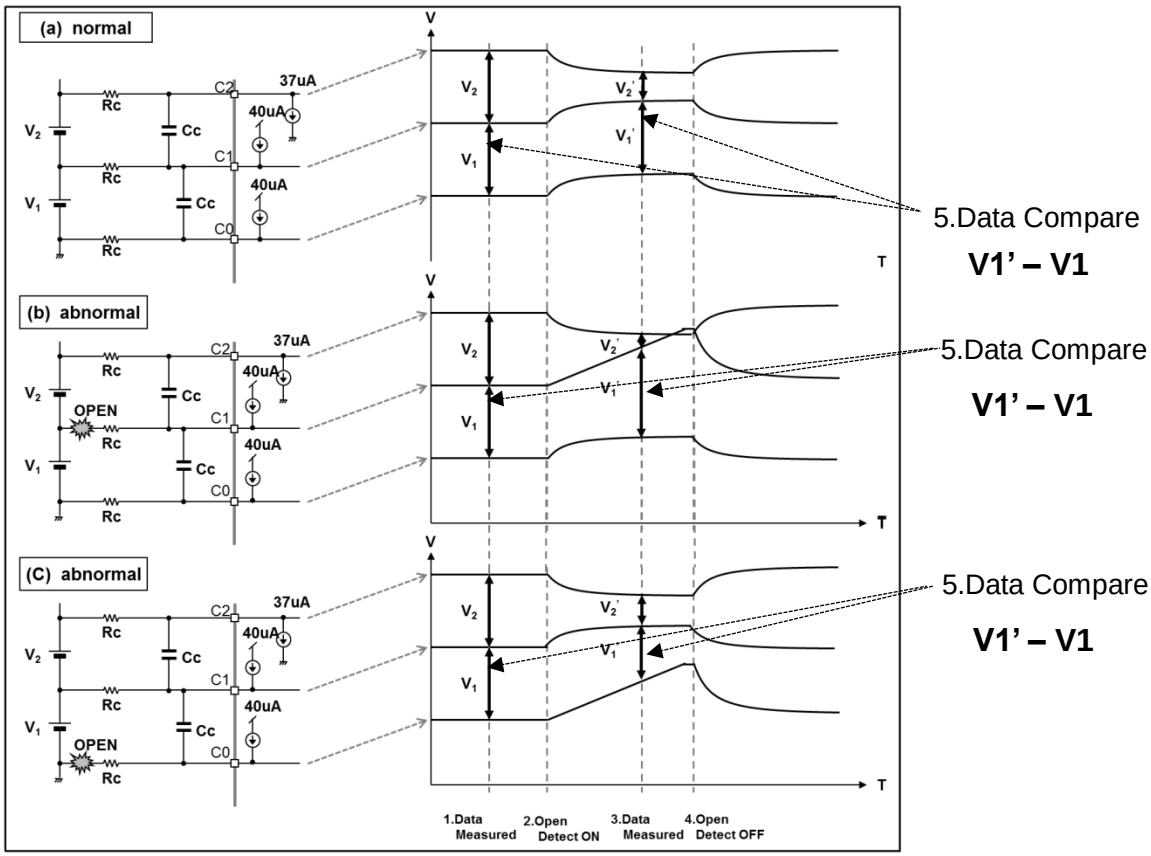


Fig.12.1.2 C0, C1 and C2 pin Voltage on Open Detection(a: normal b,c: abnormal)

Open Detection at C2 pin

Although it is similar to the C1and C0 pins, please note that when comparing the cell voltage.
If open detection with the C1 and C2 pins are done at the same time ,on the polarity of the current source , the decrease voltage of V2 will be Rc x I (Typ.77μA) in spite of normal condition.

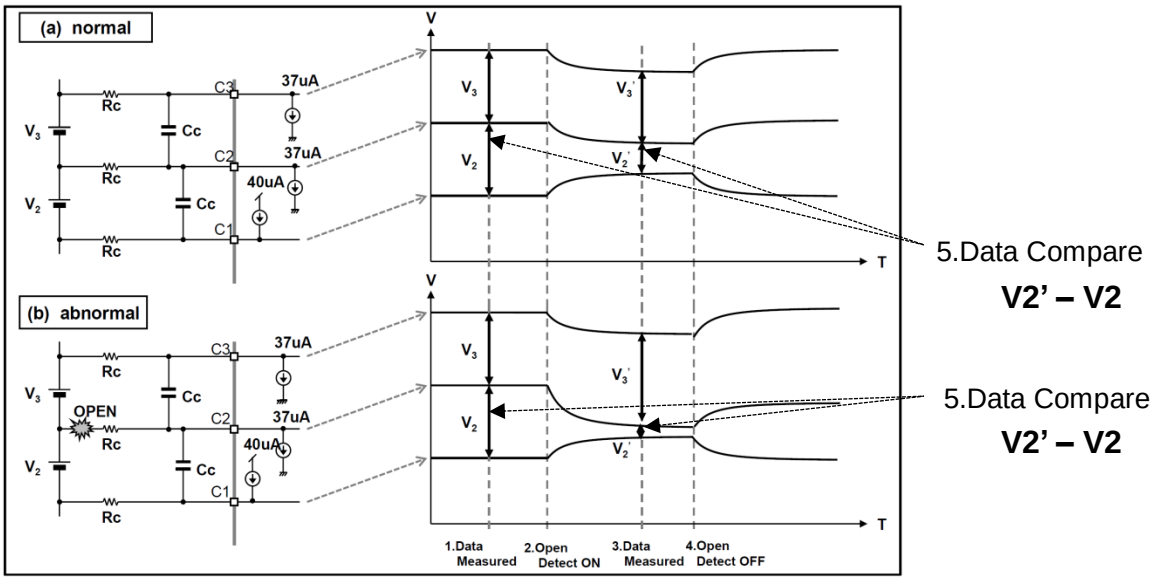


Fig.12.1.3 C2, C3 and C4 Pins Voltage on Open Detection(a: normal b: abnormal)

Open Detection at C3 ~ C16 pins

It is similar to the C1and C0 pins, first you shall obtain the cell voltage immediately before the open detection.

If open detection is done when wire is normal, the voltage of Cn-1 , Cn , and Cn+1 pins decreases and this decrease voltage is obtained from the multiplication the sink current and the resistance (Rc).

If Cn pin is open shown in Fig.12.1.3(b), the voltage of Cn pin decreases rather than normal condition by the sink current and then V_N decrease.

Then, you shall obtain the cell voltage again after the response time (latency) obtained from the following equation 12-2. If the difference between the cell voltage of open detection ON just before and the current result changes more than 100mV , it considered that the wire is open.

$$\text{the response time[ms]} = 100 \times Cc[\mu F] \quad (12\text{-}2)$$

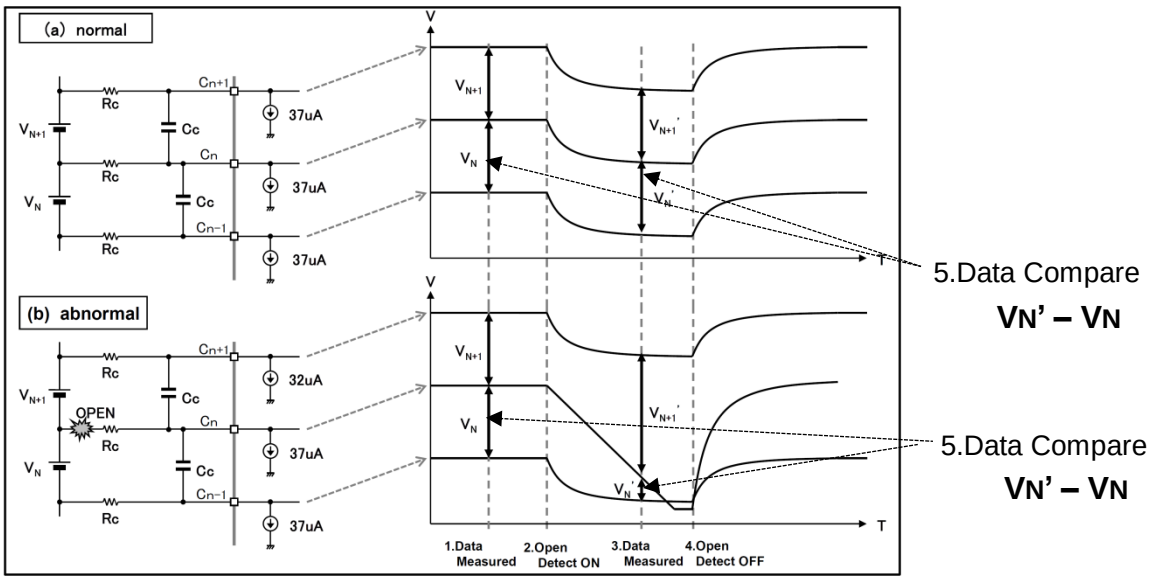


Fig.12.1.4 C3 ~ C16 Pins Voltage on Open Detection(a: normal b: abnormal)

Table.12.1.1 Example of Open Detection judgment

Open	Judgment
C0	$(CV01\_AD)_{before}$ - $(CV01\_AD)_{after}$ > 100mV
C1	$(CV01\_AD)_{after}$ - $(CV01\_AD)_{before}$ > 100mV
C2	$(CV2\_AD)_{before}$ - $(CV2\_AD)_{after}$ > 200mV ※ external resistor (Rc) =1kΩ
C3	$(CV3\_AD)_{before}$ - $(CV3\_AD)_{after}$ > 100mV
C4	$(CV4\_AD)_{before}$ - $(CV4\_AD)_{after}$ > 100mV
C5	$(CV5\_AD)_{before}$ - $(CV5\_AD)_{after}$ > 100mV
C6	$(CV6\_AD)_{before}$ - $(CV6\_AD)_{after}$ > 100mV
C7	$(CV7\_AD)_{before}$ - $(CV7\_AD)_{after}$ > 100mV
C8	$(CV8\_AD)_{before}$ - $(CV8\_AD)_{after}$ > 100mV
C9	$(CV9\_AD)_{before}$ - $(CV9\_AD)_{after}$ > 100mV
C10	$(CV10\_AD)_{before}$ - $(CV10\_AD)_{after}$ > 100mV
C11	$(CV11\_AD)_{before}$ - $(CV11\_AD)_{after}$ > 100mV
C12	$(CV12\_AD)_{before}$ - $(CV12\_AD)_{after}$ > 100mV
C13	$(CV13\_AD)_{before}$ - $(CV13\_AD)_{after}$ > 100mV
C14	$(CV14\_AD)_{before}$ - $(CV14\_AD)_{after}$ > 100mV
C15	$(CV15\_AD)_{before}$ - $(CV15\_AD)_{after}$ > 100mV
C16	$(CV16\_AD)_{before}$ - $(CV16\_AD)_{after}$ > 100mV

Note: This table is an example of detection judgment for 1-line open

12.2 Control Registers

12.2.1 Open Detection Control Registers

Table.12.2.1 shows the registers that control Open Detection.

Table.12.2.1 Open Detection control registers

Register	Address	Function	Page
INR_CTL	0x1E	Open Detection ON/OFF control register	121
INRCV1	0x1C	Selection of Open Detection Pin (C0～C15)	120
INRCV2	0x1D	Selection of Open Detection Pin (C16)	120

12.3 Open Detection Flow

Fig.12.3.1 shows Open Detection Flow

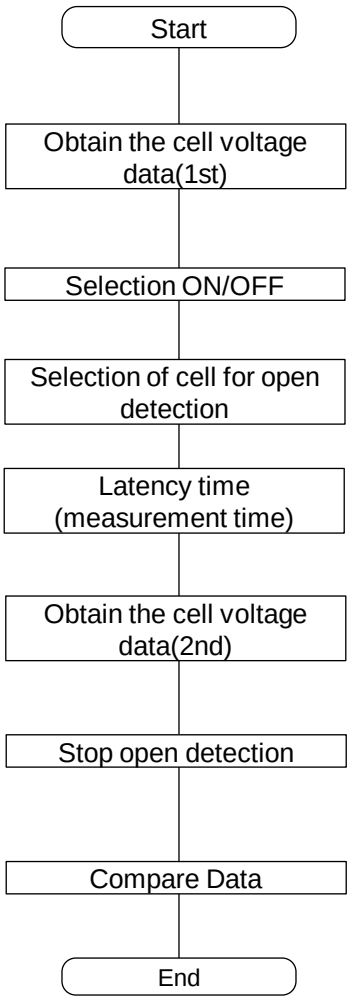


Fig.12.3.1 Open Detection Flow

■Obtain the cell voltage data（1st）
Obtain the cell voltage immediately before the open detection.
(See Chapter 9 voltage measurement)

■ Selection ON/OFF
Set INR_EN flag (INR_CTL:bp0) to “1” to open detection ON

■Selection of cell for open detection
Pin to be performed open detection is set to “1”.
C0～C15 pin
Set INR_CV flag(INR_CV1:bp15-0) to “1”.
INR_CV1 [n] is corresponding to Cn pin.
(e.g. In the case of INR_CV [0]), open detection is done at C0 pin.)
C16 pin
Set INR_CV_16 flag(INR_CV2:bp0) to “1”.

■ Latency time(measurement time)
After previous step (Selection of cell for open detection) starts , latency time is necessary. Latency time is decided by following formula and external Cc shown in Fig.12.1.2.

Latency time [ms] = 100 × Cc[μF]

(e.g. Cc=1uF Latency time is 100ms)

■Obtain the cell voltage data（2nd）
Obtain the cell voltage data again.

■Stop open detection
a. set INR_CV flag(INR_CV1:bp15-0) and INR_CV_16 flag (INR_CV2:bp0) to “0”.
b. set INR_EN flag (INR_CTL:bp0) to “0”.

■Compare Data

Compare the obtained cell voltage data first and second data.
If 100mV or more of the difference was found, it will be considered as open.
※ If open detection with the C1 and C2 pin is done at the same time ,on the polarity of the current source, the decrease voltage of V2 will be Rc x I (Typ.77μA) in spite of normal condition.

※ When the R/WL register control, please implement the LOCK register settings.

Chapter 13 SPI Communication Interface

13.1 Description of SPI Communication Interface

AN49503A communicates with MCU using four lines SPI communication interface, with SDI, SDO, SCL and SEN pins.
Refer table below for SPI function.

Table.13.1.1 SPI communication function

Use Pin	SDO(Data output: 73pin), SDI(Data input: 74pin) SCL(Clock input: 75pin) SEN(Enable input: 76pin)	
Communication mode	Data Writing(2 byte) Data writing to the set address	
	Data Reading(2 byte) Data readout to the set address	
	Continuous Reading(2 byte * M) Data reading of n consecutive addresses from set address	
Communication Time	Data Writing	$(1/f_{SCK} * 40) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$
	Data Reading	$(1/f_{SCK} * 48) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$
	Continuous Reading	$(1/f_{SCK} * (40+(16 * M))) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$
Polynomial for CRC	$X^8+X^7+X^6+X^4+X^2+1$	
Communication error detection	Output SDO Pin(When the error "L" output) Output STATUS Flag(SPI_F(SPI_STAT:bp14))	
SPI Watchdog Timer	Configurable Time : 1 ~ 4096s (Default:60s)	

M : continuous read data number
t_{SEN_xx} : delay time for communication (refer to electrical characteristic)

13.2 Control Registers

13.2.1 Registers

Table.13.2.1 shows the registers that control SPI.

Table.13.2.1 SPI Control Registers

Register	Address	Function	Page
SPIWD_CTL	0x02	SPI watchdog timer control register	100
SPICTL	0x18	Communication・VDD50 LDO Power Mode Control register	116
SPI_STAT	0x21	SPI Status register	122

13.3 Communication mode

AN49503A has built-in with the following communication mode.
- Data Writing(2bytes)
- Data Reading(2bytes)
- Continuous Reading(2bytes * M)

It is able to communicate by the following behavior.

When wake up to Active Mode from Shutdown Mode, SDO will change from “L” to “H”, indicating AN49503A is ready for communication, communication can be started after 500ns.

SDO pin is used to indicate the correctness of communication, when there is error with the communication, SDO pin will become “L”.
To find out the reason of the error, read the SPI_F flag(SPI_STAT:bp14).
Please set the always "1110000" the beginning 7bit of transmitted data.

13.3.1 Data Writing(2bytes)

The figure below is the timing chart of Data Writing(2 Bytes).

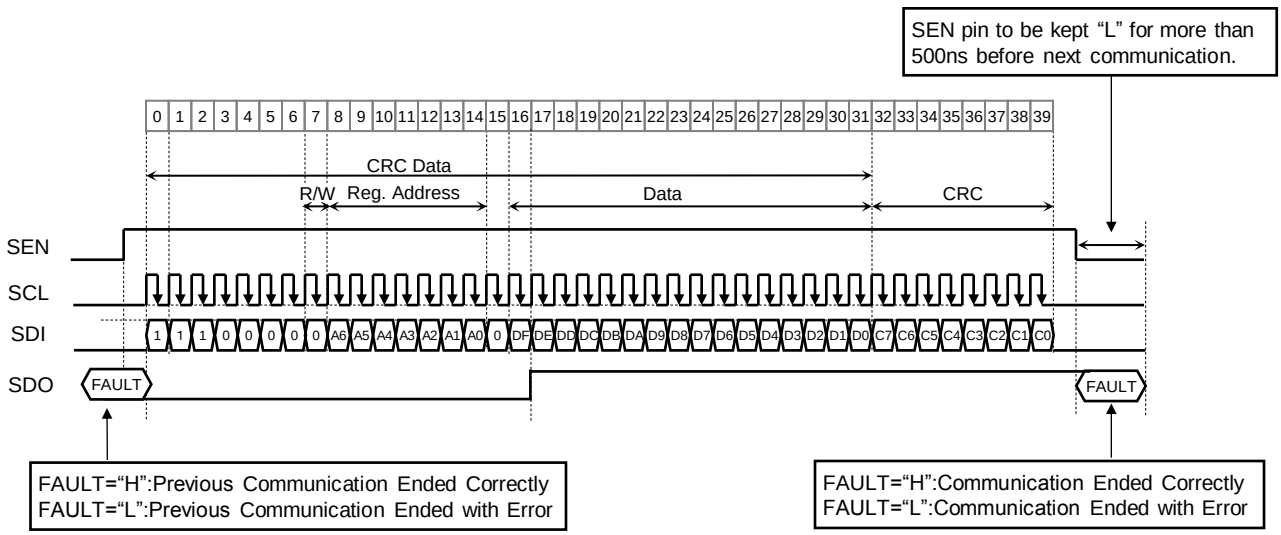


Fig.13.3.1 Data Communication Control Timing <Data Writing(2 Bytes)>

13.3.2 Data Reading(2bytes)

The figure below is the timing chart of Data Reading(2 Bytes).

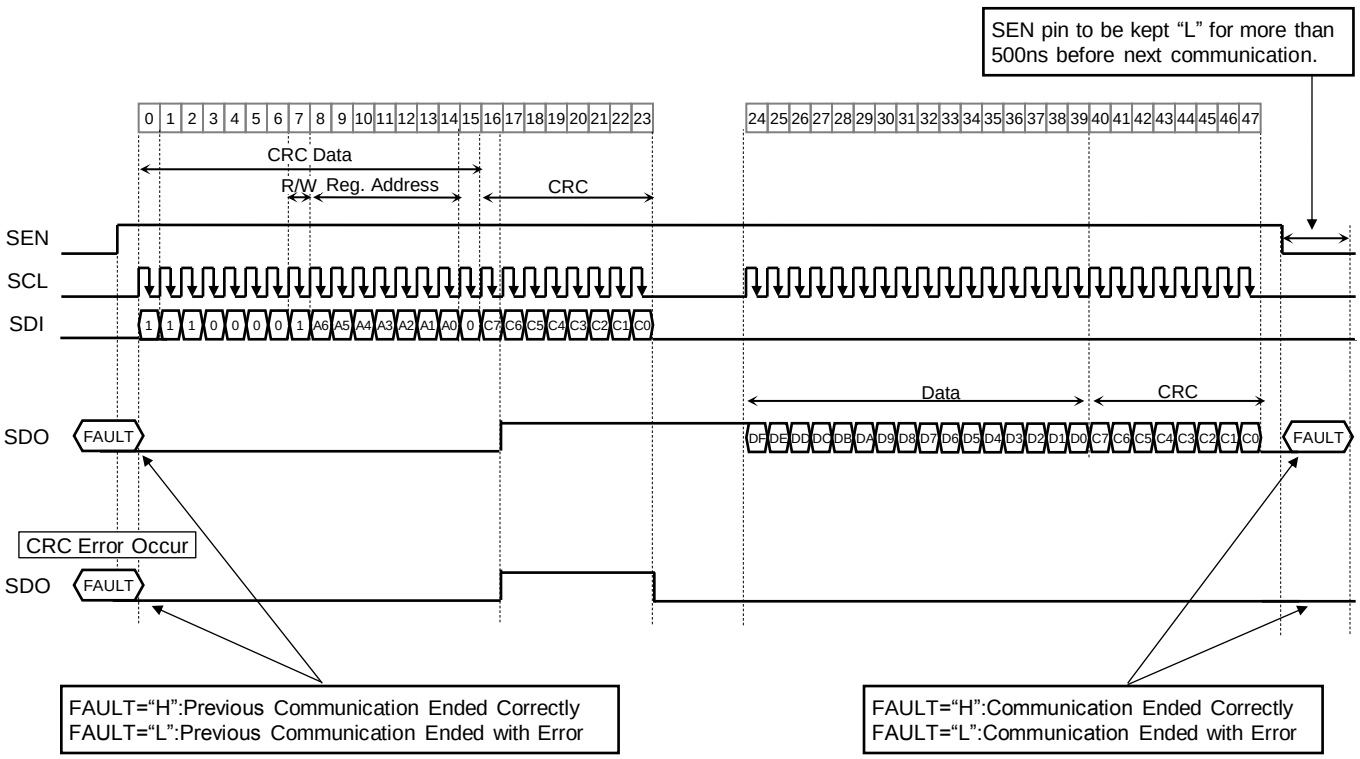


Fig.13.3.2 Data Communication Control Timing <Data Reading(2 Bytes)>

13.3.3 Continuous Reading(2bytes * M)

The figure below is the timing chart of Continuous Reading (2bytes * M).

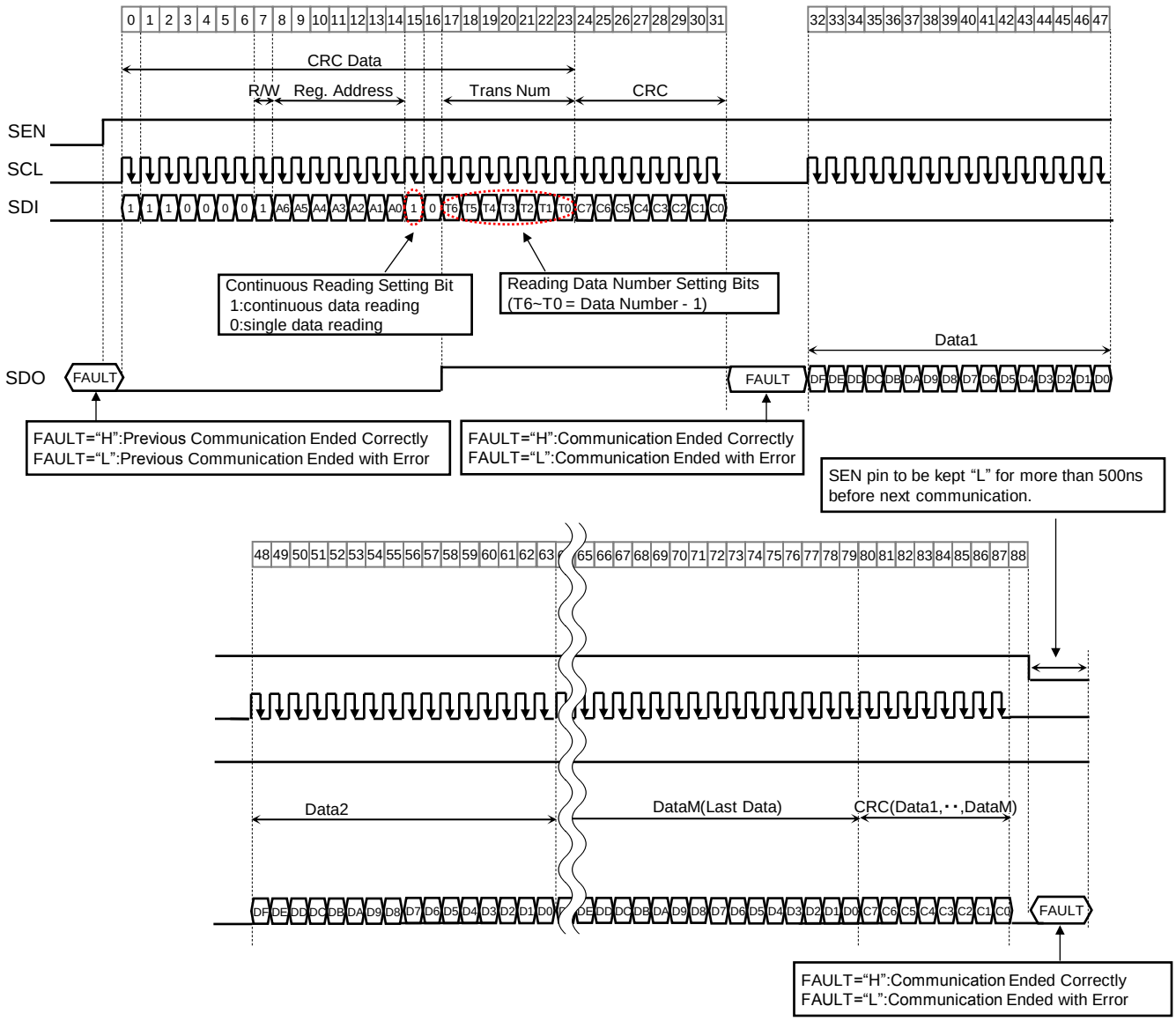


Fig.13.3.3 Data Communication Control Timing <Continuous Reading (2byte × M) >

13.4 Communication Time

Table below listed required time for communication at different operation.

Table.13.4.1 Time for communication at different operation

Communication	MCU - AN49503A Communication Time
Data Writing	$(1/f_{SCK} * 40) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$
Data Reading	$(1/f_{SCK} * 48) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$
Continuous Reading	$(1/f_{SCK} * (40+(16 * M))) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$

M : continuous read data number
t_{SEN_xx} : delay time for communication (refer to electrical characteristic)

13.5 Communication Error

During communication, SDO pin become “L” when communication error occur.
To find out the reason of the error, read the SPI_F flag (SPI_STAT:bp14).

13.6 Watchdog Timer

AN49503A will shutdown when no communication between MCU and the IC is made in set time.
Refer to Chapter 3 operating mode for Shutdown mode.

Watchdog Timer Timing Setting is set by the SPI_WDTCOUNT[11:0] flag (SPIWD_CTL:bp11-0).
When set the COMTIMON flag (SPIWD_CTL:bp12) to “1”, Watchdog Timer will be enabled.
Do not change Watchdog Timer Timing Setting when Watchdog Timer is in operation.

13.7 Communication OFF control

This IC is possible to reduce the power consumption of SPI circuit in standby mode.
It can reduce the power of the SPI communication by writing "1" to the COM_STP flag(SPICTL: bp0).
To resume communication, enter “H” to SEN pin for more than 1ms.
This communication OFF control can not run except in Standby mode.

Chapter 14 Registers

14.1 Description of Registers

This IC is equipped with registers for control, status and data. Each register consists of 16 bits flag. The accessibility of each flag is defined as:

- R : Readable
- R/W : Readable and writable always
- R/WL : Readable always and writable only when register LOCK_CONT flag (LOCK:bp15-0) = 0xE3B5

14.1.1 Write-protect registers(R/WL Registers)

This IC is equipped with write-protected registers(R/WL Registers).
To write to a R/WL register, data "0xE3B5“ needed to be written to LOCK_CONT flag (LOCK:bp15-0) first.

Table.14.3.1 Unlock code setting register

Register	Address	Function	Page
LOCK	0x0B	Unlock code setting register	108

14.2 Control Registers

It lists the registers and the register map below.

Table.14.2.1 Control Registers1

Register	Address	Function	R/W/WL
<Reserved>	0x00	<Reserved>	-
PWR_CTL	0x01	Mode of Operation・FET Driver Operation Control register	R/W
SPIWD_CTL	0x02	SPI watchdog timer control register	R/WL
FDRV_CTL	0x03	FET Driver Setting register	R/W
CVSEL	0x04	Respective cell voltage measurement ON/OFF setting register	R/WL
GVSEL	0x05	Other voltage measurement ON/OFF setting register	R/WL
OUVCTL1	0x06	OV/UV setting 1 register	R/WL
OUVCTL2	0x07	OV/UV setting 2 register	R/WL
UVMSK	0x08	UV detection setting register	R/WL
OVMSK	0x09	OV detection setting register	R/WL
OP_MODE	0x0A	ADC Operation register	R/W
LOCK	0x0B	Unlock code setting register	R/W
GPIO_CTL1	0x0C	GPIO control register 1	R/W
GPIO_CTL2	0x0D	GPIO control register 2	R/W
GPIO_CTL3	0x0E	GPIO control register 3	R/W
GPIO_CTL4	0x0F	GPIO control register 4	R/W
<Reserved>	0x10	<Reserved>	-
ALARM_CTL1	0x11	Alarm Control 1 register	R/WL
ALARM_CTL2	0x12	Alarm Control 2 register	R/WL
ALARM_CTL3	0x13	Alarm Control 3 register	R/W
CB_CTL	0x14	Cell Balance Control register	R/W
CBSEL	0x15	Cell selection for cell balance register	R/WL
<Reserved>	0x16	<Reserved>	-
GPIOSEL	0x17	GPIO output control register	R/WL
SPICTL	0x18	Communication・VDD50 LDO Power Mode Control register	R/W
ADCTL1	0x19	ADC control register1	R/WL
ADCTL2	0x1A	ADC control register2	R/WL
GPOH_CTL	0x1B	GPOH control register	R/WL

Table.14.2.2 Control Registers2

Register	Address	Function	R/W/WL
INRCV1	0x1C	Line selection 1 for Disconnection detection register	R/WL
INRCV2	0x1D	Line selection 2 for Disconnection detection register	R/WL
INR_CTL	0x1E	Disconnection detection ON/OFF register	R/WL
<Reserved>	0x1F～0x20	<Reserved>	-
SPI_STAT	0x21	SPI Status register	R/WL
MODE_STAT	0x22	Operation Mode Status register	R
<Reserved>	0x23～0x2D	<Reserved>	-
FUSE_RADR	0x2E	Address setting for FUSE Read address setting register	R/W
FUSE_DATA	0x2F	FUSE read data register	R
STAT	0x30	ADC/ALARM Status register	R/W
OVSTAT	0x31	OV Status register	R
UVSTAT	0x32	UV Status register	R
CV01_AD	0x33	Voltage measurement result for cell 1 register	R
CV02_AD	0x34	Voltage measurement result for cell 2 register	R
CV03_AD	0x35	Voltage measurement result for cell 3 register	R
CV04_AD	0x36	Voltage measurement result for cell 4 register	R
CV05_AD	0x37	Voltage measurement result for cell 5 register	R
CV06_AD	0x38	Voltage measurement result for cell 6 register	R
CV07_AD	0x39	Voltage measurement result for cell 7 register	R
CV08_AD	0x3A	Voltage measurement result for cell 8 register	R
CV09_AD	0x3B	Voltage measurement result for cell 9 register	R
CV10_AD	0x3C	Voltage measurement result for cell 10 register	R
CV11_AD	0x3D	Voltage measurement result for cell 11 register	R
CV12_AD	0x3E	Voltage measurement result for cell 12 register	R
CV13_AD	0x3F	Voltage measurement result for cell 13 register	R
CV14_AD	0x40	Voltage measurement result for cell 14 register	R
CV15_AD	0x41	Voltage measurement result for cell 15 register	R
CV16_AD	0x42	Voltage measurement result for cell 16 register	R

Table.14.2.3 Control Registers3

Register	Address	Function	R/W/WL
VPACK_AD	0x43	Voltage measurement result for VPACK register	R
TMONI1_AD	0x44	Voltage measurement result for TMONI1 register	R
TMONI2_AD	0x45	Voltage measurement result for TMONI2 register	R
TMONI3_AD	0x46	Voltage measurement result for TMONI3 register	R
TMONI4_AD	0x47	Voltage measurement result for TMONI4 register	R
TMONI5_AD	0x48	Voltage measurement result for TMONI5 register	R
VDD50_AD	0x49	Voltage measurement result for VDD50 register	R
GPIO1_AD	0x4A	Voltage measurement result for GPIO1 register	R
GPIO2_AD	0x4B	Voltage measurement result for GPIO2 register	R
CVIH_AD	0x4C	High speed current ADC measurement result register	R
CVIL_AD	0x4D	Low speed current ADC measurement result register	R
<Reserved>	0x4E～0x51	<Reserved>	-
OVL_STAT	0x52	OV detection flag register	R
UVL_STAT	0x53	UV detection flag register	R
CVDD_STAT	0x54	CVDD status register	R
FDRVSTAT	0x55	FET Driver status register	R
CBSTAT	0x56	Cell balance operation status register	R
<Reserved>	0x57～0x7F	<Reserved>	-

Table.14.2.4 Control Registers MAP1

Register		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
PWR_CTL	Flag	-	-	-	-	-	-	STB_MONEN	ADC_CONT	MSET_SHDN	NPD_RST	-	-	NPD_FDRV	FDRV_LPWR	FDRV_CHG_FET	FDRV_DIS_FET
0X01	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Initial	0x0048	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0
SPIWD_CTL	Flag	-	-	-	COMTIMON	SPI_WDTCOUNT[11:0]											
0x02	R/W	R	R	R	R/WL	R/WL											
Initial	0x103B	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1
FDRV_CTL	Flag	FDRV_ALM_SD	FDRV_ALM_RCV	FDRV_ALM_CLR	-	<Reserved>	<Reserved>	<Reserved>	FDRV_STBY	-	-	-	FDRV_LEVEL[2:0]			FDRV_OUVCTL	<Reserved>
0x03	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CVSEL	Flag	CV[16:1]SEL															
0x04	R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
Initial	0xFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
GVSEL	Flag	<Reserved>	<Reserved>	<Reserved>	<Reserved>	-	<Reserved>	<Reserved>	GPAD2SEL	GPAD1SEL	VDD50SEL	TMONI5SEL	TMONI4SEL	TMONI3SEL	TMONI2SEL	TMONI1SEL	VPACKSEL
0x05	R/W	R/WL	R/WL	R/WL	R/WL	R	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
Initial	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
OUVCTL1	Flag	-	-	OVTH[5:0]						-	-	UVTH[5:0]					
0x06	R/W	R	R	R/WL						R	R	R/WL					
Initial	0x3400	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
OUVCTL2	Flag	OVHLMT	OV_HYS[2:0]			-	UV_HYS[2:0]			-	-	OV_DLY[1:0]		-	-	UV_DLY[1:0]	
0x07	R/W	R/WL	R/WL			R	R/WL			R	R	R/WL		R	R	R/WL	
Initial	0x8000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
UVMSK	Flag	UVMSK[16:1]															
0x08	R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OVMSK	Flag	OVMSK[16:1]															
0x09	R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OP_MODE	Flag	-	<Reserved>	-	-	-	-	<Reserved>	CB_SET	-	-	-	ADC_TRG	-	ADIL_LATCH	ADIH_LATCH	ADV_LATCH
0x0A	R/W	R	R/W	R	R	R	R	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W
Initial	0x4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LOCK	Flag	LOCK_CONT[15:0]															
0x0B	R/W	R/W															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIO_CTL1	Flag	-	-	GPIO6_NOE	GPIO5_NOE	GPIO4_NOE	GPIO3_NOE	GPIO2_NOE	GPIO1_NOE	-	-	GPIO6_IE	GPIO5_IE	GPIO4_IE	GPIO3_IE	GPIO2_IE	GPIO1_IE
0x0C	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial	0x3F00	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
GPIO_CTL2	Flag	-	-	GPIO6_OD	GPIO5_OD	GPIO4_OD	GPIO3_OD	GPIO2_OD	GPIO1_OD	-	-	GPIO6_PD	GPIO5_PD	GPIO4_PD	GPIO3_PD	GPIO2_PD	GPIO1_PD
0x0D	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIO_CTL3	Flag	-	-	ST_GPIO6	ST_GPIO5	ST_GPIO4	ST_GPIO3	ST_GPIO2	ST_GPIO1	-	-	GPIO6_OUT	GPIO5_OUT	GPIO4_OUT	GPIO3_OUT	GPIO2_OUT	GPIO1_OUT
0x0E	R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIO_CTL4	Flag	-	-	-	PULLUP_SEL[5:1]					-	-	GPIO6_CHDRV	GPIO5_CHDRV	GPIO4_CHDRV	GPIO3_CHDRV	GPIO2_CHDRV	GPIO1_CHDRV
0x0F	R/W	R	R	R	R/W					R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ALARM_CTL1	Flag	ALARMSEL	-	<Reserved>	<Reserved>	-	-	<Reserved>	<Reserved>	-	-	-	-	EN_SCD	EN_OCD	EN_OCC	EN_CP
0x11	R/W	R/WL	R	R/WL	R/WL	R	R	R/WL	R/WL	R	R	R	R	R/WL	R/WL	R/WL	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note : 1. Registers address not listed is reserved registers, user shall not change value of these registers
2. There are three access category for each flag:
R : Readable
R/W : Readable and writable always
R/WL : Readable always and writable only when register LOCK_CONT flag (LOCK:bp15-0) = 0xE3B5

Table.14.2.5 Control Registers MAP2

Register		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ALARM_CTL2	Flag	-	-	SCD_D[3:0]				OCD_D[4:0]						OCC_D[4:0]			
0x12	R/W	R	R	R/WL				R/WL						R/WL			
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ALARM_CTL3	Flag	-	SCD_DLY[4:0]					-	OCD_DLY[3:0]				-	OCC_DLY[3:0]			
0x13	R/W	R	R/WL					R	R/WL				R	R/WL			
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CB_CTL	Flag	-	-	-	-	-	-	-	-	-	-	-	CB_PROTECT	-	-	<Reserved>	CB_PD
0x14	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W
Initial	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
CBSEL	Flag	DI_CBSEL[16:1]															
0x15	R/W	R/WL															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIOSEL	Flag	-	-	OSC2_DIV[1:0]		GPIO6SEL[1:0]		GPIO5SEL[1:0]		GPIO4SEL[1:0]		GPIO3SEL[1:0]		GPIO2SEL[1:0]		GPIO1SEL[1:0]	
0x17	R/W	R	R	R/WL		R/WL		R/WL		R/WL		R/WL		R/WL		R/WL	
Initial	0x0000	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
SPICTL	Flag	-	-	<Reserved>	<Reserved>	-	SDI_PLDW	SCL_PLDW	SEN_PLDW	-	-	<Reserved>	LP50EN	-	-	-	COM_STP
0x18	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W
Initial	0x0700	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
ADCTL1	Flag	<Reserved>	<Reserved>	<Reserved>		<Reserved>		-	-	<Reserved>	<Reserved>	ADI_LATCH_SET	ADV_LATCH_SET	-	<Reserved>	<Reserved>	<Reserved>
0x19	R/W	R/WL	R/WL	R/WL		R/WL		R	R	R/WL	R/WL	R/WL	R/WL	R	R/WL	R/WL	R/WL
Initial	0x0C87	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0
ADCTL2	Flag	-	-	ADSWHY_EN	ADSWSD_EN	-	-	-	-	<Reserved>	<Reserved>	<Reserved>	ISD_STOPEN	-	-	ADIL_ON	ADIH_ON
0x1A	R/W	R	R	R/WL	R/WL	R	R	R	R	R/WL	R/WL	R/WL	R/WL	R	R	R/WL	R/WL
Initial	0x0030	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
GPOH_CTL	Flag	-	-	-	-	-	-	-	-	-	-	GPOH2_ALM_ST	GPOH1_ALM_ST	-	GPOH_FET	GPOH2_EN	GPOH1_EN
0x1B	R/W	R	R	R	R	R	R	R	R	R	R	R/WL	R/WL	R	R/WL	R/WL	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INRCV1	Flag	INR_CV_[15:0]															
0x1C	R/W	R/WL															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INRCV2	Flag	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	INR_CV_16
0x1D	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INR_CTL	Flag	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	INR_EN
0x1E	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WL
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPI_STAT	Flag	-	SPI_F	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0x21	R/W	R	R/WL	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MODE_STAT	Flag	-	-	-	-	-	-	-	-	-	-	COND_SCD	COND_OCD	COND_OCC	ST_SDWN	ST_STBY	ST_ACT
0x22	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x000x	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X
FUSE_RADR	Flag	-	-	-	-	-	-	-	-	FUSE_RADR[7:0]							
0x2E	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FUSE_DATA	Flag	FUSE_DATA[15:0]															
0x2F	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0xxxxx	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Note : 1. Register address not listed is reserved register, user shall not change value of these registers
2. There are three access category for each flag:
R : Readable
R/W : Readable and writable always
R/WL : Readable always and writable only when register LOCK_CONT flag (LOCK:bp15-0) = 0xE3B5

Table.14.2.6 Control Registers MAP3

Register		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
STAT	Flag	-	-	-	-	-	-	ST_OV	ST_UV	-	ST_SCD	ST_OCD	ST_OCC	-	IADS_DONE	IADH_DONE	VAD_DONE
0x30	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OVSTAT	Flag	OV16_F	OV15_F	OV14_F	OV13_F	OV12_F	OV11_F	OV10_F	OV9_F	OV8_F	OV7_F	OV6_F	OV5_F	OV4_F	OV3_F	OV2_F	OV1_F
0x31	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
UVSTAT	Flag	UV16_F	UV15_F	UV14_F	UV13_F	UV12_F	UV11_F	UV10_F	UV9_F	UV8_F	UV7_F	UV6_F	UV5_F	UV4_F	UV3_F	UV2_F	UV1_F
0x32	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CVn_AD	Flag	CV01_AD[15:0] ~ CV16_AD[15:0]															
0x33~0x42	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VPACK_AD	Flag	VPACK_AD[15:0]															
0x43	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TMONIn_AD	Flag	TMONI1_AD[15:0] ~ TMONI5_AD[15:0]															
0x44~0x48	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VDD50_AD	Flag	VDD50_AD[15:0]															
0x49	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIO1_AD	Flag	GPIO1_AD[15:0]															
0x4A	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIO2_AD	Flag	GPIO2_AD[15:0]															
0x4B	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CVIH_AD	Flag	CVIH_AD[15:0]															
0x4C	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CHIL_AD	Flag	CVIL_AD[15:0]															
0x4D	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OVL_STAT	Flag	OV[16:1]_LF															
0x52	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
UVL_STAT	Flag	UV[16:1]_LF															
0x53	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CVDD_STAT	Flag	-	-	-	-	-	-	-	-	-	-	-	-	-	CVDD_UV	-	-
0x54	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0xx0	0	0	0	0	0	0	X	X	0	0	0	X	0	0	0	0
FDRV STAT	Flag	-	-	-	-	-	-	-	-	-	-	-	-	FDRV_DIS_ST	FDRV_CHG_ST	GPOH2_ST	GPOH1_ST
0x55	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CBSTAT	Flag	CB_ST[16:1]															
0x56	R/W	R															
Initial	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note : 1. Register address not listed is reserved register, user shall not change value of these registers
2. There are three access category for each flag :
R : Readable
R/W : Readable and writable always
R/WL : Readable always and writable only when register LOCK_CONT flag (LOCK:bp15-0) = 0xE3B5

14.3 Control register details

■Operation Mode・FET Driver Operation control register (PWR_CTL:0x01)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	-	-	-	STB_MONEN	ADC_CONT
R/W	R	R	R	R	R	R	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	MSET_SHDN	NPD_RST	-	-	NPD_FDRV	FDRV_LPWR	FDRV_CHG_FET	FDRV_DIS_FET
R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Initial	0	1	0	0	1	0	0	0

bit	Flag	explanation
15-10	-	
9	STB_MONEN	Enable for Standby Mode Monitoring/Measurement 1:During Standby Mode, when no SPI communication occurs for more than 1s, it is automatically switched to Active Mode and performs voltage measurement. Subsequently, it resumes to standby mode after measurement, please refer to specification in section 2. 0:No Voltage Monitoring/Measurement in Standby Mode * Please set to 0 whenever the ADC_CONT = 0
8	ADC_CONT	ADC Operation Setting 1:Voltage and HS current measurement is performed during Active Mode. Once this bit is set, measurement will be done repeatedly. 0:Voltage and HS Current Measurement are performed only when register (0x0a) ADC_TRG = 1
7	MSET_SHDN	Shutdown Control 1:Shutdown Mode, only function when VPC is LO. 0:Normal operation
6	NPD_RST	Soft Reset 1:Normal operation 0:Reset Auto recovery to “1” after "0“ is written.
5-4	-	
3	NPD_FDRV	High Side (CHG/DIS) NMOSFET Power Down 1:Normal 0:Power Down
2	FDRV_LPWR	High Side (CHG/DIS) NMOSFET Power Mode 1:Low Power Mode 0:Normal
1	FDRV_CHG_FET	High Side (CHG) NMOSFET ON/OFF 1:FET ON 0:FET OFF
0	FDRV_DIS_FET	High Side (DIS) NMOSFET ON/OFF 1:FET ON 0:FET OFF

■ SPI watchdog timer control register (SPIWD_CTL:0x02)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	COMTIMON	SPI_WDTCOUNT[11:8]			
R/W	R	R	R	R/WL	R/WL			
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	SPI_WDTCOUNT[7:0]							
R/W	R/WL							
Initial	0	0	1	1	1	0	1	1

bit	Flag	explanation
15-13	-	
12	COMTIMON	Watchdog Timer ON/OFF Control 1:ON 0:OFF (Default)
11-0	SPI_ WDTCOUNT [11:0]	Watchdog Timer Timing Setting Time = (value +1) x 1 s (range 1~4096s) SPI_WDTCOUNT[11:0] = 0x03B:60s (Default)

Note: Do not change Watchdog Timer Timing Setting when Watchdog Timer is in operation.

■ FET Drive control register(FDRV_CTL:0x03)

bit	15	14	13	12	11	10	9	8
Flag	FDRV_ALM_SD	FDRV_ALM_RCV	FDRV_ALM_CLR	-	<Reserved>	<Reserved>	<Reserved>	FDRV_STBY
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	-	FDRV_LEVEL[2:0]			FDRV_OUV CTL	<Reserved>
R/W	R	R	R	R/W			R/W	R/W
Initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15	FDRV_ALM_SD	CHG/DIS FET and GPOH pins response to ALARM condition 1:CHG/DIS FET auto OFF and GPOH become value set, refer to specification section 11 CHG FET OFF:OV/UV/OCC DIS FET OFF:OV/UV/OCD/SCD) 0:CHG/DIS FET and GPOH no response to ALARM condition
14	FDRV_ALM_RCV	CHG/DIS FET and GPOH pins recover when ALARM(OV/UV) condition removed (when FDRV_ALM_SD = 1) with the following setting. 1:Depend on FDRV_ALM_CLR 0:Recover when ALARM(OV/UV) condition is removed.
13	FDRV_ALM_CLR	CHG/DIS FET and GPOH pins recover when ALARM(OV/UV/OCD/OCC/SCD) condition removed (when FDRV_ALM_SD = 1 & FDRV_ALM_RCV=1) 1:CHG/DIS FET and GPOH pins recover 0:No change * This bit is not cleared automatically. * If ALARM condition continue and this bit is set, CHS/DIS FET remains OFF.
12	-	
11-9	<Reserved>	Please always set to “0”.
8	FDRV_STBY	FET Driver Standby Control 1:Standby 0:Normal
7-5	-	
4-2	FDRV_LEVEL[2:0]	Setting of External FET drive voltage 111:-7V 110:-6V 101:-5V 100:-4V 011:-3V 010:-2V 001:-1V 000: 0V
1	FDRV_OUV CTL	CHG/DIS FET OFF mode setting when alarm is asserted 1:both of CHG/DIS FET OFF when OV or UV 0:CHG FET OFF when OV, DIS FET OFF when UV (default)
0	<Reserved>	Please always set to “0”.

■ Respective cell voltage measurement ON/OFF setting register (CVSEL:0x04)

bit	15	14	13	12	11	10	9	8
Flag	CV[16:19]SEL							
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	1	1	1	1	1	1	1	1

bit	7	6	5	4	3	2	1	0
Flag	CV[8:1]SEL							
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	1	1	1	1	1	1	1	1

bit	Flag	explanation
15-0	CV[16:1]SEL	Select respective cell (from Cell 1 to Cell 16) voltage measurement ON/OFF 1:Measurement ON (Default) 0:Measurement OFF * Cell Voltage ADC measured data with these bits set to 1 will be latched to respective data registers when ADV_LATCH = 1.

■ Other voltage measurement ON/OFF setting register (GVSEL:0x05)

bit	15	14	13	12	11	10	9	8
Flag	<Reserved>	<Reserved>	<Reserved>	<Reserved>	-	<Reserved>	<Reserved>	GPAD2SEL
R/W	R/WL	R/WL	R/WL	R/WL	R	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	GPAD1SEL	VDD50SEL	TMONI5SEL	TMONI4SEL	TMONI3SEL	TMONI2SEL	TMONI1SEL	VPACKSEL
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	1

bit	Flag	explanation
15-12	<Reserved>	Please always set to “0”.
11	-	
10	<Reserved>	Please always set to “0”.
9	<Reserved>	Please always set to “0”.
8	GPAD2SEL	GPIO2 Pin Voltage Measurement ON/OFF (when set to analog input) 1:Measurement ON 0:Measurement OFF (Default) * Set in advance GPIO2_NOE = 1, GPIO2_IEN = 0 when GPAD2SEL = 1 for analog input.
7	GPAD1SEL	GPIO1 Pin Voltage Measurement ON/OFF (when set to analog input) 1:Measurement ON 0:Measurement OFF (Default) * Set GPIO1_NOE = 1, GPIO1_IEN = 0 when GPAD1SEL = 1 for analog input
6	VDD50SEL	VDD50 Voltage Measurement ON/OFF 1:Measurement ON 0:Measurement OFF (Default)
5	TMONI5SEL	TMONI5 Voltage Measurement ON/OFF 1:Measurement ON 0:Measurement OFF (Default)
4	TMONI4SEL	TMONI4 Voltage Measurement ON/OFF 1:Measurement ON 0:Measurement OFF (Default)
3	TMONI3SEL	TMONI3 Voltage Measurement ON/OFF 1:Measurement ON 0:Measurement OFF (Default)
2	TMONI2SEL	TMONI2 Voltage Measurement ON/OFF 1:Measurement ON 0:Measurement OFF (Default)
1	TMONI1SEL	TMONI1 Voltage Measurement ON/OFF 1:Measurement ON 0:Measurement OFF (Default)
0	VPACKSEL	VPACK Voltage Measurement ON/OFF 1:Measurement ON (Default) 0:Measurement OFF

■ OV/UV setting 1 register (OUVCTL1:0x06)

bit	15	14	13	12	11	10	9	8
Flag	-	-	OVTH[5:0]					
R/W	R	R	R/WL					
initial	0	0	1	1	0	1	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	UVTH[5:0]					
R/W	R	R	R/WL					
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-14	-	
13-8	OVTH[5:0]	Over-Voltage Detection Threshold 110100:4.50V ～ 100000:3.50V ～ 000010:2.00V 111111～110101 (remains at 4.5V) 000001,000000:prohibited * OVTH[5] = 1 when OVHLMT= 1
7-6	-	
5-0	UVTH[5:0]	Under-Voltage Detection Threshold 110010:3.00V ～ 000000:0.50V 111111～110011:prohibited

■ OV/UV setting 2 register (OUVCTL2:0x07)

bit	15	14	13	12	11	10	9	8
Flag	OVHLMT	OV_HYS[2:0]			-	UV_HYS[2:0]		
R/W	R/WL	R/WL			R	R/WL		
initial	1	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	OV_DLY[1:0]		-	-	UV_DLY[1:0]	
R/W	R	R	R/WL		R	R	R/WL	
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15	OVHLMT	OV Detection Threshold Lower Limit Control 1:Limit at 3.5V (Lower threshold = 3.5V) (Default) 0:Lower Threshold (Threshold < = 3.5V)
14-12	OV_HYS[2:0]	OV Detection Hysteresis Level 000:100mV(Default) 001:150mV 010:200mV 011:250mV 100:300mV 101:350mV 110:400mV 111:450mV
11	-	
10-8	UV_HYS[2:0]	UV Detection Hysteresis Level 000:100mV(Default) 001:150mV 010:200mV 011:250mV 100:300mV 101:350mV 110:400mV 111:450mV
7-6	-	
5-4	OV_DLY[1:0]	OV ALARM Delay Time Delay Time = (OV_DLY＋1)s
3-2	-	
1-0	UV_DLY[1:0]	UV ALARM Delay Time Delay Time = (UV_DLY＋1)s

■ UV detection setting register (UVMSK:0x08)

bit	15	14	13	12	11	10	9	8
Flag	UVMSK[16:9]							
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	UVMSK[8:1]							
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
Initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	UVMSK[16:1]	Cell Voltage Under-Voltage Detection ON/OFF (Cell16 to Cell 1) 1:UV OFF 0:UV ON (Default)

■ OV detection setting register (OVMSK:0x09)

bit	15	14	13	12	11	10	9	8
Flag	OVMSK[16:9]							
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	OVMSK[8:1]							
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
Initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	OVMSK[16:1]	Cell Voltage Overvoltage Detection ON/OFF (Cell 16 to Cell 1) 1:OV OFF 0:OV ON (Default)

■ Cell Balance ON/OFF control register (OP_MODE:0x0A)

bit	15	14	13	12	11	10	9	8
Flag	-	<reserved>	-	-	-	-	<Reserved>	CB_SET
R/W	R	R/W	R	R	R	R	R/W	R/W
initial	0	1	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	-	ADC_TRG	-	ADIL_LATCH	ADIH_LATCH	ADV_LATCH
R/W	R	R	R	R/W	R	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15	-	
14	<reserved>	Please always set to “1”.
13-10	-	
9	<Reserved>	Please always set to “0”.
8	CB_SET	Cell Balance Operation Enable 1:Cell Balance ON 0:Cell Balance OFF (Default)
7-5	-	
4	ADC_TRG	Manual ADC Measurement Trigger 1:Voltage ADC Measurement Start, when ADC_CONT = 0 (Auto returns to 0 after completion) 0:When ADC_CONT = 1, always set this bit = 0.
3	-	
2	ADIL_LATCH	Low Speed Current ADC Measurement Result Latch 1:Measured result latched to register 0x4D (Auto returns to 0 after data latch completed) 0:No effect
1	ADIH_LATCH	High Speed Current ADC Measurement Result Latch 1:Measured result latched to register 0x4C (auto return to 0 after data latch completed) 0:No effect
0	ADV_LATCH	Voltage ADC Measurement Result Latch 1:Measured result latched to register 0x33~0x4B (auto return to 0 after data latch completed) 0:No effect

■ Unlock code setting for accessing specific register (LOCK:0x0B)

bit	15	14	13	12	11	10	9	8
Flag	LOCK_CONT[15:8]							
R/W	R/W							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	LOCK_CONT[7:0]							
R/W	R/W							
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	LOCK_CONT [15:0]	Setting to unlock the access to specified registers (refer each register for details) Writing to write protect register (R/WL) is possible when 0xe3b5 is written to this register.

■ GPIO control register 1 (GPIO_CTL1:0x0C)

bit	15	14	13	12	11	10	9	8
Flag	-	-	GPIO6_NOE	GPIO5_NOE	GPIO4_NOE	GPIO3_NOE	GPIO2_NOE	GPIO1_NOE
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	1	1	1	1	1	1

bit	7	6	5	4	3	2	1	0
Flag	-	-	GPIO6_IE	GPIO5_IE	GPIO4_IE	GPIO3_IE	GPIO2_IE	GPIO1_IE
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-14	-	
13-8	GPIO[6:1] _NOE	GPIO6 to GPIO1 Pin Output Enable 1:Disabled (Default) 0:Enabled
7-6	-	
5-0	GPIO[6:1]_IE	GPIO6 to GPIO1 Pin Input Enable 1:Enabled 0:Disable (Default)

Note:
When GPIO pin is configured as output , GPIO[n]_PD shall not be set to “1” at the same time.
When GPIO pin is configured as Analog Input , GPIO[n]_IE shall not be set to “1” at the same time.

■ GPIO control register 2 (GPIO_CTL2:0x0D)

bit	15	14	13	12	11	10	9	8
Flag	-	-	GPIO6_OD	GPIO5_OD	GPIO4_OD	GPIO3_OD	GPIO2_OD	GPIO1_OD
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	GPIO6_PD	GPIO5_PD	GPIO4_PD	GPIO3_PD	GPIO2_PD	GPIO1_PD
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-14	-	
13-8	GPIO[6:1]_OD	GPIO6 to GPIO1 Pin Output Configuration 1:Nch Open Drain 0:Push Pull (Default)
7-6	-	
5-4	GPIO[6:1]_PD	GPIO6 to GPIO1 Pin Pull-Down Resistor 1:Pull-down resistor ON 0:Pull-down resistor OFF (Default)

Note:
When GPIO pin is configured as output , GPIO[n]_PD shall not be set to “1” at the same time.
When GPIO1/2 pin is configured as GPOH1/2 , GPIO1_OD and GPIO2_OD should be set to “0”.

■ GPIO control register 3 (GPIO_CTL3:0x0E)

bit	15	14	13	12	11	10	9	8
Flag	-	-	ST_GPIO6	ST_GPIO5	ST_GPIO4	ST_GPIO3	ST_GPIO2	ST_GPIO1
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	GPIO6_OUT	GPIO5_OUT	GPIO4_OUT	GPIO3_OUT	GPIO2_OUT	GPIO1_OUT
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-14	-	
13-8	ST_GPIO[6:1]	GPIO6 to GPIO1 pins input (Only effective when GPIO6_IE to GPIO1_IE = 1) 1:Input level “H” 0:Input level “L”
7-6	-	
5-0	GPIO[6:1] _OUT	GPIO6 to GPIO1 pins digital output data GPIO6_OD to GPIO1_OD = 0 (push pull) 1:Output “H” 0:Output “L” (Default) GPIO6_OD to GPIO1_OD = 1 (open drain) 1:Output “Hiz” 0:Output “L” (Default)

■ GPIO control register 4 (GPIO_CTL4:0x0F)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	PULLUP_SEL[5:1]				
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	GPIO6_ CHDRV	GPIO5_ CHDRV	GPIO4_ CHDRV	GPIO3_ CHDRV	GPIO2_ CHDRV	GPIO1_ CHDRV
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-13	-	
12-8	PULLUP_ SEL[5:1]	Pull up setting for TMONI1 to TMONI5 pin 1:Pull-up resistor ON 0:Pull-up resistor OFF (Default)
7-6	-	
5-0	GPIO[6:1]_ CHDRV	GPIO6 to GPIO1 Pins Output Drivability 1:4mA 0:2mA (Default)

■ Alarm Control register 1 (ALARM_CTL1:0x11)

bit	15	14	13	12	11	10	9	8
Flag	ALARMSEL	-	<Reserved>	<Reserved>	-	-	<Reserved>	<Reserved>
R/W	R/WL	R	R/WL	R/WL	R	R	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	-	-	EN_SCD	EN_OCD	EN_OCC	EN_CP
R/W	R	R	R	R	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15	ALARMSEL	ALARM1 pin setting 1:ALARM for SCD (ALARM2/GPIO6 will be used for OV/UV/OCD/OCC ALARM when GPIO6 set as ALARM2 Output) 0:ALARM for OV/UV/OCD/OCC/SCD
14	-	
13-12	<Reserved>	Please always set to “0”
11-10	-	
9-8	<Reserved>	Please always set to “0”
7-4	-	
3	EN_SCD	Short circuit detection at discharge 1:Enable 0:Disable (Default)
2	EN_OCD	Overcurrent detection at discharge 1:Enable 0:Disable (Default)
1	EN_OCC	Overcurrent detection at charge 1:Enable 0:Disable (Default)
0	EN_CP	Current Protection 1:Enable 0:Disable (Default)

■ Alarm Control register 2 (ALARM_CTL2:0x12)

bit	15	14	13	12	11	10	9	8
Flag	-	-	SCD_D[3:0]				OCD_D[4:3]	
R/W	R	R	R/WL				R/WL	
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	OCD_D[2:0]			OCC_D[4:0]				
R/W	R/WL			R/WL				
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-14	-	
13-10	SCD_D[3:0]	Short circuit detection at discharge threshold (SCD_D[3:0]+1) x 50mV 0000:50mV (Default)
9-5	OCD_D[4:0]	Overcurrent detection at discharge threshold (OCD_D[4:0]+1) x 25mV 00000:25mV (Default)
4-0	OCC_D[4:0]	Overcurrent detection at charge threshold (OCC_D[4:0]+1) x 10mV (maximum 200mV) 00000:10mV (Default) 10011~11111:200mV

■ Alarm Control register 3 (ALARM_CTL3:0x13)

bit	15	14	13	12	11	10	9	8
Flag	-	SCD_DLY[4:0]					-	OCD_DLY[3]
R/W	R	R/WL					R	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	OCD_DLY[2:0]			-	OCC_DLY[3:0]			
R/W	R/WL			R	R/WL			
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15	-	
14-10	SCD_DLY [4:0]	Delay time for Short circuit detection at discharge (SCD_DLY[4:0]+1) x 50us. If alarm condition continues after delay time, ALARM will be turned ON. 00000:50us (Default)
9	-	
8-5	OCD_DLY [3:0]	Overcurrent detection at discharge delay time (OCD_DLY[3:0]+1) x 1ms. If alarm condition continues after delay time, ALARM will be turned ON. 0000:1ms (Default)
4	-	
3-0	OCC_DLY [3:0]	Overcurrent detection at charge delay time (OCC_DLY[3:0]+1) x 1ms. If alarm condition continues after delay time, ALARM will be turned ON. 0000:1ms (Default)

■ Cell Balance Operation control register (CB_CTL:0x14)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	-	CB_ PROTECT	-	-	<Reserved>	CB_PD
R/W	R	R	R	R/W	R	R	R/W	R/W
Initial	0	0	0	0	0	0	0	1

bit	Flag	explanation
15-8	-	
7	-	
6	-	
5	-	
4	CB_PROTECT	Adjacent cell protection during balancing 1:Lower cell (n-1) has higher priority than upper cell (n) when the adjacent cells are performing cell balancing, (Note: Recommended to use when all cells are connected.) 0:cell operation as per register setting
3	-	
2	-	
1	<Reserved>	Please always set to “0”
0	CB_PD	Control of the cell balance circuit 1:Disable (Default) 0:Enable

■ Select Cell control register (CBSEL:0x15)

bit	15	14	13	12	11	10	9	8
Flag	DI_CBSEL[16:9]							
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	DI_CBSEL[8:1]							
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	DI_CBSEL [16:1]	Selection of cell for balancing 1:Cell balance selected 0:Cell balance not selected (Default)

■ GPIO output control register (GPIOSEL:0x17)

bit	15	14	13	12	11	10	9	8
Flag	-	-	OSC2_DIV[1:0]		GPIO6SEL[1:0]		GPIO5SEL[1:0]	
R/W	R	R	R/WL		R/WL		R/WL	
initial	0	0	1	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	GPIO4SEL[1:0]		GPIO3SEL[1:0]		GPIO2SEL[1:0]		GPIO1SEL[1:0]	
R/W	R/WL		R/WL		R/WL		R/WL	
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-14	-	
13-12	OSC2_DIV [1:0]	Low Speed Clock Divider (when output from GPIO4) 00:1/1 (262.144kHz) 01:1/32 (8.192kHz) 10:1/64 (4.096kHz) (Default) 11:1/128 (2.048kHz)
11-10	GPIO6SEL [1:0]	GPIO6 output selection 00:GPIO6 (Default) 01:ALARM2 10:Prohibited 11:Standby mode state output
9-8	GPIO5SEL [1:0]	GPIO5 output selection 00:GPIO5 (Default) 01:High speed AD conversion interrupt 10:Prohibited 11:Active mode state output
7-6	GPIO4SEL [1:0]	GPIO4 output selection 00:GPIO4 (Default) 01:Low speed AD conversion interrupt 10:Prohibited 11:Low speed clock output
5-4	GPIO3SEL [1:0]	GPIO3 output selection 00:GPIO3 (Default) 01:Prohibited 10:Prohibited 11:High speed clock output
3-2	GPIO2SEL [1:0]	GPIO2 output selection 00:GPIO2 (Default) 01:Prohibited 10:Analog input 11:GPOH2 output state
1-0	GPIO1SEL [1:0]	GPIO1 output selection 00:GPIO1 (Default) 01:Prohibited 10:Analog input 11:GPOH1 output state

Note:
When GPIO pin is configured as an Analog Input , GPIO[n]_IE shall not be set to “1” at the same time.
When GPIO1/2 pin is configured as GPOH1/2 , GPIO1_OD and GPIO2_OD should be set to “0”.

■ Communication・VDD50 LDO Power Mode Control register (SPICTL:0x18)

bit	15	14	13	12	11	10	9	8
Flag	-	-	<Reserved>	<Reserved>	-	SDI_PLDW	SCL_PLDW	SEN_PLDW
R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
initial	0	0	0	0	0	1	1	1

bit	7	6	5	4	3	2	1	0
Flag	-	-	<Reserved>	LP50EN	-	-	-	COM_STP
R/W	R	R	R/W	R/W	R	R	R	R/W
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-14	-	
13-12	<Reserved>	Please always set to “0”
11	-	
10	SDI_PLDW	SDI pin pull-down control signal 1:Pull-down ON (Default) 0:Pull-down OFF
9	SCL_PLDW	SCL pin pull-down control signal 1:Pull-down ON (Default) 0:Pull-down OFF
8	SEN_PLDW	SEN pin pull-down control signal 1:Pull-down ON (Default) 0:Pull-down OFF
7-6	-	
5	<Reserved>	Please always set to “0”
4	LP50EN	VDD50 power drive mode selection 1:Low power mode 0:Normal mode (Default)
3-1	-	
0	COM_STP	SPI communication control operation SPI communication can be turned OFF with this bit setting. It is required to input High to SEN pin for more than 1ms in order to resume communication. This bit is cleared automatically.

■ ADC control register1 (ADCTL1:0x19)

bit	15	14	13	12	11	10	9	8
Flag	<Reserved>	<Reserved>	<Reserved>	<Reserved>	<Reserved>	<Reserved>	-	-
R/W	R/WL	R/WL	R/WL		R/WL		R	R
initial	0	0	0	0	1	1	0	0

bit	7	6	5	4	3	2	1	0
Flag	<Reserved>	<Reserved>	ADI_LATCH _SET	ADV_LATCH _SET	-	<Reserved>	<Reserved>	<Reserved>
R/W	R/WL	R/WL	R/WL	R/WL	R	R/WL	R/WL	R/WL
initial	1	0	0	0	0	0	0	0

bit	Flag	explanation
15-12	<Reserved>	Please always set to “0000”.
11-10	<Reserved>	Please always set to “11”.
9	-	
8	-	
7-6	<Reserved>	Please always set to "10“.
5	ADI_LATCH _SET	High speed current ADC measurement data latch timing 1:After ADIH_LATCH = 1, on-going data latch when 1 cycle is completed. 0:After ADIH_LATCH = 1, previous data latch immediately (Default).
4	ADV_LATCH _SET	ADC Voltage measurement data latch Timing 1:After ADV_LATCH = 1, on-going all data latch when 1 cycle is completed. 0:After ADV_LATCH = 1, previous all data latch immediately (Default).
3	-	
2-0	<Reserved>	Please always set to “000”.

■ ADC control register2 (ADCTL2:0x1A)

bit	15	14	13	12	11	10	9	8
Flag	-	-	ADSWHY _EN	ADSWSD _EN	-	-	-	-
R/W	R	R	R/WL	R/WL	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	<Reserved>	<Reserved>	<Reserved>	ISD_ STOPEN	-	-	ADIL_ON	ADIH_ON
R/W	R/WL	R/WL	R/WL	R/WL	R	R	R/WL	R/WL
initial	0	0	1	1	0	0	0	0

bit	Flag	explanation
15-14	-	
13	ADSWHY _EN	High Speed Current ADC Enable 1:ON 0:OFF (Default)
12	ADSWSD _EN	Low Speed Current ADC Enable 1:ON 0:OFF (Default)
11-8	-	
7-5	<Reserved>	Please always set to “001”.
4	ISD_ STOPEN	Low Speed Current ADC Stop Control 1:Disable Low Speed Current ADC for high speed current ADC operation. (Default) 0:Enable simultaneous operation high speed and low speed current ADC
3-2	-	
1	ADIL_ON	Enable Low speed current ADC Operation 1:Enable 0:Disable (Default)
0	ADIH_ON	Enable High Speed current ADC operation 1:Enable 0:Disable (Default)

■ GPOH control register (GPOH_CTL:0x1B)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	GPOH2_ ALM_ST	GPOH1_ ALM_ST	-	GPOH_FET	GPOH2_EN	GPOH1_EN
R/W	R	R	R/WL	R/WL	R	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-6	-	
5	GPOH2_ ALM_ST	If using FET at GPOH2 pin, to set GPOH2 pin data to output during ALARM Effective only when FDRV_ALM_SD=1 & GPOH_FET=1 1:"L" output 0:Hiz (Default)
4	GPOH1_ ALM_ST	If using FET at GPOH1 pin, set GPOH1 pin data to output during ALARM Effective only when FDRV_ALM_SD=1 & GPOH_FET=1 1:"L" output 0:Hiz (Default)
3	-	
2	GPOH_FET	FET control settings of GPOH Pin 1:FET control use Control of FET driver ON/OFF is possible in GPOH pin by FDRV_CTL(0x03). 0:FET control no use (Default)
1	GPOH2_EN	GPOH2 output data 1:"L" output 0:Hiz (Default)
0	GPOH1_EN	GPOH1 output data 1:"L" output 0:Hiz (Default)

■ Open Detection selection register (INRCV1:0x1C)

bit	15	14	13	12	11	10	9	8
Flag	INR_CV_[15:8]							
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0							

bit	7	6	5	4	3	2	1	0
Flag	INR_CV_[7:0]							
R/W	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL	R/WL
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	INR_CV _[15:0]	Selection of cell for open detection 1:Open Detection selected 0:Open Detection not selected (Default)

■ Open Detection selection register (INRCV2:0x1D)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	INR_CV_16
R/W	R	R	R	R	R	R	R	R/WL
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-4	-	
3	-	
2	-	
1	-	
0	INR_CV_16	Selection of cell for open detection 1:Open Detection selected 0:Open Detection not selected (Default)

■ Open Detection ON/OFF control register (INR_CTL:0x1E)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	INR_EN
R/W	R	R	R	R	R	R	R	R/WL
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-1	-	
0	INR_EN	Selection of open detection 1:Open Detection ON 0:Open Detection OFF(Default)

■ SPI Status register (SPI_STAT:0x21)

bit	15	14	13	12	11	10	9	8
Flag	-	SPI_F	-	-	-	-	-	-
R/W	R	R/WL	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15	-	
14	SPI_F	SPI Communication Error Flag 1:Communication Error 0:No Communication Error If communication error is detected, SPI_F=1 and it is cleared by writing “1”.
13-0	-	

■ Operation Mode Status register (MODE_STAT:0x22)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	COND_SCD	COND_OCD	COND_OCC	ST_SDWN	ST_STBY	ST_ACT
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	x	x	x

bit	Flag	explanation
15-6	-	
5	COND_SCD	SCD detection flag 1:SCD detected (auto cleared when short circuit condition removed) 0:SCD not detected
4	COND_OCD	OCD detection flag 1:OCD detected (auto cleared when over current at discharge condition removed) 0:OCD not detected
3	COND_OCC	OCC detection flag 1:OCC detected (auto cleared when over current at charge condition removed) 0:OCC not detected
2	ST_SDWN	Shutdown mode(Operation Mode) Flag 1:Under Shutdown Mode * The initial state depend on external pins setting 0:Not under Shutdown Mode
1	ST_STBY	Standby mode (Operation Mode) Flag 1:Under Standby Mode * The initial state depend on external pins setting 0:Not Under Standby Mode
0	ST_ACT	Active mode (Operation Mode) 1:Under Active Mode * The initial state depend on external pins setting 0:Not under Active Mode

■ FUSE Read address setting register (FUSE_RADR:0x2E)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	FUSE_RADR[7:0]							
R/W	R/W							
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-8	-	
7-0	FUSE_RADR [7:0]	Setting for FUSE read address The value of this register is shown in 0x2F register.

■ FUSE read data register (FUSE_DATA:0x2F)

bit	15	14	13	12	11	10	9	8
Flag	FUSE_DATA[15:8]							
R/W	R							
initial	X	X	X	X	X	X	X	X

bit	7	6	5	4	3	2	1	0
Flag	FUSE_DATA[7:0]							
R/W	R							
initial	X	X	X	X	X	X	X	X

bit	Flag	explanation
15	FUSE_DATA [15:0]	FUSE value of the address set in FUSE_RADR(0x2E) is stored in the register.

■ ADC/ALARM Status register (STAT:0x30)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	-	-	-	ST_OV	ST_UV
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	ST_SCD	ST_OCD	ST_OCC	-	IADS_DONE	IADH_DONE	VAD_DONE
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-10	-	
9	ST_OV	OV detection status display 1:OV detected 0:OV not detected If OV is detected in any cell, OVSTAT=1 is shown.
8	ST_UV	UV detection status display 1:UV detected 0:UV not detected If UV is detected in any cell, UVSTAT=1 is shown.
7	-	
6	ST_SCD	SCD detection flag 1:SCD detected 0:SCD not detected If SCD is detected, ST_SCD=1 and it is cleared by writing “1”. ALARM1 pin outputs LOW when ST_SCD=1.
5	ST_OCD	OCD detection flag 1:OCD detected 0:OCD not detected If OCD is detected, ST_OCD=1 and it is cleared by writing “1”. Either ALARM1 pin or ALARM2 pin outputs LOW when ST_OCD=1.
4	ST_OCC	OCC detection flag 1:OCC detected 0:OCC not detected If OCC is detected, ST_OCC=1 and it is cleared by writing “1”. Either ALARM1 pin or ALARM2 pin outputs LOW when ST_OCC=1.
3	-	
2	IADS_DONE	Low speed current ADC completion flag 1:Measurement completed 0:Measurement incomplete It is cleared to “0” by writing "1“
1	IADH_DONE	High speed current ADC completion flag 1:Measurement completed 0:Measurement incomplete It is cleared to “0” by writing "1“
0	VAD_DONE	Voltage measurement ADC Completion flag 1:Measurement completed 0:Measurement incomplete It is cleared to “0” by writing "1“

■ OV Status register (OVSTAT:0x31)

bit	15	14	13	12	11	10	9	8
Flag	OV[16:9]_F							
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	OV[8:1]_F							
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	OV[16:1]_F	Cell n OV detection output *automatic update 1:Abnormal 0:Normal

■ UV Status register (UVSTAT:0x32)

bit	15	14	13	12	11	10	9	8
Flag	UV[16:9]_F							
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	UV[8:1]_F							
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	UV[16:1]_F	Cell n UV detection output *automatic update 1:Abnormal 0:Normal

■ Voltage measurement result for cell 1 register (CV01_AD:0x33)

bit	15	14	13	12	11	10	9	8
Flag	CV01_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	CV01_AD[7:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	CV01_AD [15:0]	Cell 1Voltage Measurement output. Value: 0x3FFF:4.999695V ～ 0x2000:2.5V ～ 0x0001:0.000305V 0x0000:0V Measured Voltage = Value x 0.000305V * bit15,14 are always "0“.

Note:
The definition for register addresses 0x34(CV02_AD) ~ 0x42(CV16_AD) are the same as register 0x33(CV01_AD).

■ Voltage measurement result for VPACK register (VPACK_AD:0x43)

bit	15	14	13	12	11	10	9	8
Flag	VPACK_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	VPACK_AD[7:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	VPACK_AD [15:0]	VPACK Voltage Measurement output Value: 0x3FFF:99.993896V ～ 0x2000:50V ～ 0x0001:0.006104V 0x0000:0V Measured Voltage = value x 0.006104V * bit15,14 are always "0“.

■ Voltage measurement result for TMONI1 register (TMONI1_AD:0x44)

bit	15	14	13	12	11	10	9	8
Flag	TMONI1_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	TMONI1_AD[7:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	TMONI1_AD [15:0]	TMONI1Voltage Measurement output Value: 0x3FFF:4.999695V ～ 0x2000:2.5V ～ 0x0001:0.000305V 0x0000:0V Measured Voltage = Value x 0.000305V * bit15,14 are always "0“.

Note:
The definition for register addresses 0x45(TMONI2_AD) ~ 0x48(TMONI5_AD) are the same as register 0x44(TMONI1_AD).

■ Voltage measurement result for VDD50 register (VDD50_AD:0x49)

bit	15	14	13	12	11	10	9	8
Flag	VDD50_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	VDD50_AD[7:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	VDD50_AD [15:0]	VDD50 Voltage Measurement output Value: 0x3FFF:7.499542V ～ 0x2000:3.75V ～ 0x0001:0.000458V 0x0000:0V Measured Voltage = Value x 0.000458V * bit15,14 are always "0“.

■ Voltage measurement result for GPIO1 register (GPIO1_AD:0x4A)

bit	15	14	13	12	11	10	9	8
Flag	GPIO1_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	GPIO1_AD[7:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	GPIO1_AD [15:0]	GPIO1Voltage Measurement output Value: 0x3FFF:4.999695V ～ 0x2000:2.5V ～ 0x0001:0.000305V 0x0000:0V Measured Voltage = Value x 0.000305V * Note: bit15,14 are always "0“.

Note:
The definition for register address 0x4B(GPIO2_AD)is the same as register 0x4A(GPIO1_AD).

■ High speed current ADC measurement result register (CVIH_AD:0x4C)

bit	15	14	13	12	11	10	9	8
Flag	CVIH_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	CVIH_AD[8:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	CVIH_AD [15:0]	High speed current ADC Measurement output Value: 0x7FFF:179.994507mV ～ 0x0001:0.005493mV 0x0000:0V 0xFFFF:-0.005493mV ～ 0x8001:-179.994507mV 0x8000:-180mV Voltage/step = 0.005493mV Measured voltage = 2's complement data * 360mV/2^16

■ Low speed current ADC measurement result register (CVIL_AD:0x4D)

bit	15	14	13	12	11	10	9	8
Flag	CVIL_AD[15:8]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	CVIL_AD[8:0]							
R/W	R							
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	CVIL_AD [15:0]	Low speed current ADC measurement output Value: 0x7FFF:179.994507mV ～ 0x0001:0.005493mV 0x0000:0V 0xFFFF:-0.005493mV ～… 0x8001:-179.994507mV 0x8000:-180mV Voltage/step = 0.005493mV Measured voltage = 2's complement data * 360mV/2^16

■ OV detection flag register (OVL_STAT:0x52)

bit	15	14	13	12	11	10	9	8
Flag	OV[16:9]_LF							
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	OV[8:1]_LF							
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	OV[16:1]_LF	Cell n OV detection flag 1:OV detected 0:OV not detected

* If OV is detected, the related flag will become “1”.
To cleared any flag in this register, write “0x0000” to this register.

■ UV detection flag register (UVL_STAT:0x53)

bit	15	14	13	12	11	10	9	8
Flag	UV[16:9]_LF							
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	UV[8:1]_LF							
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-0	UV[16:1]_LF	Cell n UV detection flag 1:UV detected 0:UV not detected

* If UV is detected, the related flag will become “1”.
To cleared any flag in this register, write “0x0000” to this register.

■ CVDD Status register (CVDD_STAT:0x54)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	X	X

bit	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	CVDD_UV	-	-
R/W	R	R	R	R	R	R	R	R
Initial	0	0	0	X	0	0	0	0

bit	Flag	explanation
15-3	-	
2	CVDD_UV	CVDD pin UV detection flag 1:UV release(CVDD > 2.8V (typ)) 0:UV detect (CVDD < 2.45V (typ))
1-0	-	

■ FET Driver status register (FDRVSTAT:0x55)

bit	15	14	13	12	11	10	9	8
Flag	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Flag	-	-	-	-	FDRV_DIS_ST	FDRV_CHG_ST	GPOH2_ST	GPOH1_ST
R/W	R	R	R	R	R	R	R	R
initial	0	0	0	0	0	0	0	0

bit	Flag	explanation
15-4	-	
3	FDRV_DIS_ST	DIS Pin state
2	FDRV_CHG_ST	CHG Pin state
1	GPOH2_ST	GPOH2 state 0:Hiz, 1:Output “L”
0	GPOH1_ST	GPOH1 state 0:Hiz, 1:Output “L”

■ Cell balance operation status register (CBSTAT:0x56)

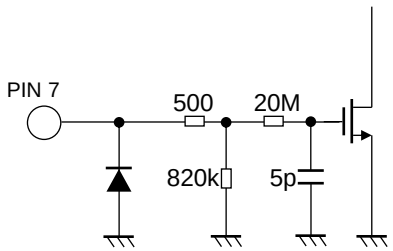
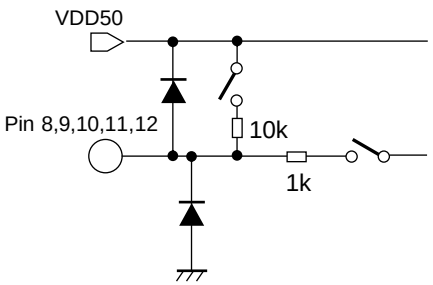
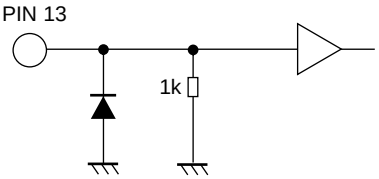
bit	15	14	13	12	11	10	9	8
Flag	CB_ST[16:9]							
R/W	R							
initial	0	0	0	0	0	0	0	0

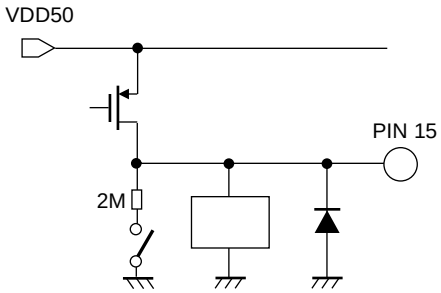
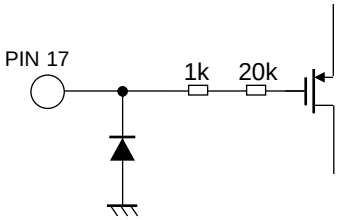
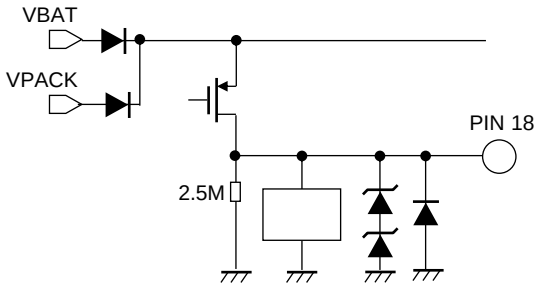
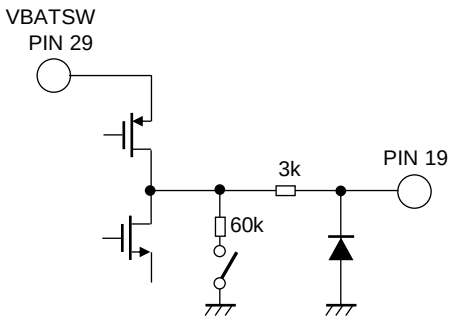
bit	7	6	5	4	3	2	1	0
Flag	CB_ST[8:1]							
R/W	R							
initial	0	0	0	0	0	0	0	0

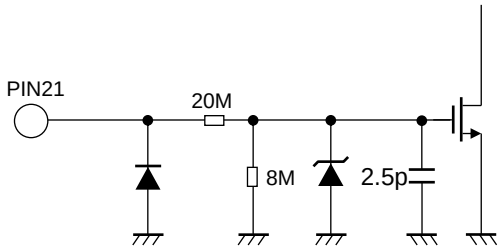
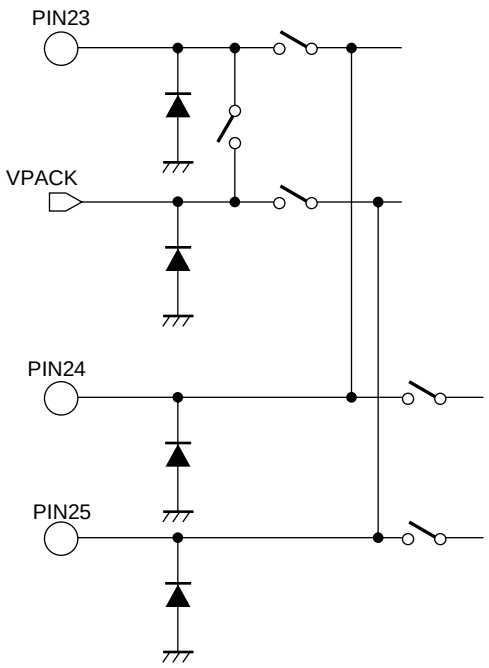
bit	Flag	explanation
15-0	CB_ST[16:1]	Display of Individual cell balance control status. 1:Cell balance ON 0:Cell balance OFF

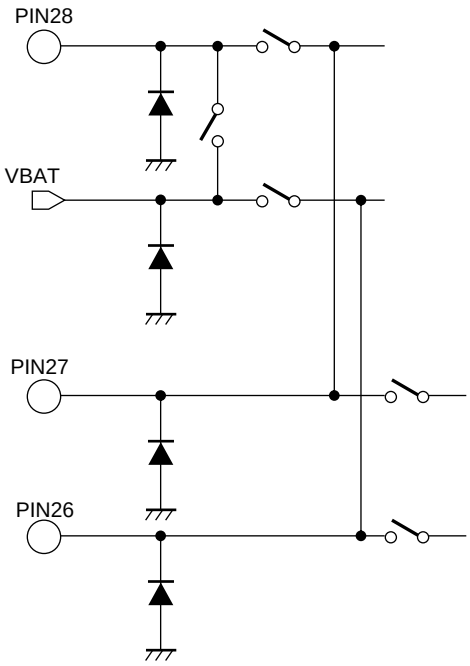
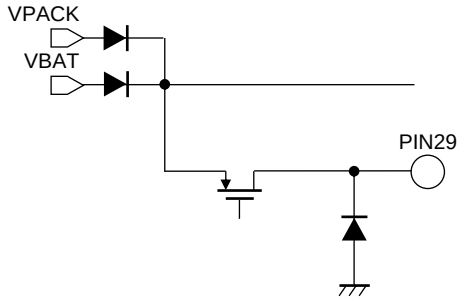
Chapter 15 Pin configuration diagram

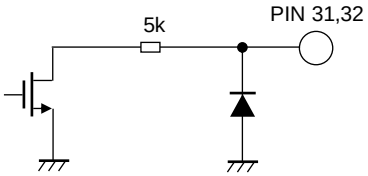
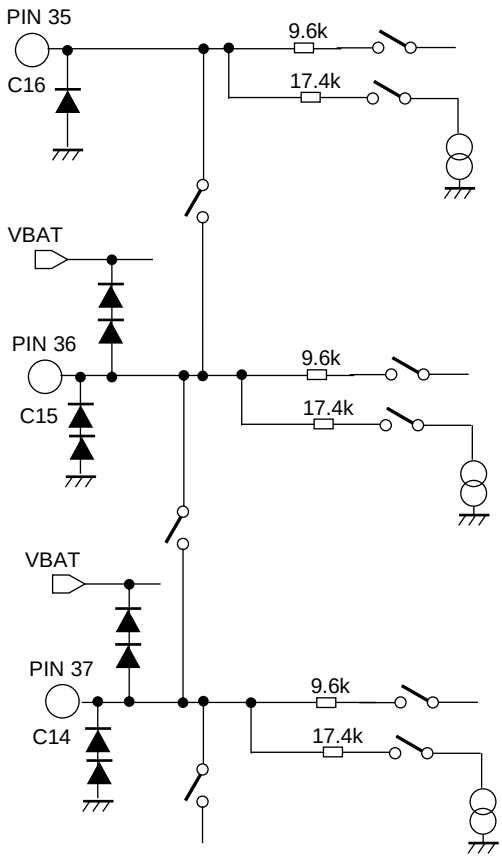
Note: The following information is design value for reference purpose, the value is not guaranteed by test.

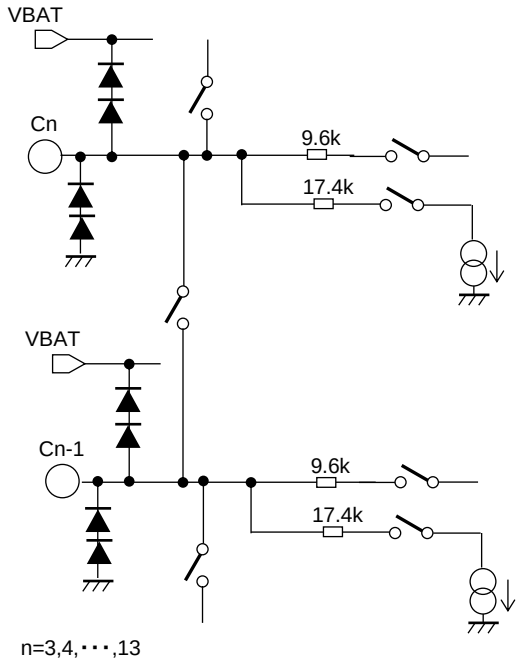
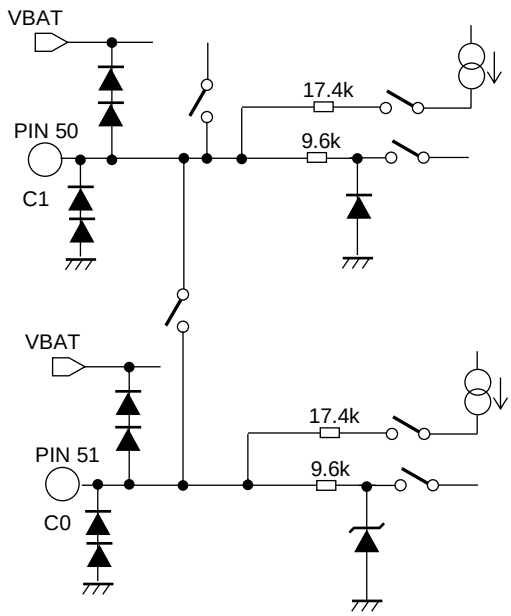
Pin No.	Waveform / voltage	Internal Circuit	Description
6	DC		Digital IO Power Supply Pin (CVDD)
7	DC		Shutdown Control Signal Input Pin (SHDN)
8 9 10 11 12	DC		Analog Voltage Input Pin (TMONI1-5)
13	DC		Test Mode Setting Pin (MODE)

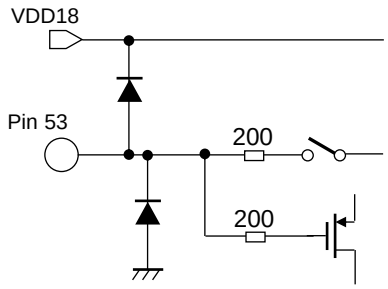
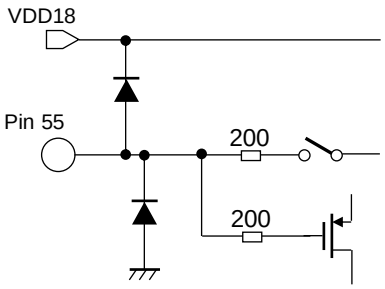
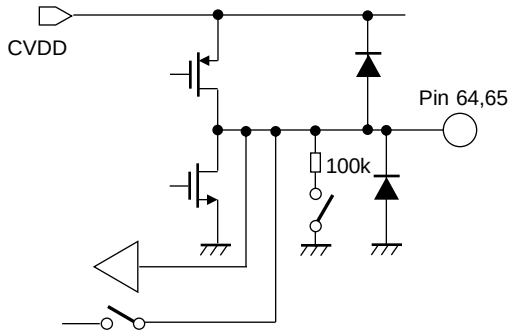
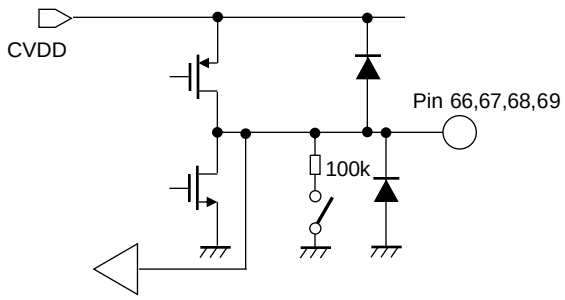
Pin No.	Waveform / voltage	Internal Circuit	Description
15	DC		Internal Regulator Pin (VDD18)
17	DC		VDD50R
18	DC		5V Regulator Pin (VDD50)
19	DC		5V Regulator External NMOS Gate Pin (LDOG)

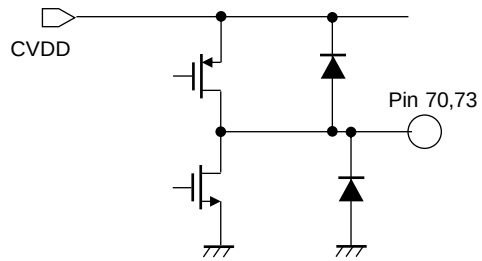
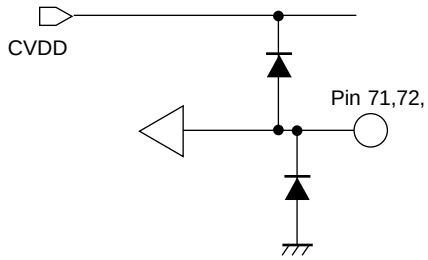
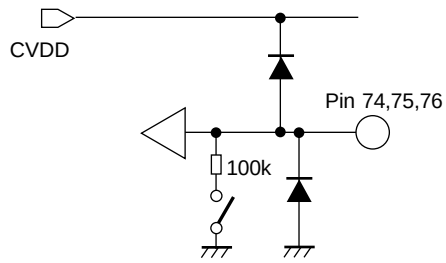
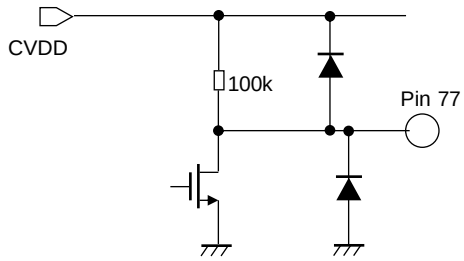
Pin No.	Waveform / voltage	Internal Circuit	Description
21	DC		Wake Up Signal Pin (VPC)
23	AC		External DIS_FET (NMOS) Gate Driver Pin (DIS)
24	AC		Charge Pump Capacitor Pin (CP1)
25	AC		Charge Pump Capacitor Pin (CN1)

Pin No.	Waveform / voltage	Internal Circuit	Description
26	AC		Charge Pump Capacitor Pin (CN2)
27	AC		Charge Pump Capacitor Pin (CP2)
28	AC		External CHG_FET (NMOS) Gate Driver Pin (CHG)
29	DC		5V Regulator External NMOS Drain Pin (VBATSW)

Pin No.	Waveform / voltage	Internal Circuit	Description
31 32	DC		High Breakdown Voltage GPO Pin (GPOH2/GPOH1)
35	DC		Cell Voltage Input Pin (C16)
36	DC		Cell Voltage Input Pin (C15)
37	DC		Cell Voltage Input Pin (C14)

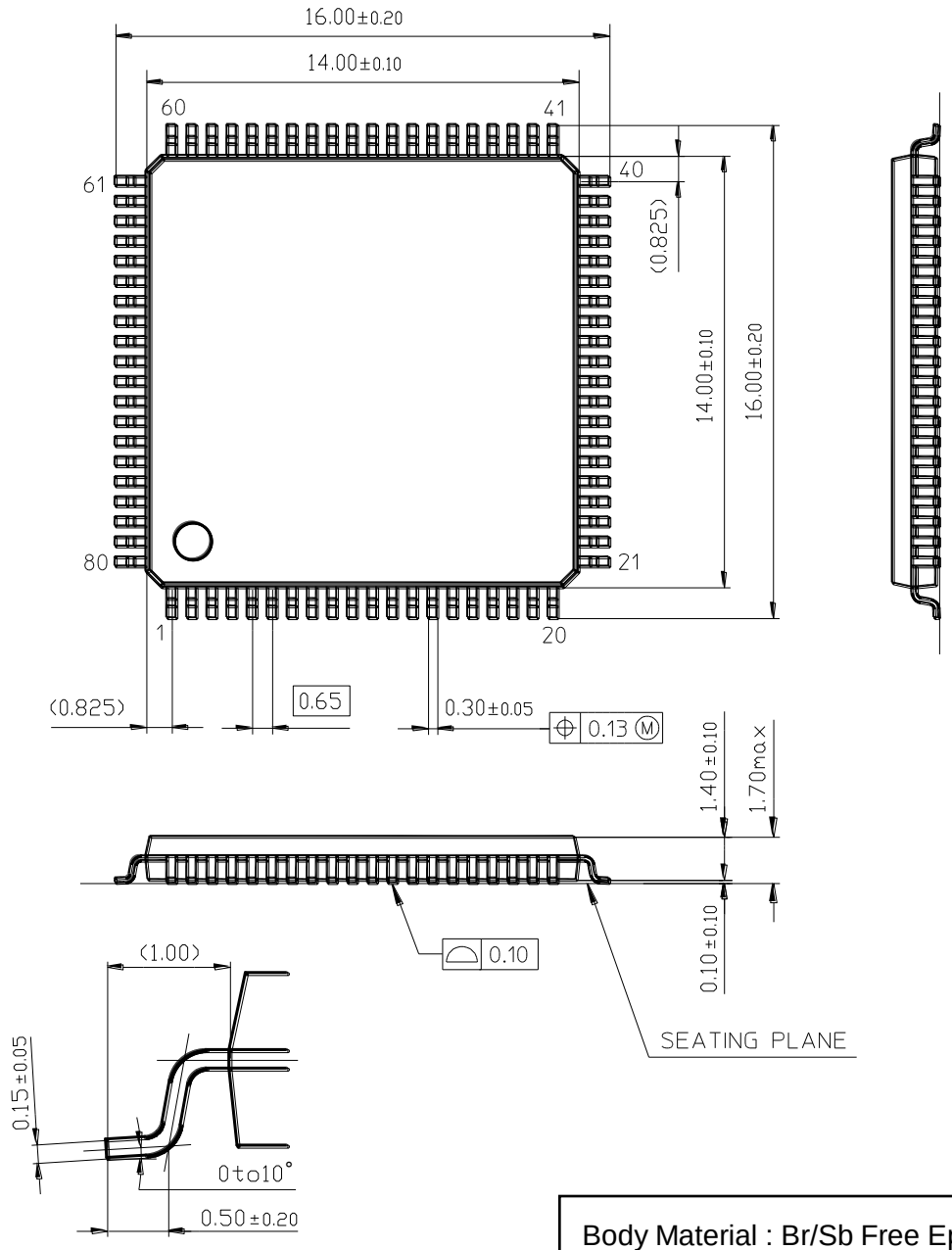
Pin No.	Waveform / voltage	Internal Circuit	Description
38 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49	DC		Cell Voltage Input Pin (C13,C12,C11・・・C2)
50	DC		Cell Voltage Input Pin (C1)
51	DC		Cell Voltage Input Pin (C0)

Pin No.	Waveform / voltage	Internal Circuit	Description
53	DC		Shunt Current Monitor Pin (+ve) (SRP)
55	DC		Shunt Current Monitor Pin (-ve) (SRN)
64 65	DC		GPIO1/2 Pin (GPIO1/GPIO2)
66 67 68 69	DC		GPIO3/4/5/6 Pin (GPIO3-GPIO6)

Pin No.	Waveform / voltage	Internal Circuit	Description
70 73	DC		Digital Output Pin (ALARM1,SDO)
71 72	DC		Digital Input Pin (FETOFF,STB)
74 75 76	DC		Digital Input Pin (SDI,SCL,SEN)
77	DC		Power ON Reset Output Pin (NRST)

Package Information

Package Code : LQFP080-P-1414FZ



Body Material : Br/Sb Free Epoxy Resin
Lead Material : Cu Alloy
Lead Finish Method : Pd Plating

Important Notice

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board),
   it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins.
   In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
10. This IC may be changed in order to improve the performance without notice, please make sure the latest specification is used before your final design.