Panasonic

AN49503A Operation Quick Reference

Panasonic Semiconductor Solutions Co., Ltd.

This Operation Quick Reference provides brief explanation for AN49503A functionality. For full function information, please refer to the AN49503A Product Standards.

Overview

In this document, basic operation of AN49503A and register initialization are explained to give a quick overview of how to use AN49503A. It does not contains full function of AN49503A, refer to AN49593A Product Standards for full information.

Operation Mode		
Shutdown Mode		All circuit stopped functioning Condition: From any mode: - [SHDN pin -> HI (> 1ms) or register MSET_SHDN = 1(>1ms)] & VPC = LO or - (Watchdog, Thermal shutdown or VDD50 UVLO) & VPC = LO
Active Mode		Operation mode which all function could be activated. Status of Active Mode is indicated by register ST_ACT. Condition: From Shutdown Mode - ((VBAT or VPACK) > 12.5V) & VPC from LO to HI (> 5ms), set VPC to LO after that - VDD50 will become 5V follow by the SDO and NRST pins become HI. From Standby Mode - STB pin from HI to LO (> 2ms) and hold
Standby Mode	Active Mode *	Operation mode which is entered automatically from Standby Mode every 1s when no SPI communication. After one voltage measurement cycle, it will resume to Standby Mode automatically. OV/UV can be detected in Standby Mode when this mode is enabled. To enable this mode, it requires registers STB_MONEN and ADC_CONT =1.
	Standby Mode (Communication ON)	Operation mode when HS current ADC and voltage ADC is not operating. SPI communication is enabled. Status of Standby Mode is indicated by ST_STBY. Condition: From Active Mode - STB pin LO -> HI. From Standby Mode (Communication OFF) - SEN pin HI (>2ms) then LO
	Standby Mode (Communication OFF)	Operation mode when HS current ADC and voltage ADC is not operating. SPI communication is disable. Condition: From Standby Mode (Communication ON) - Set Register COM_STP = 1
LDO Power Mode		
(Active Mode/ Standby Mode) LDO Normal Mode		5V LDO drivability set at 50mA. The drivability is 50mA for Active mode always and can be set in Standby Mode. Set by register LP50EN = 0 in Standby Mode.
(Standby Mode) LDO Low Power Mode		5V LDO drivability set at 5mA, only available in Standby Mode. Cell balance should not be used under this mode. Set by register LP50EN = 1 in Standby Mode.

NOTE: VPC shall be set to LO after wake up (from Shutdown Mode to Active Mode) at all time
NOTE: ((VBAT or VPACK) > 12.5V) is required at all time for AN49503A

Register Initialization

<table>
<tr><th>Initialization</th><th>Explanation</th></tr>
<tr><td>OV/UV Threshold/Delay/Hysteresis Setting</td><td>Set OV/UV detection threshold level, delay time and hysteresis level
- Register 0x06 OUVCTL1
- Register 0x07 OUVCTL2</td></tr>
<tr><td>OCC/OCD/SCD Threshold/Delay Setting</td><td>Set OCC/OCD/SCD detection threshold level and delay time to ALARM triggered
- Register 0x12 ALARM_CTL2
- Register 0x13 ALARM_CTL3</td></tr>
<tr><td>Cell Select and OV/UV Mask</td><td>Set cell voltage to be latched and to detect OV/UV, set according to battery cell connected
- Register 0x04 CVSEL
- Register 0x08 UVMSK
- Register 0x09 OVMSK</td></tr>
<tr><td>Other voltage measurement selection</td><td>Set other voltage measurement to be latched
- Register 0x05 GVSEL
- Other voltage includes GPIO1/GPIO2, VDD50, TMONI1~5 and VPACK voltage</td></tr>
<tr><td>Watchdog Timer and On/OFF</td><td>Watchdog timer ON/OFF and Timing Setting
- Register 0x02 SPIWD_CTL
Note: Do not change Watchdog Timer Timing Setting when Watchdog Timer is in operation.</td></tr>
<tr><td>ALARM pin setting</td><td>Register 0x11 b15 ALARMSEL set the ALARM1/2 pins indication for ALARM condition as shown in table below
- ALARM pins will be triggered LO when ALARM condition occurred, and will resume HI after ALARM condition released.
Note: ALARM2 is multiplexed with GPIO6 pin, When used as ALARM2, GPIO6 is required to be set for ALARM2 output. (Refer to next page)
<table>
<tr><th rowspan="2"></th><th rowspan="2">Alarm</th><th>ALARMSEL=0</th><th colspan="2">ALARMSEL=1</th></tr>
<tr><th>ALARM1</th><th>ALARM1</th><th>ALARM2</th></tr>
<tr><td rowspan="2">Abnormal</td><td>OV/UV
OCC/OCD</td><td>"L"</td><td>"H"</td><td>"L"</td></tr>
<tr><td>SCD</td><td>"L"</td><td>"L"</td><td>"H"</td></tr>
<tr><td>Normal</td><td>-</td><td>"H"</td><td>"H"</td><td>"H"</td></tr>
</table></td></tr>
<tr><td>FET/GPOH(1/2) /GPIO(1/2) Response to ALARM Setting</td><td>Set how FET/GPOH/GPIO response and release from ALARM condition, including OV/UV/OCC/OCD and SCD.
- Register 0x03 b15 FDRV_ALM_SD
- set if FET/GPOH/GPIO response to ALARM condition
- Register 0x03 b14 FDRV_ALM_RCV
- set if FET/GPOH/GPIO recover from OV/UV automatically
- Register 0x03 b2 FDRV_OUVCTL
- set if CHG/DIS response to OV/UV together or separately
- Register 0x1B b2 GPOH_FET
- set if GPOH(1/2)/GPIO(1/2) pins response to ALARM condition
- Register 0x1B b5:b4 GPOHx_ALM_ST
- set state of GPOH1/2 at ALARM condition
Note: GPIO1/2 to be set to mirror GPOH1/2 pins for response abovementioned(refer next page)</td></tr>
</table>

Note : The initialization step order is not fixed and some registers may be omitted depend on application requirement eg. If Watchdog Timer is not used , no changes is needed for Watchdog Timer.
Note : Some registers accessibility property is R/WL, which required LOCK register 0x0B to be set to 0xE3B5 before these registers can be written.

Register Initialization

Initialization	Explanation
GPIO1/2 configured to mirror GPOH1/2 output	GPIO1/2 can be configured as output pins that mirror GPOH1/2 output - Register 0x0C b9:b8 GPIOx_NOE , b1:b0 GPIOx_IE - set GPIOx_NOE to “0”, GPIOx_IE to “0” - Register 0x0D b9:b8 GPIOx_OD, b1:b0 GPIOx_PD - GPIOx_OD set accordingly, GPIOx_PD set to “0”; - Register 0x17 b3:b0 GPIOxSEL[1:0] - set GPIOxSEL[1:0] to “11”
GPIO4 configured as ADIRQ2 output and GPIO5 configured as ADIRQ1 output	GPIO4/5 can be configured as ADIRQ2/ADIRQ1 as interrupt for Low Speed AD conversion and High Speed (HS current / voltage) AD conversion - Register 0x0C b12:b11 GPIOx_NOE , b4:b3 GPIOx_IE - set GPIOx_NOE to “0”, GPIOx_IE to “0” - Register 0x0D b12:b11 GPIOx_OD, b4:b3 GPIOx_PD - set accordingly - Register 0x17 b9:b6 GPIOxSEL[1:0] - set GPIOxSEL[1:0] to “01”
GPIO6 configured as ALARM2 output	When ALARMSEL = 1, GPIO6 will be used as ALARM2 to indicate ALARM for OV/UV/OCC/OCD. GPIO6 is required to be configured accordingly as: - Register 0x0C b13 GPIO6_NOE , b5 GPIO6_IE - set GPIOx_NOE to “0”, GPIOx_IE to “0” - Register 0x0D b13 GPIO6_OD, b5 GPIO6_PD - set accordingly Register 0x17 b11:b10 GPIO6SEL[1:0] - set GPIO6SEL[1:0] to “01”

Note : The initialization step order is not fixed and some registers may be omitted depend on application requirement eg. If Watchdog Timer is not used , no changes is needed for Watchdog Timer.
Note : Some registers accessibility property is R/WL, which required LOCK register 0x0B to be set to 0xE3B5 before these registers can be written.

Basic Operation

Basic Operation/Setup	Explanation
Set how FET/GPOH1/2 / GPIO1/2 response to ALARM condition (UV/OV/OCC/OCD/SCD) * For current alarm detection, register 0x11 b3:b0 EN_SCD, EN_OCD, EN_OCC and EN_CP required to be enabled. * GPIO1/2 to be set to mirror GPOH1/2 (refer to previous page)	Set how CHG/DIS pins and GPOH1/2 and GPIO1/2 pins response to ALARM condition (UV/OV/OCC/OCD/SCD) **[Operation]** CHG/DIS pins output response to ALARM condition accordingly when FDRV_ALM_SD (register 0x03 b15) = 1. Refer to table below for how it response to different ALARM condition. It does not response to ALARM condition when FDRV_ALM_SD = 0, when it does not response to ALARM condition, its output is determined by FDRV_CHG_FET and FDRV_DIS_FET (register 0x01 b1:b0) setting. GPOH1/2 and GPIO1/2 pins output response to ALARM condition accordingly when FDRV_ALM_SD=1 and GPOH_FET (register 0x1B b2) =1. Its response depend on GPOH1_ALM_ST and GPOH2_ALM_ST(register 0x1B b5:b4). It does not response to ALARM condition when FDRV_ALM_SD = 0 or GPOH_FET=0, when it does not response to ALARM condition, its output is determined by GPOH1_EN and GPOH2_EN (register 0x1B b1:b0). The status of CHG.DIS and GPOH1/2 pins can de determined by FDRV_DIS_ST, FDRV_CHG_ST, GPOH2_ST and GPOH1_ST (register 0x55 b3:b0)

Abnormal	FDRV_ALM_SD	FDRV_OUV CTL = 0		FDRV_OUV CTL = 1		GPOH1	GPOH2	GPIO1	GPIO2
		CHG	DIS	CHG	DIS				
UV/OV/OCC /OCD/SCD	0	-	-	-	-	According to GPOH1_EN	According to GPOH2_EN	According to GPOH1_EN	According to GPOH2_EN
Normal	1	-	-	-	-	According to GPOH1_EN	According to GPOH2_EN	According to GPOH1_EN	According to GPOH2_EN
UV	1	-	OFF	OFF	OFF	According to GPOH1_ALM_ST	According to GPOH2_ALM_ST	According to GPOH1_ALM_ST	According to GPOH2_ALM_ST
OV	1	OFF	-	OFF	OFF				
OCC	1	OFF	-	OFF	-				
OCD/SCD	1	-	OFF	-	OFF				

Basic Operation

Basic Operation/Setup	Explanation
Set how FET/GPOH/ GPIO recover from ALARM condition * GPIO1/2 to be set to mirror GPOH1/2 * GPOH_FET is set to 1 (refer to previous page)	Set how CHG/DIS pins, GPOH1/2 and GPIO1/2 pins recover from ALARM condition When CHG/DIS pins, GPOH1/2 and GPIO1/2 pins are set to response to ALARM condition, after ALARM condition released (may required judgment by host eg. Current ALARM condition), CHG/DIS pins, GPOH1/2 and GPIO1/2 pins have to be set to recover from ALARM condition. **[Operation]** FDRV_ALM_RCV (register 0x03 b14) determine how CHG/DIS, GPOH1/2 and GPIO1/2 pins response when OV/UV ALARM condition released. When FDRV_ALM_RCV = 0, CHG/DIS, GPOH1/2 and GPIO1/2 pins recover automatically when OV/UV ALARM condition released (after same delay time set for UV/OV detection). When FDRV_ALM_RCV = 1, CHG/DIS, GPOH1/2 and GPIO1/2 pins recover only when FDRV_ALM_CLR (register 0x03 b13) set to 1. For OCC/OCD/SCD ALARM condition, it always recovers only by setting FDRV_ALM_CLR to 1. Please be cautious to control the recovery of CHG/DIS, GPOH1/2 and GPIO1/2 pins from current ALARM, as the factor that cause current ALARM may still be exist eg. Short circuit condition. **[Recovery State]** For CHG/DIS pins, the recovery state is determined by FDRV_CHG_FET and FDRV_DIS_FET (register 0x01 b1:b0) setting. For GPOH1/2 and GPIO1/2 pins, the recovery state is determined by GPOH1_EN and GPOH2_EN (register 0x1B b1:b0) setting. **Note: When FDRV_ALM_RCV is used for recovering from OV/UV condition automatically, it should be set to "0" during initialization.** **FDRV_ALM_CLR is used for recovering from ALARM condition manually, set FDRV_ALAM_CLR = 0 at all time when not use.**
Voltage Measurement	A voltage measurement cycle required 1.3ms. It measure GPIO1/2, VPACK, TMONI1~5, VDD50 and cell voltage C1~C16. Voltage measurement will only be done in Active Mode (and Active Mode* under Standby Mode). **[ON/OFF]** There is two voltage measurement modes available, 1shot measurement (register 0x01 b8 ADC_CONT=0) and continuous mode (register 0x01 b8 ADC_CONT=1). Under continuous mode, voltage measurement repeat after each measurement cycle, while under 1shot measurement, measurement only been done each time when ADC_TRG set to 1 once. ADC_TRG will be auto clear to 0 when the measurement cycle completed. **[Operation]** ADIRQ1 pin (when GPIO5 pin is configured as ADIRQ1 pin.) will be triggered HI and VAD_DONE (register 0x30 b0) will become "1" when a voltage measurement cycle completed. VAD_DONE will be cleared by writing "1" to this register. ADIRQ1 pin will be reset to LO after the measured data been latched to data register 0x33 ~ 0x4B by setting ADV_LATCH (register 0x0A b0) to 1. Only measured data set by CVSEL (register 0x04) and GVSEL (register 0x05) will be latched to data register. To enable Active Mode * in Standby Mode, it is required ADC_CONT =1 and STB_MONEN=1.

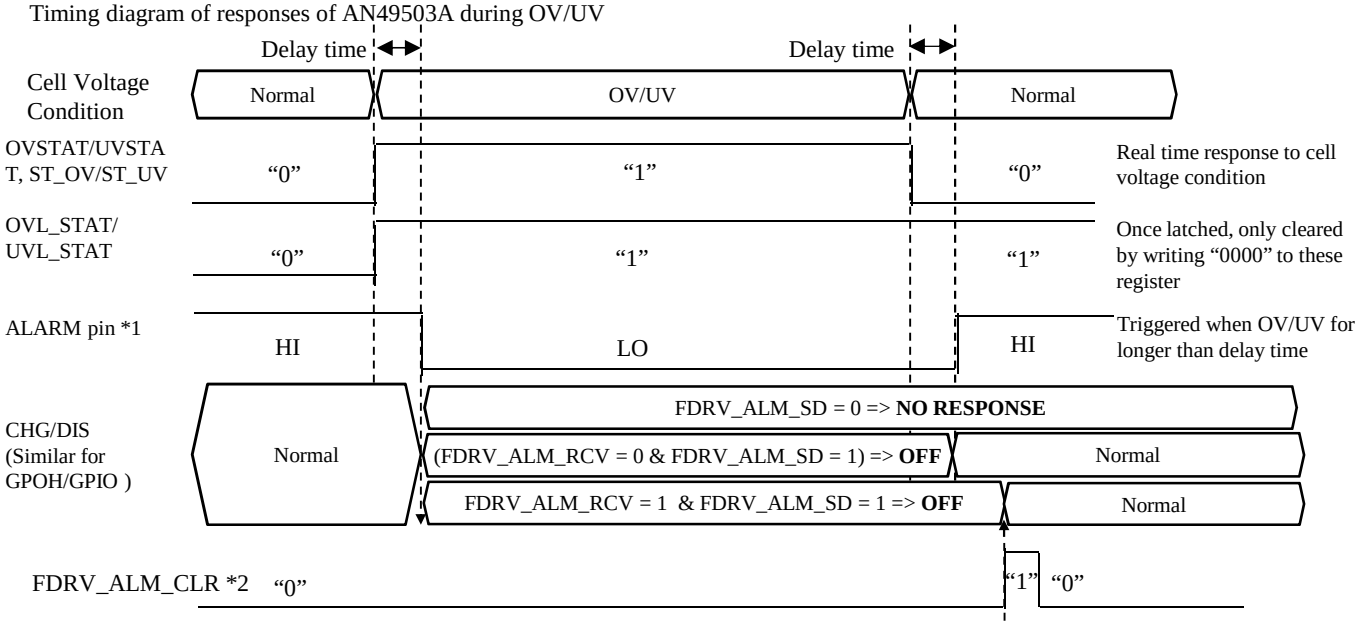
Basic Operation

Basic Operation/Setup	Explanation
Low Speed (LS) Current Measurement	Low speed current measurement is a coulomb counter that average the voltage across SRP and SRN pins for a period of every 250ms. The current can be calculated as measured voltage divided by sense resistor across SRP and SRN pins. The measurement range is -0.18V to 0.18V. **[ON/OFF]** The measurement starts when ADIL_ON (register 0x1A b1) =1 and ADSWSD_EN (register 0x1A b12) = 1. And the current measurement will be continuous in both Active Mode and Standby Mode. **[Operation]** ADIRQ2 pin (when GPIO4 pin is configured as ADIRQ2 output) will be triggered HI and IADS_DONE (register 0x30 b2) will become 1 when a LS current measurement completed. IADS_DONE will be cleared by writing 1 to this register. ADIRQ2 pin will be reset to LO after the measured data been latched to data CVIL_AD(register 0x4D) by setting ADIL_LATCH (register 0x0A b2) to 1.
High Speed (HS) Current measurement	High speed current measurement measures the voltage across SRP and SRN pins for 0.81ms in a 1.3ms cycle. The current can be calculated as measured voltage divided by sense resistor across SRP and SRN pins. The measurement range is -0.18V to 0.18V. **[ON/OFF]** The measurement starts when ADIH_ON (register 0x1A b0) =1 and ADSWHY_EN (register 0x1A b13) = 1. And the current measurement will be continuous in Active Mode only. To perform HS current measurement, voltage measurement is required to be ON. **[Operation]** ADIRQ1 pin (when GPIO5 pin is configured as ADIRQ1 output) will be triggered HI and IADH_DONE (register 0x30 b1) will become 1 when HS current measurement completed. IADH_DONE will be cleared by writing 1 to this register. ADIRQ1 pin will be reset to LO after the measured data been latched to data CVIH_AD(register 0x4C) by setting ADIH_LATCH (register 0x0A b1) to 1.

Basic Operation

Basic Operation/Setup	Explanation
Voltage ALARM Detection (OV/UV)	Voltage ALARM (OV/UV) detection is done through voltage measurement. It can only be done under Active Mode and Active Mode* under Standby Mode. The cell voltage to be detected by OV/UV is set in register OVMSK and UVMSK. **[ON/OFF]** In Active Mode, if continuous voltage measurement is set (i.e. register ADC_CONT=1), the voltage ALARM detection is done continuously. If 1shot voltage measurement is set (i.e. register ADC_CONT =0), the voltage ALARM detection is done every time register ADC_TRG is set to 1. In Standby Mode, as voltage measurement is stopped, OV/UV can only be done under Active Mode* when no SPI communication between AN49503A and host for 1 second. This required both registers ADC_CONT and STB_MONEN to be set to 1. (refer to previous pages) **[Setting]** The setting parameters for OV/UV including threshold voltage, delay time and hysteresis level. (refer to previous pages) **[Trigger]** When a voltage condition meet the threshold level set for longer than delay time set, ALARM pins (refer to "ALARM pin setting" from previous pages) will be triggered LO. Also, the OV/UV status can be read from status register 0x30 STAT, 0x31 OVSTAT, 0x32 UVSTAT, 0x52 OVL_STAT, 0x53 UVL_STAT. DIS/CHG, GPOH1/2 and GPIO1/2 pins will response to this ALARM depend on the register FDRV_ALM_SD and GPOH_FET (refer to previous pages) setting. **[Release]** When the voltage condition removed (by hysteresis level set from threshold level) for longer than delay time set, the ALARM condition is cleared. How DIS/CHG, GPOH1/2 and GPIO1/2 pins will response to the clearance of voltage ALARM condition depend on FDRV_ALM_RCV and FDRV_ALM_CLR (refer to previous pages) setting.

Timing diagram of responses of AN49503A during OV/UV

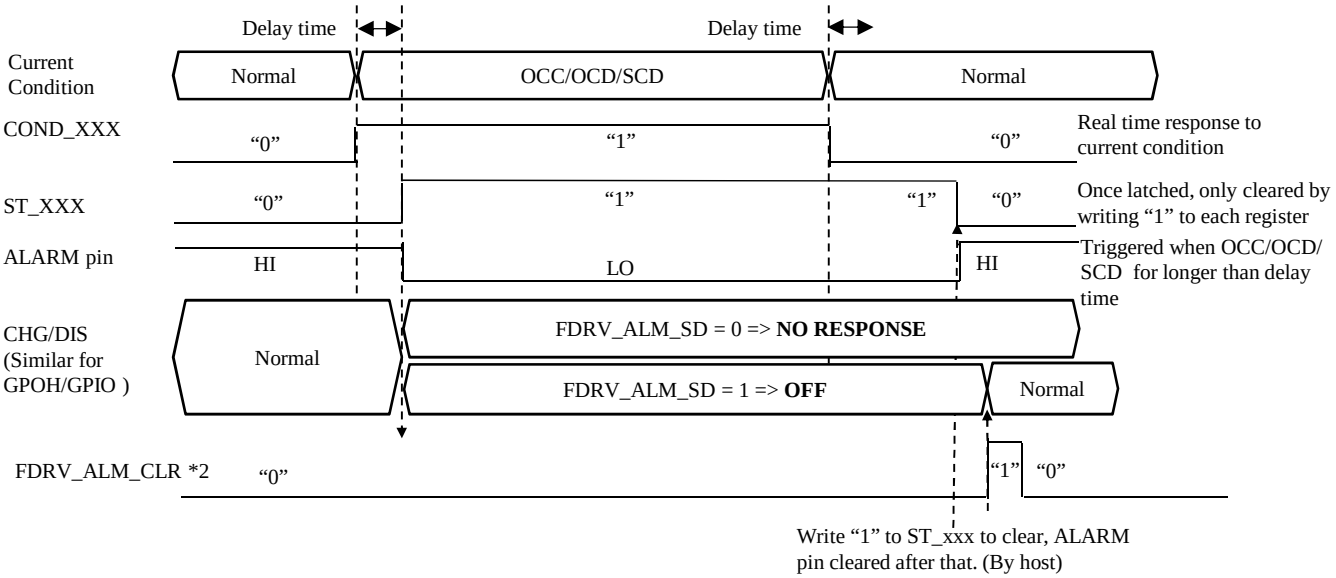


***1 The ALARM pin to response to OV/UV depend on ALARMSEL setting**
***2 FDRV_ALM_CLR should only be set to "1" to release ALARM condition of CHG/DIS, it should be set to "0" after this. The timing to activate it is depend on host.**

Basic Operation

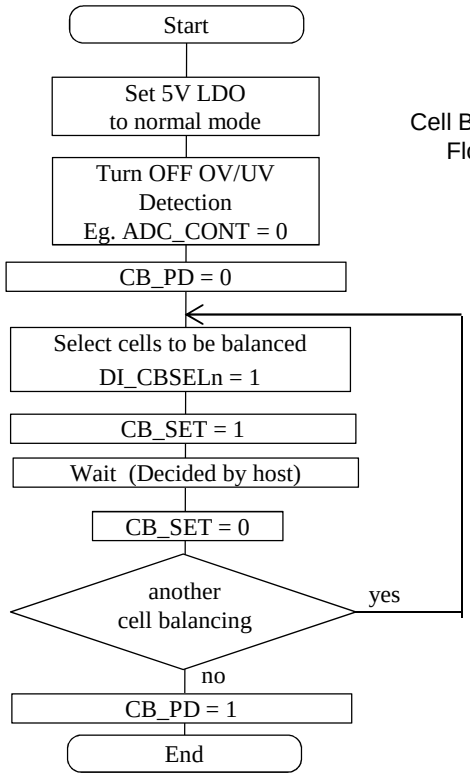
Basic Operation/Setup	Explanation
Current ALARM Detection (OCC/OCD/SCD)	The current ALARM (OCC/OCD/SCD) detection is done by comparators comparing voltage between SRP and SRN pins and threshold level set. **[ON/OFF]** The current ALARM detection started with register 0x11 b3:b0 EN_SCD, EN_OCD, EN_OCC and EN_CP set to 1. It operates in both Active Mode and Standby Mode. **[Setting]** The setting parameters for OCC/OCD/SCD including threshold voltage and delay time. (refer to previous pages) **[Trigger]** When a current abnormal condition over the threshold level set for longer than delay time set, ALARM pins (refer "ALARM pin setting" from previous pages) will be triggered. Register 0x22 b5:b3 COND_SCD, COND_OCD, COND_OCC will be set to 1 once current condition meet the threshold set, when the ALARM pins triggered, register 0x30 b6:b4 ST_SCD, ST_OCD and ST_OCC will be set to 1. DIS/CHG, GPOH1/2 and GPIO1/2 pins will response to this ALARM depend on the register FDRV_ALM_SD and GPOH_FET (refer to previous pages) setting. **[Release]** To clear ALARM cause by current ALARM condition, register FDRV_ALM_CLR is used. (refer to previous pages). DIS/CHG, GPOH1/2 and GPIO1/2 pins will response to the clearance of current ALARM condition depend on FDRV_ALM_CLR. (refer to previous pages) COND_OCC, COND_OCD and COND_SCD will be cleared once current condition removed, while ST_OCC, ST_OCD and ST_SCD required to be cleared by writing 1. **Note: When CHG/DIS pins are turned OFF upon current ALARM condition, the current level may be reduced to none, while the cause of current ALARM condition (eg. Short at pack output) may remain exist. The removal of cause of current ALARM condition required the judgment of host.**

Timing diagram of responses of AN49503A during OCC/OCD/SCD

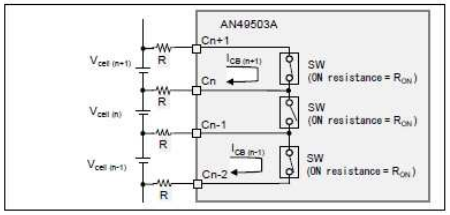


***1 The ALARM pin response to OCC/OCD/SCD depend on ALARMSEL setting**
***2 FDRV_ALM_CLR should only be set to "1" to release ALARM condition of CHG/DIS, it should be set to "0" after this. The timing to activate it is depend on host.**

Basic Operation

Basic Operation/Setup	Explanation
Cell Balance	The cell balance function is a control of the internal switch between each adjacent cell input pins e.g. C15 and C14, C14 and C13 etc With external circuit, cell balance can be achieved (refer to figure below) by bypassed cell voltage dependent current through internal switch (internal cell balance) or external MOSFET (external cell balance).  Cell Balance Setting Flow Example **Note : The cell balance threshold level and the duration for turning on the cell balance are controlled by host, there are no register built into AN49503A. There is the only control of ON/OFF for the switch in AN49503A.** **Note : As the cell balance turn ON the internal switch between cell voltage input, measured cell voltage could be abnormal. OV/UV detection should be turned OFF during cell balance operation. Eg. The OV/UV should be disabled if cell balance is to be performed under Standby Mode with Active Mode* ON.** **Note : LDO should be in Normal Mode (50mA drivability) instead of Low Power Mode (5mA drivability) during cell balance mode.** **Note : Adjacent cells should not be cell balanced at the same time.**

Internal Cell Balance Circuit Example



External Cell Balance Circuit Example