Panasonic

**AN49502A**

# Multicell Battery Stack Monitor IC

## FEATURES

- Voltage measurement of up to 10 battery cells
- High accuracy voltage detection (total 10 cells)
  Measurement accuracy: ±10mV
- Control signal output for cell balancing switch
- Temperature measurement pin: 2-channels
- Built-in 14-bit delta-sigma ADC
- Serial control with microcomputer interface
- Daisy chain connection enable
- Built-in regulator (5V) for the peripheral circuits

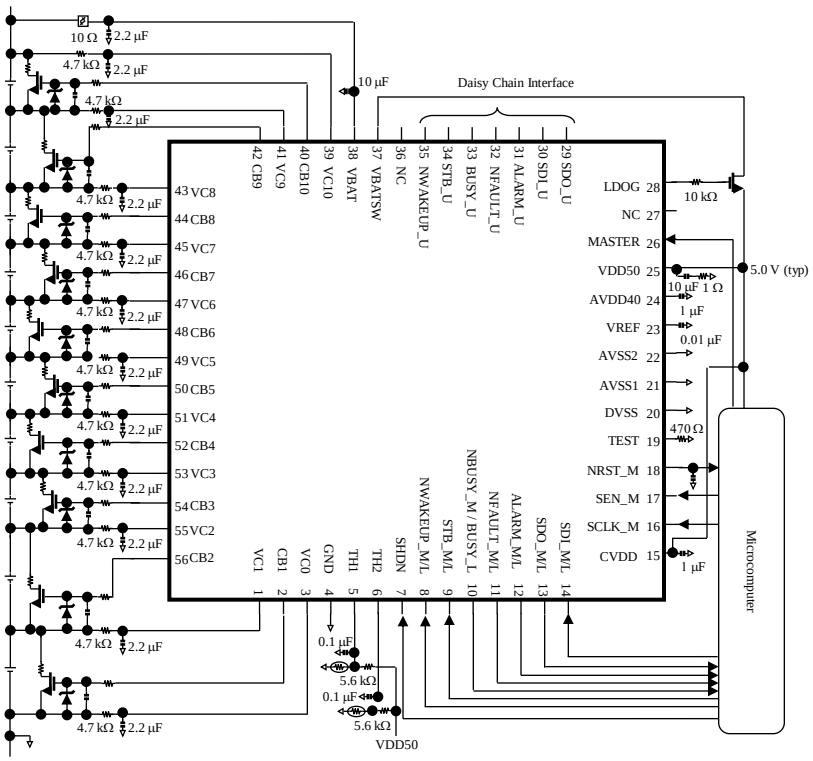
## DESCRIPTION

AN49502A is a multicell battery stack monitor IC.
This IC, capable of voltage measurement of up to 10 battery cells connected in series with maximum 53-V input common mode voltage, is optimized for applications such as batteries for high-voltage operation.
This IC has a built-in regulator necessary for the peripheral circuits.

## APPLICATIONS

- UPS for server, storage battery, etc

### SIMPLIFIED APPLICATION




Notes: *This application circuit is an example. Operation of mass production set is not guaranteed.
Perform enough evaluation and verification on the design of mass production set.

## CONTENTS

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit | Notes |
|---|---|---|---|---|
| Supply Voltage | $V_{VBAT}$ | 58 | V | *1 |
| | $V_{CVDD}$ | 6.5 | V | *1 |
| Operating Ambient Temperature | $T_{opr}$ | -40 ~ +85 | °C | *2 |
| Operating Junction Temperature | $T_j$ | -40 ~ 125 | °C | *2 |
| Storage Temperature | $T_{stg}$ | -55 ~ 125 | °C | *2 |
| Power dissipation | $P_D$ | 254 | mW | *3 |
| Input Voltage Range | VCn (n=0~10), THn (n=1, 2) | -0.3 ~ 58 | V | — |
| | SHDN, NWAKEUP_M/L, STBM/L, SDI_M/L, SCLK_M, SEN_M, TEST, MASTER | -0.3 ~ 6.5 | V | — |
| | SDI_U, ALARM_U, NFAULT_U, BUSY_U | -0.3 ~ 58 | V | — |
| Output Voltage Range | CBn (n=1~10) | -0.3 ~ 58 | V | — |
| | NBUSY_M/BUSY_L, NFAULT_M/L, ALARM_M/L, SDO_M/L, NRST_M, VDD50 | -0.3 ~ 6.5 | V | — |
| | SDO_U, STB_U, NWAKEUP_U | -0.3 ~ 58 | V | — |
| | LDOG, VBATSW | -0.3 ~ 58 | V | — |
| Allowable Voltage between Pins | $VC_n - VC_{n-1}$ | -0.3 ~ 11 | V | *4 |
| | $CB_n - VC_{n-1}$ | -0.3 ~ 11 | V | *4 |
| | $VC_n - CB_n$ | -0.3 ~ 11 | V | *4 |
| | $V_{GND\_N+1} - V_{VBAT\_N}$ | -1 ~ 1 | V | *5 |
| ESD | HBM | ±2000 | V | — |

Notes: This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1 :The values are defined, provided that the IC is used within all of the above absolute maximum ratings including the power dissipation.

*2 : All ratings are at Ta = 25°C, except the power dissipation, operating ambient temperature, and storage temperature.

*3: The power dissipation shown is the value at Ta = 85℃ for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the PD-Ta diagram (refer pg.49) of the package standard and design the heat radiation with sufficient margin not to exceed the allowable value based on the conditions of power supply voltage, load, and ambient temperature.

*4: n = 1 ~ 10 (refer to cell number)

*5: If the daisy chain communication is used, the voltage between $V_{GND\_N+1}$ and $V_{VBAT\_N}$ should be within +/- 1V. ($V_{GND\_N+1}$ : GND voltage of #(N+1) device, $V_{VBAT\_N}$ : VBAT voltage of #N device, N:refer to device number)

)

## POWER DISSIPATION RATING

| Package | θ j-a | θ j-c | $P_D$(Ta=25°C ) | $P_D$(Ta=85°C ) |
|---|---|---|---|---|
| TQFP056-P-1010 | 84.3 ° C/W | 8.3 ° C/W | 637 mW | 254 mW |

Note: For the actual usage, please refer to the $P_D$-Ta characteristics diagram (refer to pg.49) in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

**CAUTION**

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage range | $V_{VBAT}$ | 12.5 | — | 53 | V | *1 |
| | $V_{CVDD}$ | 3.2 | — | 5.5 | V | *1,*2 |
| | | $V_{VDD}$ | | | V | *1,*3 |
| | $V_{GND\_N+1} - V_{VBAT\_N}$ | -1 | — | +1 | V | *4 |
| Input Voltage Range | $V_{(VCn - VCn-1)}$ (n=1~10) | 0 | 3.7 | 5 | V | — |
| | $V_{THn}$ (n=1, 2) | 0 | — | 4 | V | — |
| | $V_{SHDN}$, $V_{NWAKEUP\_M/L}$ | 0 | — | $V_{VC1}$ | V | — |
| | $V_{STBM/L}$, $V_{SDI\_M/L}$, $V_{SCLK\_M}$, $V_{SEN\_M}$, $V_{TEST}$, $V_{MASTER}$ | 0 | — | $V_{CVDD}$ | V | — |
| | $V_{SDI\_U}$, $V_{ALARM\_U}$, $V_{NFAULT\_U}$, $V_{BUSY\_U}$ | $V_{VBAT}$ - 3 | — | $V_{VBAT}$ + 0.1 | V | — |
| Output Voltage Range | $V_{CBn}$ (n=1~10) | $V_{VCn-1}$ | — | $V_{VCn}$ | V | — |
| | $V_{NBUSY\_M/BUSY\_L}$, $V_{NFAULT\_M/L}$, $V_{ALARM\_M/L}$, $V_{SDO\_M/L}$, $V_{NRST\_M}$, $V_{VDD50}$ | 0 | — | $V_{CVDD}$ | V | — |
| | $V_{SDO\_U}$, $V_{STB\_U}$, $V_{NWAKEUP\_U}$ | 0 | — | $V_{VBAT}$ + 0.1 | V | — |

Notes: *1: The value is defined, provided that the IC is used within all of the above absolute maximum ratings including the power dissipation.

*2: This value is shown when external voltage is supplied (MASTER = "H").

*3: $V_{VDD}$ is VDD50 pin (pin25) voltage. Connect CVDD pin to VDD50 pin in Slave device (MASTER = "L").

*4: If the daisy chain communication is used, the voltage between $V_{GND\_N+1}$ and $V_{VBAT\_N}$ should be within +/- 1V. ($V_{GND\_N+1}$ : GND voltage of #(N+1) device, $V_{VBAT\_N}$ : VBAT voltage of #N device)

## ELECTRICAL CHARACTERISTICS

$V_{VBAT}$ = 37 V

Note: Ta= 25°C ± 3°C, unless otherwise specified.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Supply Current (VBAT)** | | | | | | | |
| VBAT Active (CVDD = VDD50) | $I_{BAT1}$ | — | — | 10 | 13 | mA | *1 |
| VBAT Standby (CVDD = VDD50) | $I_{BAT2}$ | — | — | 170 | 340 | μA | *1 |
| VBAT Shutdown | $I_{BAT3}$ | — | 0 | — | 1 | μA | — |
| **LDO** | | | | | | | |
| VDD50 output voltage | $V_{VDD}$ | — | 4.5 | 5.0 | 5.5 | V | — |
| VDD50 drive current (1) | $I_{REG1}$ | Active mode | 0 | — | 15 | mA | — |
| VDD50 drive current (2) | $I_{REG2}$ | Standby mode | 0 | — | 5 | mA | — |
| **DC Bias** | | | | | | | |
| AVDD40 pin voltage | $V_{AVDD}$ | — | 3.8 | 4.0 | 4.2 | V | — |
| VREF pin voltage | $V_{REF}$ | — | 1.8 | 2.0 | 2.2 | V | — |
| **Cell Balancing Control Output** | | | | | | | |
| Output voltage (High) | $V_{CB1}$ | — | $VC_n$ – 0.2 | $VC_n$ | $VC_n$ + 0.2 | V | — |
| Output voltage (Low) | $V_{CB2}$ | — | $VC_{n-1}$ – 0.2 | $VC_{n-1}$ | $VC_{n-1}$ + 0.2 | V | — |
| Discharge Switch-On Resistance (CB1-9) | $R_{CB1}$ | $\Delta VC_n \geq 3V$ | — | 5 | 6.5 | κΩ | — |
| Discharge Switch-On Resistance (CB10) | $R_{CB2}$ | $\Delta VC_{10} \geq 3V$ | — | 12.5 | 16.3 | kΩ | — |
| **Thermal Shutdown** | | | | | | | |
| Shutdown threshold | $T_{THUT}$ | Tj | — | 170 | — | °C | *2, 3 |

Notes: *1: The value does not include sink and source current flowing into daisy chain interface pins.

*2: When Thermal Shutdown is activated, all circuits are shut down. Therefore, run the wake up sequence again.

*3: These are values checked by design but not production tested.

## ELECTRICAL CHARACTERISTICS (continued)

$V_{VBAT}$ = 37 V

Note: Ta= 25°C ± 3°C, unless otherwise specified.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Cell Voltage Monitor** | | | | | | | |
| Input voltage range | $\Delta VC_n$ | $\Delta VC_n = VC_n - VC_{n-1}$<br>$VC_{10} \leq V_{VBAT} + 1$ V | 0 | — | 5 | V | *4, 5 |
| Voltage resolution | $V_{RES}$ | 0.3 mV/LSB | — | 14 | — | Bits | *3 |
| Voltage accuracy (1) Average | $V_{ACC\_VC1}$ | $\Delta VC_n$ = 2.5 V, 4.5 V | –10 | 0 | 10 | mV | *5 |
| Voltage accuracy (2) Average | $V_{ACC\_VC1}$ | $\Delta VC_n$ = 1.5 V | –50 | 0 | 50 | mV | *5 |
| Conversion time | $t_{CONV}$ | — | 7 | 8 | 9 | ms | *6 |
| Effective Input current | $I_{IN}$ | Active mode<br>$\Delta VC_n$ = 5.0 V | –5 | 0 | 5 | µA | *1 |
| Input leakage current | $I_{LK}$ | Shutdown mode<br>$\Delta VC_n$ = 5.0 V | –1 | 0 | 1 | µA | *1 |
| **Thermistor Voltage Monitor** | | | | | | | |
| Input voltage range | $V_{IN}$ | — | 0 | — | 4 | V | *4 |
| Voltage resolution | $V_{RES}$ | 0.3 mV/LSB | — | 14 | — | Bits | *3 |
| Voltage accuracy | $V_{ACC\_TH}$ | $\Delta VC_n$ = 0.5 V, 4 V | –75 | 0 | 75 | mV | — |
| Effective Input current | $I_{IN}$ | Active,Vin = 0 V, 4 V | –5 | 0 | 5 | µA | — |
| **Daisy chain I/O(BUSY_L, NFAULT_L, ALARM_L, SDO_L)** | | | | | | | |
| Source current | $I_O$ | MASTER = "L" | –1.3 | –1.0 | –0.7 | mA | *7 |
| **Daisy chain I/O(SDO_U)** | | | | | | | |
| Sink current | $I_O$ | — | 0.7 | 1.0 | 1.3 | mA | *8 |
| **Daisy chain I/O(NWAKEUP_U)** | | | | | | | |
| Sink current | $I_O$ | — | 35 | 50 | 65 | µA | *8 |
| **Daisy chain I/O(STB_U)** | | | | | | | |
| Sink current | $I_O$ | — | 70 | 100 | 130 | µA | *8 |

Notes: *1: The value does not include sink and source current flowing into daisy chain interface pins.

*3: These are values checked by design but not production tested.

*4: Exceeding the voltage described above might generate rush current due to the clamp in internal circuit.

*5: n = 1 to 10

*6: The value is required time for voltage measurement of 10 cells.

*7: 0 V ≤ Pin voltage ≤ +1.0 V

*8: $V_{CVDD} \leq$ Pin voltage $\leq V_{VBAT}$ + 0.3 V

## ELECTRICAL CHARACTERISTICS (continued)

$V_{VBAT}$ = 37 V

Note: Ta= 25°C ± 3°C, unless otherwise specified.

| Parameter | | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| **Digital Input(1) (NWAKEUP_M)** | | | | | | | | |
| | Input Voltage High | $V_{IH}$ | — | 0.8 × $V_{VC1}$ | — | $V_{VC1}$ | V | — |
| | Input Voltage Low | $V_{IL}$ | — | $V_{DVSS}$ | — | 0.2 × $V_{VC1}$ | V | — |
| | Pull-up resistance | $R_{IH}$ | — | 150 | 250 | 400 | kΩ | — |
| **Digital Input(2) (SHDN)** | | | | | | | | |
| | Input Voltage High | $V_{IH}$ | — | 0.8 × $V_{VC1}$ | — | $V_{VC1}$ | V | — |
| | Input Voltage Low | $V_{IL}$ | — | $V_{DVSS}$ | — | 0.2 × $V_{VC1}$ | V | — |
| | Pull-down resistance | $R_{IL}$ | — | 300 | 820 | 1300 | kΩ | — |
| **Digital Input (3)(SDI_M, SCLK_M, SEN_M,)** | | | | | | | | |
| | Input Voltage High | $V_{IH}$ | — | 0.8 × $V_{CVDD}$ | — | $V_{CVDD}$ | V | *9, 10 |
| | Input Voltage Low | $V_{IL}$ | — | $V_{DVSS}$ | — | 0.2 × $V_{CVDD}$ | V | *9, 10 |
| | Input leakage current | $I_{LK}$ | — | –10 | 0 | 10 | μA | *9, 10 |
| **Digital Input (4)(STB_M)** | | | | | | | | |
| | Input Voltage High | $V_{IH}$ | — | 0.8 × $V_{CVDD}$ | — | $V_{CVDD}$ | V | — |
| | Input Voltage Low | $V_{IL}$ | — | $V_{DVSS}$ | — | 0.2 × $V_{CVDD}$ | V | — |
| | Pull-up resistance | $R_{IL}$ | — | 60 | 100 | 160 | kΩ | — |
| **Digital Output(1) (NFAULT_M, NBUSY_M, SDO_M)** | | | | | | | | |
| | Output Voltage High | $V_{OH}$ | $I_{OH}$ = –1 mA | $V_{CVDD}$ – 0.6 | — | $V_{CVDD}$ | V | *9, 10 |
| | Output Voltage Low | $V_{OL}$ | $I_{OH}$ = +1 mA | 0 | — | 0.4 | V | *9, 10 |
| **Digital Output(2) (NRST_M)** | | | | | | | | |
| | Output Voltage Low | $I_{OL}$ | $I_{OH}$ = 0 mA | 0 | — | 0.4 | V | — |
| | Pull-up resistance | $R_{IL}$ | — | 60 | 100 | 160 | kΩ | — |

Notes: *9: In Shutdown mode, each digital pin is set to Hi-Z, and connected to pull-down resistor of 100 kΩ (typ) simultaneously.

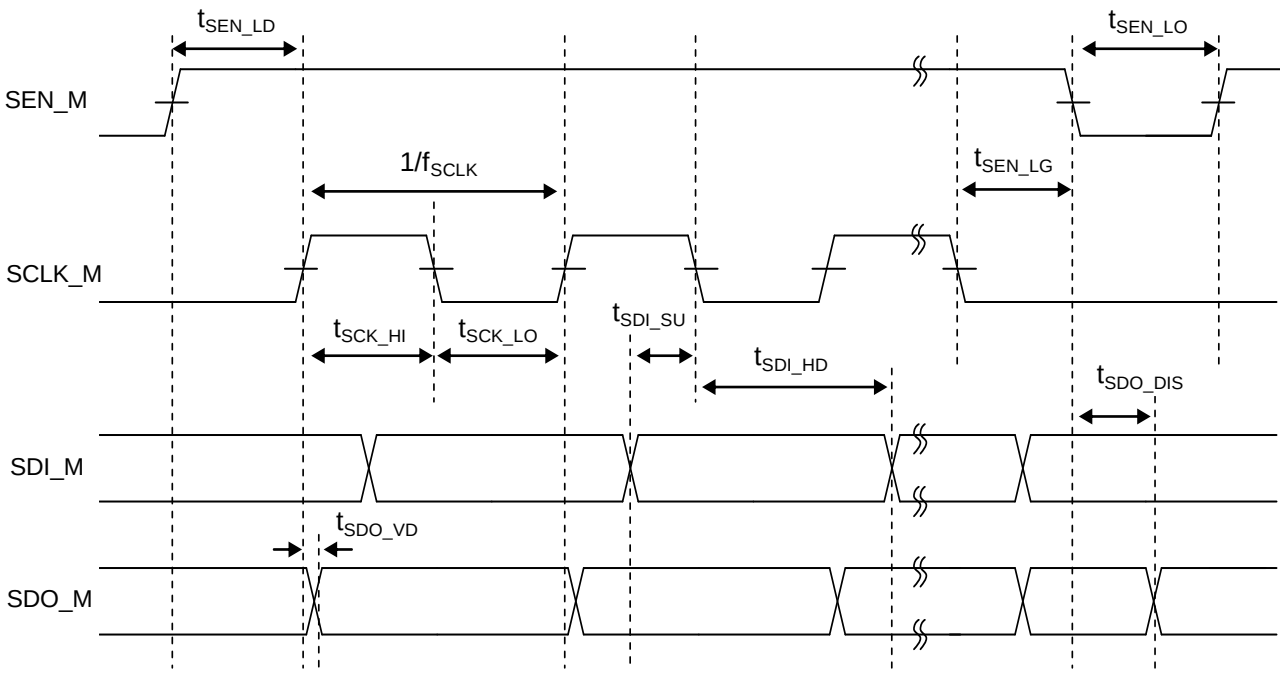
*10: The value is not applicable to SCLK_M and SEN_M when MASTER = “L”.

## ELECTRICAL CHARACTERISTICS (continued)

$V_{VBAT}$ = 37 V

Note: Ta= 25°C ± 3°C, unless otherwise specified.

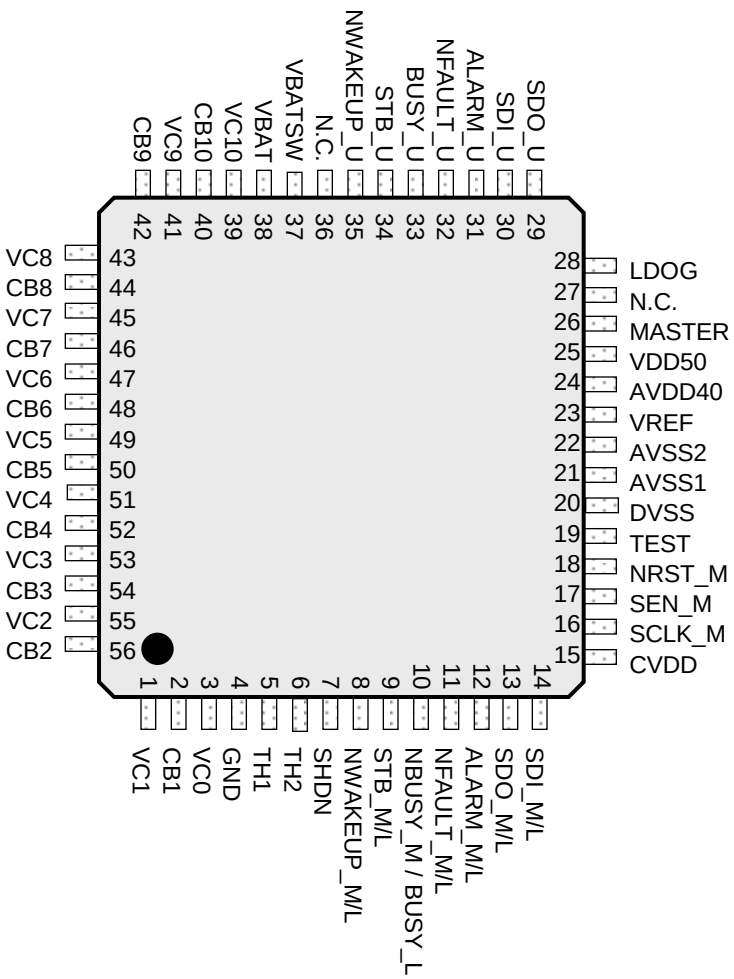
| Parameter | | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| **Microcomputer SPI data interface** | | | | | | | | |
| | SCLK_M frequency | $f_{SCK}$ | — | — | — | 500 | kHz | — |
| | SCLK_M Duty cycle | $t_{DUTY}$ | — | 45 | 50 | 55 | % | — |
| | SEN_M rising to SCLK_M rising | $t_{SEN\_LD}$ | — | 100 | — | — | ns | — |
| | SCLK_M falling to SEN_M falling | $t_{SEN\_LG}$ | — | 100 | — | — | ns | — |
| | SEN_M "Low" width | $t_{SEN\_LO}$ | — | 500 | — | — | ns | — |
| | SDI_M setup time | $t_{SDI\_SU}$ | SDI_M valid to SCLK_M falling | 100 | — | — | ns | — |
| | SDI_M hold time | $t_{SDI\_HD}$ | SCLK_M falling to SDI_M valid | 100 | — | — | ns | — |
| | SDO_M valid time | $t_{SDO\_VD}$ | SCLK_M rising to SDO_M valid $C_L \leq 50$ pF | — | — | 400 | ns | — |
| | SDO_M disable time | $t_{SDO\_DIS}$ | SEN_M falling to SDO_M disable | — | — | 400 | ns | — |
| | WDT | $t_{WDT}$ | default = 22min.(typ) | –10 | 0 | 10 | % | — |




SPI Timing Diagram

## PIN CONFIGURATION

Top View



## PIN FUNCTIONS

| Pin No | Pin Name | Type | Description |
|---|---|---|---|
| 1 | VC1 | Input | Cell 2 voltage input (-)/ cell 1 voltage input (+) |
| 2 | CB1 | Output | Transistor drive for cell balancing 1 |
| 3 | VC0 | Input | Cell 1 voltage input (-) |
| 4 | GND | Ground | Ground for analog circuit |
| 5 | TH1 | Input | Thermistor voltage input 1 |
| 6 | TH2 | Input | Thermistor voltage input 2 |
| 7 | SHDN | Input | Shutdown control signal input ("L": Active, "H": Shutdown) |
| 8 | NWAKEUP_M/L | Input | MASTER = "H": Wake up control voltage input ("L": Wake up, "H": Normal)<br>MASTER = "L": Wake up control current input ("L": Wake up, "H": Normal) |
| 9 | STB_M/L | Input | MASTER = "H": Standby signal input for microcomputer interface ("L": Wake up, "H": Standby)<br>MASTER = "L": Standby signal input for daisy chain interface ("L": Standby, "H": Wake up) |
| 10 | NBUSY_M/ BUSY_L | Output | MASTER = "H": BUSY signal output for microcomputer interface<br>MASTER = "L": BUSY signal output for daisy chain interface |
| 11 | NFAULT_M/L | Output | MASTER = "H": FAULT signal output for microcomputer interface<br>MASTER = "L": FAULT signal output for daisy chain interface |
| 12 | ALARM_M/L | Output | MASTER = "H": ALARM signal output for microcomputer interface<br>MASTER = "L": ALARM signal output for daisy chain interface |
| 13 | SDO_M/L | Output | MASTER = "H": Serial data output for microcomputer interface<br>MASTER = "L": Serial data output for daisy chain interface |
| 14 | SDI_M/L | Input | MASTER = "H": Serial data input for microcomputer interface<br>MASTER = "L": Serial data input for daisy chain interface |
| 15 | CVDD | Power Supply | Supply voltage for digital I/O |
| 16 | SCLK_M | Input | Serial clock input for microcomputer interface |
| 17 | SEN_M | Input | SPI for microcomputer interface enable ("H": Enable) |
| 18 | NRST_M | Output | Power-on reset output for microcomputer |
| 19 | TEST | Input | Test mode select (* Connect to DVSS fixed.) |
| 20 | DVSS | Ground | Ground for digital circuit |
| 21 | AVSS1 | Ground | Ground for analog circuit |
| 22 | AVSS2 | Ground | Ground for analog circuit |
| 23 | VREF | Output | Reference voltage for ADC: 2.0 V (typ) |
| 24 | AVDD40 | Output | Internal regulator pin for analog circuit: 4.0 V (typ) |
| 25 | VDD50 | Output | Sense pin for external high withstand voltage regulator: 5.0 V (typ) |
| 26 | MASTER | Input | "H" (CVDD): Master device connected with microcomputer<br>"L" (DVSS) : Slave device connected in daisy chain configuration |

## PIN FUNCTIONS (continued)

| Pin No | Pin Name | Type | Description |
|---|---|---|---|
| 27 | NC | — | N.C. |
| 28 | LDOG | Output | External power transistor gate |
| 29 | SDO_U | Output (Sink) | Serial data output for daisy chain interface |
| 30 | SDI_U | Input (Pull-down) | Serial data input for daisy chain interface |
| 31 | ALARM_U | Input (Pull-down) | ALARM signal input for daisy chain interface |
| 32 | NFAULT_U | Input (Pull-down) | FAULT signal input for daisy chain interface |
| 33 | BUSY_U | Input (Pull-down) | BUSY signal input for daisy chain interface |
| 34 | STB_U | Output (Sink) | Standby signal output for daisy chain interface |
| 35 | NWAKEUP_U | Output (Sink) | Wake up signal output for daisy chain interface |
| 36 | NC | — | N.C. |
| 37 | VBATSW | Output | External power transistor drain |
| 38 | VBAT | Power Supply | Maximum voltage |
| 39 | VC10 | Input | Cell 10 voltage input (+) |
| 40 | CB10 | Output | Transistor drive for cell balancing 10 |
| 41 | VC9 | Input | Cell 10 voltage input (-)/ cell 9 voltage input (+) |
| 42 | CB9 | Output | Transistor drive for cell balancing 9 |
| 43 | VC8 | Input | Cell 9 voltage input (-)/ cell 8 voltage input (+) |
| 44 | CB8 | Output | Transistor drive for cell balancing 8 |
| 45 | VC7 | Input | Cell 8 voltage input (-)/ cell 7 voltage input (+) |
| 46 | CB7 | Output | Transistor drive for cell balancing 7 |
| 47 | VC6 | Input | Cell 7 voltage input (-)/ cell 6 voltage input (+) |
| 48 | CB6 | Output | Transistor drive for cell balancing 6 |
| 49 | VC5 | Input | Cell 6 voltage input (-)/ cell 5 voltage input (+) |
| 50 | CB5 | Output | Transistor drive for cell balancing 5 |
| 51 | VC4 | Input | Cell 5 voltage input (-)/ cell 4 voltage input (+) |
| 52 | CB4 | Output | Transistor for drive cell balancing 4 |
| 53 | VC3 | Input | Cell 4 voltage input (-)/ cell 3 voltage input (+) |
| 54 | CB3 | Output | Transistor drive for cell balancing 3 |
| 55 | VC2 | Input | Cell 3 voltage input (-)/ cell 2 voltage input (+) |
| 56 | CB2 | Output | Transistor drive for cell balancing 2 |

## OPERATION

1.Analog to Digital Conversion

1.1 Overview

Cell voltage can be converted to digital code by built-in ADC.

1.2 Analog Level vs Digital Code

1.2.1 Cell Voltage

- Maximum input value: 4.999695 V = 5.0 V × $(2^{14} - 1) / 2^{14}$
- Minimum input value: 0 V
- Theoretical resolution: 0.000305 V = 5.0 V / $2^{14}$

| Analog level [V] (typ) | Code | Digital output (Address : 0x12, CSEL01_[13:0] to Address : 0x1B, CSEL10_[13:0]) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MSB | | | | | | | | | | | | | LSB |
| | | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 4.999695 | 0x1FFF | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| 2.500305 | 0x0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2.500000 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2.499695 | 0x3FFF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| 0.000305 | 0x2001 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0.000000 | 0x2000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

1.2.2 Thermistor Voltage

- Maximum input value: 4.999695 V + 0.02 V = 5.0 V × $(2^{14} - 1) / 2^{14}$ + 0.02 V
- Minimum input value: 0 V + 0.02 V
- Theoretical resolution: 0.000305 V = 5.0 V / $2^{14}$

Note: The above values are theoretical values. The actual maximum input value is 4.0 V.

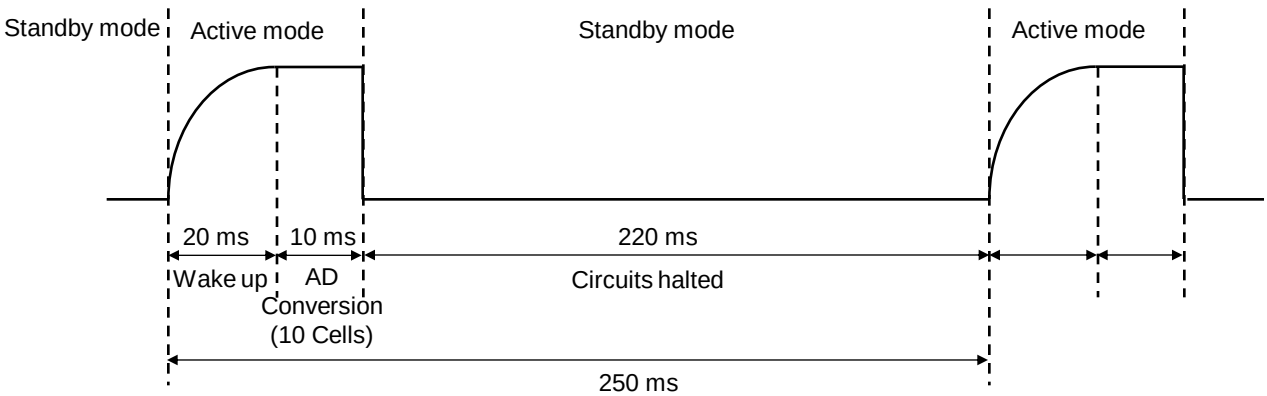
| Analog level [V] (typ) | Code | Digital output (Address : 0x1C, TH1_[13:0], Address : 0x1D, TH2_[13:0]) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MSB | | | | | | | | | | | | | LSB |
| | | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 4.999695+0.02 | 0x1FFF | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| 2.500305+0.02 | 0x0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2.500000+0.02 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2.499695+0.02 | 0x3FFF | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| 0.000305+0.02 | 0x2001 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0.000000+0.02 | 0x2000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## OPERATION (continued)

1.Analog to Digital Conversion (continued)

1.3 Measurement of Cell Voltage

- Power consumption can be reduced by switching to Standby mode after cell voltages are converted and read during Active mode.
- It takes about 20 ms to stabilize circuits after entering Active mode from Standby mode.
- After the elapse of 10 ms from circuit stabilized, the A/D conversion values of 10 cells are stored to data registers when ADC_CONV = 1.
- Enter Standby mode from Active mode when STB_M pin = "H".




Example of intermittent operation (Active mode to Standby mode and repeating)

## OPERATION (continued)

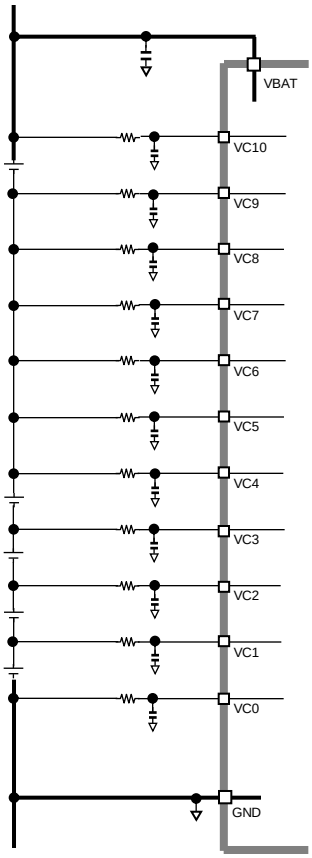
2. Cell Voltage Monitor

2.1 Notes for the Number of Cell Connection

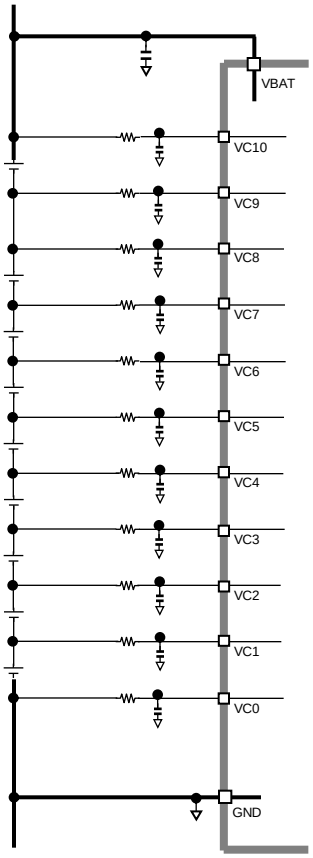
- Must supply VC1-GND over 1.5 V.
- Must use VC10-VC9, VC4-VC3, VC3-VC2, VC2-VC1, and VC1-VC0.
  (VC10–VC9 ≥ 1.3 V, VC4–VC3 ≥ 1.3 V, VC3–VC2 ≥ 1.3 V, VC2–VC1 ≥ 1.3 V, VC1–VC0 ≥ 1.5 V)
- Connect unused VC pins to adjacent VC pins to equalize potential. (See below diagrams.)
- Disable MUX signal for unused cells by CVSEL[10:1] (0x08) setting. If MUX signal for unused cells is enabled, the accuracy of voltage measurement might be decayed.

2.2 Connection Diagram

Recommended connection diagrams are shown in below diagrams.




5-cell connection



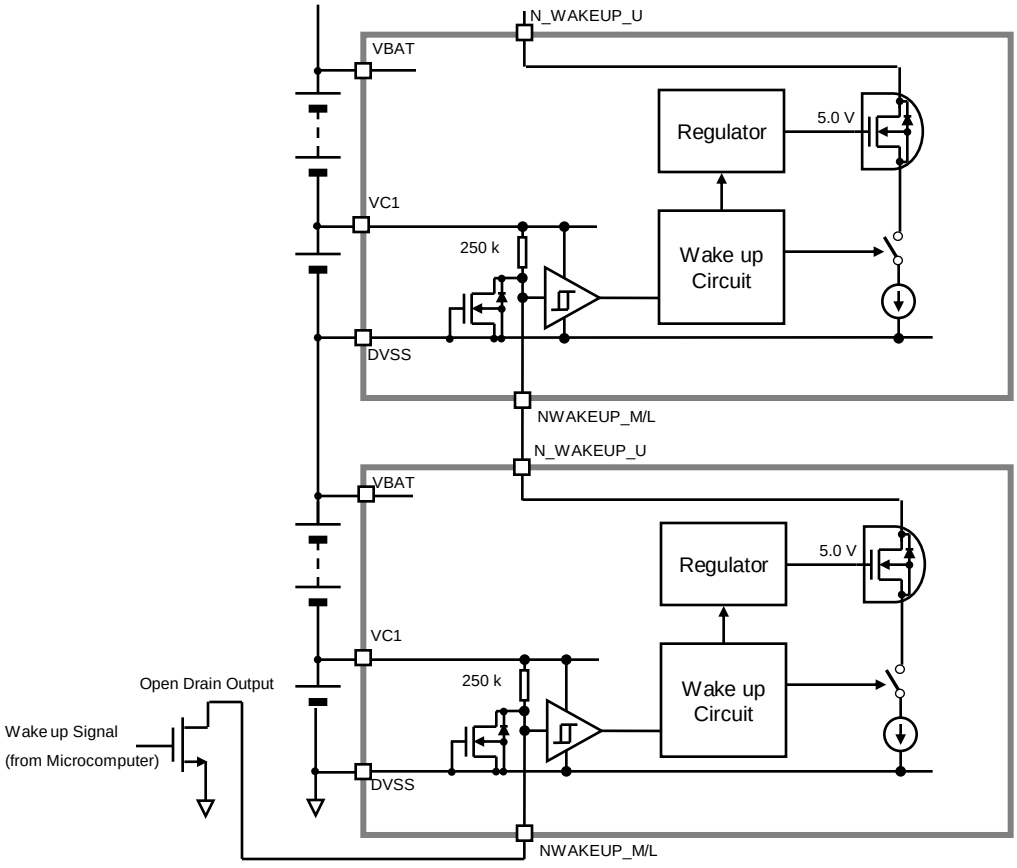

9-cell connection

## OPERATION (continued)

3. Operation Mode

3.1 Active Mode

- When NWAKEUP_M/L pin = "L" for the master device, all circuits are woken up and operate in Active mode. In addition, the master device can wake up all slave devices from bottom to top via daisy chain interface (NWAKEUP_M/L and NWAKEUP_U).
- Supply VC1-GND over 1.5 V.
- After all devices are woken up and given device addresses, NFAULT_M pins are changed to "H". Then, set NWAKEUP pin to open.



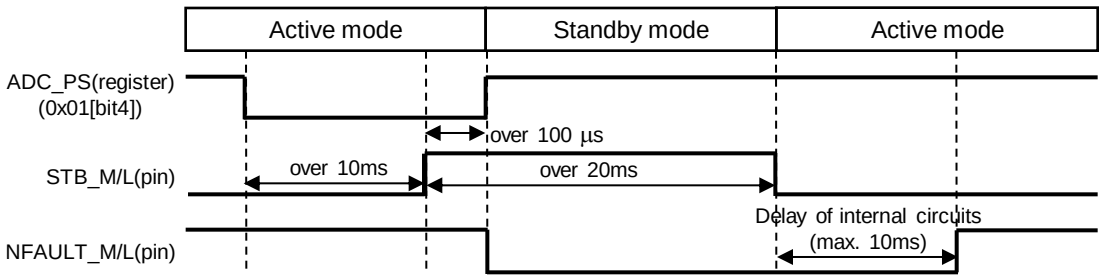

Block Diagram of Wake up Circuit

## OPERATION (continued)

3. Operation Mode

3.2 Standby Mode

- When all the devices are in active mode after LDOs are woken up, the mode is changed to standby mode and NFAULT_M pin is changed to low by following steps. *1
  - i) write "0" to ADC_PS register.
  - ii) after more than 10ms, change STB_M pin to high.
  - iii) after more than 100us , write "1" to ADC_PS register.
- In standby mode, as all circuits except the regulator for VDD50 are halted, this IC operates with low power consumption. Even though microcomputer cannot access registers due to the SPI disable, the condition before halted is retained.
- When STB_M/L pin = "L" for the master device, the slave devices can be returned to Active mode from bottom to top via daisy chain interface (STB_M/L, STB_U).



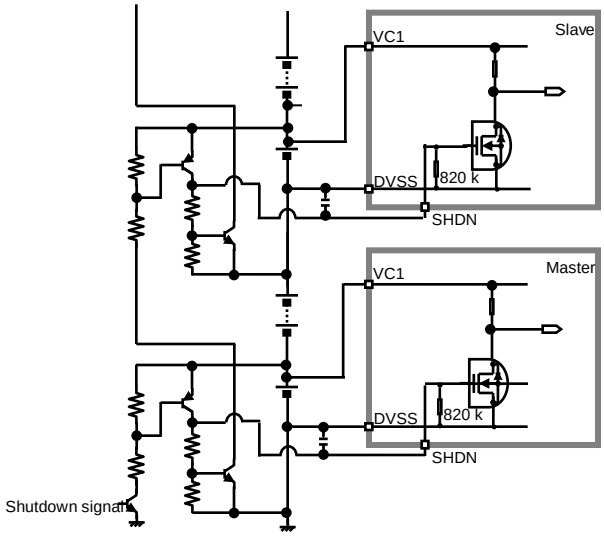

Note: *1 : If the alarm signal, which is generated within 20ms after transition from Standby to Active, can be ignored, there is no need to perform the ADC_PS operation shown above.

## OPERATION (continued)

3. Operation Mode

3.3 Shutdown Mode

- When SHDN pin = "H" (≥ 10 ms) or NSHDN (0x01) = 0, all circuits are shut down forcibly.
- Supply VC1-GND over 1.5 V.
- To shut down all devices connected in the daisy chain configuration by NSHDN setting, set NSHDN of devices from top to bottom.
- Shutdown signal is not included in the daisy chain protocol. (It's because the upper slave device cannot be shut down if the lower slave device has a failure.)

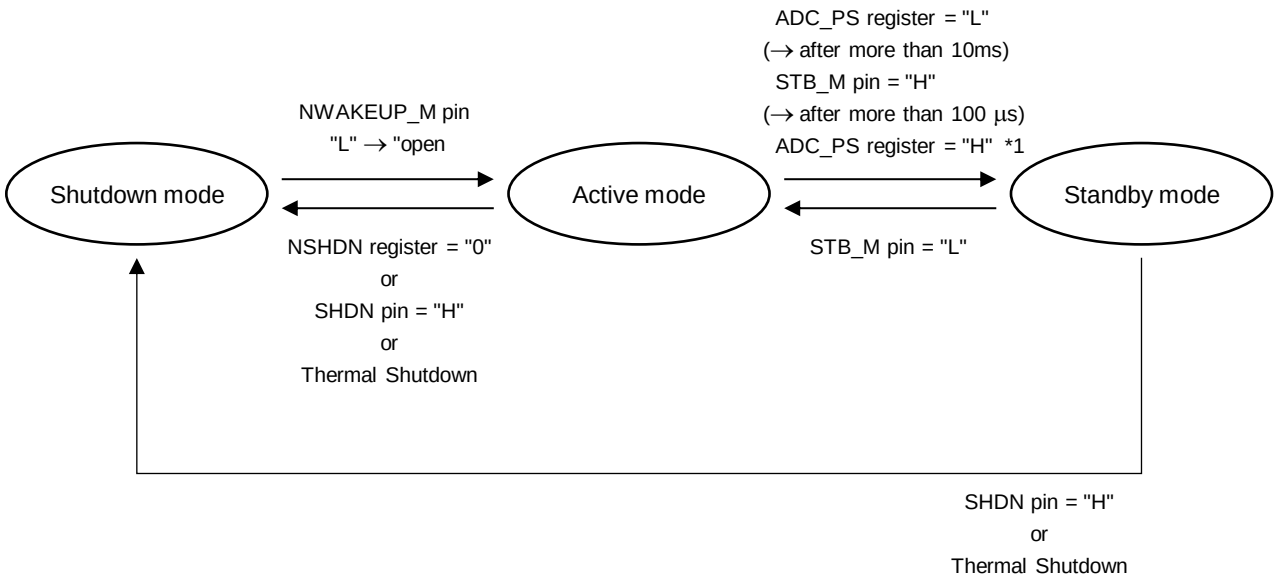


## OPERATION (continued)

3. Operation Mode

3.4 State Transition Diagram of Each Operation Mode

- State transition diagram of active mode, shutdown mode, and standby mode is shown below.



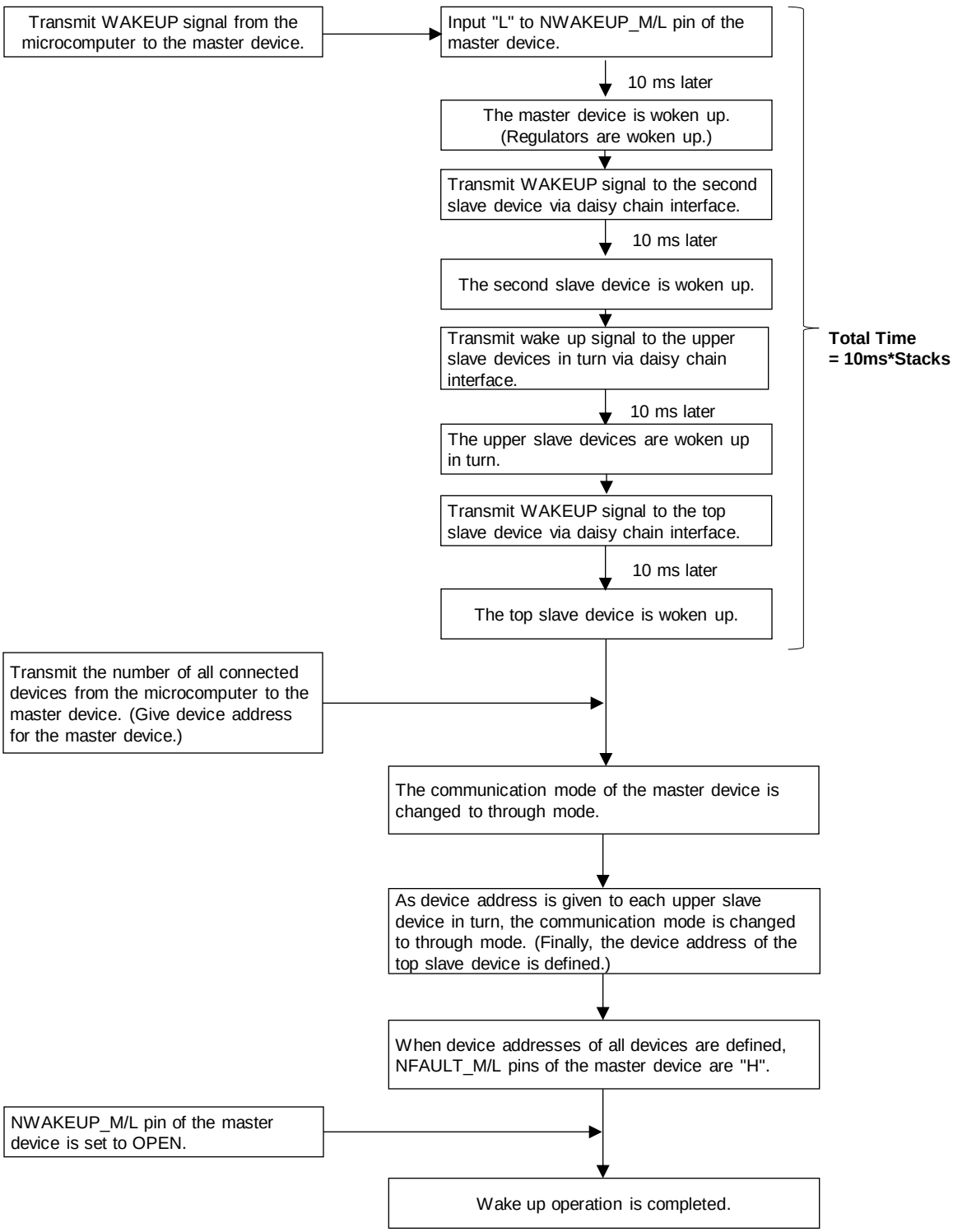

| Mode | $V_{VBAT}$ | VC1 | VDD50 | AVDD40 | SPI |
|---|---|---|---|---|---|
| Active | ≥ 12.5V | ≥ 1.5V | on | on | enable |
| Standby | ≥ 12.5V | ≥ 1.5V | on | off | disable |
| Shutdown | don't care | don't care | off | off | disable |

Note: *1 : If the alarm signal, which is generated within 20ms after transition from Standby to Active, can be ignored, there is no need to perform the ADC_PS operation shown above

## OPERATION (continued)

3. Operation Mode (continued)

3.4 Wake up Sequence (via daisy chain interface)



## OPERATION (continued)

4. Communications

4.1 Microcomputer Interface

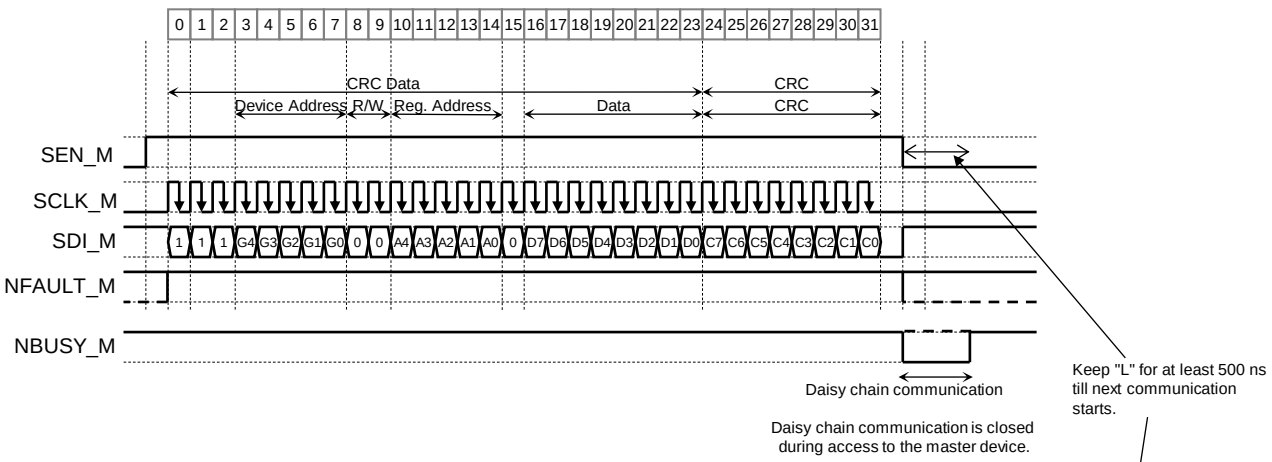
4.1.1 Overview

- The communication between this IC and microcomputer utilizes synchronous communication by 4-line SPI (SDI_M, SDO_M, SCLK_M, and SEN_M).
- NFAULT_M pin is "H" during normal communication, and "L" during abnormal communication (CRC error, preamble, or signal width violation). With interrupt control by NFAULT signal, microcomputer can identify the error cause by reading status register.
- NBUSY signal for communication flow control is output from NBUSY_M pin. The microcomputer can control communication flow by checking NBUSY signal. NBUSY signal is "L" while any device connected in the system is communicating and "H" while any device connected in the system is waiting for communication.
- When there is no communication access for a period of time, this IC enters Shutdown mode by Watchdog Timer (WDT).
  Set value of WDT can be changed by WDT (0x02, [1:0]) register setting.

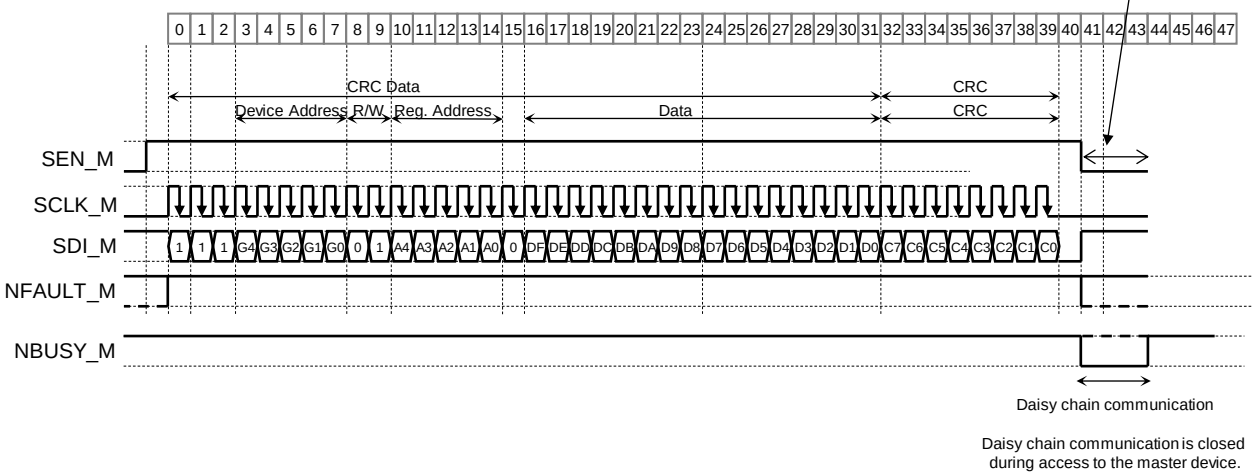
4.1.2 Data Format

(1) Communication between Microcomputer and Master Device

[Data Write (1 Byte)]




[Data write (2 Byte)]



## OPERATION (continued)

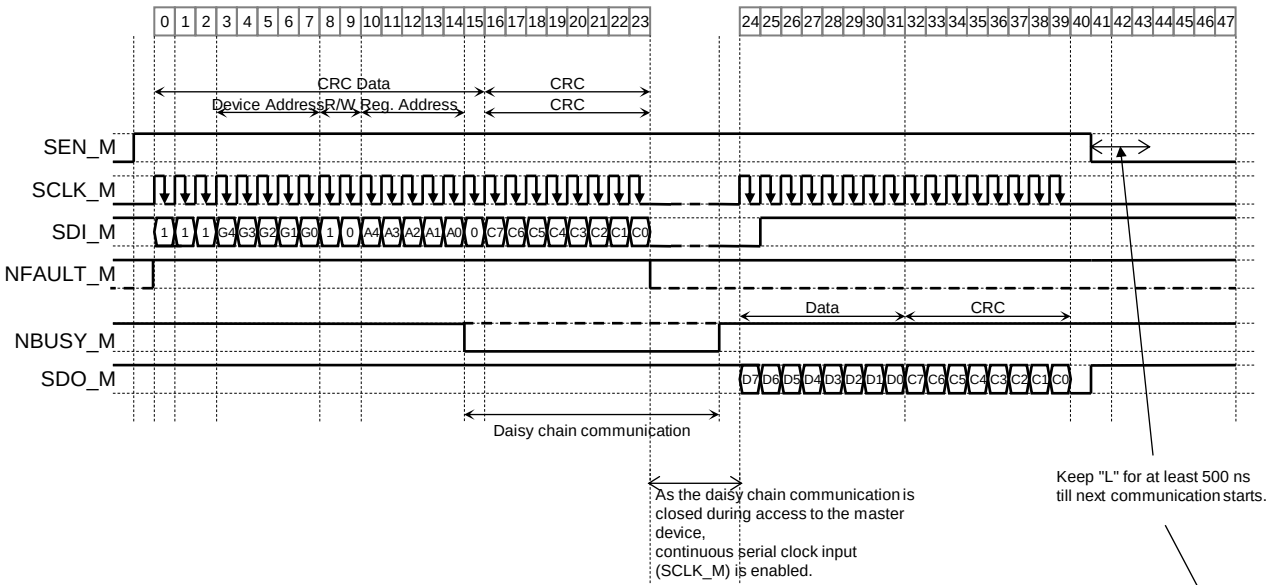
4. Communications (continued)

4.1 Microcomputer Interface (continued)

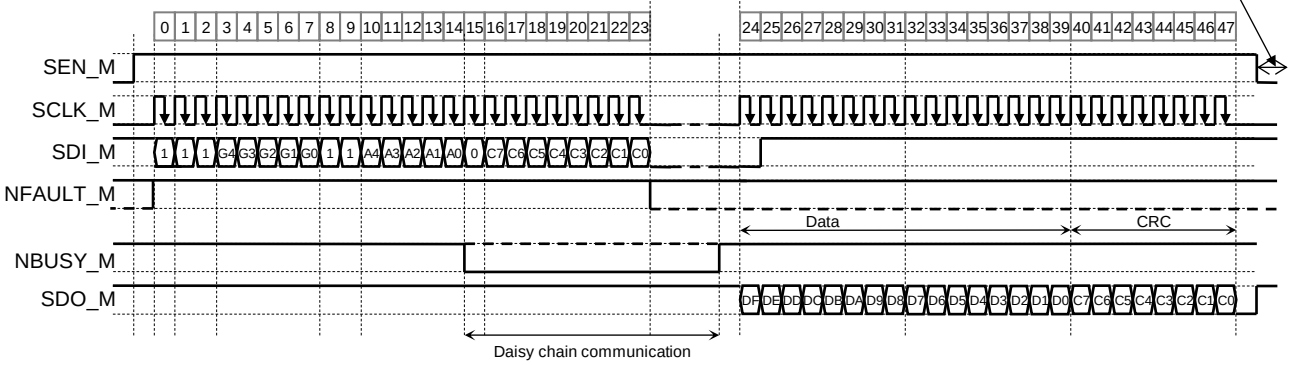
4.1.2 Data Format (continued)

(1) Communication between Microcomputer and Master Device (continued)

[Single Data Read (1 Byte)]




[Single Data Read (2 Byte)]



## OPERATION (continued)

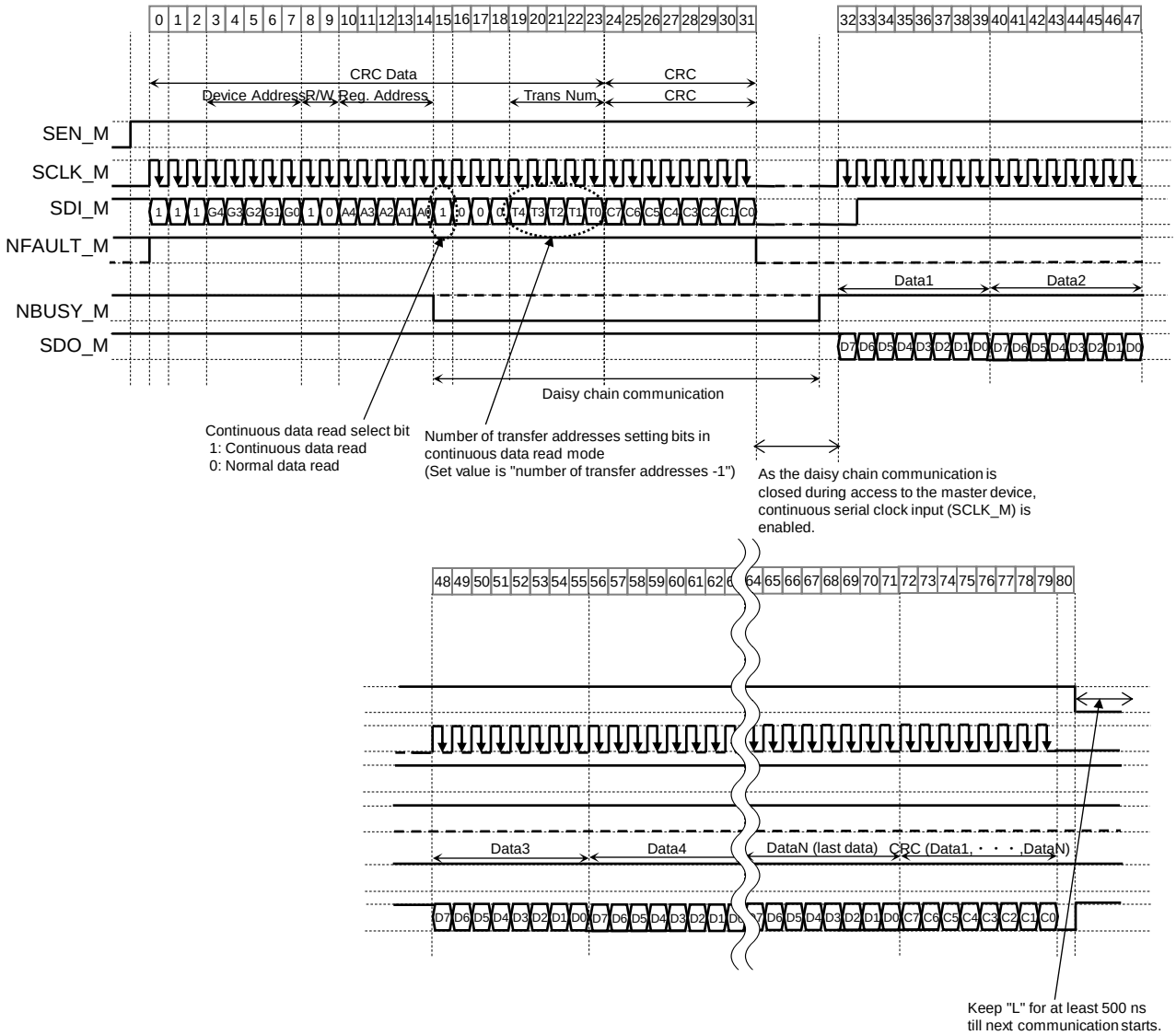
4. Communications (continued)

4.1 Microcomputer Interface (continued)

4.1.2 Data Format (continued)

(1) Communication between Microcomputer and Master Device (continued)

[Continuous Data Read (1 Byte)]



## OPERATION (continued)

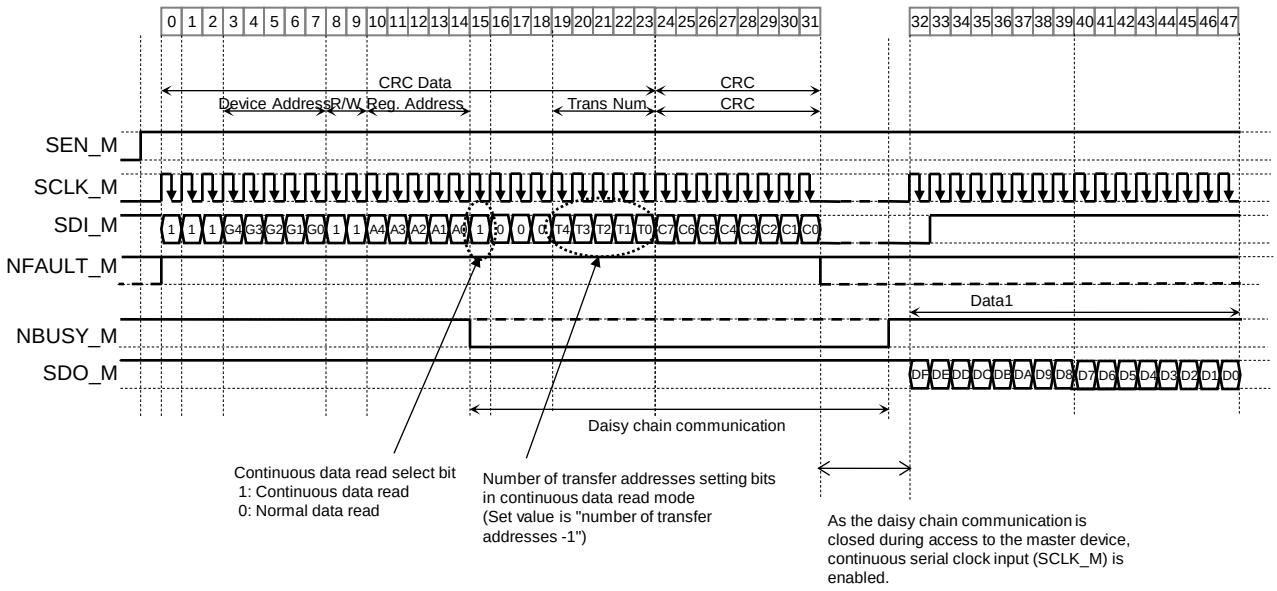
4. Communications (continued)

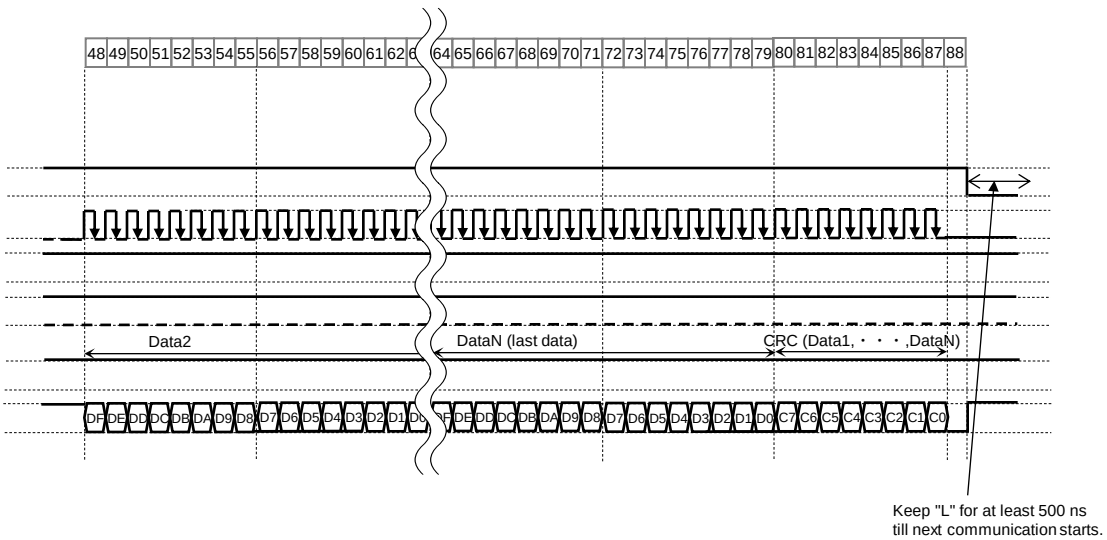
4.1 Microcomputer Interface (continued)

4.1.2 Data Format (continued)

(1) Communication between Microcomputer and Master Device (continued)

[Continuous Data Read (2 Byte)]



## OPERATION (continued)

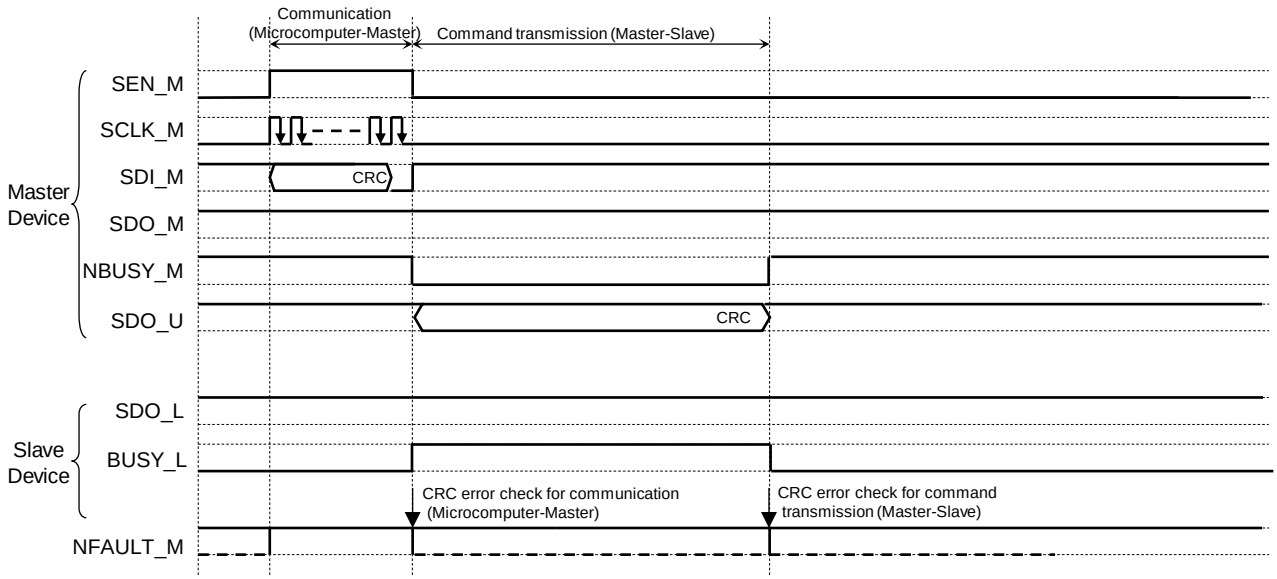
4. Communications (continued)

4.1 Microcomputer Interface (continued)

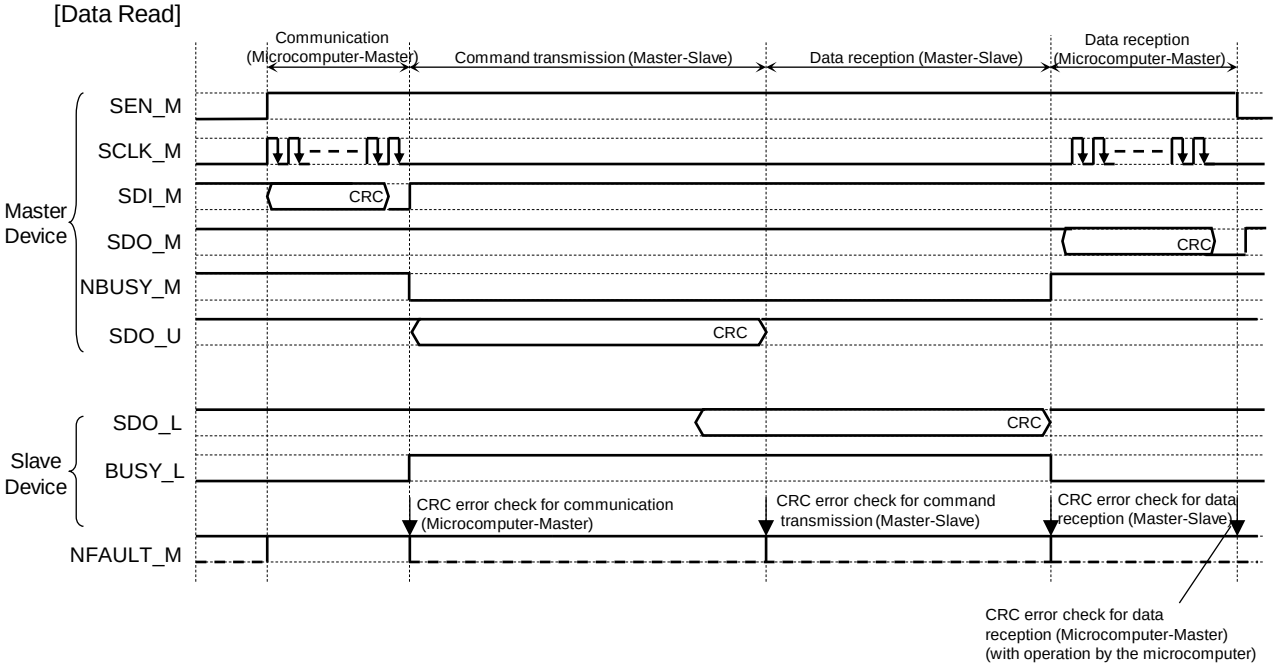
4.1.2 Data Format (continued)

(2) Communication between Microcomputer, Master device, and Slave Device

[Data Write]




[Data Read]



## OPERATION (continued)

4. Communications (continued)

4.2 Daisy Chain Interface

4.2.1 Overview

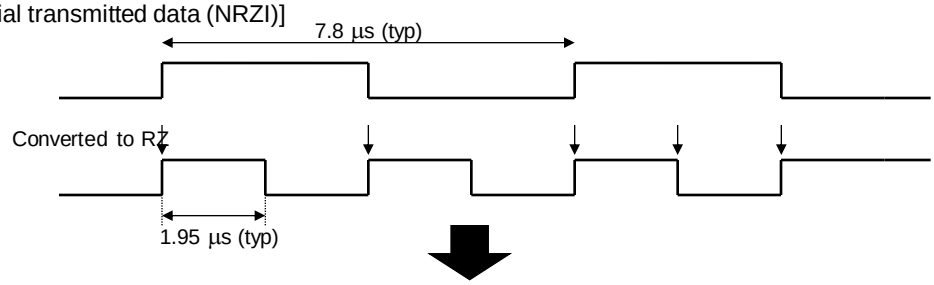
- With daisy chain interface, communication between upper and lower devices with various supply voltages is enabled.

4.2.2 Description for Signals

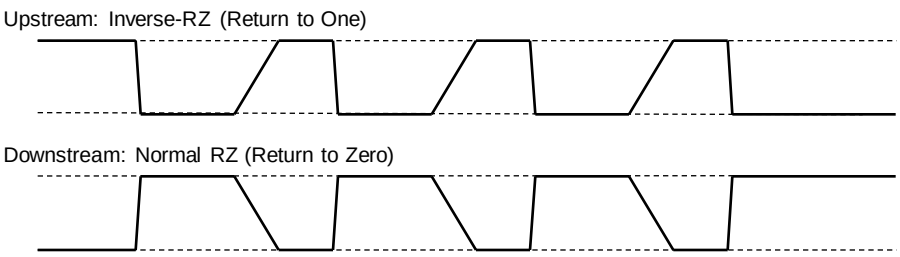
(1) Serial Data Signal: SDI_U, SDI_L, SDO_U, SDO_L

- Upstream serial communication (Destination; pull-up) is done between SDO_U and SDI_L pins.
- Downstream serial communication (Destination; pull-down) is done between SDO_L and SDI_U pins.
- In order to prevent the communication error due to the difference between rise time and fall time, transmit the RZ signal synchronizing the edge of the NRZI signal.
- Serial data signal is transmitted as an inverse-RZ signal (Return to One) for upstream and as a normal RZ signal (Return to Zero) for downstream, and demodulated into the NRZI signal by fetching former edge.
- In order to prevent malfunctions caused by noise, filter out the pulse of 250 ns or less against transmitted RZ pulse of 1.95 μs not to fetch as data. (Filtering width can be changed by DCH (0x04)setting.)

[Serial transmitted data (NRZI)]




[Current output waveform of serial transmitted data]



## OPERATION (continued)

4. Communications (continued)

4.2 Daisy Chain Interface (continued)

4.2.2 Description for Signals (continued)

(2) NFAULT Signal: NFAULT_U, NFAULT_L

- NFAULT signals are "H" during normal communication and "L" during abnormal communication, from the upper device to the lower device.

(3) BUSY Signal: BUSY_U, BUSY_L

- BUSY signal, for communication flow control, is "H" while any device connected in the system is communicating and "L" while waiting for communication from the upper to the lower device.

## OPERATION (continued)

4. Communications (continued)

4.2 Daisy chain I/F (continued)

4.2.3 Data Format

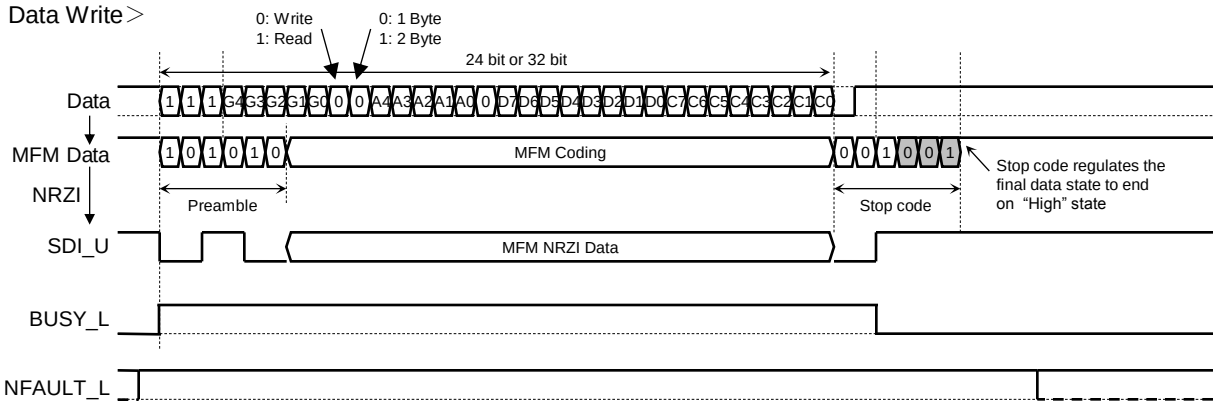
Daisy chain I/F communication is done in MFM (Modified Frequency Modulation) Modulation (1-3 RLL (Run Length Limited) Coding) + NRZI system.

| Data | | MFM Modulation | | | | |
|---|---|---|---|---|---|---|
| 0 | 0 | ? | 0 | 1 | 0 | ? |
| 0 | 1 | ? | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | ? |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 |

| Conversion Example | Data | MFM Modulation | NRZI |
|---|---|---|---|
| 2T (1f) | 11111 | 1010101010 | 1100110011 |
| 3T (1.5f) | 10010 | 100100100? | 111000111? |
| 4T (2f) | 10101 | 1000100010 | 1111000011 |

※In 2T/3T/4T NRZI, the frequency taken from MFM(1-3 RLL) will be halved.

＜ Data Write＞



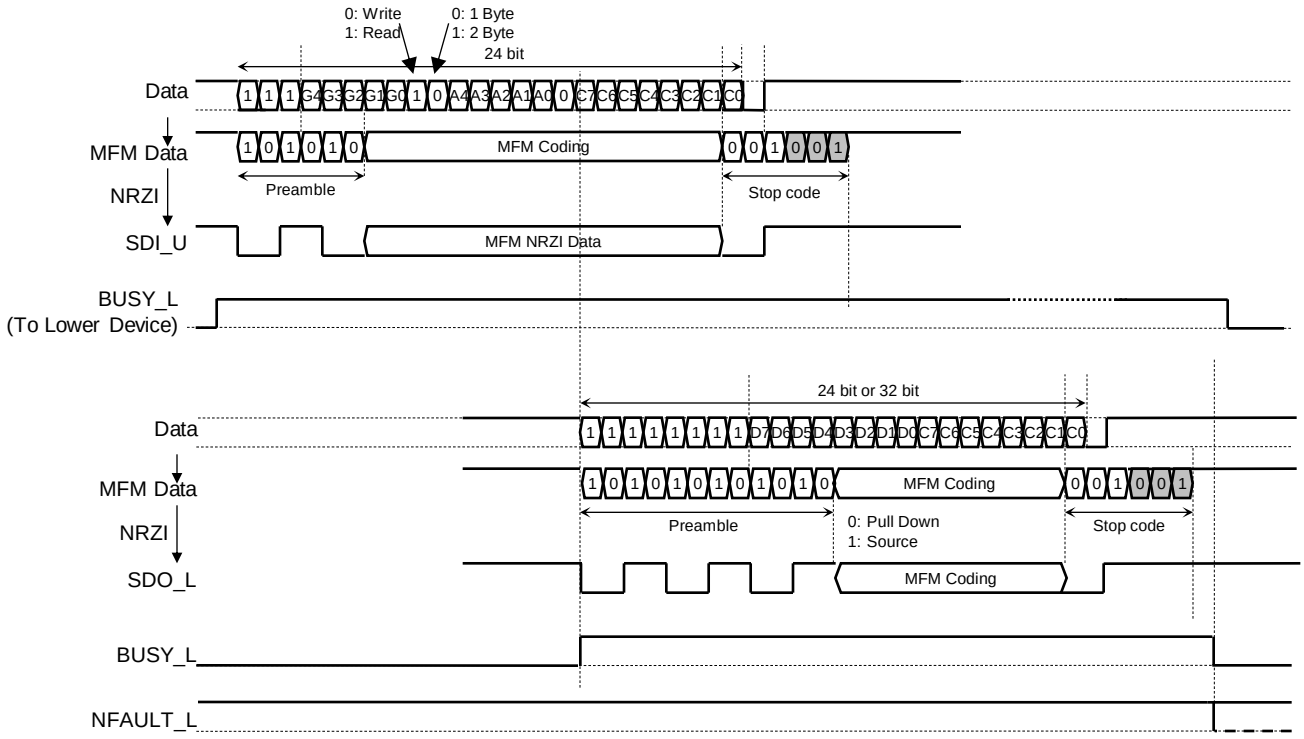
## OPERATION (continued)

4. Communications (continued)

4.2 Daisy chain I/F (continued)

4.2.3 Data Format (continued)

＜ Data Read＞

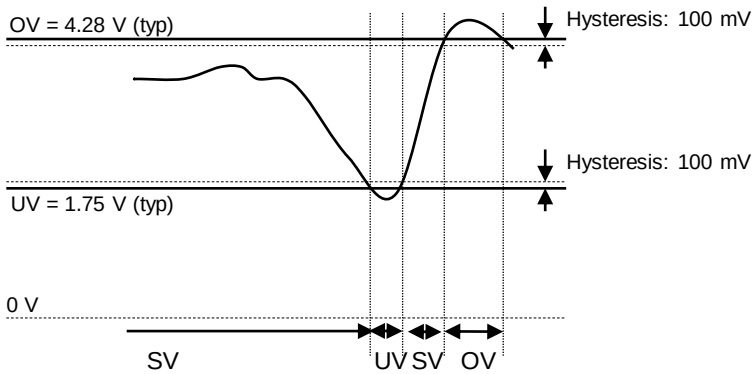


## OPERATION (continued)

4. Communications (continued)

4.3 ALARM signal: ALARM_U, ALARM_M/L

- With built-in two hysteresis comparators to detect Over Voltage (OV) and Under Voltage (UV), the result of the comparison between the cell voltage converted to digital code and the set value of OV/UV is output as ALARM signal.
- There are 2 kinds of ALARM signal, and they can be selected by OVMOD register (Address:0x07).
  [Mode 1] 1kHz(typ) pulse wave output (default)
  [Mode 2] level output
- With Mode 1, ALARM signal is frequency signal of 1 kHz (typ), indicates 3 states defined by variable duty as shown below.
- With Mode 2, ALARM signal is high in OV, and low in Standard Voltage (SV) /UV.
- The comparison result is stored to the register every 1 ms (typ), and status register flag (Address:0x11) is set when ALARM signal is generated. The flag is cleared by writing 1.



## OPERATION (continued)

4. Communications (continued)

4.3 ALARM signal: ALARM_U, ALARM_M/L (continued)

OV setting

| OVSEL2 | OVSEL1 | OVSEL0 | Over Voltage [V] |
|---|---|---|---|
| 0 | 1 | 1 | 4.43 |
| 0 | 1 | 0 | 4.38 |
| 0 | 0 | 1 | 4.33 |
| 0 | 0 | 0 | 4.28 |
| 1 | 1 | 1 | 4.23 |
| 1 | 1 | 0 | 4.18 |
| 1 | 0 | 1 | 4.13 |
| 1 | 0 | 0 | 4.08 |

UV setting

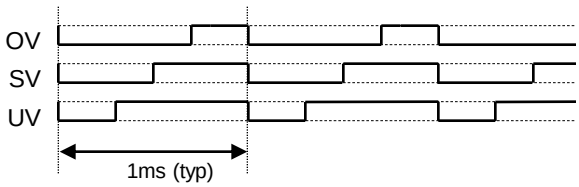
| UVSEL1 | UVSEL0 | Under Voltage [V] |
|---|---|---|
| 1 | 1 | 1.90 |
| 1 | 0 | 1.85 |
| 0 | 1 | 1.80 |
| 0 | 0 | 1.75 |

Relation between condition and ALARM signal (Mode1)

| Condition | ALARM | ALARAM output signal |
|---|---|---|
| Over Voltage | OV | 25% Duty 1kHz Waveform |
| Standard Voltage | SV | 50% Duty 1kHz Waveform |
| Under Voltage | UV | 75% Duty 1kHz Waveform |

Relation between condition and ALARM signal (Mode 2)

| Condition | ALARM | ALARAM output signal |
|---|---|---|
| Over Voltage | OV | High |
| Standard Voltage | SV | Low |
| Under Voltage | UV | Low |




Notes: Don't use ALARM signal for control anything when the device address is not written because the ALARM signal reflect only the measurement data of master device.

## OPERATION (continued)

4. Communications (continued)

4.4 Schematic Diagram

- Diagram 1 and 2 show schematic diagrams when a single device used and when multiple devices used with daisy chain.

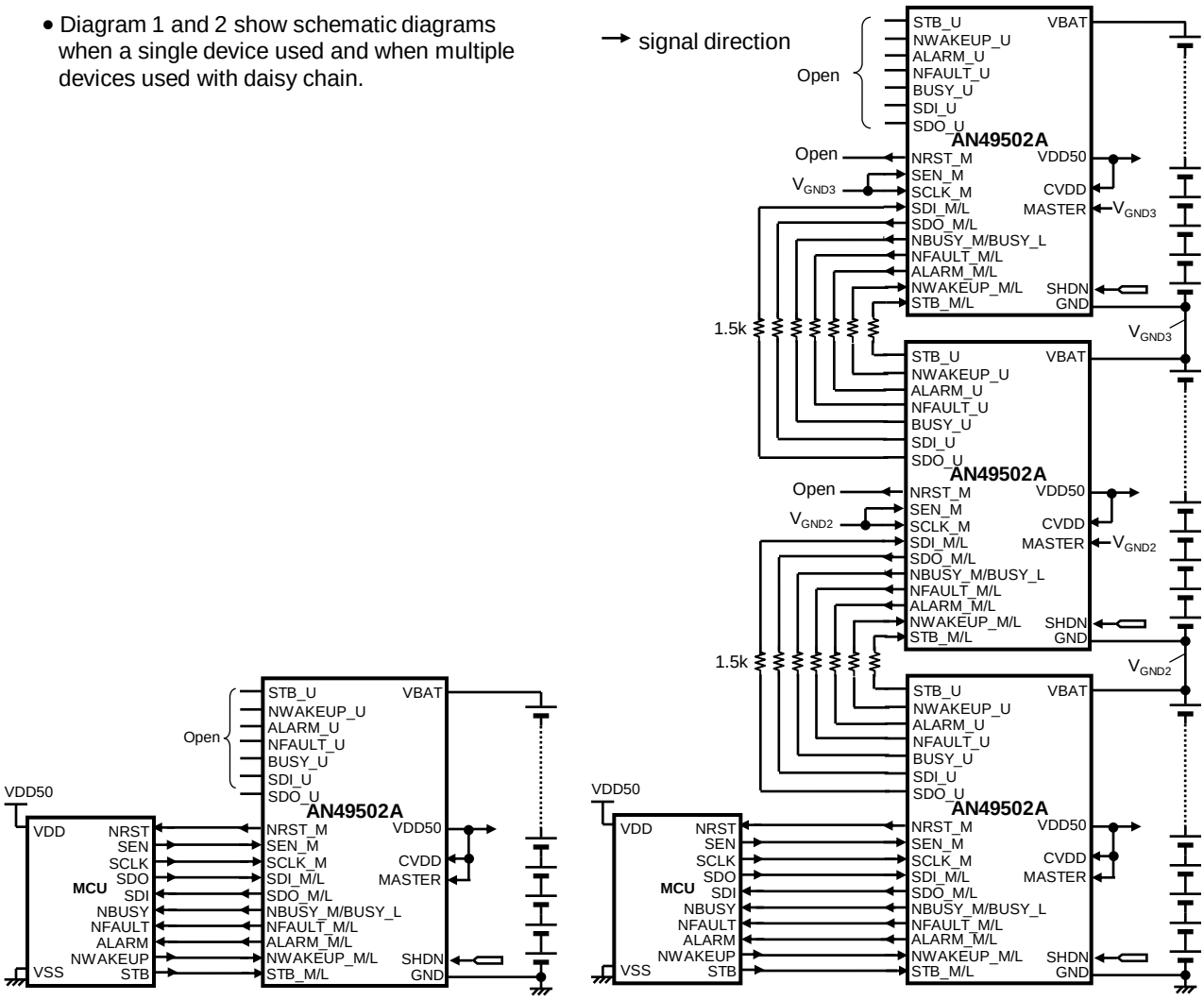



Diagram 1: Single device used

Diagram 2: Multiple device with daisy chain interface used

Notes: *This application circuit is an example. Operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.

- * Use external resistors with accuracy of ±1%.
- * If the daisy chain communication is used, the voltage between $V_{GND\_N+1}$ and $V_{VBAT\_N}$ should be within +/- 1V. ($V_{GND\_N+1}$ : GND voltage of #(N+1) device, $V_{VBAT\_N}$ : VBAT voltage of #N device)

5. Mode Setting

5.1 Master/Slave select

- Master or slave are selectable in a daisy chain communication by MASTER pin setting.

| MASTER pin | "H" | "L" |
|---|---|---|
| Operation mode | Master | Slave |

## OPERATION (continued)

6. Descriptions of Registers

6.1 Register Map

This IC has 8- and 16-bit registers described below.
Refer to the following table for the register map and the following pages for the detailed descriptions.

Notes: * Writing to forbidden registers (for Test) might have effect on IC operation.
* Writing to reserved registers have no effect on IC operation.

Register Map

| Address | Register Name | Bit Length | Description |
|---|---|---|---|
| 0x00 | Address register | 8 | Device address |
| 0x01 | Control register | 16 | Shutdown / Soft reset |
| 0x02 | | 8 | ADC/WDT |
| 0x03 | | 16 | Test |
| 0x04 | | 16 | Detecting disconnection / daisy chain interface |
| 0x05 | | 16 | Test |
| 0x06 | | 16 | |
| 0x07 | | 16 | OV and UV setting / cell balancing |
| 0x08 | | 16 | Select cells for voltage measurement |
| 0x09 | Test register | 16 | — |
| 0x0A | | 16 | |
| 0x0B | | 16 | |
| 0x0C | | 16 | |
| 0x0D | | 16 | |
| 0x0E | | 16 | |
| 0x0F | | 16 | |
| 0x10 | Status register | 16 | Status 1 |
| 0x11 | | 16 | Status 2 |
| 0x12 | Data register | 16 | Measured data of cell 1 |
| 0x13 | | 16 | Measured data of cell 2 |
| 0x14 | | 16 | Measured data of cell 3 |
| 0x15 | | 16 | Measured data of cell 4 |
| 0x16 | | 16 | Measured data of cell 5 |
| 0x17 | | 16 | Measured data of cell 6 |
| 0x18 | | 16 | Measured data of cell 7 |
| 0x19 | | 16 | Measured data of cell 8 |
| 0x1A | | 16 | Measured data of cell 9 |
| 0x1B | | 16 | Measured data of cell 10 |
| 0x1C | | 16 | Measured data of thermistor voltage 1 |
| 0x1D | | 16 | Measured data of thermistor voltage 2 |
| 0x1E | Test register | 16 | — |
| 0x1F | Data stack register | 16 | Data stack |

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions

Address: 0x00 (Device Address Register)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | — | — | — | — | G[3:0] | | | |
| Initial | — | — | — | — | — | — | — | — | — | — | — | — | 0 | 0 | 0 | 0 |
| R/W | — | — | — | — | — | — | — | — | — | — | — | — | R/W | R/W | R/W | R/W |

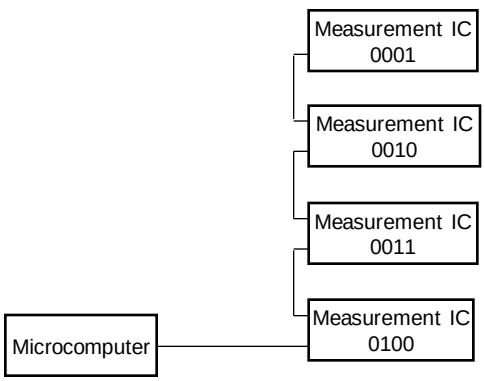
—: Forbidden

[Define device address]

1) Device Address Register is initialized after waking up or reset, and the communication mode is changed to sequential transmission mode, at which mode the master waiting for device address setting. After the waking up, when the microcomputer sets the number of all devices to G[3:0] of the master device, the communication mode of the master device is changed to through mode, which is normal working mode.
2) When the master device sets the value, which is decremented by 1 from G[3:0] of the master device, to G[3:0] of the upper slave device, the communication mode of the upper slave device is changed to through mode.
3) When the slave device sets the value, which is decremented by 1 from G[3:0] of the master device, to G[3:0] of the upper slave device, the communication mode of the upper slave device is changed to through mode in turn.
4) 3) is repeated until G[3:0] of connected slave devices becomes 0001.
5) The slave device (G[3:0] = 0001) is defined as the top device, and access to the upper devices is disabled. Finally, device addresses of all devices are defined and the communication mode of all devices is changed to through mode.

* Set the number of devices connected with daisy chain to the device address of the master device.
* The device address of 0000 is used for a broadcast address which all devices respond to.
* When the microcomputer specifies an illegal device address to read, invalid data are read. When the microcomputer specifies an illegal device address to write, the instruction is ignored.
* The device address can be set only once while Shutdown/Reset is released.

| Bit | Name | Description |
|---|---|---|
| [15:4] | — | Test (Forbidden) |
| [3:0] | G[3:0] | 4-bit register for device address<br>0000 : Forbidden (broadcast address) (default)<br>0001 : Single-stage connection<br>to<br>1000 : 8-stage connection |




Example of given device address (4-stage connection)

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x01 (Control Register 1: Power Control)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | NSHDN | NPD_RST | — | ADC_PS | — | — | — | — |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

* When NPD_RST = 0, all registers except NSHDN are initialized by soft reset. NPD_RST is also returned to 1 automatically after reset is completed. When NSHDN = 0, all circuits are shut down and need to be woken up. Whereas when NPD_RST = 0, registers except shutdown mode setting registers are initialized and each supply voltage or system clock is not halted.
Besides, as Device Address Register is also initialized when NPD_RST = 0, device address should be given before the communication starts.

| Bit | Name | Description |
|---|---|---|
| [15:8] | — | Test |
| 7 | NSHDN | Shutdown control<br>1 : Active (default)<br>0 : Shut down all circuits |
| 6 | NPD_RST | Soft reset control<br>1 : Active (default)<br>0 : Reset logic block (This bit is returned to 1 after reset is completed.) |
| 5 | — | Test |
| 4 | ADC_PS | ADC power down control<br>1 : Active (default)<br>0 : ADC power down |
| [3:0] | — | Test |

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x02 (Control Register 2: ADC and WDT)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | ADC_CONV | — | — | — | — | EN_WDT | WDT[1:0] | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:8] | — | Test |
| 7 | ADC_CONV | Storing measured data<br>1 : The A/D conversion value is stored to the register. (This bit is cleared after stored.)<br>0 : The A/D conversion value is retained. |
| [6:3] | — | Test |
| 2 | EN_WDT | Watch Dog Timer (WDT) control<br>1 : WDT ON<br>0 : WDT OFF |
| [1:0] | WDT[1:0] | Watch Dog Timer (WDT) setting (typ)<br>11 : 44 min<br>10 : 22 min (default)<br>01 : 11 min<br>00 : 2 sec |

Address: 0x03 (Test Register)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x04 (Control Register 3: Daisy Chain Interface)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | EN_VCPD[1:0] | | — | — | — | — | — | — | — | DCH6 | DCH5 | DCH4 | — | — | DCH1 | DCH0 |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | EN_VCPD | Pull-up resistor control for detecting disconnection<br>11 : Test mode *1<br>10 : OFF<br>01 : Normal mode *1<br>00 : OFF |
| [13:7] | — | Test |
| 6 | DCH6 | Fix NFAULT_L pin of daisy chain interface to "L". (for detecting ground-fault/disconnection)<br>1 : "L" fixed<br>0 : Don't Care |
| [5:4] | DCH[5:4] | Noise filter width of daisy chain interface select<br>11 : 400 ns<br>10 : 350 ns<br>01 : 300 ns<br>00 : 250 ns (default) |
| [3:2] | — | Test (Forbidden) |
| 1 | DCH1 | Baud rate of daisy chain interface select<br>11 : 400 kbps<br>10 : 1 Mbps<br>01 : 800 kbps<br>00 : 500 kbps (default) |
| 0 | DCH0 | |

*1: Detecting disconnection is supported for only VC0 to VC9 pins. It takes about 90 s to set OV/UV flag after detecting disconnection in Active mode.

Address: 0x05 (Test Register)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

Address: 0x06 (Test Register)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x07 (Control register 4: OV and UV Setting/Cell Balancing)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | OVSEL[2:0] | | | OVMOD | UVSEL[1:0] | | CBSEL[10:1] | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:13] | OVSEL[2:0] | Over Voltage setting (two's complement)<br>011 : 4.43 V<br>010 : 4.38 V<br>001 : 4.33 V<br>000 : 4.28 V (default)<br>111 : 4.23 V<br>110 : 4.18 V<br>101 : 4.13 V<br>100 : 4.08 V |
| 12 | OVMOD | ALARM_M output setting<br>1 : [Mode 2] level output<br>0 : [Mode 1] 1kHz(typ) pulse wave output (default) |
| [11:10] | UVSEL[1:0] | Under Voltage setting (two's complement)<br>11 : 1.90 V<br>10 : 1.85 V<br>01 : 1.80 V<br>00 : 1.75 V (default) |
| 9 | CBSEL10 | Control of Cell Balance for Cell 10 (between VC10 and VC9)<br>1 : Cell Balance ON<br>0 : Cell Balance OFF (default) |
| to | to | to |
| 0 | CBSEL1 | Control of Cell Balance for Cell 1 (between VC1 and VC0)<br>1 : Cell Balance ON<br>0 : Cell Balance OFF (default) |

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x08 (Control Register 6: Select Cell for Voltage Measurement)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | TSEL1 | TSEL0 | CVSEL 10 | CVSEL 9 | CVSEL 8 | CVSEL 7 | CVSEL 6 | CVSEL 5 | CVSEL 4 | CVSEL 3 | CVSEL 2 | CVSEL 1 |
| Initial | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:12] | — | Test (Forbidden) |
| 11 | TSEL1 | TH2 select<br>1 : MUX select signal enable<br>0 : MUX select signal disable (default) |
| 10 | TSEL0 | TH1 select<br>1 : MUX select signal enable<br>0 : MUX select signal disable (default) |
| 9 | CVSEL10 | Cell 10 select (between VC10-VC9 pins)<br>1 : MUX select signal enable (default)<br>0 : MUX select signal disable |
| to | to | to |
| 0 | CVSEL1 | Cell 1 select (between VC1-VC0 pins)<br>1 : MUX select signal enable (default)<br>0 : MUX select signal disable |

Address: 0x09 (Test Register)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R | R | R | R |

—: Forbidden

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x0A - 0x0B (Test Register)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

Address: 0x0C - 0x0F (Test Register)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x10 (Status Register)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MUX_FAIL[3:0] | | | | MASTER | — | — | — | — | PREAMBLE | PERIOD | DCL_CRC | TESTON | — | — | — |
| Initial | 0 | 0 | 0 | 0 | × | × | × | × | 0 | 0 | 0 | 0 | × | × | 1 | 0 |
| R/W | R/W | R/W | R/W | R/W | R | R | R | R | R/W | R/W | R/W | R/W | R | R | R | R/W |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:12] | MUX_FAIL_[3:0] | MUX control flag * If any of bits is 1, A/D conversion value may be abnormal.<br>1 : Error (This bit is cleared by writing 1.)<br>0 : Normal |
| 11 | MASTER | Status of MASTER pin<br>1 : MASTER pin = "H"<br>0 : MASTER pin = "L" |
| [10:7] | — | Test |
| 6 | PREAMBLE | Error detection for communication format of daisy chain interface (Preamble)<br>1 : Error (This bit is cleared by writing 1.)<br>0 : Normal |
| 5 | PERIOD | Error detection for communication format of daisy chain interface (Signal width violation of data block)<br>1 : Error (This bit is cleared by writing 1.)<br>0 : Normal |
| 4 | DC_CRC | Error detection for communication format of daisy chain interface (CRC)<br>1 : Error (This bit is cleared by writing 1.)<br>0 : Normal |
| 3 | TESTON | Status of TEST pin *1<br>1 : TEST pin = "H" (ASIC test mode)<br>0 : TEST pin = "L" (normal) |
| [2:0] | — | Test |

Note: *1: When TEST pin = "H", this IC enters ASIC test mode. If forbidden registers are written in ASIC mode, an unexpected operation may occur.
To prevent it, TEST pin must be "L" fixed.

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x11 (Status Register)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | OV | UV | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| 15 | OV | Over Voltage flag<br>1 : Error (This bit is cleared by writing 1)<br>0 : Normal |
| 14 | UV | Under Voltage flag<br>1 : Error (This bit is cleared by writing 1)<br>0 : Normal |
| [13:0] | — | Test |

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x12 (Data Register: Measured Data of Cell 1)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | CEL01_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test |
| [13:0] | CEL01_[13:0] | Measured data of Cell 1 (VC1-VC0) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

Address: 0x13 (Data Register: Measured Data of Cell 2)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | CEL02_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test |
| [13:0] | CEL02_[13:0] | Measured data of Cell 2 (VC2-VC1) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

Address: 0x14 (Data Register: Measured Data of Cell 3)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | CEL03_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test |
| [13:0] | CEL03_[13:0] | Measured data of Cell 3 (VC3-VC2) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x15 (Data Register: Measured Data of Cell 4)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | CEL04_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test |
| [13:0] | CEL04_[13:0] | Measured data of Cell 4 (VC4-VC3) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

Address: 0x16 (Data Register: Measured Data of Cell 5)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | CEL05_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test |
| [13:0] | CEL05_[13:0] | Measured data of Cell 5 (VC5-VC4) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

Address: 0x17 (Data Register: Measured Data of Cell 6)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | CEL06_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test |
| [13:0] | CEL06_[13:0] | Measured data of Cell 6 (VC6-VC5) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x18 (Data Register: Measured Data of Cell 7)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | CEL07_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test |
| [13:0] | CEL07_[13:0] | Measured data of Cell 7 (VC7-VC6) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

Address: 0x19 (Data Register: Measured Data of Cell 8)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | CEL08_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test |
| [13:0] | CEL08_[13:0] | Measured data of Cell 8 (VC8-VC7) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

Address: 0x1A (Data Register: Measured Data of Cell 9)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | CEL09_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test |
| [13:0] | CEL09_[13:0] | Measured data of Cell 9 (VC9-VC8) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x1B (Data Register: Measured Data of Cell 10)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | CEL10_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test |
| [13:0] | CEL10_[13:0] | Measured data of Cell 10 (VC10-VC9) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

Address: 0x1C (Data Register: Measured Data of Thermistor Voltage 1)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | TH1_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test (Forbidden) |
| [13:0] | TH1_[13:0] | Measured data of thermistor voltage (TH1 pin) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

Address: 0x1D (Data Register: Measured Data of Thermistor Voltage 2)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | TH2_[13:0] | | | | | | | | | | | | | |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

| Bit | Name | Description |
|---|---|---|
| [15:14] | — | Test (Forbidden) |
| [13:0] | TH2_[13:0] | Measured data of thermistor voltage (TH2 pin) (The A/D conversion value is stored to this register when ADC_CONV = 1.) |

## OPERATION (continued)

6. Descriptions of Registers (continued)

6.2 Detailed Descriptions (continued)

Address: 0x1E (Test Register)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

Address: 0x1F (Test Register)

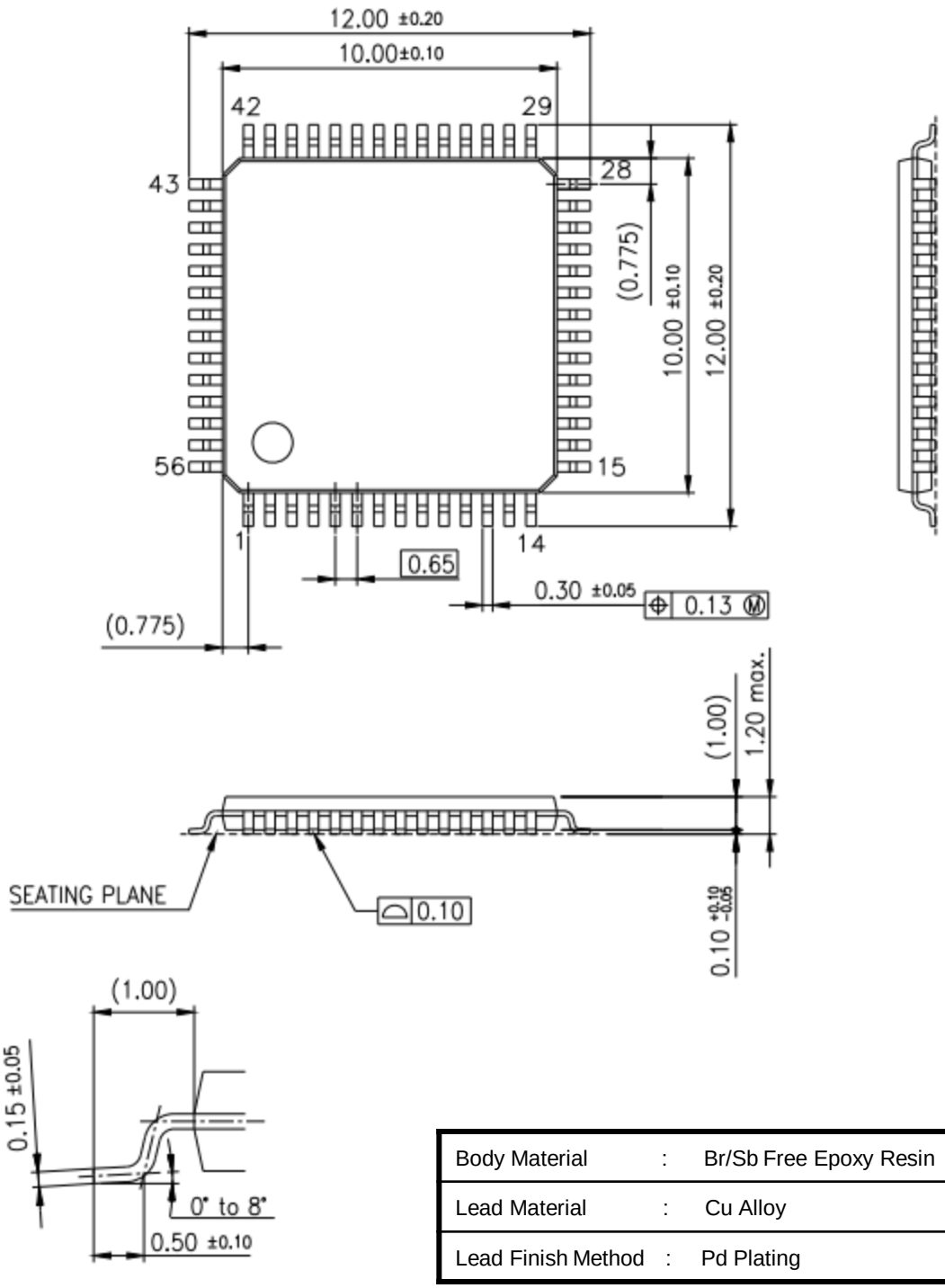
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

—: Forbidden

## PACKAGE INFORMATION (Reference Data)

**Package Code : TQFP056-P-1010**

unit : mm



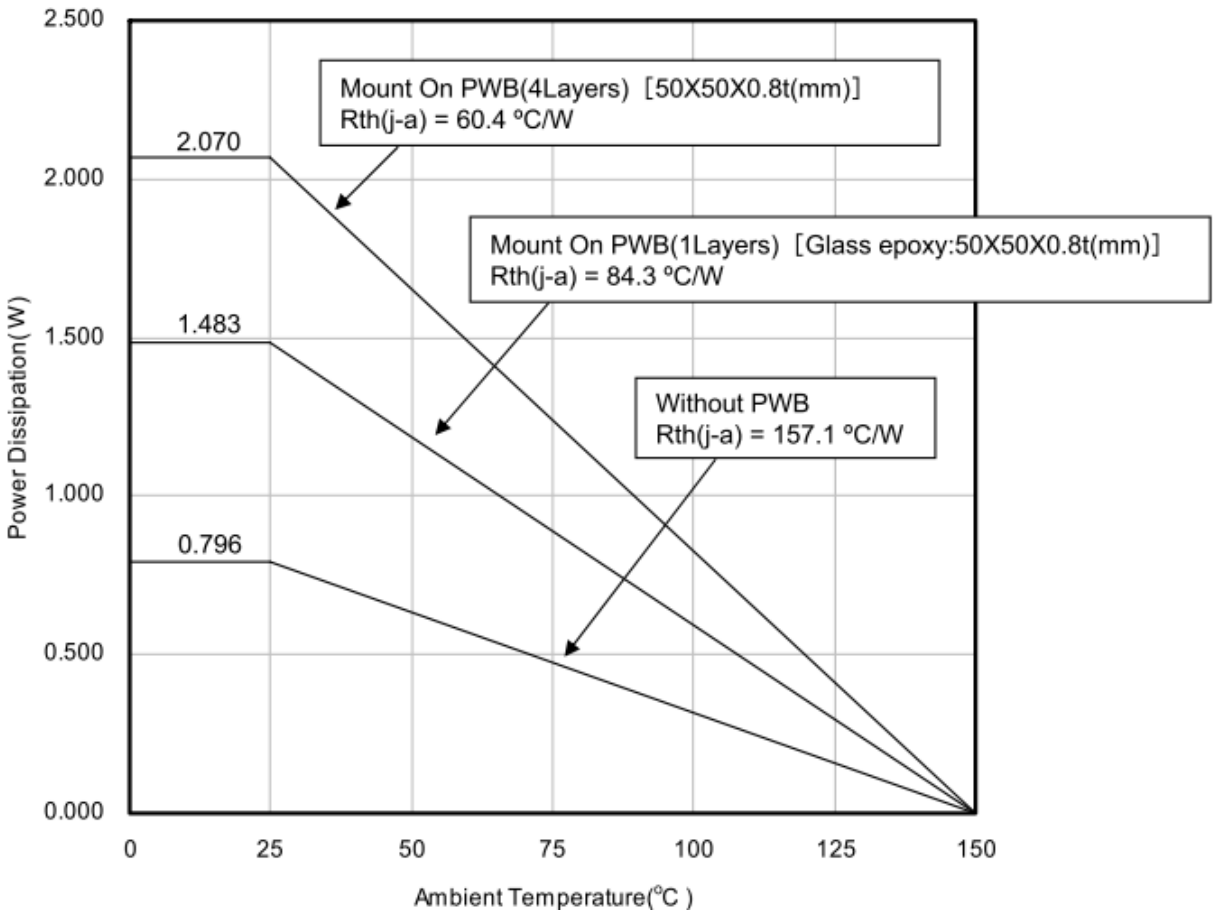

| | | |
|---|---|---|
| Body Material | : | Br/Sb Free Epoxy Resin |
| Lead Material | : | Cu Alloy |
| Lead Finish Method | : | Pd Plating |

## PACKAGE INFORMATION ( Reference Data ) (continued)

### Power dissipation (Supplementary explanation)

Note : The characteristics indicated below are reference values derived from the design of the LSI and are not guaranteed.

**Package Code : TQFP056-P-1010**



## PACKAGE INFORMATION ( Reference Data ) (continued)

### Power dissipation (Supplementary explanation)

**[Experiment environment]**

Power Dissipation (Technical Report) is a result in the experiment environment of SEMI standard conformity. (Ambient air temperature (Ta) is 25 degrees C)

**[Supplementary information of PWB to be used for measurement]**

The supplement of PWB information for Power Dissipation data (Technical Report) are shown below.

| Indication | Total Layer | Resin Material |
|---|---|---|
| Glass-Epoxy | 1-layer | FR-4 |
| 4-layer | 4-layer | FR-4 |

**[Notes about Power Dissipation (Thermal Resistance) ]**

Power Dissipation values (Thermal Resistance) depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value (Technical Report) is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

**[Definition of each temperature and thermal resistance]**

Ta : Ambient air temperature
The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc : It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj : Semiconductor element surface temperature (Junction temperature)

Rth(j-c) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a) : The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

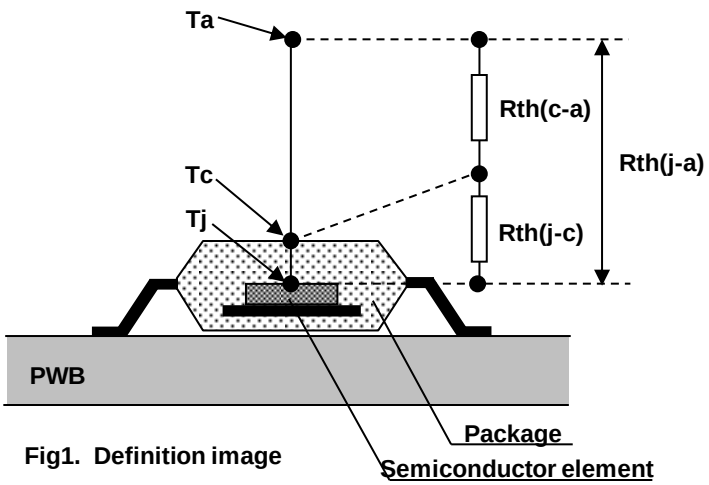



Fig1. Definition image

**[Definition formula]**

$$Tj = \{ Rth(j\text{-}c) + Rth(c\text{-}a) \} \times P + Ta$$

$$= Rth(j\text{-}a) \times P + Ta$$

$$Rth(j\text{-}c) = \frac{Tj - Tc}{P} \quad (°C/W)$$

$$Rth(c\text{-}a) = \frac{Tc - Ta}{P} \quad (°C/W)$$

$$Rth(j\text{-}a) = \frac{Tj - Ta}{P} \quad (°C/W)$$

$$= Rth(j\text{-}c) + Rth(c\text{-}a)$$

P : power (W)

## IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Product which has specified ASO (Area of Safe Operation) should be operated in ASO.
13. Verify the risks which might be caused by the malfunctions of external components.