Interim

AN49503A Application Note

AN49503A Application Note – Ver_0.20(E)

Panasonic Semiconductor Solutions Co., Ltd.

Panasonic

AN49503A Application Note

Contents

Chapter 1 Overview

1.1 Description

This is the application note for using AN49503A, which is a battery monitoring IC with protection function. All the materials in this application are provided for references. The mass production is not guaranteed, sufficient evaluation and verification is required.

Chapter 2 How to choose input RC and charge pump capacitor

2.1 For external Cell Balancing

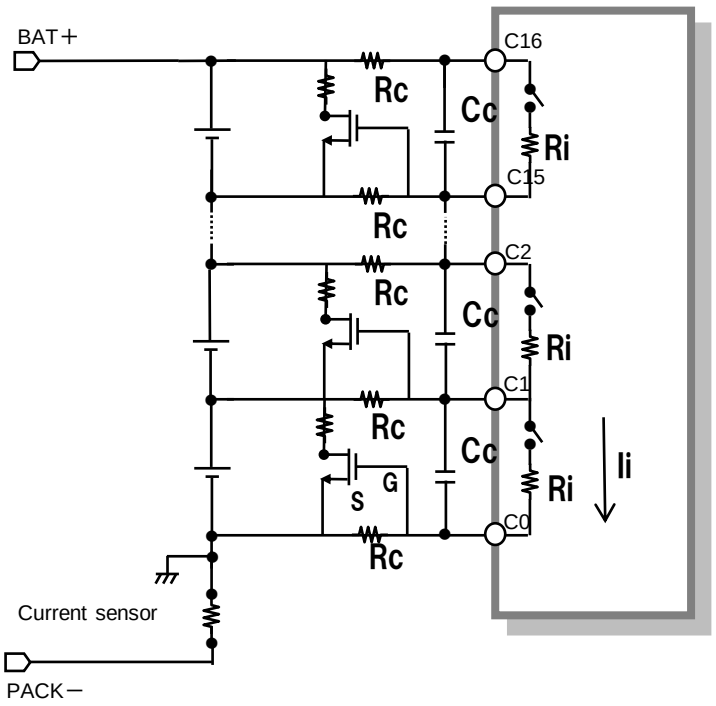


Fig.2.1.1 Parameter for external cell balance

1) *Calculate Rc*

$$Vgs = \frac{Vcell * Rc}{2Rc + Ri} \qquad Ri = 20ohm$$

$$Vgs \geq Vth(in\ order\ to\ turn\ on\ FET)$$

$$Suppose\ Vth = 1.5V\ \ \text{Vcell} = 3.7\text{V}$$

$$Rc \geq Ri * \frac{Vth}{Vcell - 2Vth} = 43ohm$$

$$and\ Rc < 5kohm\ (for\ input\ impedance\ limitation)$$

$$we\ recommend\ using\ Rc = 1kohm{\sim}4kohm$$

2) *Calculate Cc*

$$fc = \frac{1}{2\pi * 2Rc * Cc} \leq \frac{fs}{2}$$

$$fc\ depends\ on\ the\ sampling\ time\ of\ our\ system$$

$$\left(MAX(fc) = \left(\frac{fs}{2}\right) = \frac{1}{50us * 2} = 10KHz\right)$$

$$eg.when\ fs = 20KHz, Rc = 1kohm$$

$$Cc \geq \frac{1}{fs * \pi * 2Rc} = 0.008\text{uF}$$

$$we\ recommend\ using\ 10 * Cc$$

2.2 For internal Cell Balancing

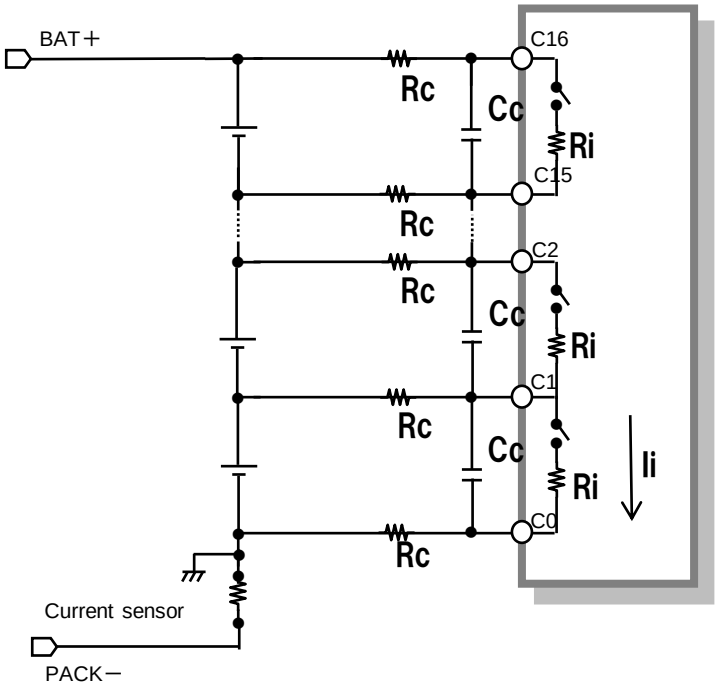


Fig.2.2.1 Parameter for internal cell balance

1) *Calculate Rc*

$$Ii = \frac{Vcell}{2Rc + Ri}$$

$$Ii\ depends\ on\ the\ design\ target\ of\ your\ system\ (Max(Ii) = 50mA)$$

$$Suppose\ Vcell = 4.2V\ \ Ii = 50\text{mA}$$

$$Rc \geq \frac{1}{2} * \left(\frac{Vcell}{Ii} - Ri\right) = 32ohm$$

2) *Calculate Cc*

$$fc = \frac{1}{2\pi * 2Rc * Cc} \leq \frac{fs}{2}$$

$$fc\ depends\ on\ the\ sampling\ time\ of\ our\ system\ (MAX(fc) = \left(\frac{fs}{2}\right) = \frac{1}{50us*2} = 10KHz)$$

$$eg.when\ fs = 20KHz, Rc = 40ohm$$

$$Cc \geq \frac{1}{fs * \pi * 2Rc} = 0.2\text{uF}$$

$$we\ recommend\ using\ 10 * Cc$$

Chapter 2 How to choose input RC and charge pump capacitor

2.3 Charge Pump capacitor

Please use the Charge Pump Capacitor (flying capacitor) as we recommended, changing flying capacitor will take very little effect to rising and falling speed.

As fig.2.3.2 shows there is flat area t_{step} included in t_{rise} which is decided by charging period of charge pump and have no concern with flying capacitor.

And for the slope area, changing flying capacitor will have very little effect to rise and fall time. Fig.2.3.3 is a simulation result, it shows using too small flying capacitor (100nF) results in no enough charging to Load capacitor, and using too big flying capacitor(1500nF) results in no enough charging to flying capacitor at charging period.

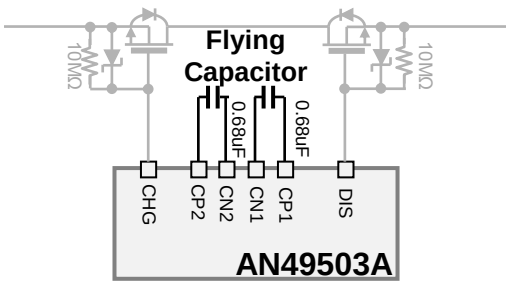


Fig. 2.3.1 Flying Capacitor

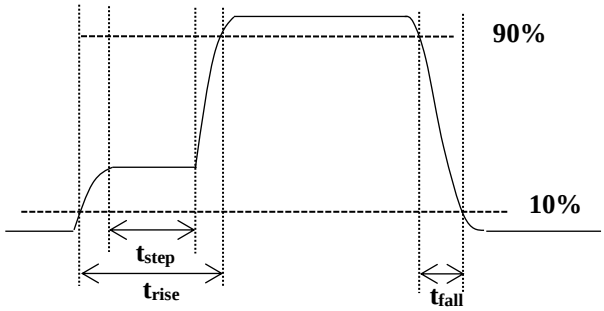


Fig. 2.3.2 FET Driver rise and fall time

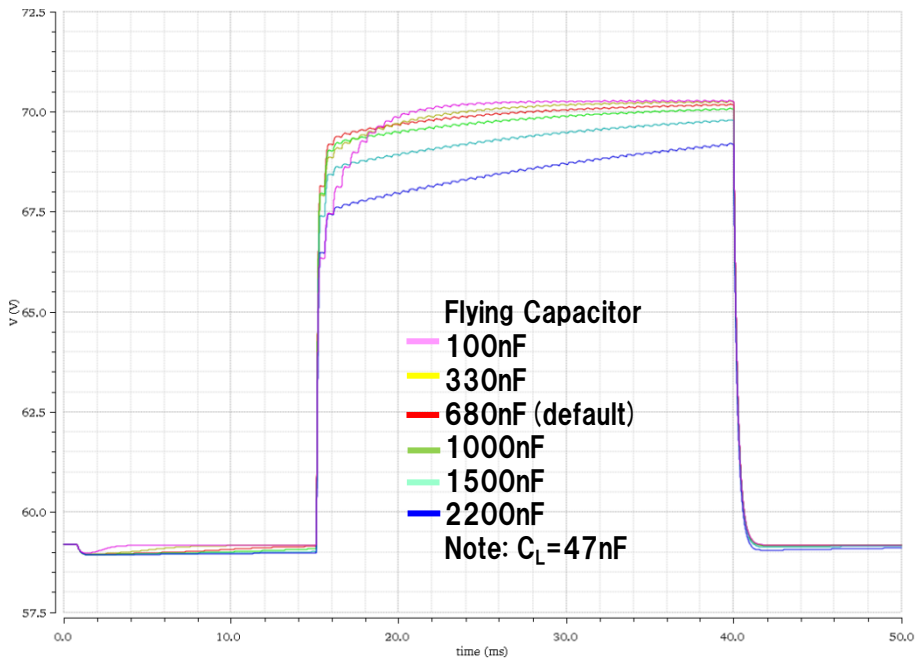


Fig. 2.3.3 Rise time and fall time vs. Flying Capacitor

Chapter 3 How to choose FET and BJT

3.1 High-side NMOS

In order to achieve rise/fall time as described in specification, Cg (the capacitance viewed from gate of FET) should be about CL as described in specification. The bigger capacitance causes the longer switch time.

For example,

FET has the following characteristic.

It means when Vdd=50V and Id=180A,

you need discharge 165nC

to get Vgs back from 10V to 0V,

so Cg=Qg/Vgs=16.5nF.

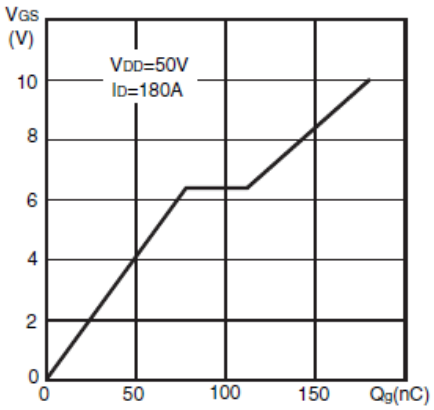


Fig. 3.1.1 Gate charge vs gate-source voltage

The following figure shows our simulation result , fall time Vs. CL.

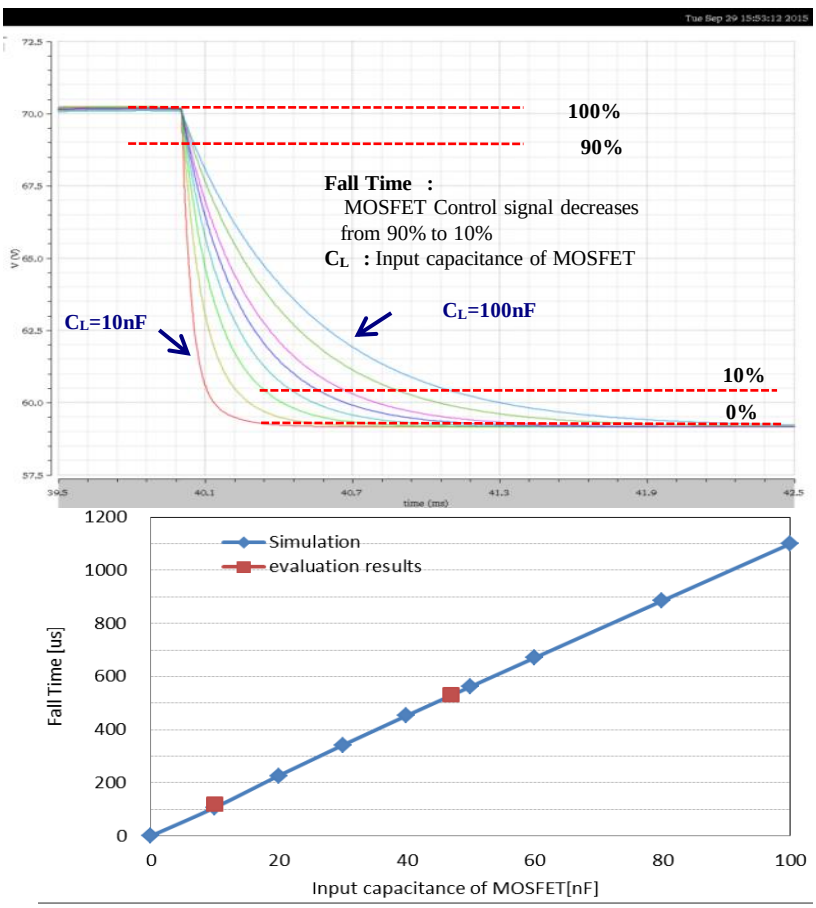


Fig. 3.1.2 FET fall time Vs. C_L

Chapter 3 How to choose FET and BJT

3.2 High-side PMOS

GPOH1/2 are driven by open-drain FET, so the Cg need not to be taken too much care of. But a resistor bigger Than 100kohm to limit the current should be applied between Gate and GPOH pin.

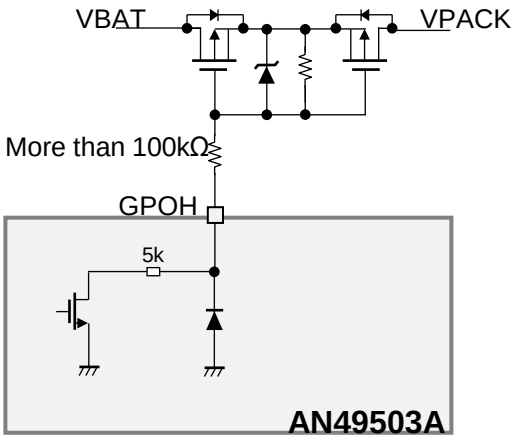


Fig. 3.2.1 circuit example when using GPOH

3.3 NMOS for external cell balancing

When you apply VBAT, the high voltage may occur transiently between the external FET pins for cell balance, since there is a time constant of the RC.

The FET with high voltage tolerance is highly recommended.

Or if high voltage tolerance is unacceptable for your system, you may separate VBAT from C16 as Fig.3.3.2

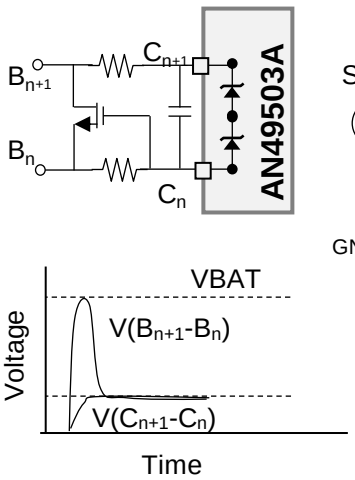


Fig. 3.3.1 Transient High Voltage

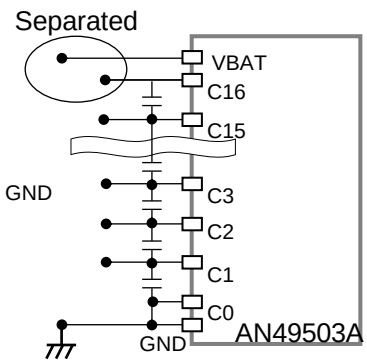


Fig. 3.3.2 Separated VBAT

Chapter 3 How to choose FET and BJT

3.4 LDO FET

LDO FET must be connected as Fig .3.4.1.

FET, C_g, R_g, C_s, R_s should be selected according to the loop characteristic of LDO.

We suggest the following pattern:

When C_{iss} is around 530pF such as RSD050N10

C_g = 15nF R_g= 12K C_s = 2ohm R_s =10uF

When Ciss is around 1200pF

C_g = 22nF R_g= 6.8K C_s = 2ohm R_s =10uF

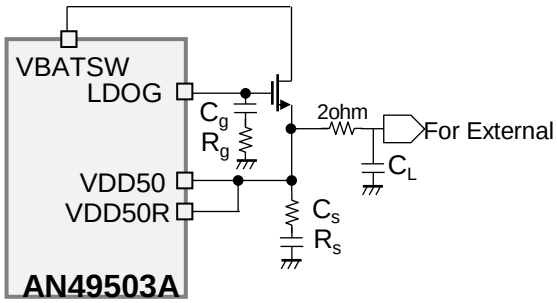


Fig. 3.4.1 LDO circuit

Note: Please make sure that C_L is between 6uF and 16uF

3.5 BJT for external cell balancing

External Cell balance

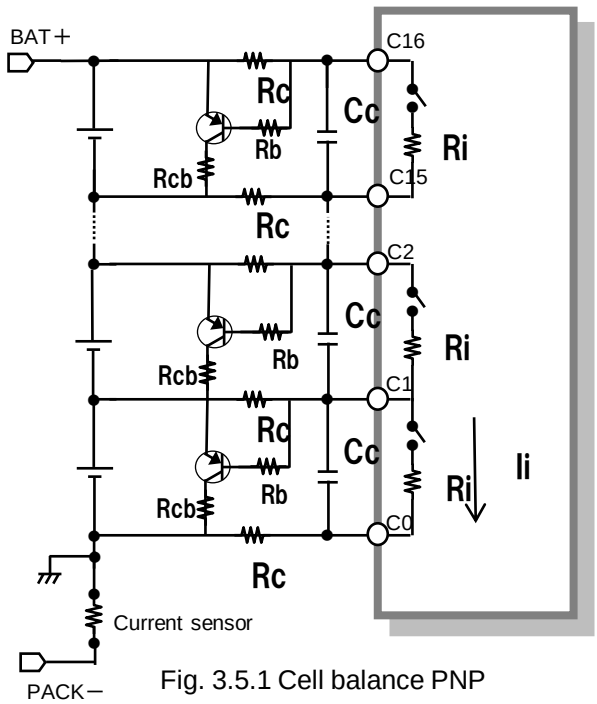


Fig. 3.5.1 Cell balance PNP

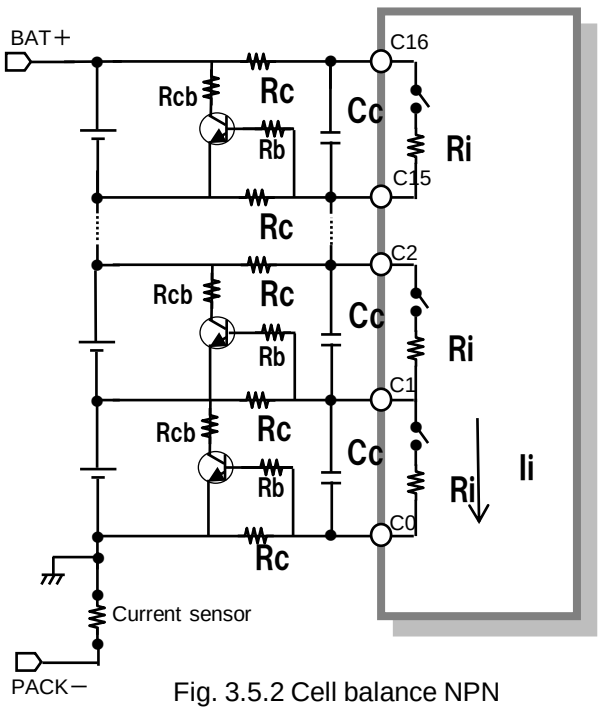


Fig. 3.5.2 Cell balance NPN

Eg. for parameter choosing:

Rc=1kohm, Rcb =75ohm, Rb=100ohm

PNP BJT BC856 (Veb = 0.8V,Vce(sat)=-0.1V)

Icb = (Vcell + Vce(sat)) / Rcb = 48mA when Vcell = 3.7V

Note: when open circuit detection is on, current (max. 80uA typ.40uA) will be drew though Rc, please make sure Rc* I is smaller than On threshold of BJT.

Chapter 4 How to deal with unused pins

1) All pin named NC should be leave unconnected

2) For the unused battery cells pins (C3~C13)

Fig.4.1 is a example for 4-cell solution, the cells can be added from lower to upper(C3,C4…) for the solution which need more cells.

3) For the unused function pins

Table.4.1 is a list for unused function pins.

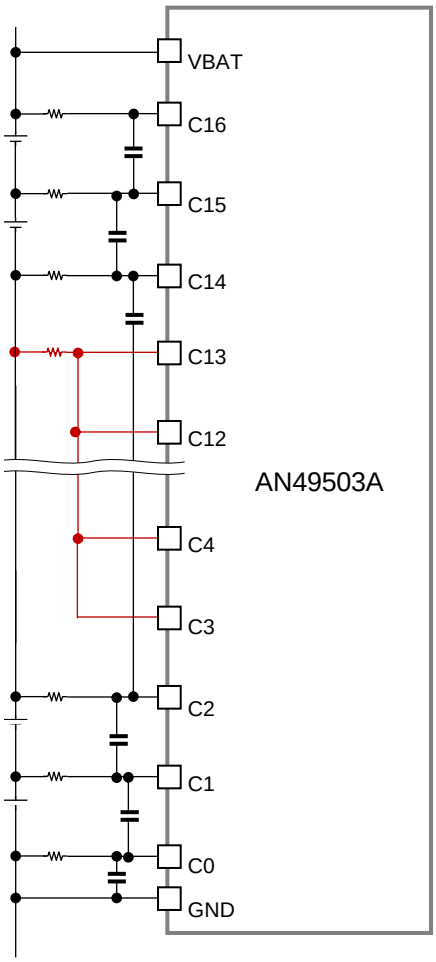


Fig.4.1 Cell Connection Example with only 4 cell connected

Function	Pin	Connection
Temperature	TMONIn (n=1~5)	Open
Nch FET	CHD, CP2, CN2 DIS, CP1, CN1	Open
Pch FET	GPOH1,GPOH2	Open
Function pin	ALARM1	Open
	FETOFF	Ground
	STB	Ground
	SHDN	Ground
MCU communication	SDO, NREST	Open
	SDI, SCL, SEN	Open
Current	SRP/SRN	Floating or Ground
GPIO	GPIOn (n=1~6)	Open*1

*1 Enabling the pull-down resistor by software is needed

Table.4.1 Connection Example for unused function pins

Chapter 5 Connection sequence

5.1 Recommendation

We strongly suggest to follow our recommendation described as our specification

Battery cells connection sequence:

Connect the GND pin followed by VBAT pin. After that, it should be connected from the lower cell in turn.

GND -> VBAT -> Cell between C0-C1 -> Cell between C1-C2 ->…

5.2 Special case

If our recommendation can not be followed, such as random connection or partial random connection sequence is required.

Please make input resistor bigger than 100ohm for a fully random connection sequence.

For input resistor smaller than 100ohm, connect GND and VBAT first and than random connection for others cell voltage pin.

Note: Connection sequence for special case is verified by simulation with limited numbers of IC test, it seems no risks.

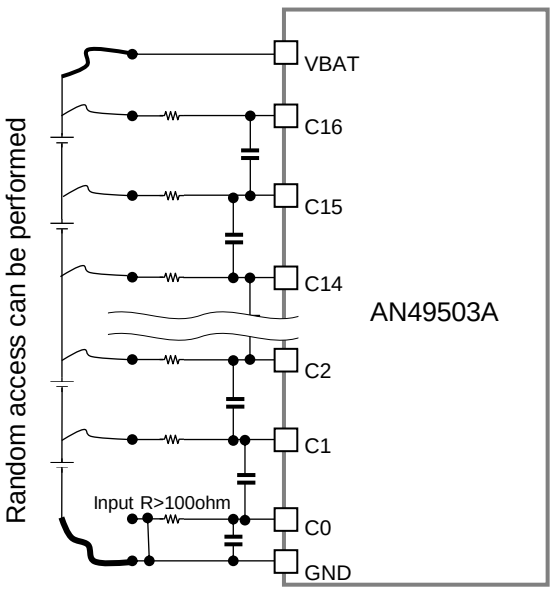


Fig. 5.2.1 Input Resistor bigger than 100ohm

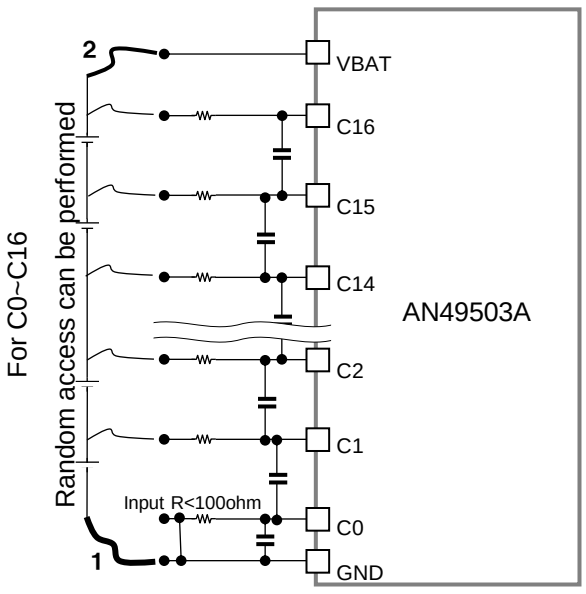


Fig. 5.2.2 Input Resistor smaller than 100ohm

Chapter 6 How to use Operation Mode

6.1 Introduction of each mode

There are three kinds of operation mode, Active mode, Standby mode and Shutdown mode.

In Shutdown mode, all function is stopped to save the power. We recommend that only use this mode when the system do not need to or can not protect the battery system.

In Active mode every function is activated and of course the current consumption is the highest. In Standby mode, Cell voltage measurement is stopped to lower power consumption. For more details, please refer to Specifications.

We recommend that keep most of time in Standby mode and change to Active mode only when it is necessary to lower the current consumption.

The following example shows that periodically switched between Active mode and Standby mode.

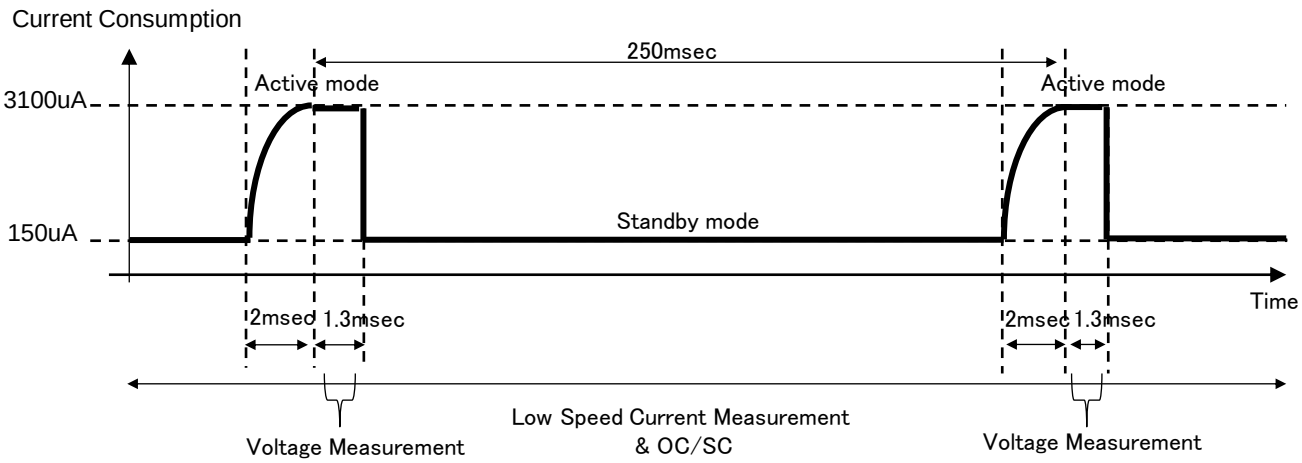


Fig. 6.1.1 operation mode

I_{AVG}=189uA=(3100uA*3.3ms+150uA*(250ms-3.3ms))/250ms

Chapter 7 Standalone without MCU

7.1 Introduction standalone

After initializing the registers according to your system, This IC can work without a MCU on the board which is called standalone mode.

Note:

The average current consumption is about 140uA.

The register initialization should be done after power up, since the register value is volatilized.

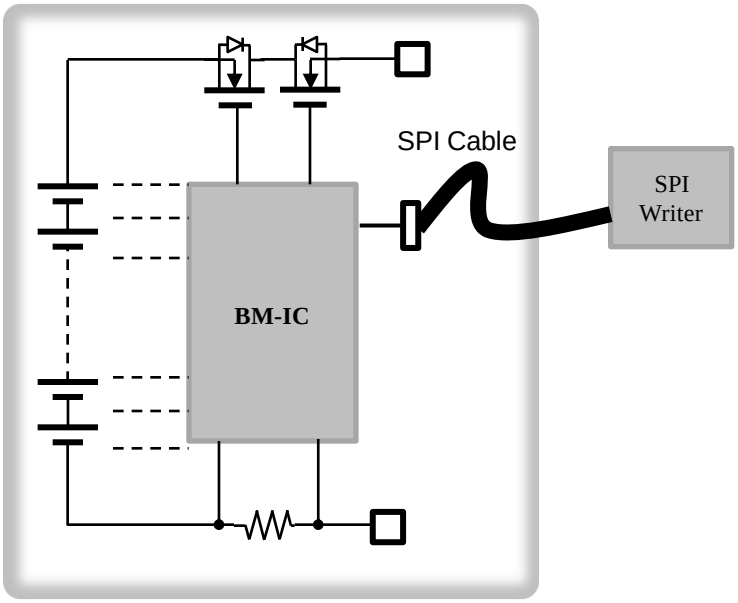


Fig.7.1.1 Standalone

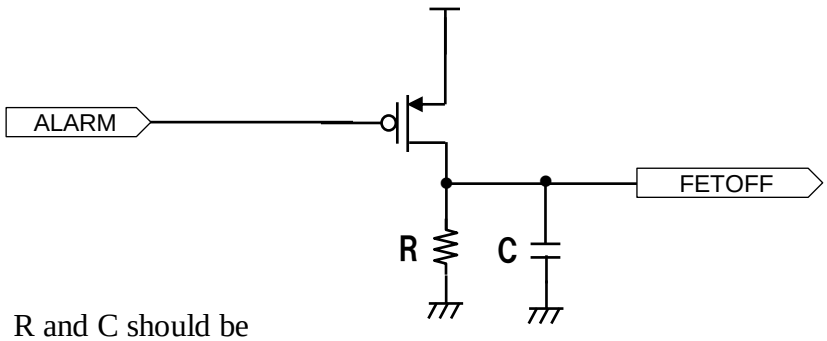
In this mode the voltage is measured every 1 second, and the over current is continuously monitored. Alarm signal can be output and FET control can be done automatically.

7.2 For OV(over voltage), UV(under voltage)

When the OV or UV alarm occurred, the FET(charge FET for OV and discharge FET for UV) will be turned off and when the alarm is released, the FET can be recovered automatically.

7.3 For OCC(Over Current of Charge) ,OCD(Over Current of Discharge)

If a recovery from over current is need, please set the listed register as List 7.3.1 and implement the external circuit such as figure 7.3.1 to generate recovery time delay.



R and C should be decided according to delay time requirement

figure 7.3.1 circuit for generating recovery time delay

register	flag	Setting Value and description
FDRV_CTL bp15	FDRV_ALM_SD	Enable protection output when alarm is asserted 1:Enable protection output
FDRV_CTL bp14	FDRV_ALM_RCV	protection output Clear Condition 1: Manual Clear (By write 1 to FDRV_ALM_CLR)
FDRV_CTL bp13	FDRV_ALM_CLR	Manual Clear 1:Clear

Table.7.3.1 Setting for OCD/OCC recovery

7.4 For SCD(Short Circuit in Discharge)

you can also generate a shutdown signal when SCD detected.

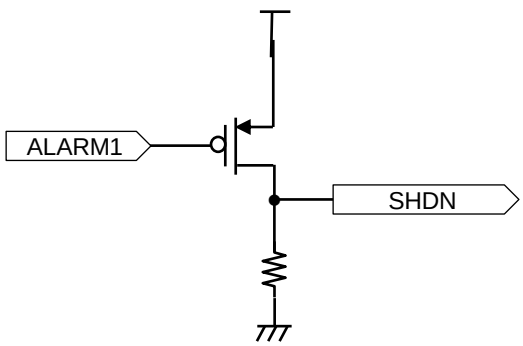


figure 7.4.1 circuit for generating shutdown signal

Chapter 8 High-side FET connection

8.1 Examples for high-side FET connection

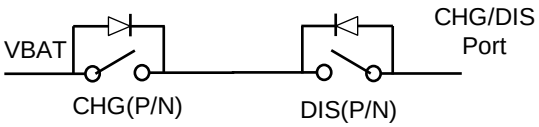


figure 8.1.1 Single Port

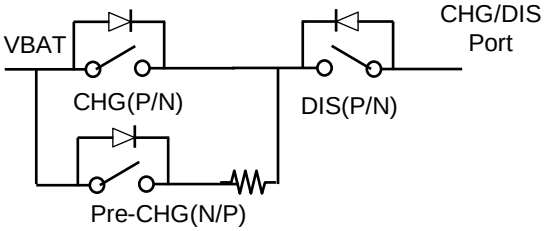


figure 8.1.2 Single Port with Pre-charge

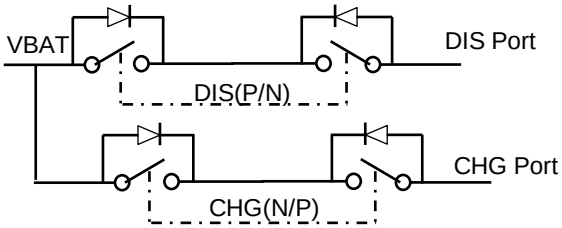


figure 8.1.3 Separated port

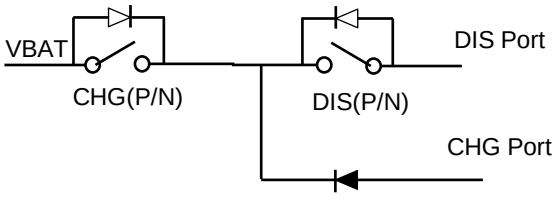


figure 8.1.4.a Separated port(Low cost)

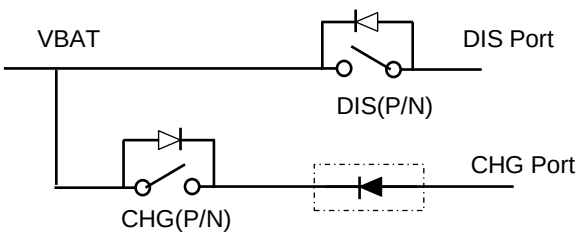
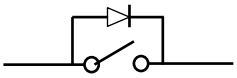


figure 8.1.4.b Separated port(Low cost)

Note:  MOSFET

CHG: Charge DIS: Discharge P:P-ch MOSFET N:N-ch MOSFET

8.2 For UPS (Use battery only at emergency)

Some systems such as UPS, need only use Battery when the external power failed. The following example is shown to explain how to switch the power for this kinds of system.

Open or close FET(PowerLoss) by using CHG(N) pin, according to the monitored Voltage of Ext Power from VPACK pin. Making sure the threshold voltage for switching is correctly set in case IC loses its power before FET is on.

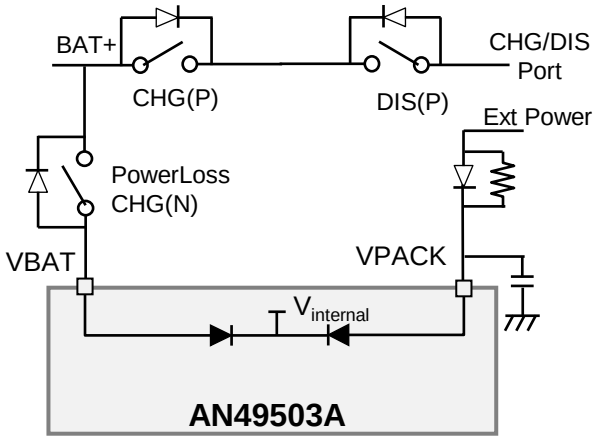


figure 8.2.1 Switch Power by GPOH

Chapter 9 Low-side FET connection

9.1 Examples for low-side FET connection

GPIO1/2 can be used to output digital signal(0,5V) for control of FET, Relay etc.
If the 5V is not enough for your FET and you do not want to implement a extra driver,
The following diagram may be your solution.

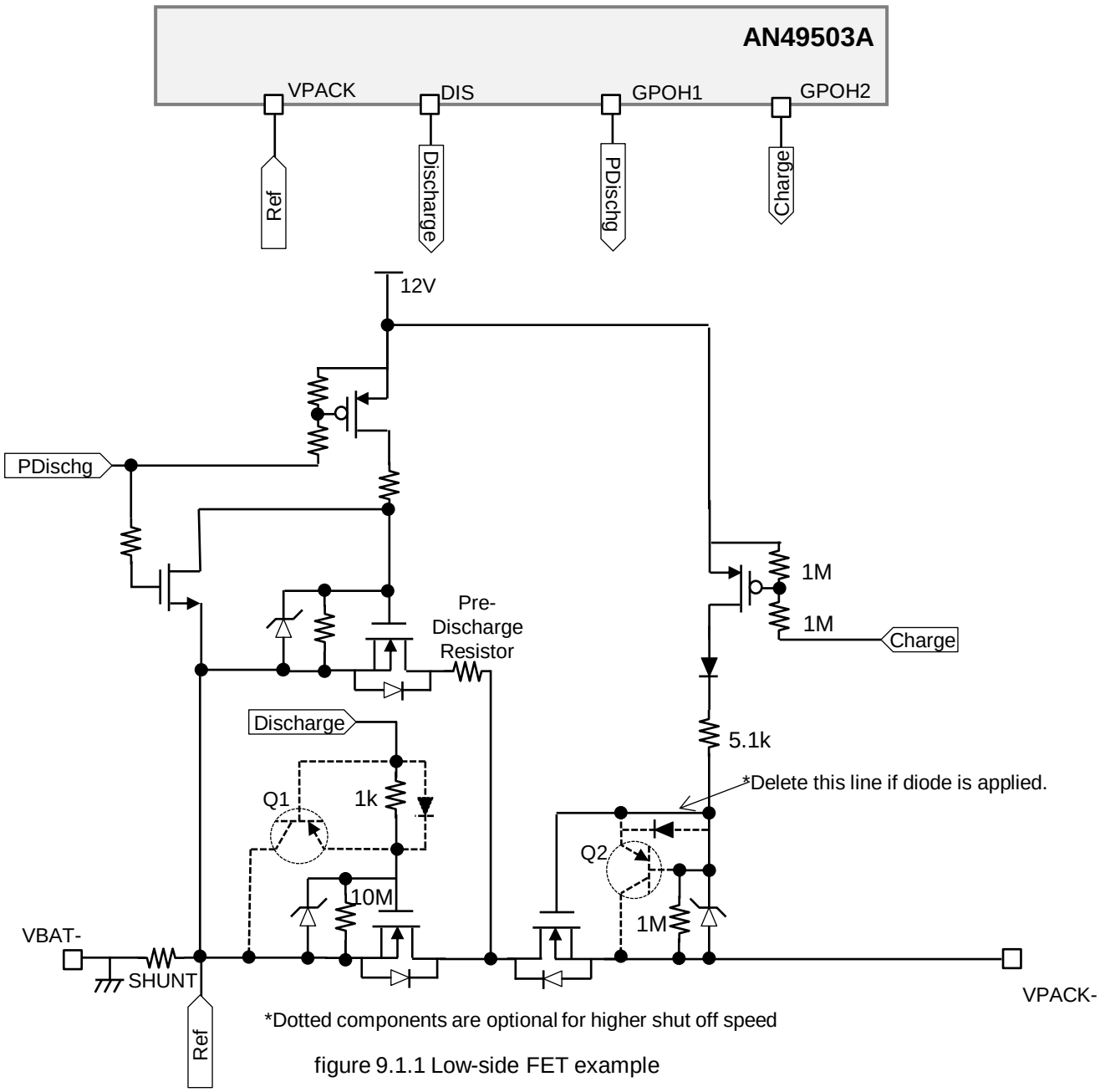


figure 9.1.1 Low-side FET example

Note1:Can not achieve short turn off Time for charge FET if Q2 is not applied.
Note2:Charge FET may not be able fully turned on when Pre-discharge Current * Pre-discharge resistor is too large.
Note3:Please check specification for turning off timing of GPOH when hardware protection is on.

Chapter 9 Low-side FET connection

If C_L is beyond our requirement since too much FET should be implemented, the following push-pull structure for low-side FET may be your solution.

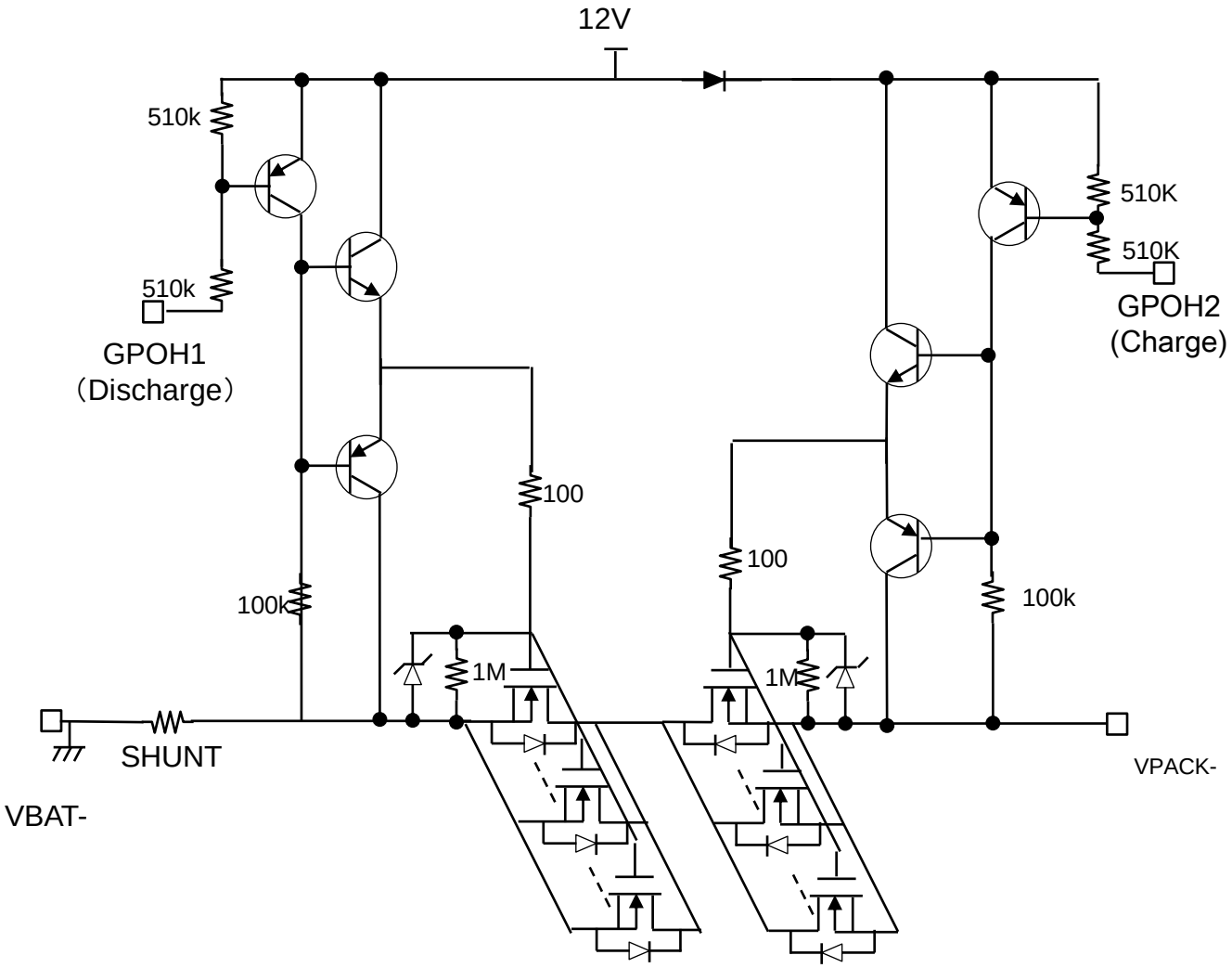


figure 9.1.2 Low-side FET example (push pull structure)

Note1:GPOH can be control through register access.

Chapter 10 Output high accurate clock from GPIO

10.1 high accurate clock from GPIO

The high accurate clock can be output from GPIO. It can be used such as a reference for MCU to increase the coulomb counter accuracy.

The following clock can be outputted from GPIO.

GPIO3:
- Accuracy (under 5%)
- 5kHz

GPIO4:
- Accuracy (under 2%)
- 1/1 (262.144kHz)
- 1/32 (8.192kHz)
- 1/64 (4.096kHz) (Default)
- 1/128 (2.048kHz)

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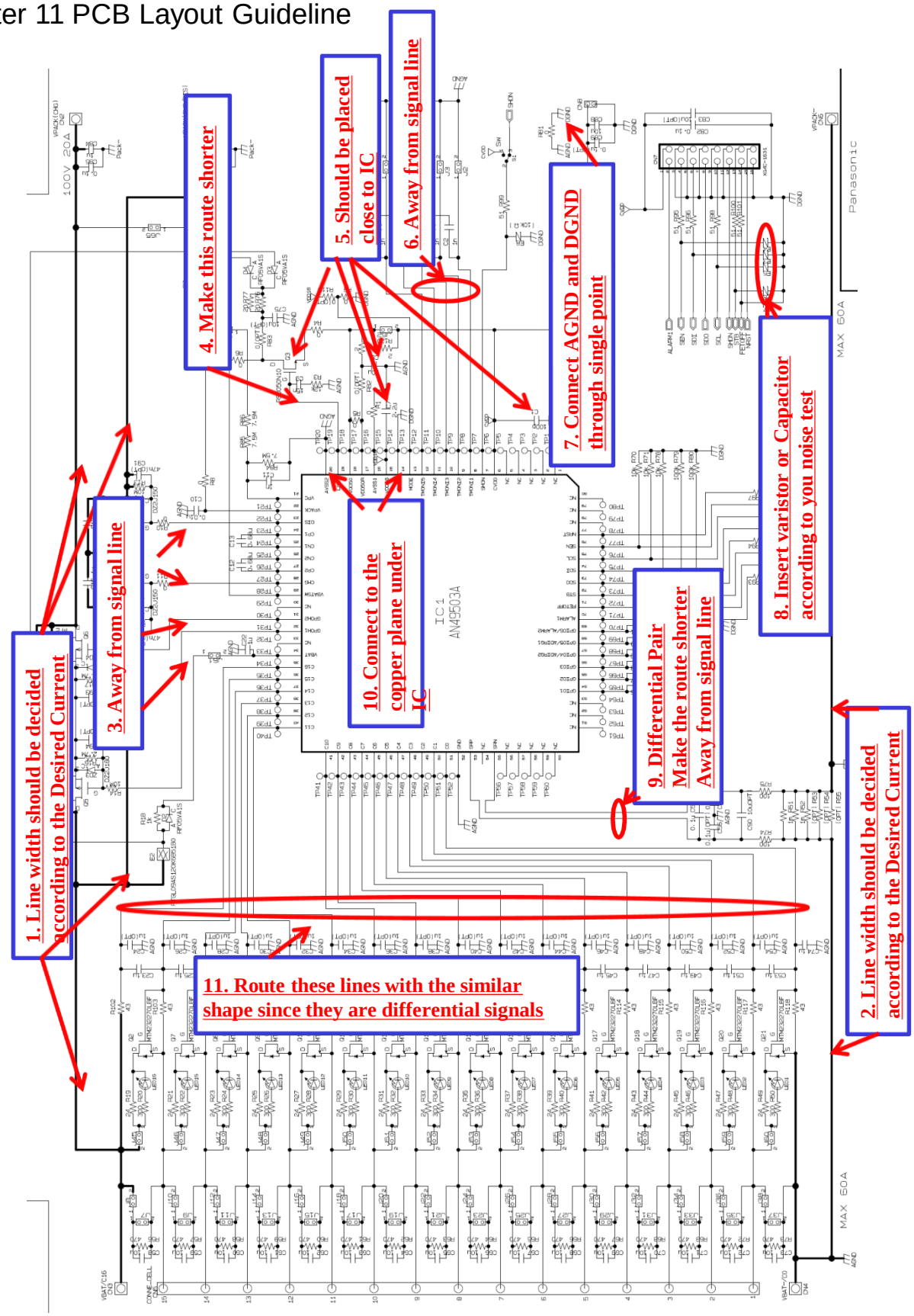
AN49503A Application Note

Chapter 11 PCB Layout Guideline



Important Notice

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board),
   it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins.
   In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.

Panasonic

AN49503A Application Note

Revision History

Control number	Revision date	Page	Item	Before revision	After revision
Ver0.10(E)	2015.08.18			Preliminary release	
Ver0.13(E)	2015.12.25				Fix some chapter number Add connection sequence Add LDO FET selection Add charge pump parameter
Ver0.14(E)	2015.01.07				Add BJT for cell balancing Change low-side proposal
Ver0.15(E)	2015.01.14				Fix chapter number and page
Ver0.20(E)	2015.01.22				Change Chapter No. Add figure 3.1.2 And Release