Panasonic

AN49502A EVB User Guide

Ver 1.00

Panasonic Semiconductor Solutions
Co. Ltd.

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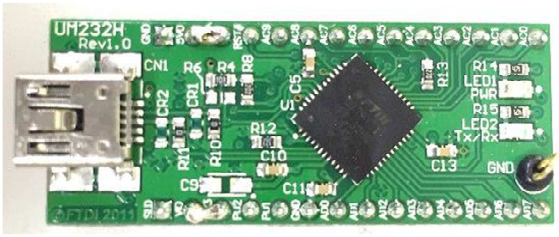
AN49502A EVB is an evaluation board for AN49502A, a 5~10 cells Li-ion battery monitoring IC with daisy chain communication supporting stackable design. Each of the evaluation board consists of two AN49502A ICs with peripheral circuitry. A system with up to 20 battery cells can be evaluated with one evaluation board. The evaluation system can be extended for system required more than 20 battery cells by using multiple evaluation boards. With the evaluation software provided, user can evaluate AN49502A function such as daisy chain, voltage measurement, OV/UV protection etc.

1. Features

- Two AN49502A ICs on one board supporting evaluation system up to 20 battery cell
- Support daisy chain for multiple boards for higher battery cell system
- On-board cell balance circuitry
- PC software available for evaluation boards

1.1 Evaluation Kit Contents

- AN49502A Evaluation Board
- 2 ways cable x 1 (optional)
- 10ways cable x 1 (optional)
- 16ways cable x 1
- UM232H Interface Module for PC Software



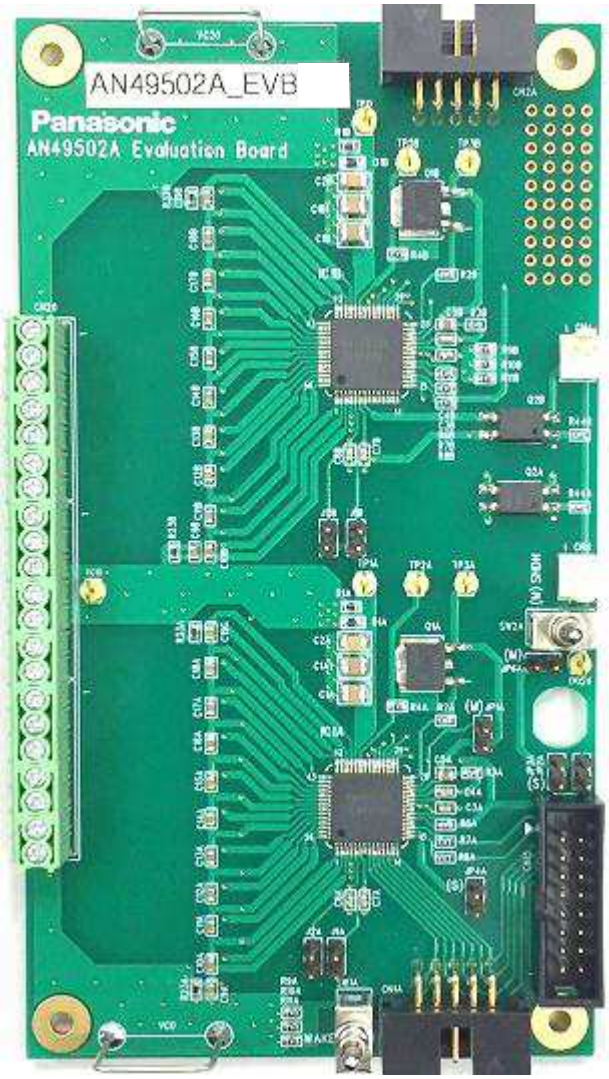


Figure 1 (i) AN49502A Evaluation Board (Top View) (ii) UM232H Interface Module

2. Definition of terms

- AN49502A EVB – Evaluation board with 2 AN49502A ICs designed in stacking. The upper IC (IC1B) is pre-configured as Slave IC while the lower IC (IC1A) is configurable as Master IC or Slave IC.
- Master board – an AN49502A EVB with the IC1A configured as Master IC. During the evaluation, a Master board must be connected to MCU/SPI interface board by CN15. CN1A must not be used. In one system, there must be one and only one Master board.
- Slave board – an AN49502A EVB with the IC1A configured as Slave IC in the evaluation. A Slave board must be connected to at least one lower board, which could be another slave board or master board through CN1A. CN15 must not be used. In one system, there may be maximum three Slave boards.
- Stacking – AN49502A could be designed in stacking connection, in each AN49502A EVB, there are two AN49502A connected in stacking. When evaluation in stacking, one and only one IC/board must be configured as IC/Master board, while other ICs/boards must be configured as Slave IC/board.
- Upper board – an AN49502A EVB connected to the CN2A of EVB referred.
- Lower board – an AN49502A EVB connected to the CN1A of EVB referred. A Master board is always the lowest board in a system.
- Device address – when multiple AN49502A ICs are used, each IC has to be assigned a unique device address, the device address has to be setup immediately after wake up. The device address is setup by writing total devices number to register 0x00 of Master IC, the device address will be automatically assigned as:
    a. Master IC : equal to total device number set
    b. Slave IC : subsequent upper ICs are Slave ICs and will be assigned device address with decrement of 1 from lower IC.

3. AN49502A EVB connectors

Several connectors are available to interface from AN49502A EVB to

- battery cells,
- upper or lower board for stacking evaluation
- SPI & I/O communication interface.

Connector	Description
CN1A	Daisy Chain Communication Connector to lower board (used only for Slave board)
CN15	SPI and I/O ports (used only for Master board)
CN2A	Daisy Chain Communication Connector to upper board
CN3	Shutdown signal from lower board
CN4	Shutdown signal to upper board
CN20	Battery cells input C0 ~ C20

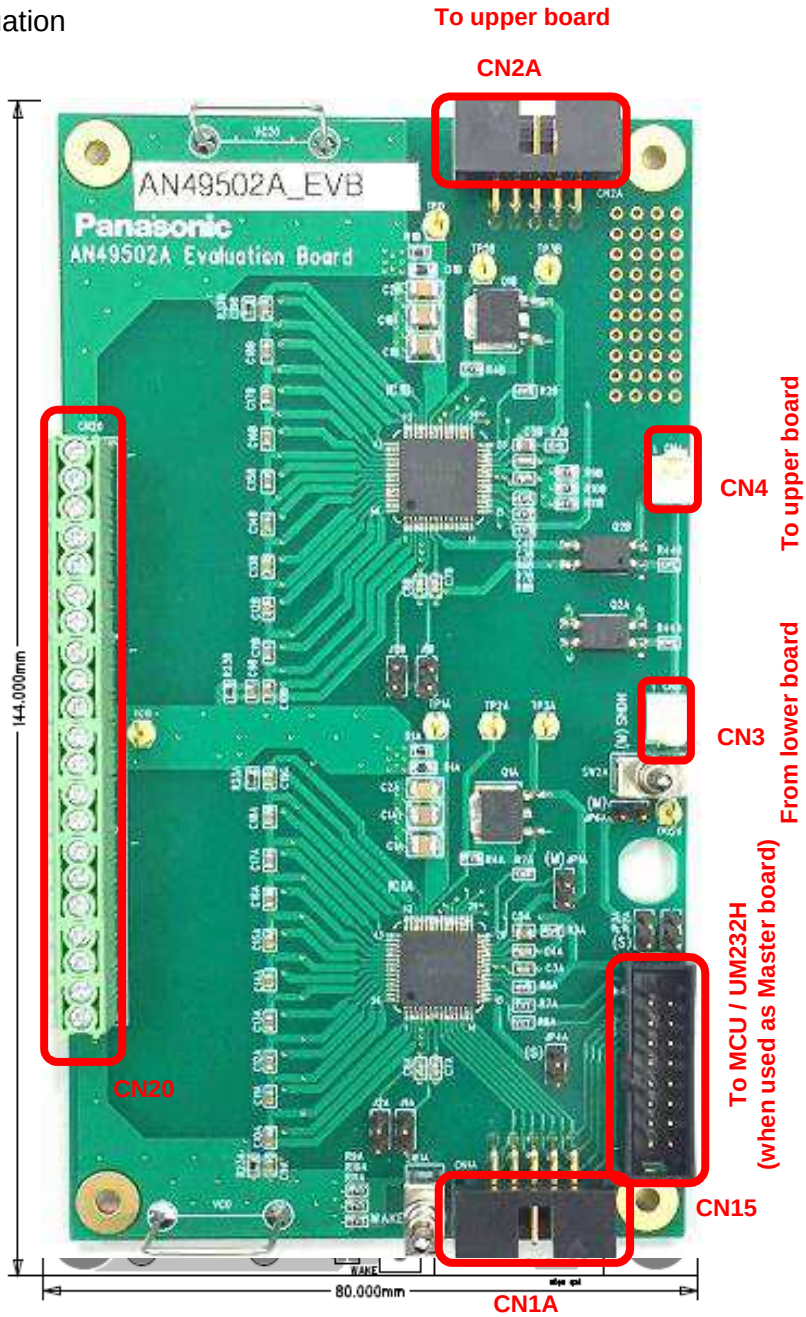


Figure 2 AN49502A EVB Connectors

3.1 Connector pin configuration

CN1A – used to connect to CN2A of lower board

CN1A	Description
1 SDI_L	SDI from lower board
2 SDO_L	SDO to lower board
3 ALARM_L	ALARM to lower board
4 NFAULT_L	NFAULT signal to lower board
5 BUSY_L	BUSY signal to lower board
6 STB_L	Standby control from lower board
7 NWAKEUP_L	Wake up control from lower board
8 NC	-
9 NC	-
10 NC	-

CN2A – used to connect to CN1A of upper board

CN2A	Description
1 SDO_U	SDI signal to upper board
2 SDI_U	SDO signal from upper board
3 ALARM_U	ALARM signal from upper board
4 NFAULT_U	NFAULT signal from upper board
5 BUSY_U	BUSY signal to upper board
6 STB_U	Standby control to upper board
7 NWAKEUP_U	Wake up control to upper board
8 NC	-
9 NC	-
10 NC	-

CN15 – used only on Master Board

CN15	Description
1 SCLK_L	SCLK for SPI communication
2 SDI_L	SDI for SPI communication
3 SDO_L	SDO for SPI communication
4 SEN_L	SEN for SPI communication
5 STB_L	Standby pin control
6 NFAULT_L	NFAULT status pin
7 BUSY_L	BUSY status pin
8 ALARM_L	ALARM status pin
9 NC	-
10 DGND	Digital ground to AN49502A
11 NC	-
12 NC	-
13 NC	-
14 NC	-
15 NC	-
16 CVDDA	CVDDA, supply voltage to AN49502A

CN3 – used to connect to CN4 of lower board
CN4 – used to connect to CN3 of upper board

CN3/CN4	Description
1 DGND_M	Master board digital ground
2 SHDN_M	Shutdown Control Signal - Signal propagated from Master board **- 5V/0V as referred to Master board ground**

Note : voltage at CN3/CN4 is referred to ground of Master board and may has large different potential to the board voltage.

4. AN49502A EVB configuration before evaluation

There are two AN49502A ICs and peripheral circuitry built on each AN49502A Evaluation Board. When evaluation is done with one board, the lower IC should be configured as Master IC by setting jumpers accordingly. The upper IC on EVB has been pre-configured as Slave IC. When evaluating with multiple boards, one IC has to be configured as Master IC while other ICs set as Slave IC.

4.1 Evaluation with one EVB

NOTE: (i) Adjust jumpers setting only when power is OFF or when no batteries connected

4.1.1 Configuring EVB jumpers for one board evaluation –

Lower IC is required to be configured as Master IC following table below

Master board	Setting
JP1A-1	To JP4A-1 as shown
JP2A	Open
JP3A	Open
JP4A-1	To JP1A-1 as shown
JP6A	Short

Other jumpers

J1A, J2A, J1B, J2B	Thermistor

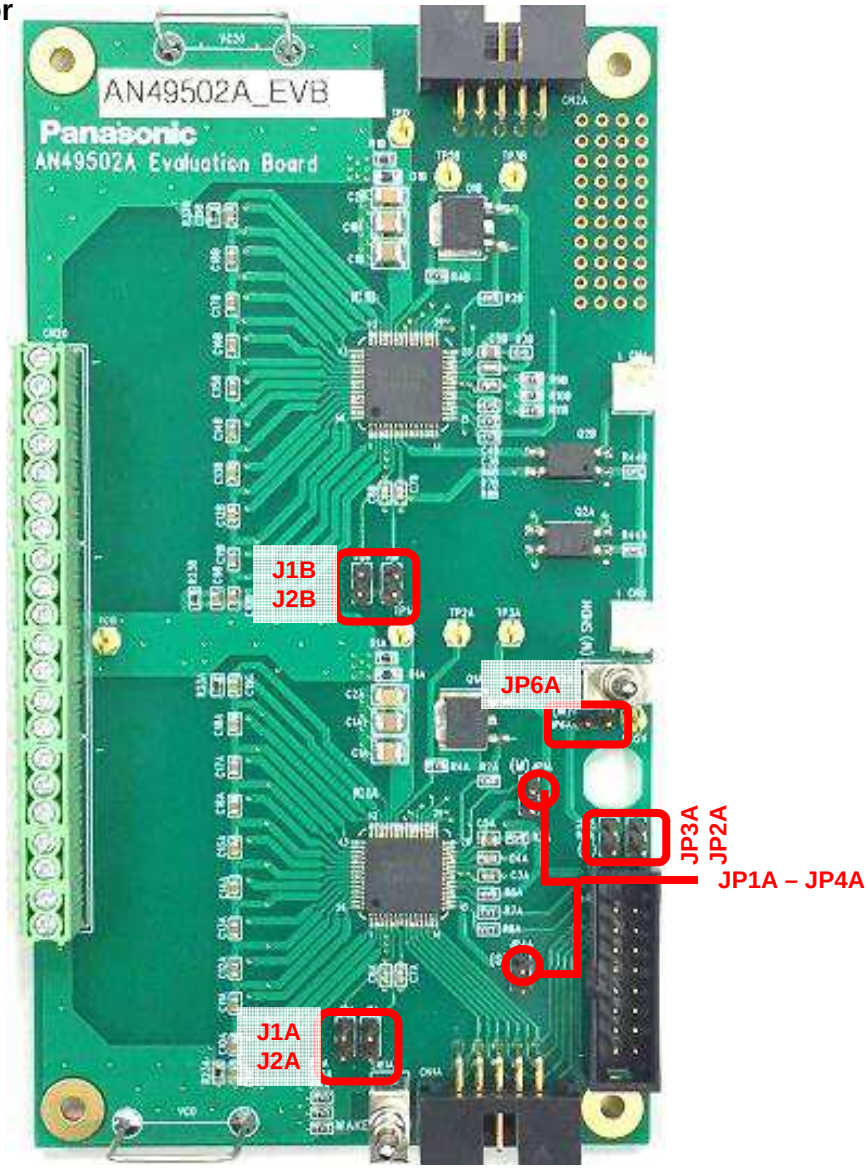


Figure 3 AN49502A EVB Jumpers

4.1.2 Power connection to the EVB

The EVB may be evaluated with actual battery cells or using power supplies with resistor divider to simulate the cell voltage. Two power supplies used in cascaded connection are required for one EVB board. The smaller the resistor used, the higher the current will be drawn by the resistor divider, and the effect to the cell balance current will be less.
A 5V supply is required for shutdown control on this EVB.

Unused cell input should be shorted together except for cell 1 to cell 4 and cell 10.

(a) with actual battery cells
Sequence:
VC0 -> VC10 -> VC20
-> from lower VC to higher
-> set (M)5V to 5V

(b) with resistor divider
Sequence:
VC0 -> VC10 -> VC20
-> set (M)5V to 5V

NOTE: resistor divider is required to be connected before connecting power

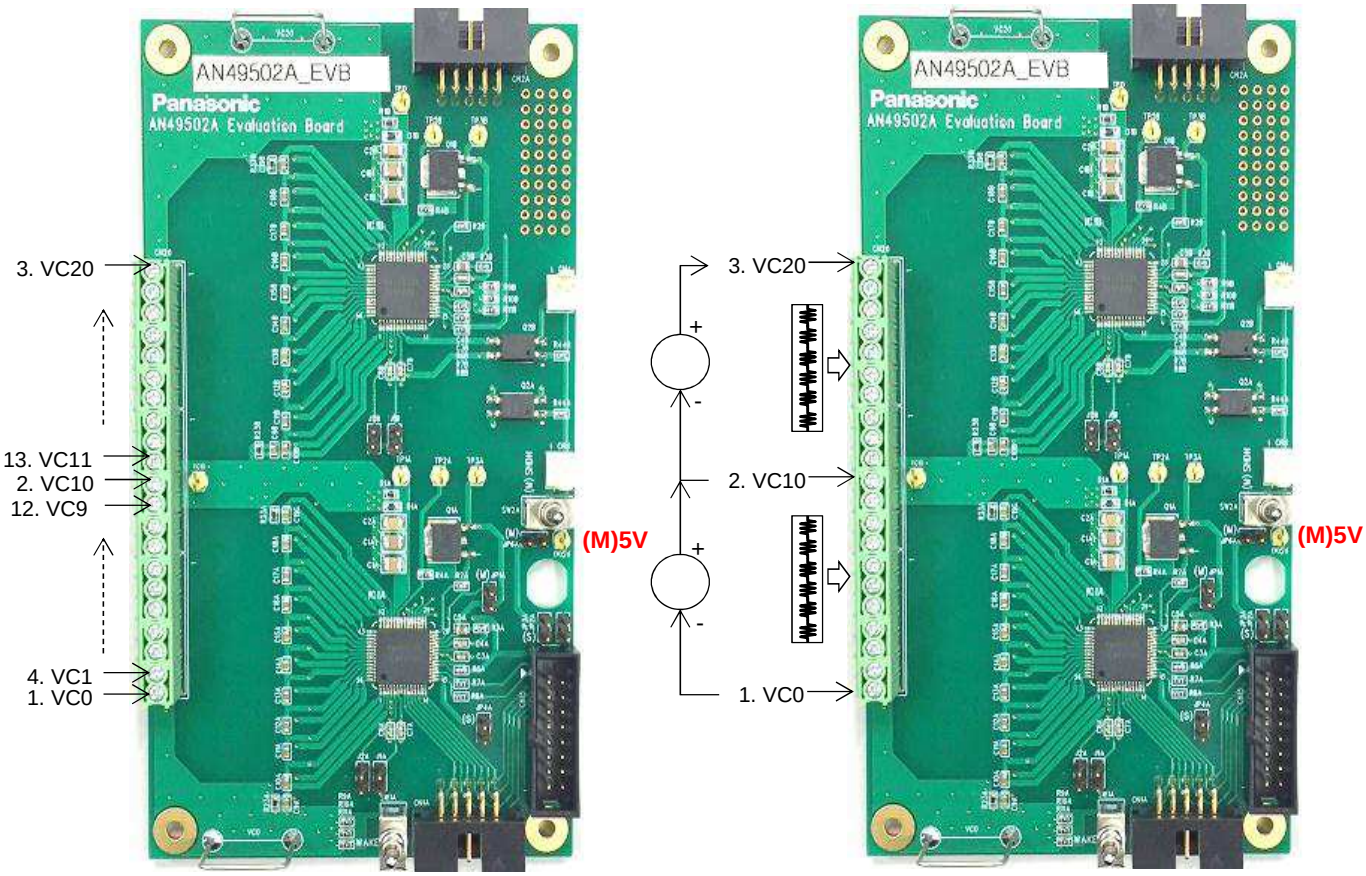


Figure 4 AN49502A EVB Connecting with (a) battery cells (b) power supply

4.1.3 Connecting to PC for evaluation

Connect the SPI and I/O ports to UM232H board and to USB port from PC accordingly. The evaluation setup is completed and is ready to start.

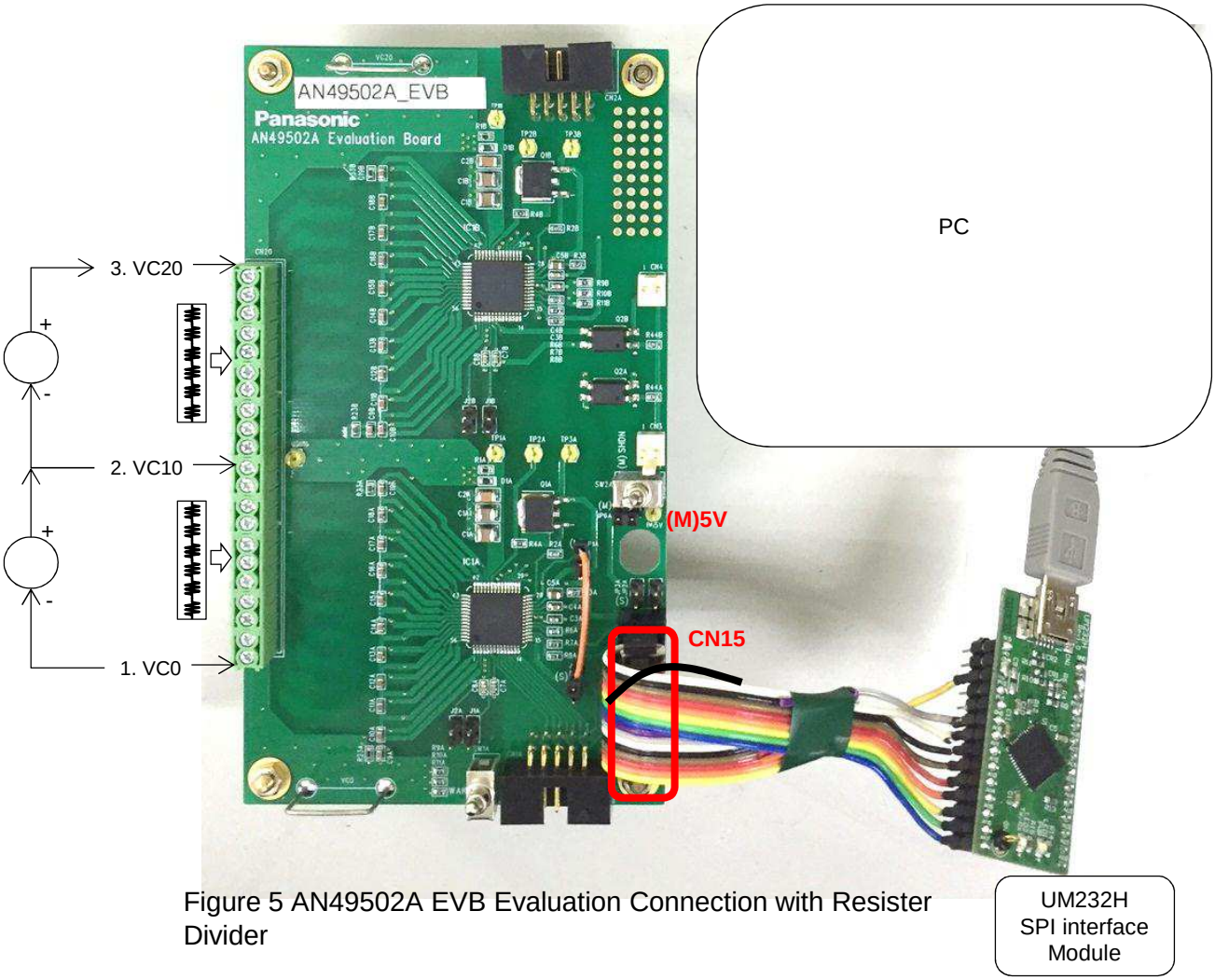


Figure 5 AN49502A EVB Evaluation Connection with Resister Divider

4.2 Evaluation with multiple EVBs in stacking

NOTE: Adjust jumpers setting only when power is OFF or when no batteries connected

4.2.1 Configuring EVB jumpers and switches for multiple EVBs evaluation –

When multiple EVBs are used for evaluation. One of the board is used as the Master board while other boards will be used as Slave board. Jumpers and switches should be set accordingly for Master board and Slave board.

Master Board	Setting
JP1A	To JP4A as shown
JP2A	Open
JP3A	Open
JP4A	Open
JP6A	Short

Switches

SW1A	Refer to section 6
SW2A	Refer to section 6

Slave Board	Setting
JP1A	Open
JP2A	Short
JP3A	Short
JP4A	Short
JP6A	Open

Other jumpers

J1A, J2A, J1B, J2B	Thermistor

Switches

SW1A	Center position
SW2A	Upper position

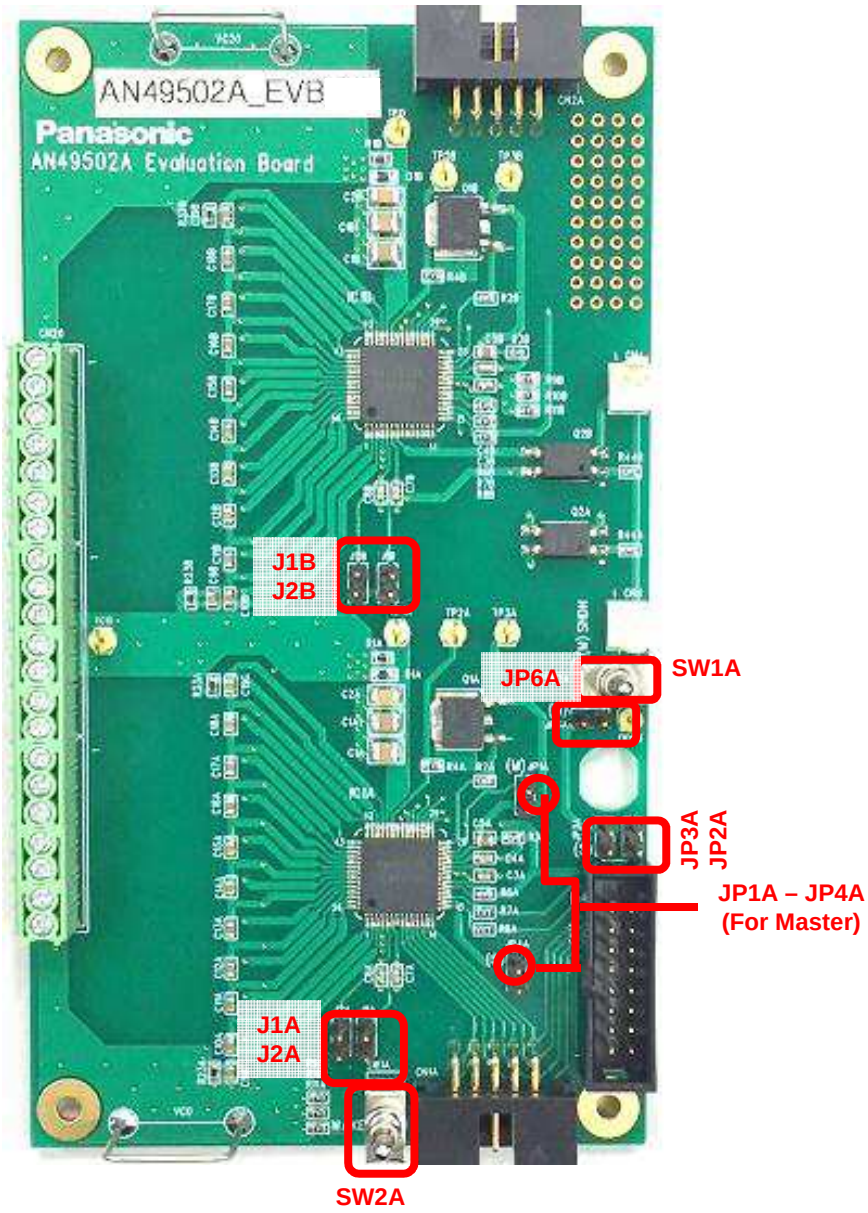


Figure 6 AN49502A EVB jumpers and switches

4.2.2 Connecting multiple EVBs - connector

When multiple EVBs are used for evaluation, the CN2A of lower board are required to be connected to CN1A of upper board for daisy chain communication. CN4 of lower board are required to be connected to CN3 of upper board for shutdown signal.

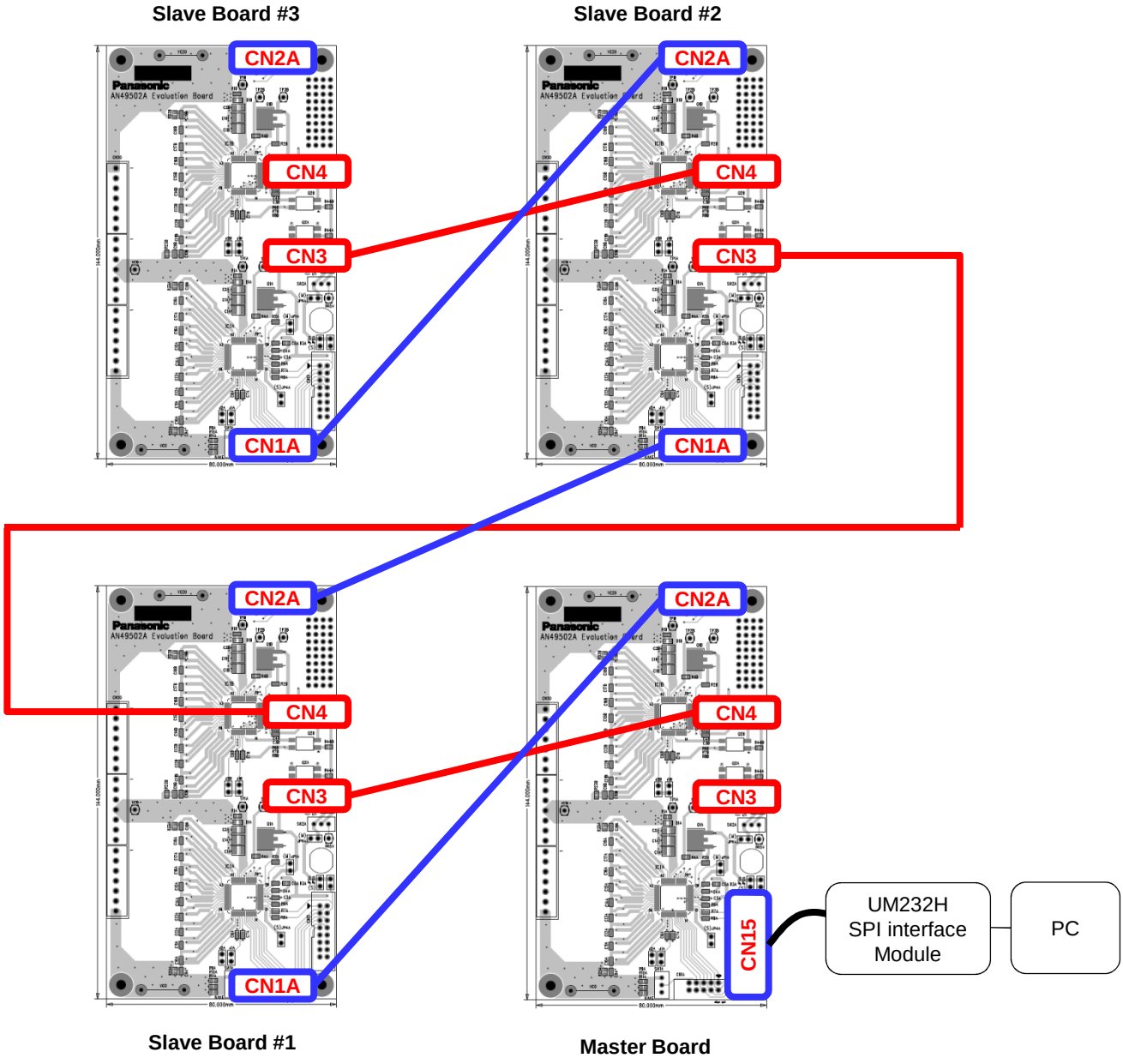


Figure 7 Example for 4 boards evaluation connection –
(i) connectors

4.2.3 Connecting multiple EVBs - power

Power connection for each EVB is same as 3.1.2 for each board. **The (M)5V should be applied only for Master board**. For connecting between EVBs, the highest voltage VC20 of lower board is to be connected to lowest voltage VC0 of upper board.

Precaution: 1. The DC voltage level could be more than few hundreds volt for stacking evaluation.
2. The voltage at CN3 and CN4 of each board is 0V/5V as refer to Master board ground, while the voltage at each board may exceed hundreds volt, the voltage difference of CN3/CN4 with other part of the boards may exceed hundreds volt.

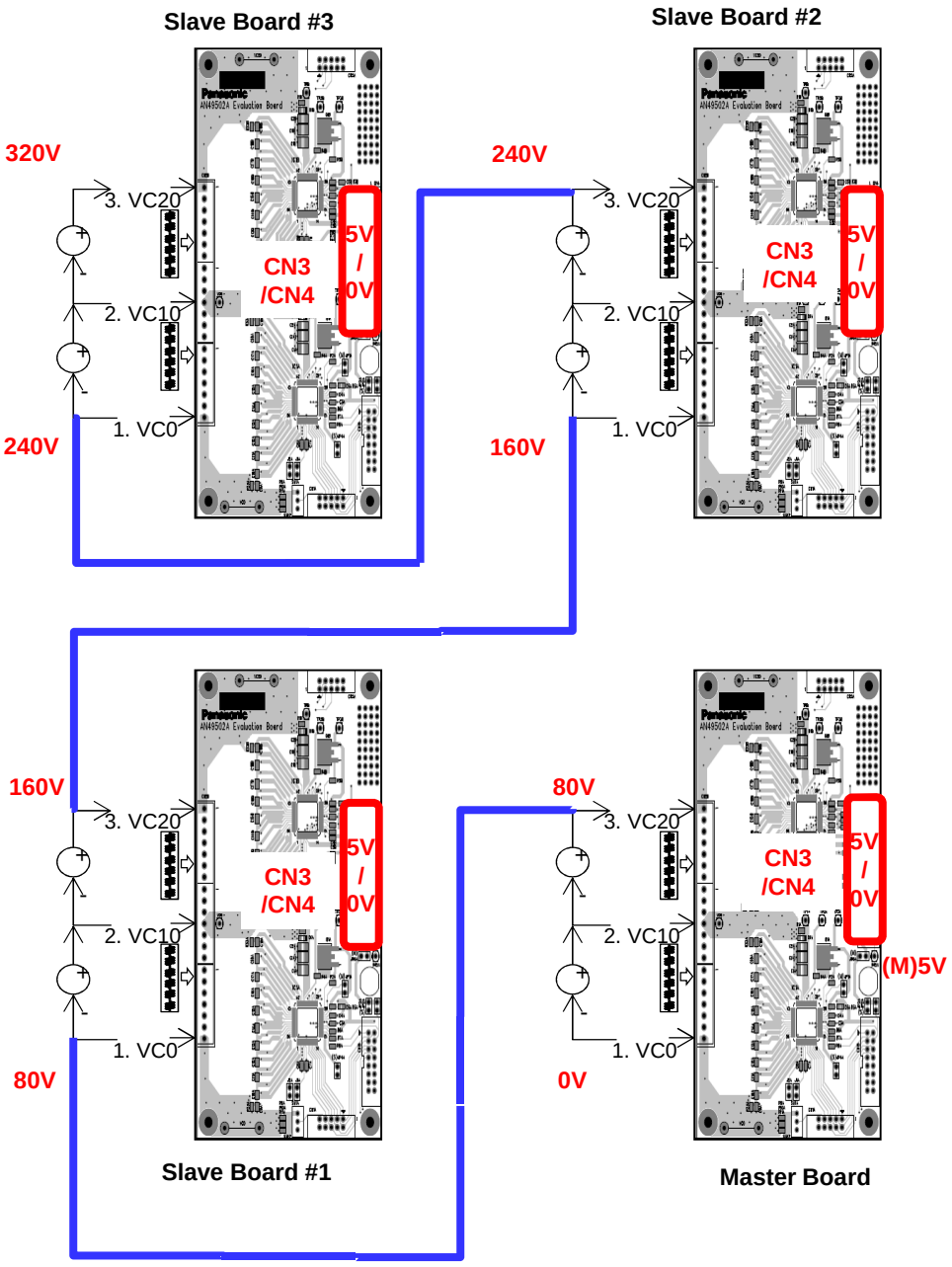


Figure 8 Example for 4 boards evaluation connection –
(ii) Power - the voltage is assumed to be 40V/ICs

4.2.4 Connecting multiple EVBs - example

One example of connecting 4 EVBs for evaluation is given as follow. The EVBs are stacked in the order from Master board(top) to Slave Board #3 (bottom). The Master board is placed on top for convenient so that switches can be controlled during evaluation. It may be stacked in other ways as long as it follows the instruction from previous section.

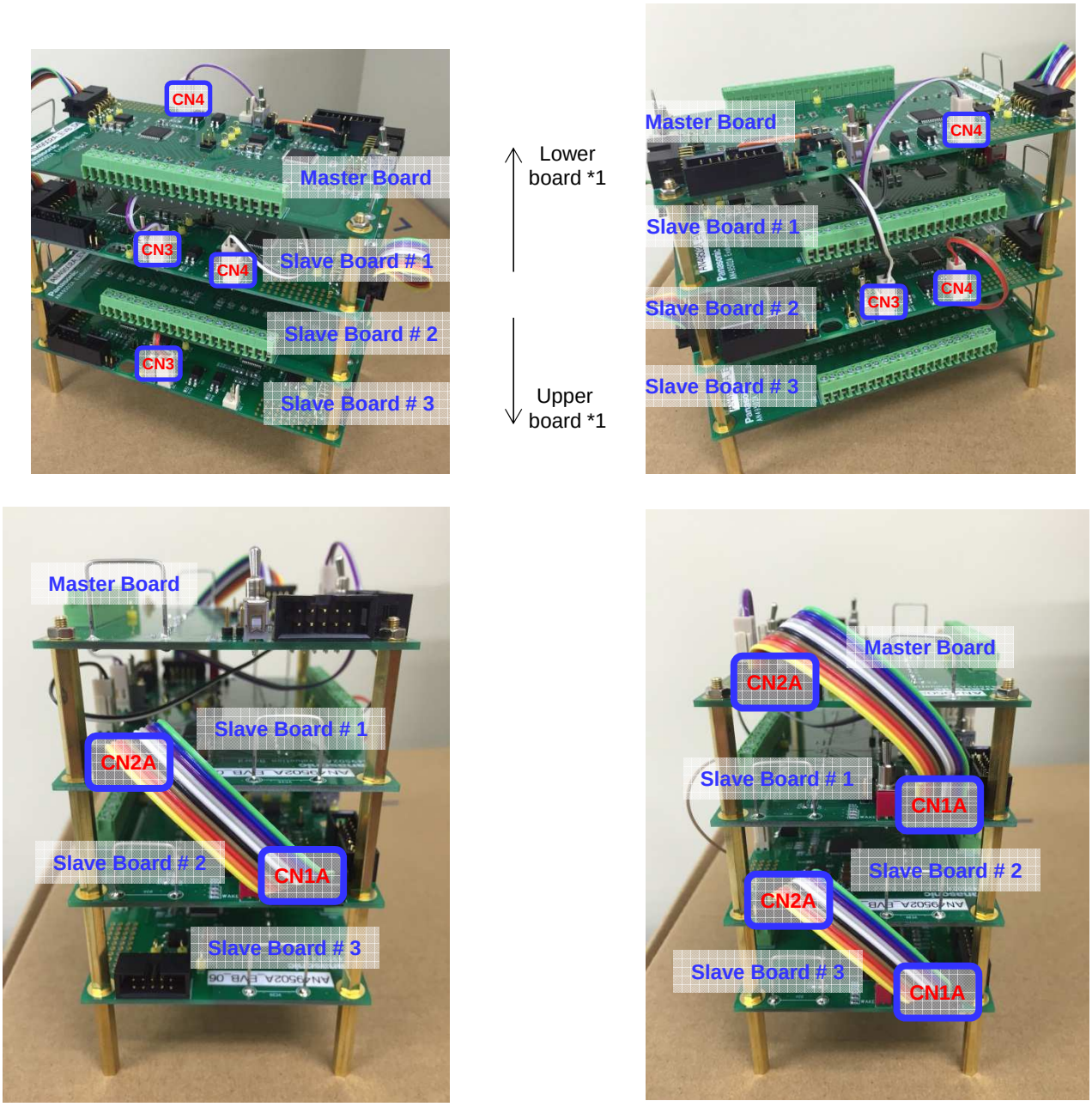


Figure 9 Example for 4 boards evaluation connection
– different angle of view

*1 : The lower board and upper board in a system is defined as in Section 2 depend on the connection instead of physical placement. In this example, the upper board is placed at the bottom instead for convenient of use.

5. Software installation and running

AN49502A using SPI communication protocol for Master IC to host (MCU/PC), user may control the EVB using SPI protocol through CN15 using MCU. For evaluation purpose, Windows software has been provided.

Software installation and verification procedure:

1. Install FTDI D2XX driver
2. Put AN49502A Evaluation Software VerX.xx.exe in the installed directory.
3. Connect USB cable from PC to UM232H board, and communication cable from UM232H board to EVB.
4. Wait for the LED on UM232H to be turned ON, and run AN49502A Evaluation Software VerX.xx.exe
5. In “Result Log” text box in software display window, it should display “FTDI Device Open OK”. If it display otherwise, check the connection and click “FTDI Device Initialization” button.
6. Refer to software manual for details function of the software.

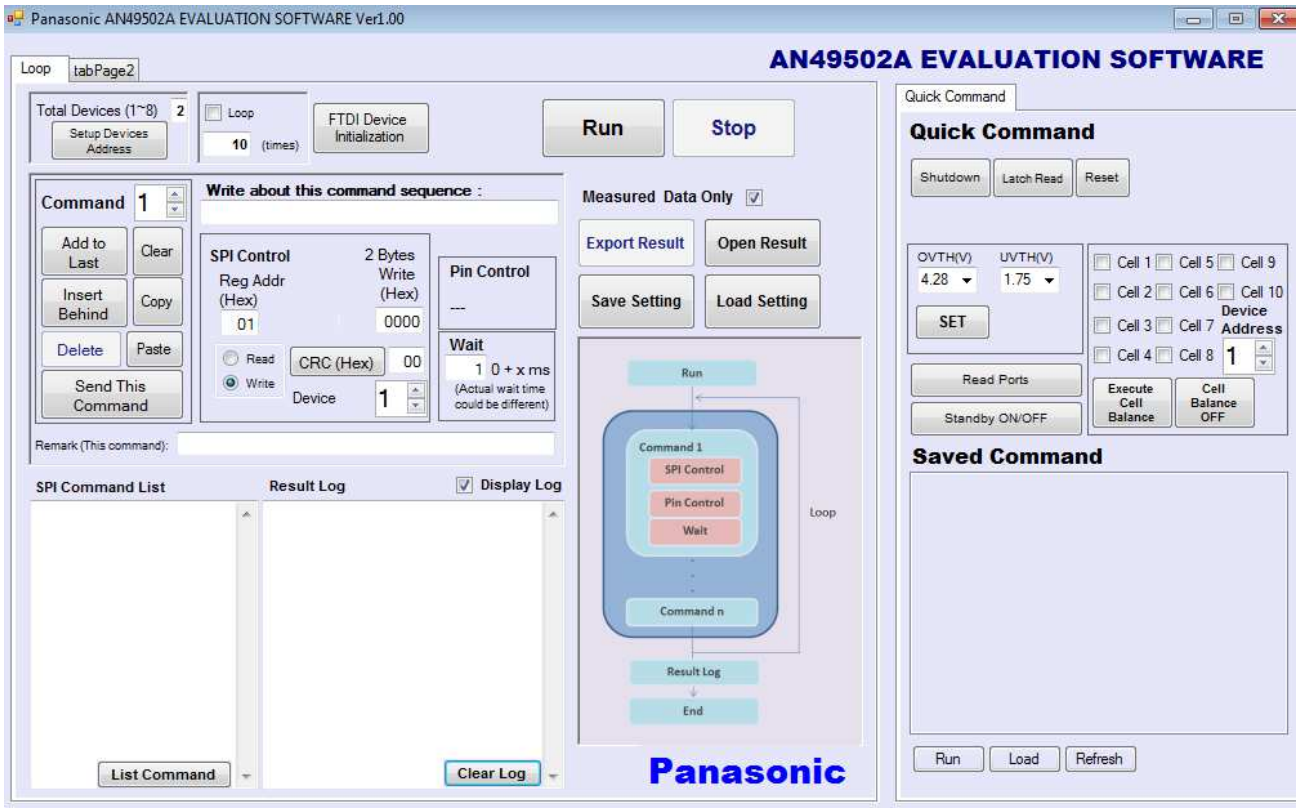


Figure 10 AN49502A Evaluation Software Display Screen

6. Start evaluation and using the software

To start evaluation, follow the procedure

1. Connect EVB(s) following the instruction from previous chapter
2. Power up the EVB following the instruction from previous chapter
3. Connect UM232H board to PC and EVB, run the software and check if the FTDI Device Open successfully. *1
4. Start evaluating the EVB.

a. wake up the ICs by switching SW1A to Wake Up position, switch to Open position after wake up. (make sure SW2A is not at Shutdown position)

	Description
SW1A	Wake up Lower : Wake Up Upper : Open (switch to Open position after wake up)
SW2A	Shutdown Left : Shutdown Center : Open Right : GND (switch to GND position after shutdown)

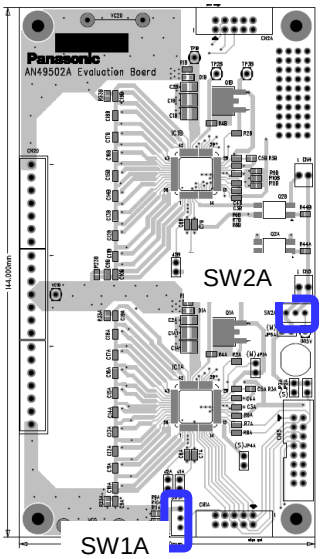


Figure 11 AN49502A EVB Switches

b. after wake up, setup devices address by input 1~8 to Total Devices textbox and click “Setup Devices Address” button. Eg. When two boards are used together, a number of 4 (ICs) should be inputted.

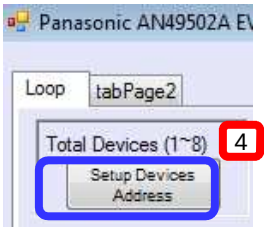
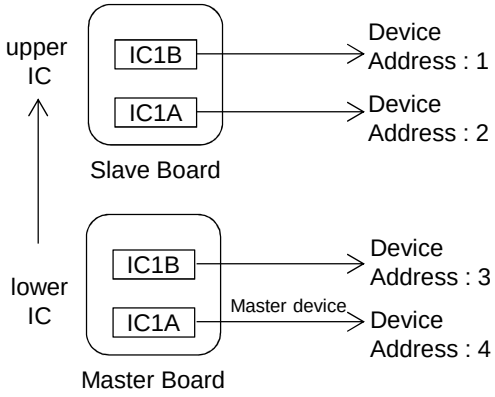


Figure 12 AN49502A evaluation software Setup devices address screen



The device address will be assigned as:

1. Master IC will be assigned the device address inputted, ie. 4
2. The device address of subsequent upper ICs will be decremented by 1

*1 : The AN49502A EVB is in Standby mode by default during power up, it will enter Active mode after the software first run or “FTDI Device Initialization” button click.

7. EVB BOM List

No.	Reference	Size	Value	Rating	Maker	Description
1	CN20				Phoenix Contact	Fixed Terminal Blocks PT 1.5/7-3.5H 7POS HRZ 3.5mm SCREW
2	CN3-4					2 ways header (Thru Hole Vertical)
3	IC1A IC1B	TQFP056-P-1010			Panasonic	AN49502A
4	SW1A	DIP				2stateSW
5	SW2A	DIP				2stateSW_(with_Mid-point)
5	C10A C10B C11A C11B C12A C12B C13A C13B C14A C14B C15A C15B C16A C16B C17A C17B C18A C18B C19A C19B C9A C9B	JIS1608[EIA0603]	2.2uF	25V	MURATA	GRM188C71E225KE11
6	C4A C4B	JIS1608[EIA0603]	1uF	10V	MURATA	GRM188R71C105KE15#
7	C3A C3B	JIS1608[EIA0603]	0.01uF	25V	MURATA	GRM188R71E103JA01#
8	C6A C6B C7A C7B C8A C8B	JIS1608[EIA0603]	0.1uF	25V	MURATA	GRM188R71E104JA01#
9	C21A C21B C22A C22B C23A C23B C24A C24B C25A C25B C26A C26B C27A C27B C28A C28B C29A C29B C20A C20B	JIS1608[EIA0603]	0.22uF	25V	MURATA	GRM188R71E224JA88#
10	C5A C5B	JIS1608[EIA0603]	10uF	25V	MURATA	GRM21BC71E106KE11
11	C2A C2B	JIS3216[EIA1206]	2.2uF	100V	MURATA	GRM31CR72A225KA73#
12	C1A C1A1 C1B C1B1	JIS3225[EIA1210]	4.7uF	80V	MURATA	GRM32ER71K475KE14#
13	D1A D1B	SSMini2-F5-B			Panasonic	DA2S10100L
14	ZD10A ZD10B ZD1A ZD1B ZD2A ZD2B ZD3A ZD3B ZD4A ZD4B ZD5A ZD5B ZD6A ZD6B ZD7A ZD7B ZD8A ZD8B ZD9A ZD9B	SMini2-F5-B	200 mW 20 Ohms	6.8V	Panasonic	DZ2J068
15	AGND_A VBAT_B	DIP			Metallic Wire	GND_Wire/45mm=(W=15mm)+(H=15mm)x2
16	Q2A Q2B	PDIP-4 Gull Wing	50mA	1.4V	Avago	HCPL-817-300E

7. EVB BOM List

No.	Reference	Size	Value	Rating	Maker	Description
17	J1A J1B J2A J2B JP1A JP2A JP3A JP4A JP6A					
18	TP1A TP1B TP2A TP2B TP3A TP3B TP4A VC10	DIP			MAC8	TestPin(Large_r=0.4mm)
19	Q10A Q10B Q11A Q11B Q12A Q12B Q13A Q13B Q4A Q4B Q5A Q5B Q6A Q6B Q7A Q7B Q8A Q8B Q9A Q9B	SMini3-G1-B			Panasonic	MTM232270LBF
20	R10A R10B R11A R11B R7A R7B R8A R8B R9A R9B R4A R4B	JIS1608[EIA0603]	R=0	0.1W	Panasonic	ERJ3GEY0R00V
21	R2A R2B R19A R19B R20A R20B	JIS1608[EIA0603]	R=10K	0.1W	Panasonic	ERJ3GEYJ103V
22	R15A R15B R16A R16B R17A R17B R18A R18B R12A R12B R13A R13B R14A R14B	JIS1608[EIA0603]	R=1.5K	0.1W	Panasonic	ERJ3GEYJ152V
23	R3A R3B	JIS1608[EIA0603]	R=1	0.1W	Panasonic	ERJ3GEYJ1R0V
24	R6A R6B	JIS1608[EIA0603]	R=470	0.1W	Panasonic	ERJ3GEYJ471V
25	R5A R5B	JIS1608[EIA0603]	R=510K	0.1W	Panasonic	ERJ3GEYJ514V
26	R1A R1B	JIS1608[EIA0603]	R=1K	0.2W	Panasonic	ERJP03F1001V
27	R23A R23B R24A R24B R25A R25B R26A R26B R27A R27B R28A R28B R29A R29B R30A R30B R31A R31B R32A R32B R33A R33B	JIS1608[EIA0603]	R=4.7K	0.2W	Panasonic	ERJP03F4701V
28	R44A R44B	JIS1608[EIA0603]	R=330	>1W	Panasonic	ERJ3GEYJ331V
29	R34A R34B R35A R35B R36A R36B R37A R37B R38A R38B R39A R39B R40A R40B R41A R41B R42A R42B R43A R43B	JIS2550[EIA1020]	R=43	1W	Panasonic	ERJB1AF430U
30	Q1A Q1B	TO-252/ SOT 428	5A	100V	ROHM	RSD050N10TL
31			9A		ADVANCED POWER ELECTRONICS	AP18T10AGH-HF-3TR
32	CN1A CN2A					10 way header (Thru Hole right angle)
	CN15					16 ways header (Thru Hole Vertical)
33	R21A R21B	JIS1608[EIA0603]	R=5K	0.0W	Panasonic	ERJ3EKF5101V
34	ZZ9-12	r=3.2mm			MAC8	SQ-XX_(L=XXmm_r=3.2mm_M3)_MetalicHexagonSpacer

8. PCB Layout Pattern

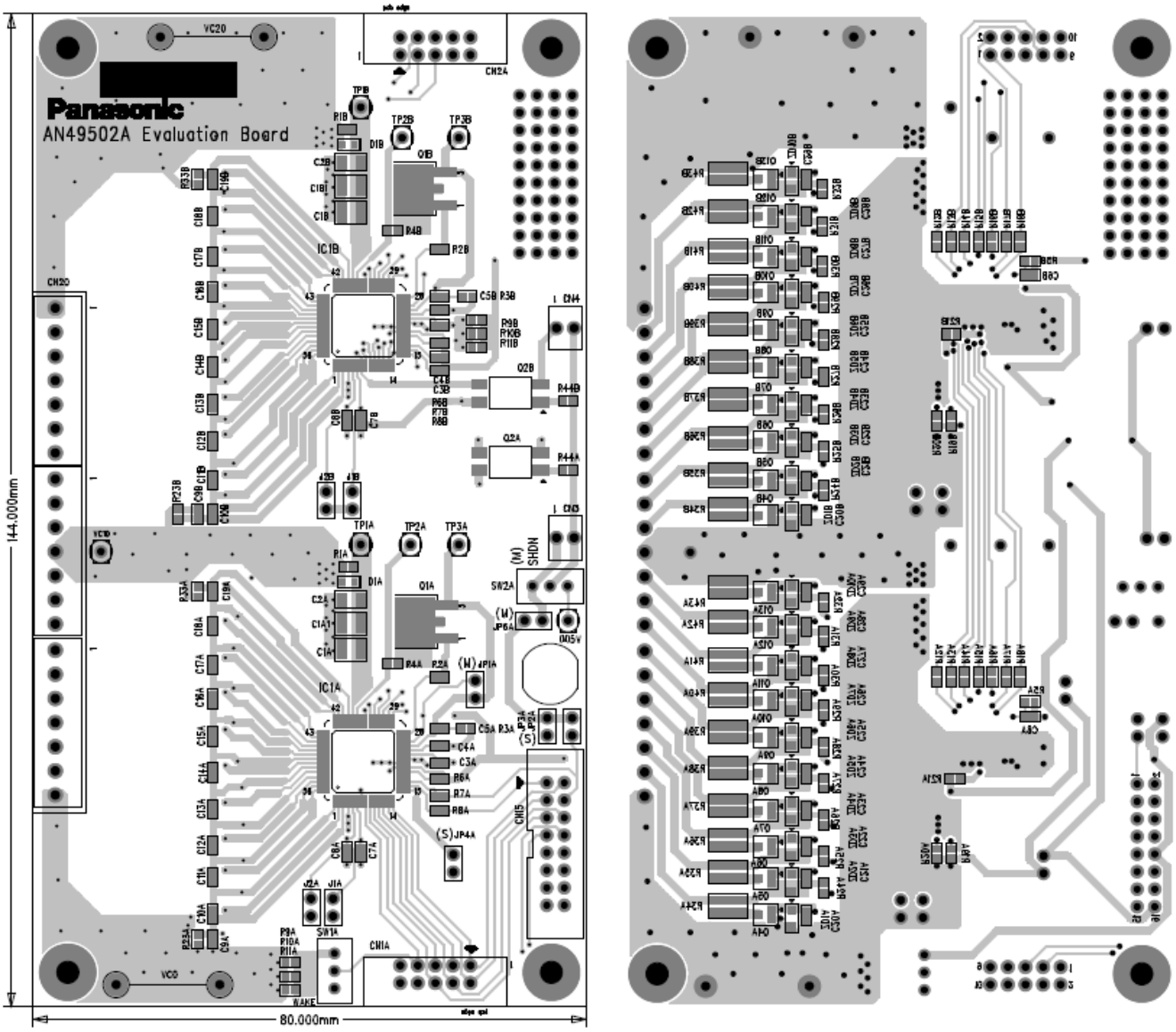
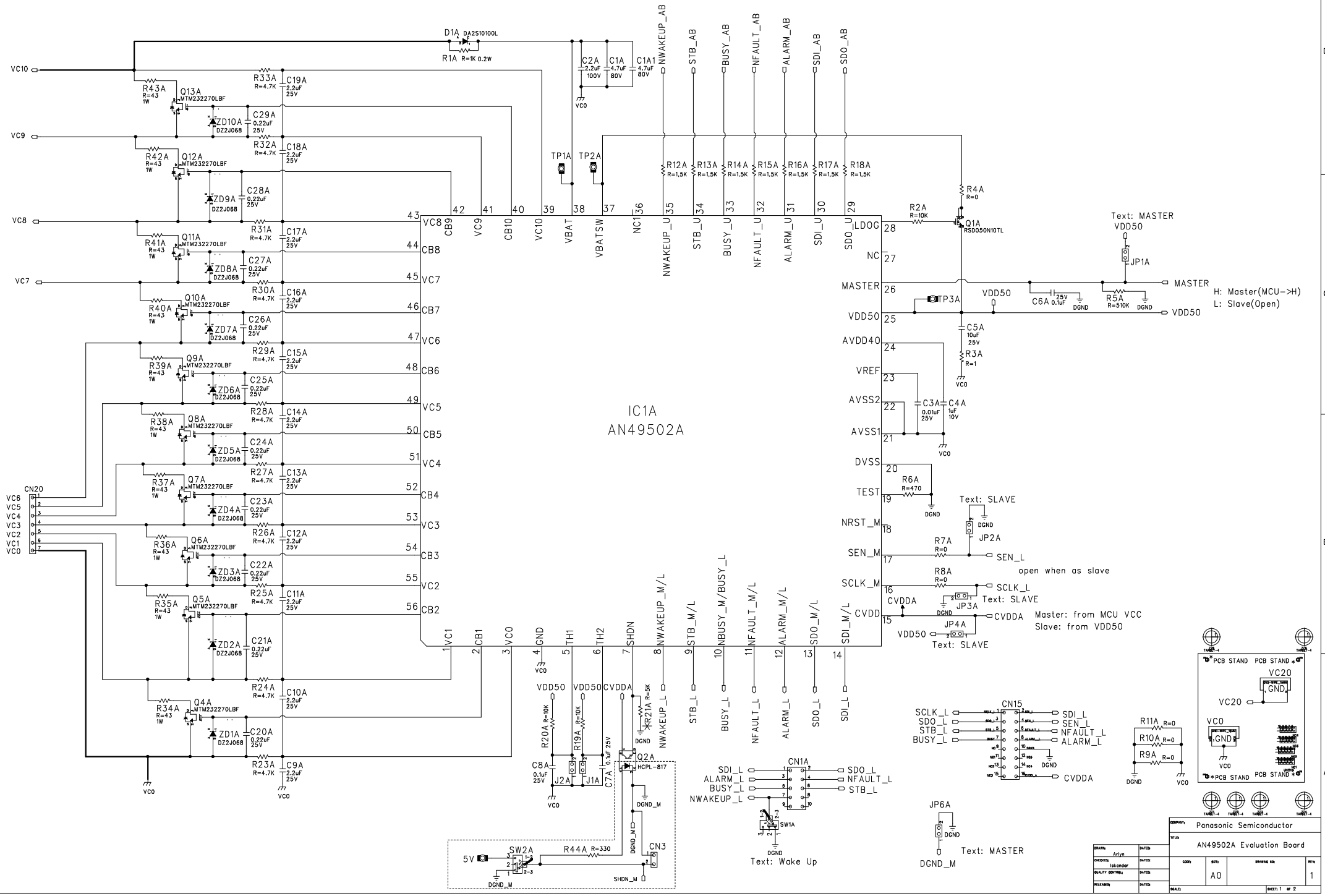
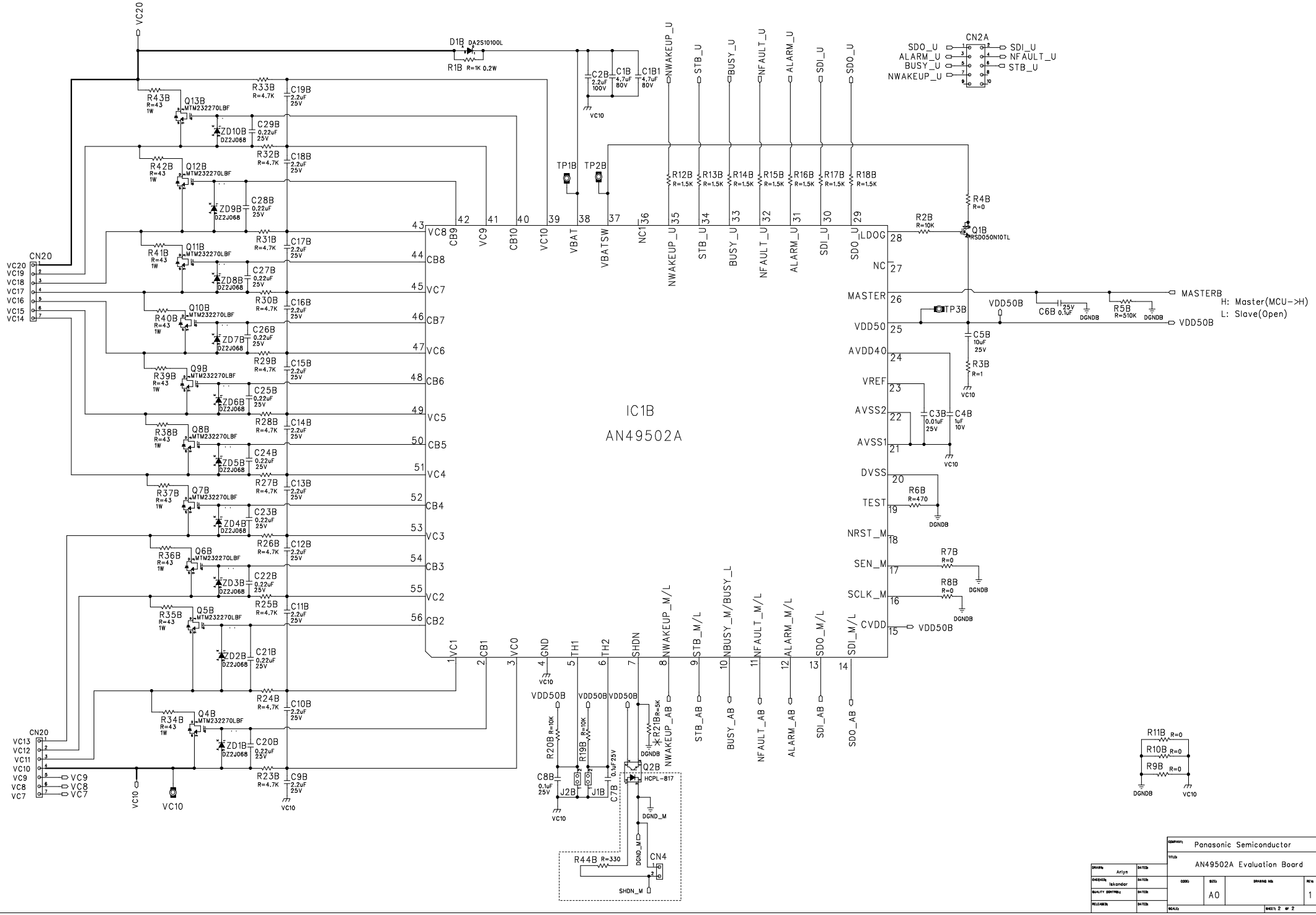


Figure 13 AN49502A EVB PCB Layout Pattern
(i) Top view (ii) Bottom view

AN49502A Evaluation Board [Ver 1.00]




IC1B
AN49502A
CN20
CN2A
CN4
D1B DA2S10100L
R1B R=1K 0.2W
Q1B RSD050N10TL
TP1B
TP2B
TP3B
MASTERB
H: Master(MCU->H)
L: Slave(Open)
VDD50B
DGNDB
DGND_M
SHDN_M
HCPL-817
SDO_U
ALARM_U
BUSY_U
NWAKEUP_U
SDI_U
NFAULT_U
STB_U
Panasonic Semiconductor
AN49502A Evaluation Board
Arlyn
Iskandar
A0
1
SHEET: 2 of 2

Appendix – A. Configuring UM232H SPI interface module and interfacing with AN49502A EVB

The UM232H module and 16 ways cable received with the evaluation kit has been configured for AN49502A EVB and can be used without extra configuration. However, user may obtain a UM232H module from other sources and require some configuration before using with AN49502A EVB. The required steps are :

(i) The UM232H SPI interface module is first configured with VIO shorted with 3V3, 5V0 shorted with USB.

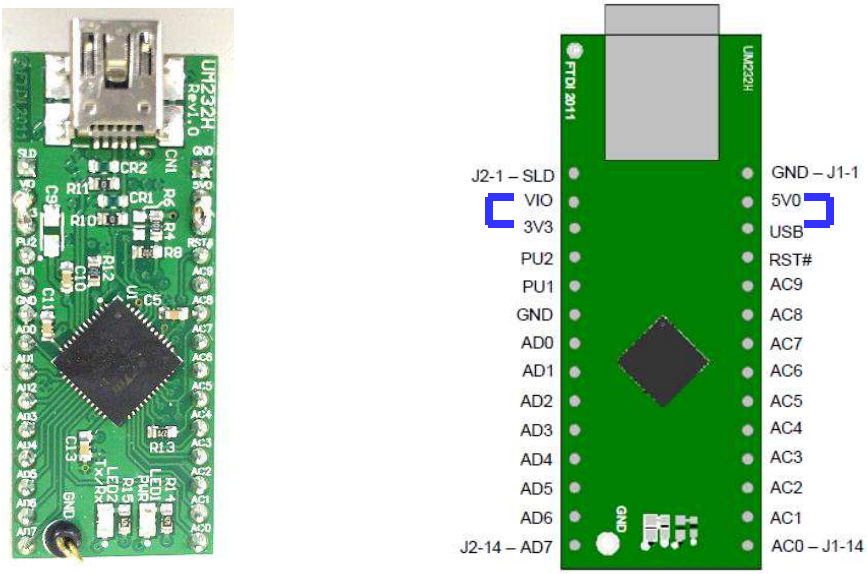


Figure 14 UM232H Module (i) top view and (ii) pin configuration

(ii) Table below shows the interface between UM232H to AN49502A EVB

UM232H Port Name	FTDI Function	AN49502A EVB CN15	CN15 Port Name
J2-1 - SLD	-	-	-
VIO	-	-	-
3V3	3.3V	CN15-16	CVDDA
PU2	-	-	-
PU1	-	-	-
GND	GND	CN15-8	DGND
AD0	SK	CN15-1	SCLK_L
AD1	DO	CN15-2	SDI_L
AD2	DI	CN15-3	SDO_L
AD3	CS	CN15-4	SEN_L
AD4	GPIOL0	CN15-5	STB_L
AD5	GPIOL1	CN15-6	NFAULT_L
AD6	GPIOL2	CN15-7	BUSY_L
J2-14 AD7	GPIOL3	CN15-8	ALARM_L

Appendix – B. Example of configuring AN49502A EVB

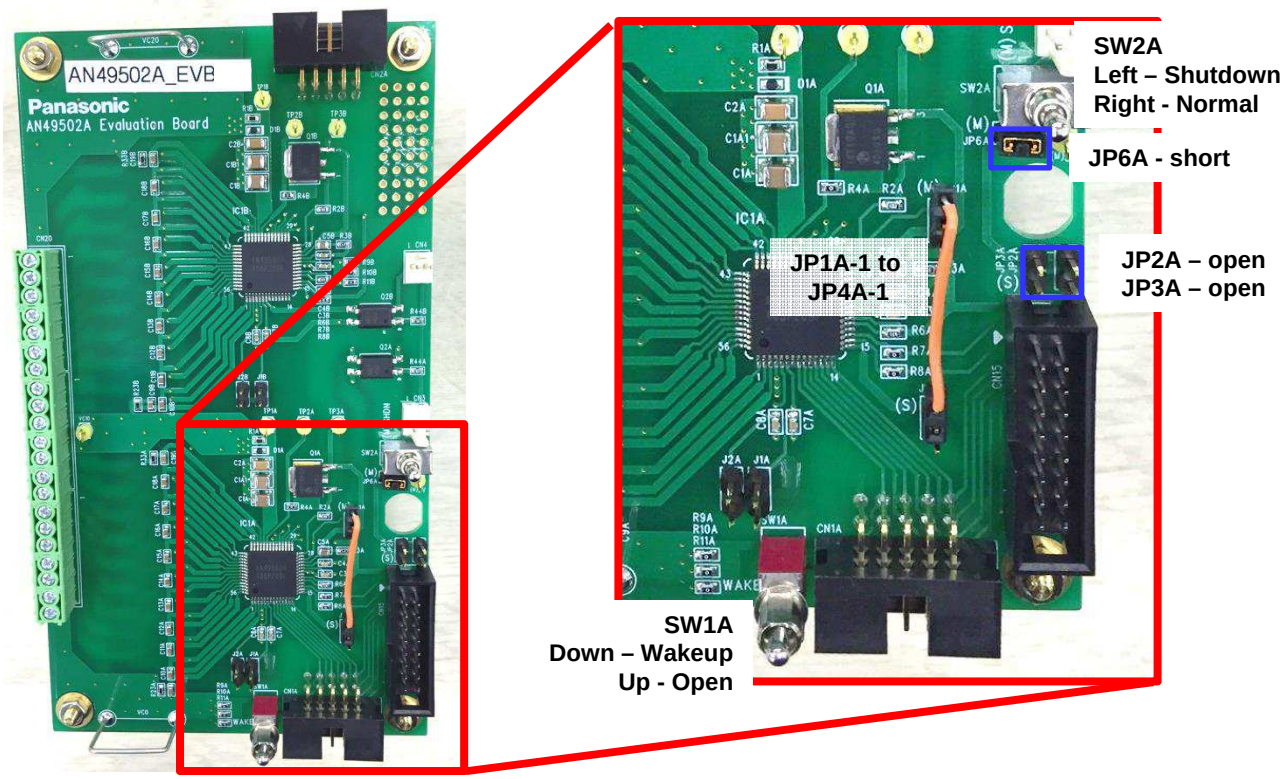


Figure 15 AN49502A EVB Configured as Master board

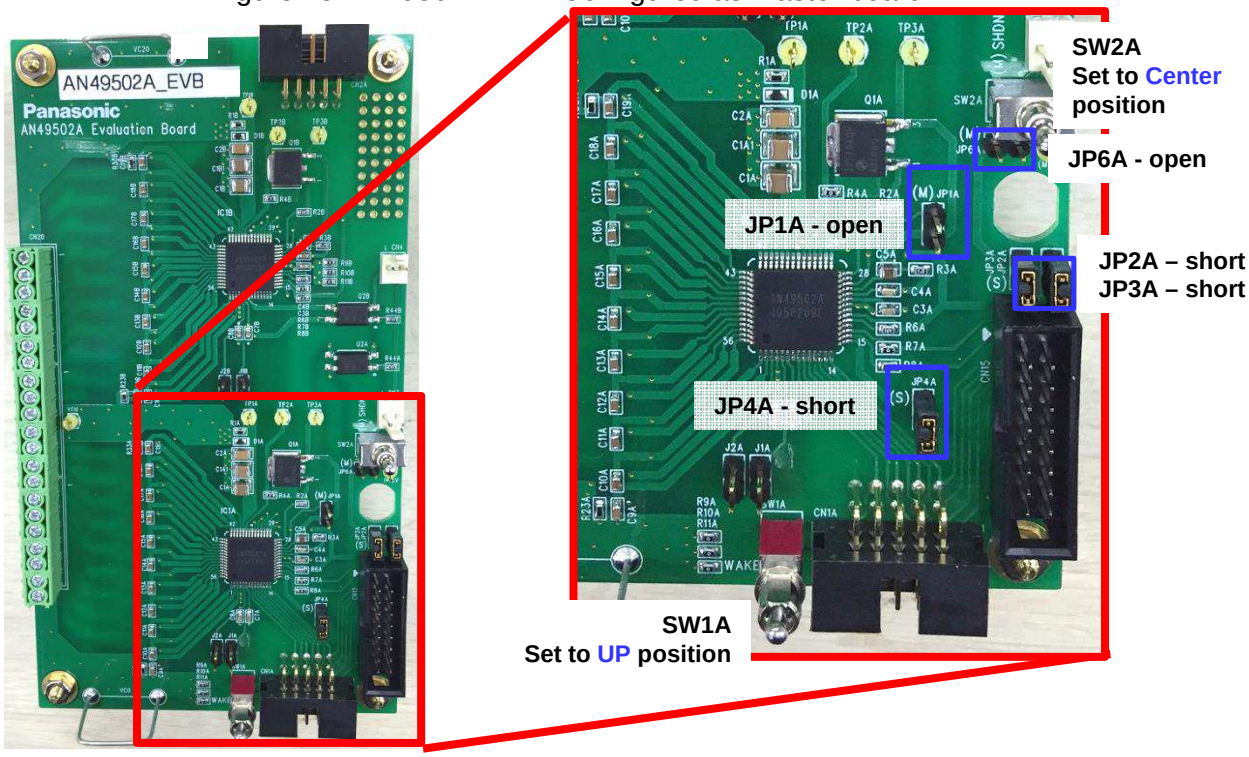


Figure 16 AN49502A EVB Configured as Slave board

Appendix – C. Example of connecting two AN49502A EVBs in stacking

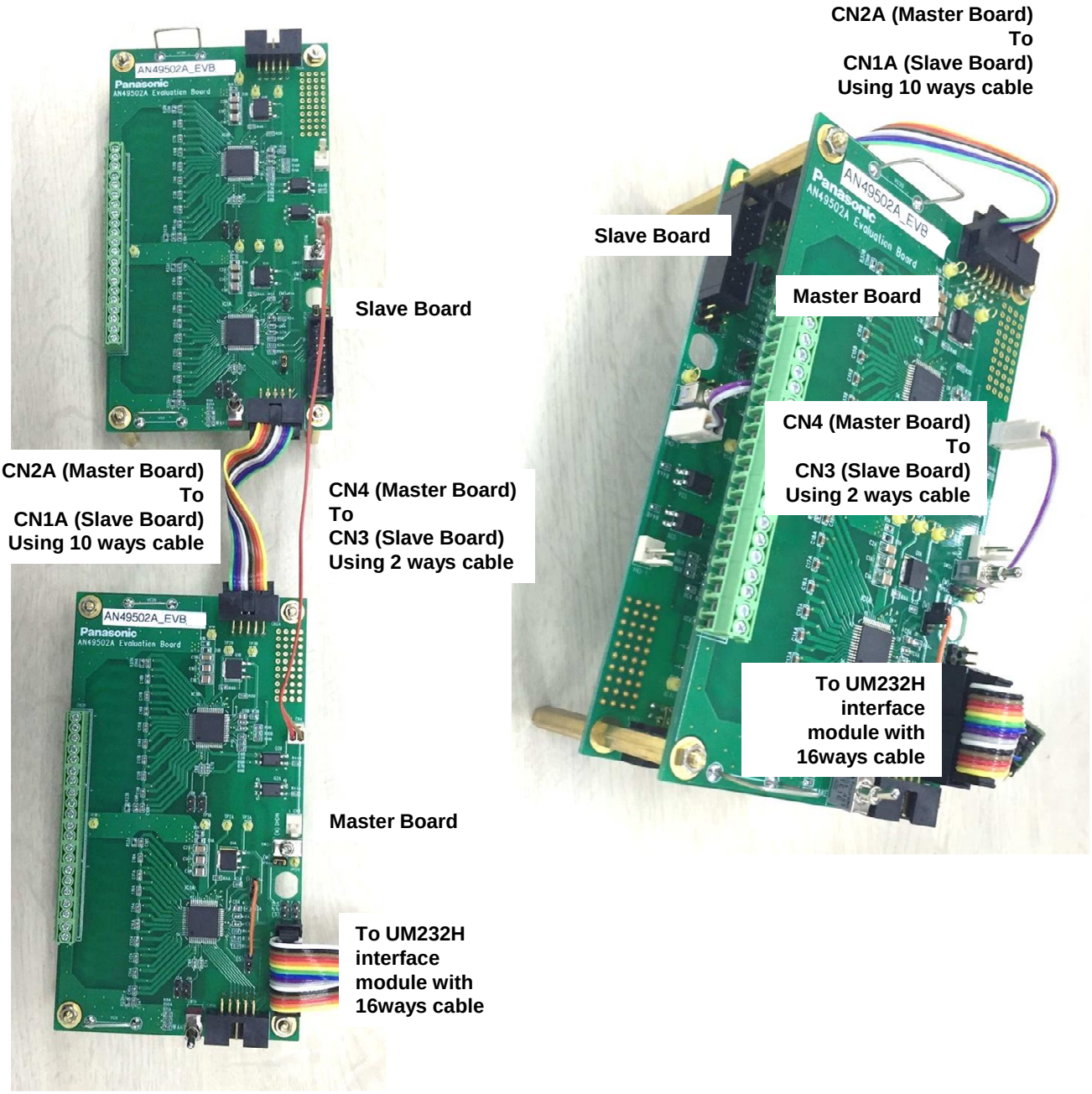


Figure 17 Two AN49502A EVB Connected in Stacking
(i) Two boards laying on same plane and (ii) Two boards stacked together (Master board on top)

Appendix – D. Connecting Power Supply in Stacking Evaluation

When evaluating AN49502A EVB with power supply unit and resistor divider, it is important that the power supply COM is to be floating, i.e it should not be connect to GND of the power supply.

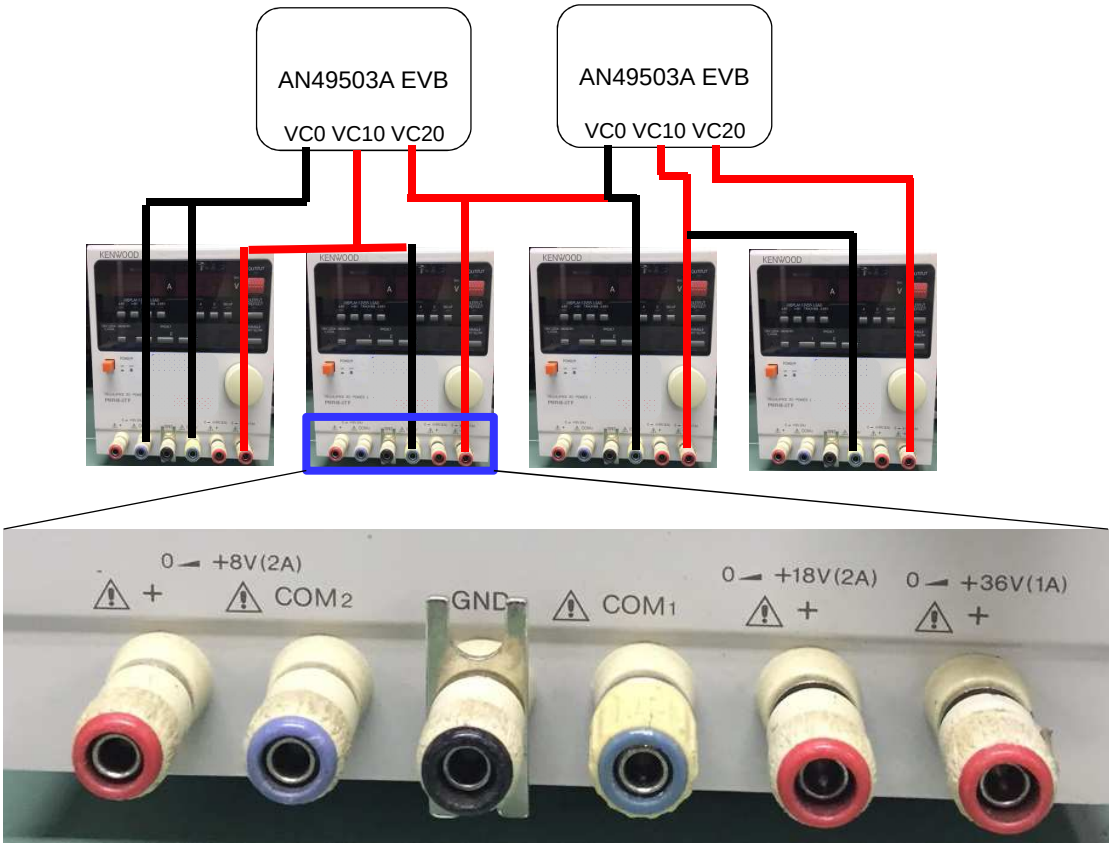


Figure 18 Example of connecting power supply for two AN49502A EVB