Term Project: Integrated Circuit Package Recognition using Deep Learning

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Abstract

This paper presents an approach to recognize integrated circuit packages using deep learning. The proposed approach is based on a convolutional neural network (CNN) that is trained on a dataset of integrated circuit package images. The model achieved an accuracy of 0.950 on the test set, indicating good generalization performance. The model can be further improved by collecting more data, using more advanced CNN architectures, and fine-tuning the model on real-world data.

Keywords: Deep learning, Convolutional neural network (CNN), ResNet, IC package recognition, Computer vision

1. Introduction

Beginner electronics engineers often struggle with selecting the correct footprint for an integrated circuit (IC) package. The footprint is the physical layout of the pads on a printed circuit board (PCB) that the IC package will be soldered to. Each package type has a certain procedure for installation and soldering on automatic Pick-and-Place machines, which have a limited number of nozzles and can only handle a certain package type. Incorrectly selected footprint on the PCB can lead to damage to the IC, the PCB, or the Pick-and-Place machine.

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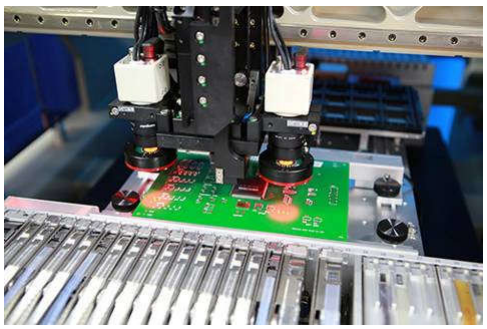


Figure 1: Pick-and-Place machine [1]

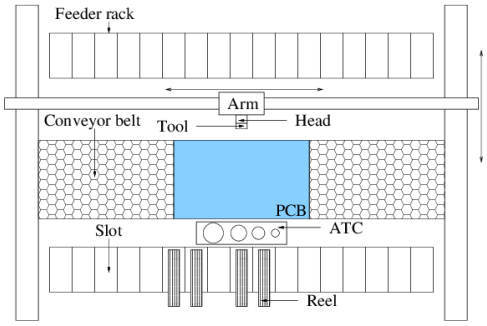


Figure 2: Pick-and-Place machine diagram [2]

1.1. Motivation and relevant works

The article «Hand-drawn electronic component recognition using deep learning algorithm» (Wang et al.) [3] describes a similar project. The authors use a convolutional neural network (CNN) to recognize hand-drawn electronic components.

Another research, «Integrated Circuit Packaging Recognition with Tilt Auto Adjustment using Deep Learning Approach» (Loh et al.) [4], uses YOLOv5 to detect and classify IC packages. The authors focus on IC detection on the PCB, i.e. after installation. It operates on images of the PCB, not individual IC packages.

The research «Text Recognition in PCBs: an object character recognition algorithm» (Nájera et al.) [1] describes approaches currently used in the industry to recognize objects on PCBs. The authors use a computer vision setup on the Pick-and-Place machine head to recognize text on the PCB.

1.2. Contribution and scope

Mentioned researches are similar to the proposed one, but they are not directly applicable. The proposed project is focused on recognizing individual IC packages before soldering, potentially in real-time. It can then be expanded to recognize other components, such as resistors, capacitors, and inductors.

The ability to recognize ICs on the fly can significantly reduce the possibility of damage to the expensive Pick-and-Place machines and the PCBs, serving as an extra protection measure. The

resulting model can be used in a computer vision setup on the feed line («Reel» on Figure 2) of the Pick-and-Place machine, in addition to the existing sensors.

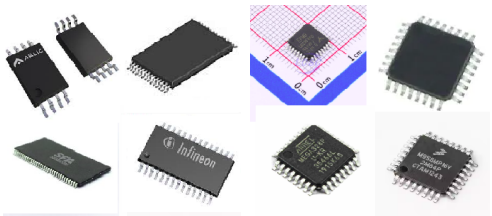
2. Datasets

A dataset of IC packages is collected from the supplier websites, mainly Digi-Key, and Mouser. The dataset contains images of IC packages in various resolutions and aspect ratios. The dataset is divided into four classes: SOP, QFP, SOIC, and DIP. Each class contains at least 175 images. Augmentation is performed during dataset loading and includes grayscale conversion, contrast/sharpness adjustments, and random flipping. The images are scaled and cropped to a fixed size of 128x128 pixels for better performance.

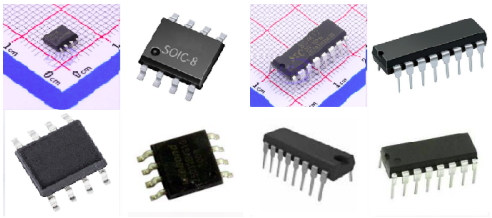
Figure 3 shows examples of IC packages from the dataset. Table 1 lists the packages and their corresponding labels.

Package	Example	Label
SOP		chip-sop
QFP		chip-qfp
SOIC		chip-soic
DIP		chip-dip

Table 1: Integrated circuit packages



(a) SOP (b) QFP



(c) SOIC (d) DIP

Figure 3: Integrated circuit packages from the dataset

The dataset is split into training and validation sets with a 5/1 ratio. The training set contains 480 images, and the validation set contains 120 images. The dataset is balanced, with 175 images in each class. A separate test set of 20 images is used to evaluate the model's performance.

Data collection and initial classification were performed manually by the author.

3. Methodology

Training was performed in two stages: initial testing and hyperparameter tuning. For the first stage, a ResNet18 CNN is used for IC package classification. Three approaches were tested: training the model from scratch, fine-tuning a pre-trained model, and using a pre-trained model as a feature extractor. The model is trained using the SGD optimizer with a batch size of 4. Cross entropy loss is used as the loss function. The model was trained for 50 epochs.

For the second stage, hyperparameter tuning was performed manually. The learning rate, weight decay, and number of epochs were varied. The best model was selected based on the validation accuracy.

Finally, confusion matrix, accuracy, precision, recall, and F1 score were calculated for the validation dataset. The model was evaluated on the test dataset to assess its generalization performance.

4. Results

The first stage results are shown in Table 2. The best model was obtained by **fine-tuning a pre-trained model**. The model achieved an accuracy of 0.876 on the validation set. Severe overfitting was observed for the other two approaches, indicating issues with the dataset. Figure 4 shows one of the training runs.

Approach	**LR**	**Weight decay**	**Epochs**	**Validation Acc**
Scratch	0.001	0.01	50	0.817
Fine-tuning	0.001	0.01	50	0.876
Feature extractor	0.001	0.01	50	0.800

Table 2: Results for the first stage

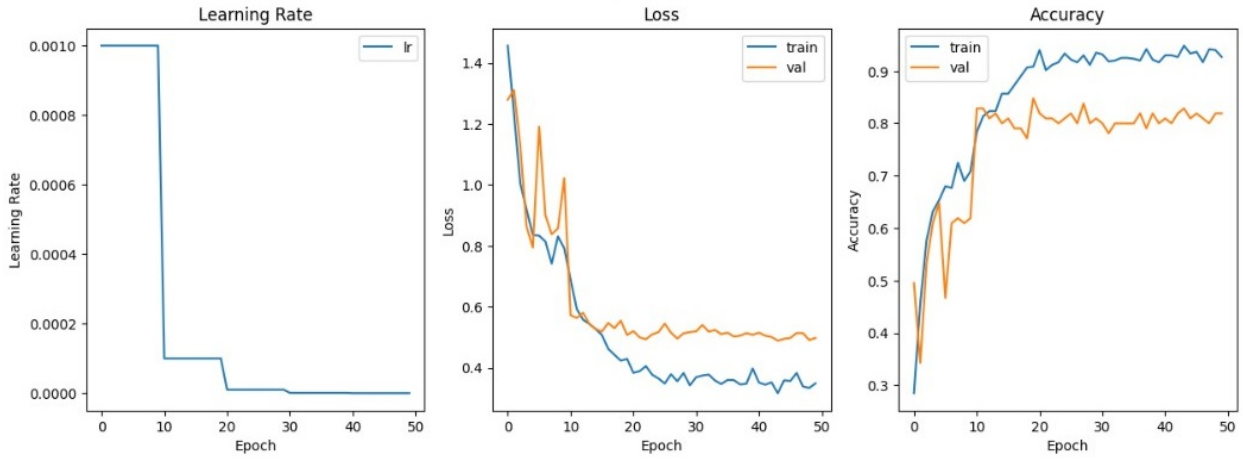


Figure 4: Training history for the From Scratch approach

It was observed that there were no improvements in the validation accuracy after 30 epochs. Therefore, the number of epochs was reduced to 30 for the second stage.

Second stage manual optimization results are shown in Table 3. The best model was obtained with a learning rate of 0.001, weight decay of 0.05, and 30 epochs. The model achieved an accuracy of 0.962 on the validation set. Batch size was increased to 8. Figure 5 shows the training history for the best model.

LR	**Weight decay**	**Epochs**	**Validation Acc**
0.001	0.01	30	0.886
0.001	0.05	30	0.962
0.001	0.1	30	0.933

Table 3: Results for the second stage

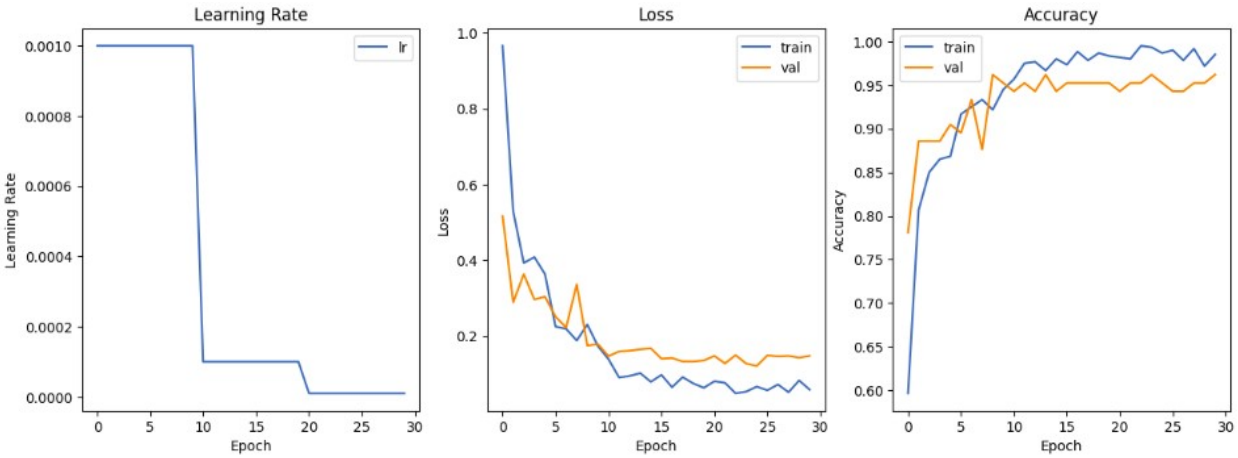
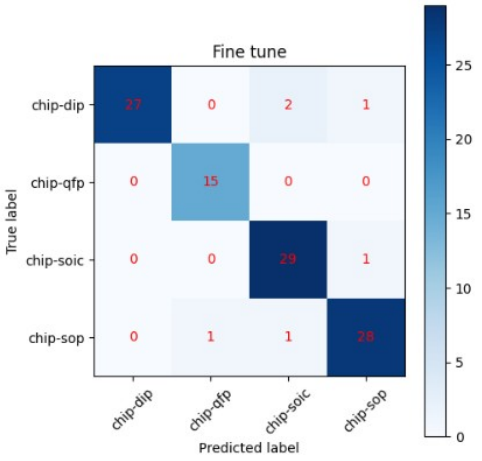


Figure 5: Training history for the best model, fine-tuned/pre-trained

The confusion matrix for the best model is shown in Table 6. Table 4 shows the evaluation metrics for the best model on the validation set.



Class	Recall	Precision	F1 Score
chip-dip	0.900	1.000	0.947
chip-qfp	1.000	0.938	0.968
chip-soic	0.967	0.906	0.935
chip-sop	0.933	0.933	0.933
Accuracy	0.962		

Table 4: Evaluation metrics for the best model

Figure 6: Confusion matrix for the best model

After evaluating the model on the validation set, the model was tested on the test set. The model achieved an accuracy of 0.950 on the test set, indicating good generalization performance. Figure 7 shows the test results. Only one IC package was misclassified, marked in red.

Figure 7: Test results for the best model

4.1. Discussion

During training, multiple issues were observed:

- The dataset was too small, leading to overfitting.
- Dataset collection from supplier websites has limitations, such as fixed resolutions and rotation angles.
- Suppliers tend to re-use images for different packages, leading to incorrect labels. This also reduces the diversity of the dataset.

- Some IC packages, such as SOIC-8 and SOP-8, are visually similar, leading to misclassification. It is challenging to distinguish between them even for an experienced engineer.
- Finally, the model was not tested on real-world data, which have different lighting conditions, angles, and backgrounds.

Considering the limitations, the model achieved good performance on the test set. The model can be further improved by collecting more data, using more advanced CNN architectures, and fine-tuning the model on real-world data.

A possible solution to the dataset limitations is to collect images of IC packages on the Pick-and-Place machine itself. This can be done by setting up a camera on the feed line of the machine and capturing images of IC packages as they pass by. The model can then be re-trained on this data to improve its performance in real-world conditions.

5. Conclusion

The approach to recognize integrated circuit packages using deep learning was presented. The results have shown that ResNet is a suitable architecture for IC package recognition. The best model achieved an accuracy of 0.950 on the test set, indicating good generalization performance. The model can be further improved by using a better dataset and fine-tuning the model on real-world data.

Future work includes evaluating the model in real-world conditions, and measuring the model's performance on other components, such as resistors, capacitors, and inductors. Response time will also be evaluated to determine if the model can be used in real-time applications.

The code for this project is available on GitHub: `https://github.com/thepetrovich/ntu-dl-term-project`.

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References

[1] Yuzo Iano, Daniel Bonello, and Umberto Neto. Text recognition in pcbs: An object character recognition (ocr) algorithm. International Journal of Development Research, 10:1–7, 07 2020.

[2] Abel García Nájera and Carlos Brizuela. Pcb assembly: An efficient genetic algorithm for slot assignment and component pick and place sequence problems. volume 2, pages 1485–1492, 01 2005.

[3] Haiyan Wang, Tianhong Pan, and Mian Ahsan. Hand-drawn electronic component recognition using deep learning algorithm. International Journal of Computer Applications in Technology, 62:13, 01 2020.

[4] Siu Loh, Peh Teh, Sim Jia Jia, Kim Ho Yeap, and Yong Lee. Integrated circuit packaging recognition with tilt auto adjustment using deep learning approach. Journal of Engineering Technology and Applied Physics, 5:79–84, 09 2023.