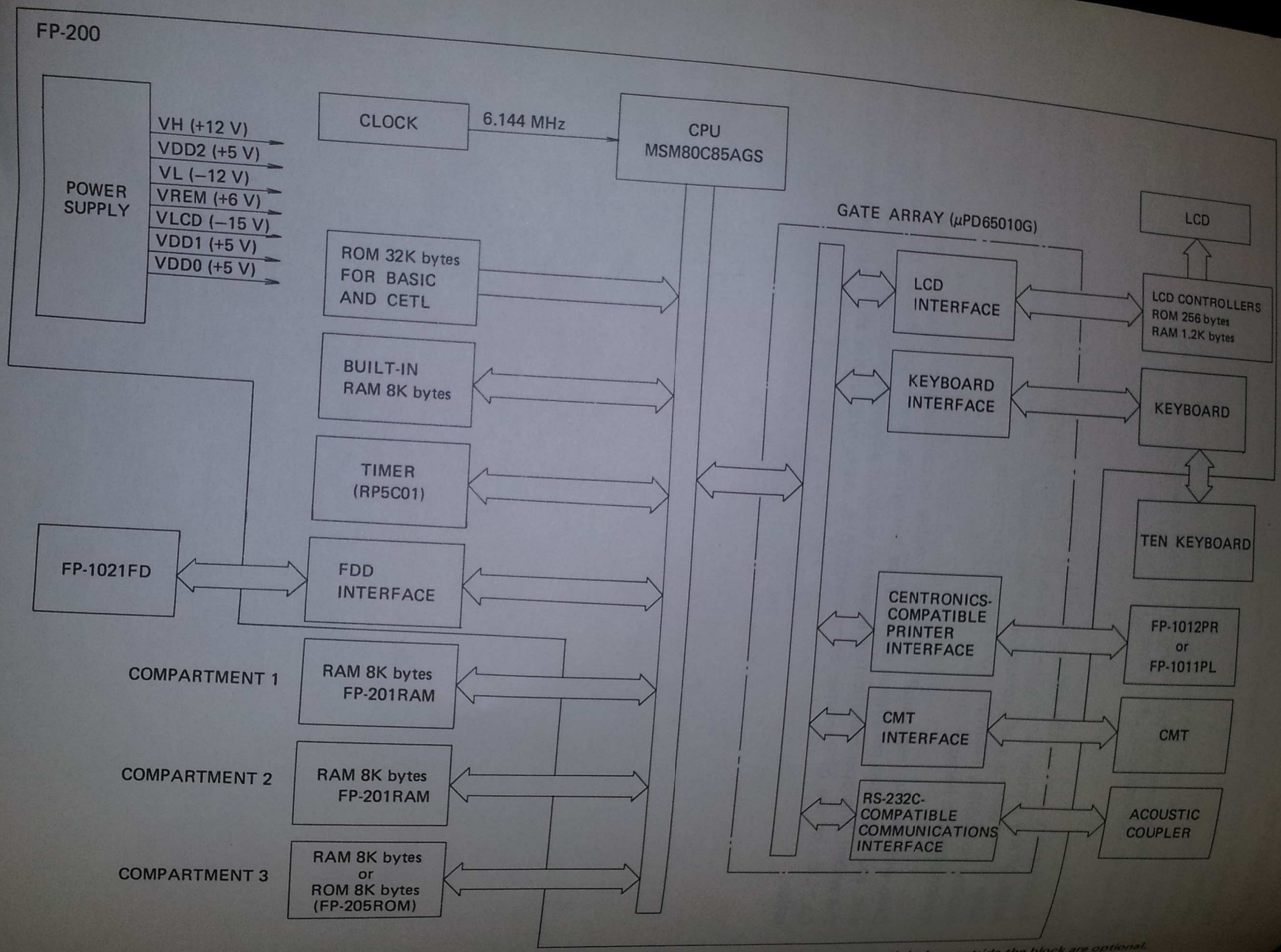
2. SYSTEM BLOCK DIAGRAM



Note: Components, circuits, and devices enclosed by the solid line are provided as standard; components and devices outside the block are optional.

3.

3. SPECIFICATIONS

CPU

- MSM80C85AGS 8-bit microprocessor.
- 6.144 MHz clock frequency.
- Compatible with INTEL8085.
- One wait period (one clock cycle added) for RAM and ROM access.
- Two wait periods (two clock cycles added) for I/O device access.

RAM

- 8K bytes built-in (standard) and can be expanded to 32K bytes.

ROM

- 32K bytes built-in (standard) for BASIC and CETL interpreters.
- Expandable to 40K bytes.

DISPLAY

- Liquid Crystal Display (LCD)
- 1/64 duty cycle
- Adjustable contrast
- Capacity of display

In text mode:	20 characters x 8 lines (160 characters)
In graphics mode:	64 (H) x 160 (W) dots (10,240 dots)
Number of dots per character:	8 x 8 (16 dots)

I/O INTERFACE CONTROLLER

- μPD65010G (GATE ARRAY)
- Kansas City standard for CMT
- Centronics (parallel) standard for printer and mini-plotter.
- RS-232C (serial) standard for I/O port.

INTERFACE

- CMT: Baud rate 300
  Remote control
  Input/output specifications

MIC	Output impedance	5 KΩ
	Output voltage	3 mVp-p
EAR	Input impedance	10 KΩ
	Input voltage	3 – 10 Vp-p
Remote		DC 24 V, 1 A or less

- PRINTER: 8-bit parallel output
  Data transfer via handshaking
- Communication: Compatible with RS-232C standard
  Serial I/O
  Baud rate 300
  Half-duplex transmission

...are provided as standard; components and devices outside the block are optional.

POWER SOURCE

- AD4180 adaptor (+6 V output) for AC-powered operation and use of mini-floppy disk drive FP-1021FD, graphics printer FP-1012PR, mini-plotter FP-1011PL, and RS-232C interface.
- SUM-3 (4 pcs) for DC-powered operation
- SUM-3 (2 pcs) for memory backup
- Battery life expectancy

  Operating battery: 6 hours for SUM-3 or 11 hours for AM-3 (4 batteries)

  Memory backup battery: 6 months for SUM-3 (2 batteries)

OPERATING ENVIRONMENT

- Temperature 0 – 40°C (32 – 104°F)
- Humidity 20 – 85%

DIMENSIONS

- 310 (W) x 220 (D) x 55.5 (H) mm

NET WEIGHT

- 1.54 Kg (3.4 lb)

4. ADDRESS MAPS

4-1. MEMORY MAP

The CPU in the FP-200 hand-held computer has 16 address lines and can address 65,536 bytes (64K) by changing its high-low signal status timesharingly.
As built-in standard memory, the first 32K from 0000H to 7FFFH is allocated to ROM, which contains fixed data and the BASIC and CETL interpreters; the next 8K (8000H to 9FFFH) is RAM used for the system work area, available to BASIC and CETL programs.
Besides this 40K of memory, up to 24K of RAM or up to 16K of RAM and 8K of ROM (a total of 24K of memory) can be added easily by installing optional RAM pack FP-201RAM and ROM pack FP-205ROM in the FP-200's compartments.
The entire memory structure is shown below. Adresses are in hexadecimal.

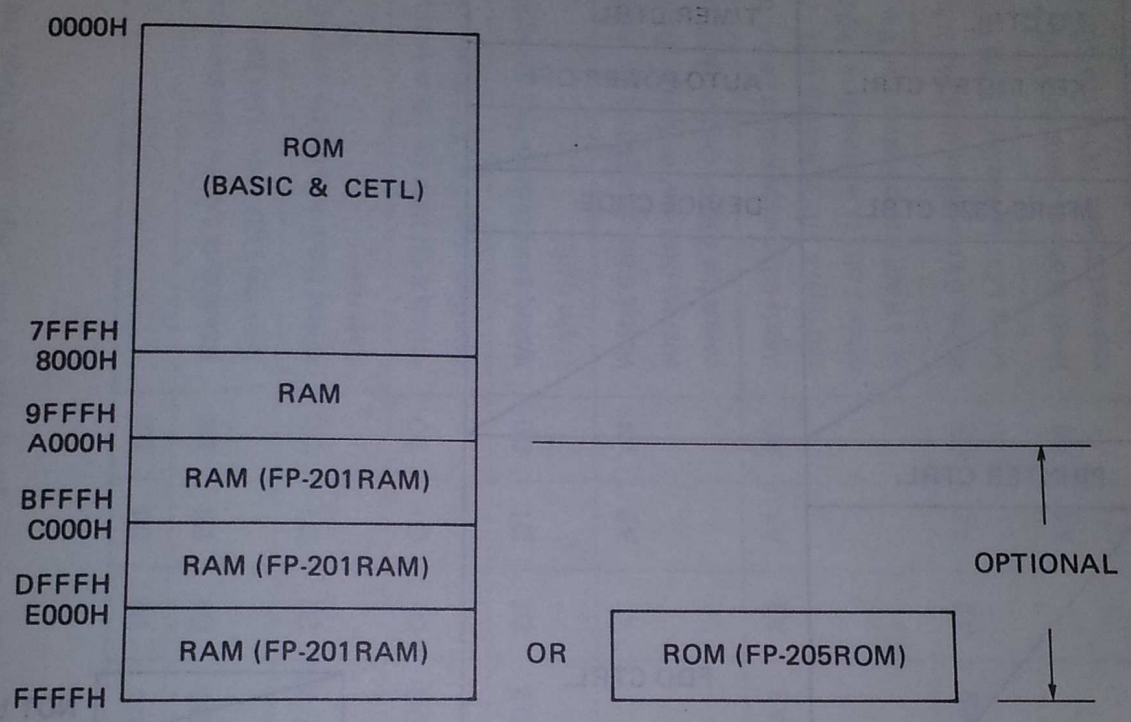
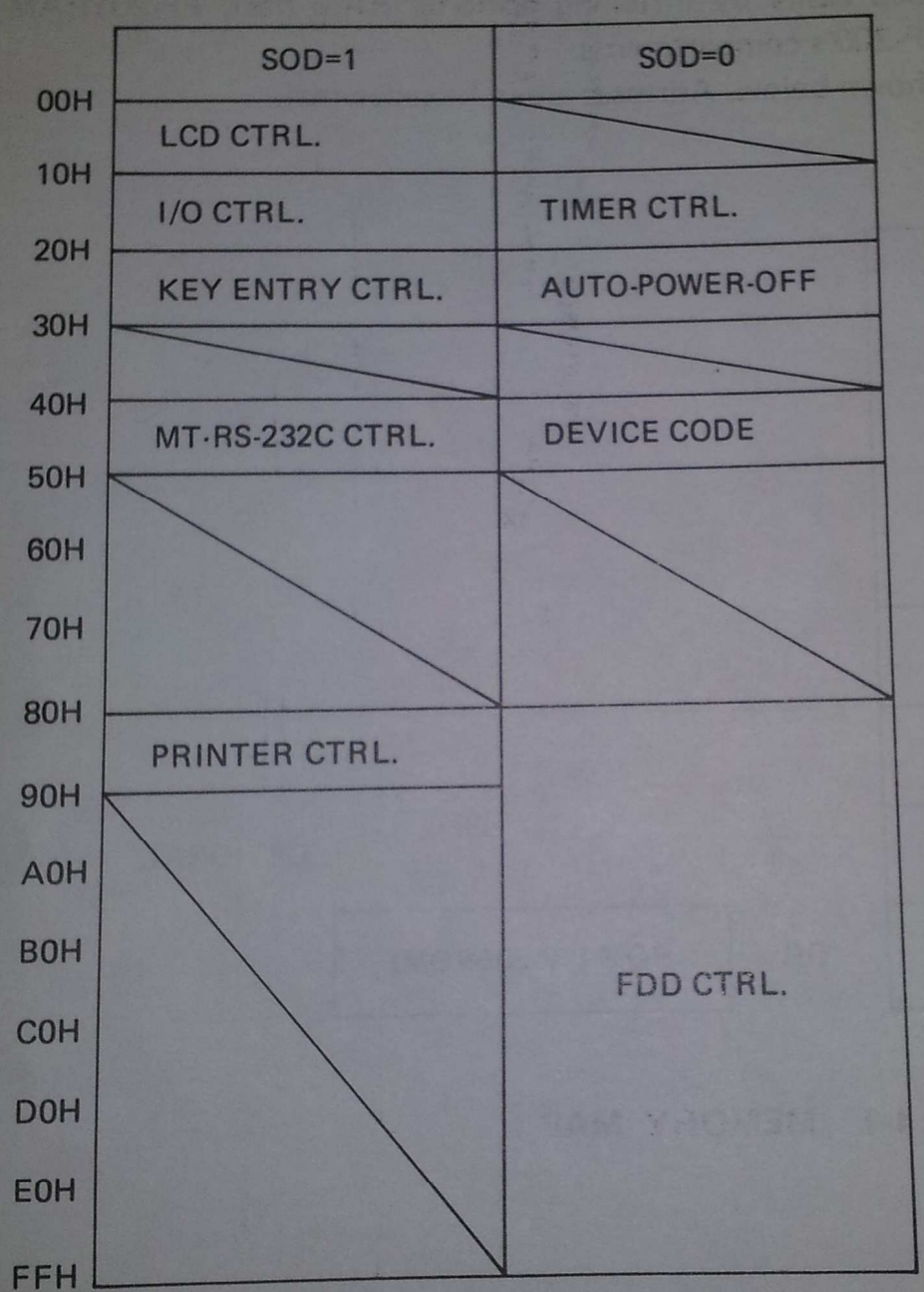


Fig. 4-1 MEMORY MAP

4-2. I/O ADDRESS MAP

To control and access I/O devices in this unit, I/O addresses are allocated as shown below. This I/O address map is two pages by output from the SOD (serial output data) terminal of the CPU by changing its output status bit 1 or 0. This causes the address map to be switched to the other side (left or right) to control access the I/O device functions.
When an I/O device is addressed, the 8 low-address lines (AD0 to AD7) are used, enabling the designation of any of up to 256 addresses for each page.



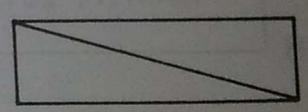


Fig. 4-2 I/O ADDRESS MAP

4-3. DETAILED I/O ADDRESS MAP

On this page, the I/O address explained briefly on the previous page will be explained in detail. It is strongly recommended that the reader fully understand the I/O address map on the last page before going on to this page. Even then, he will find the previous page useful if used as a reference when reading this page.

SOD	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
1	01	R	D7	D6	D5	D4	D3	D2	D1	D0	Reads data for the operation code in the LCD controller's RAM and transfers it to the LCD driver (left half).
1	01	W	D7	D6	D5	D4	D3	D2	D1	D0	Writes 8-bit data for the operation code in the LCD controller's RAM (left half).
1	02	R	D7	D6	D5	D4	D3	D2	D1	D0	Reads 8-bit data for the operation code in the LCD controller's RAM and transfers it to the LCD driver (right half).
1	02	W	D7	D6	D5	D4	D3	D2	D1	D0	Writes 8-bit data for the operation code in the LCD controller's RAM (right half).
1	08	W	S3	S2	S1	S0	–	–	A9	A8	Writes 6-bit data (S0-S3 for the status code and high 2 bits of the 6-bit address data that designates the address allocated in 00-3F for Y) in the LCD controller's RAM (left or right half).
1	09	R	A7	A6	A5	A4	A3	A2	A1	A0	Reads 8-bit address data (low 4 bits of address data (A0-A3)) for the X address and high 4 bits of address data (A4-A7) which reforms 6-bit address data with other 2 bits of address data (A8-A9) for the Y address) in the LCD controller's RAM and transfers it to the LCD driver (left or right half).
1	09	W	A7	A6	A5	A4	A3	A2	A1	A0	Writes 8-bit address data (A0-A3) for X and (A4-A7) for part of the Y address in the LCD controller's RAM (left or right half).
1	08	R	S3	S2	S1	S0	–	–	A9	A8	Reads 6 bits of status data and Y address data (written by the operation at address 08) and "W" in the LCD controller's RAM and transfers it to the LCD driver (left or right half).
1	10	R	–	–	–	–	–	E	–	R	If D0 is 0 "READY" in a serial I/O device is set and if D2 is 1 "PAPER EMPTY" in printer is set.

SOD	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
1	10	W	–	–	–	–	–	–	M	–	D1 indicates whether data is output to CMT or RS-232C (0 for CMT, and 1 for RS-232C port).
1	11	W	–	–	–	–	–	0	1	0	By writing 0 at bits D0 and D2 and 1 at bit D1 into gate array μPD65010G, ports P0 and P2 of the gate array are designated as input ports and P1 of the same is designated as an output port.

			MODE 00					MODE 01				
			FUNCTION	D3	D2	D1	D0	FUNCTION	D3	D2	D1	D0
0	10	R/W	SECOND CTR.	D3	D2	D1	D0	–	X	X	X	X
0	11	R/W	TEN-SECOND CTR.	X	D2	D1	D0	–	X	X	X	X
0	12	R/W	MINUTE CTR.	D3	D2	D1	D0	ALARM MINUTE REGISTER	NOT USED			
0	13	R/W	TEN-MINUTE CTR.	X	D2	D1	D0	ALARM TEN-MINUTE REGIST.	NOT USED			
0	14	R/W	HOUR CTR.	D3	D2	D1	D0	ALARM HOUR REGISTER	NOT USED			
0	15	R/W	TEN-HOUR CTR.	X	X	D1	D0	ALARM TEN-HOUR REGISTER	NOT USED			
0	16	–	WEEK CTR.	NOT USED				ALARM WEEK REGISTER	NOT USED			
0	17	R/W	DAY CTR.	D3	D2	D1	D0	ALARM DAY REGISTER	NOT USED			
0	18	R/W	TEN-DAY CTR.	X	X	D1	D0	ALARM TEN-DAY REGISTER	NOT USED			
0	19	R/W	MONTH CTR.	D3	D2	D1	D0	–	NOT USED			
0	1A	R/W	TEN-MONTH CTR.	X	X	X	D0	$\overline{12H}$/24H SELECTOR	NOT USED			
0	1B	R/W	YEAR CTR.	D3	D2	D1	D0	LEAP-YEAR REGISTER	NOT USED			
0	1C	R/W	TEN-YEAR CTR.	D3	D2	D1	D0	–	NOT USED			
0	1D	R/W	MODE REGISTER	TE	AE	M1	M0	MODE REGISTER	NOT USED			
0	1E	W	TEST REGISTER	T3	T2	T1	T0	TEST REGISTER	NOT USED			
0	1F	W	RESET CONTROL	1H	16H	TR	AR	RESET CONTROL	NOT USED			

X: DO NOT CARE AT WRITE AND 0 AT READ.

T3: TEST MODE 3
T2: TEST MODE 2
T1: TEST MODE 1
T0: TEST MODE 0

TE: TIMER ENABLE
AE: ALARM ENABLE

1H: 1 Hz ON
16H: 16 Hz ON
TR: TIMER RESET
AR: ALARM RESET
M1: MODE 01
M0: MODE 00

BITS D4-D7 ARE NOT USED.

MODE REGISTER

D3	D2	D1	D0
TE	AL	M1	M0

MODE REGISTER

D3	D2	D1	D0	
TE	AL	M1	M0	
		0	0	→ SELECT MODE 00 FOR PROGRAMMING OF TIME AND READ OUT.
		0	1	→ SELECT MODE 01 FOR PROGRAMMING OF ALARM, $\overline{12H}$/24H, LEAP YEAR, AND READ OUT.
		1	0	→ SELECT WRITE/READ IN RAM OF BLOCK 10.
		1	1	→ SELECT WRITE/READ IN RAM OF BLOCK 11.
	→ IF 1 ENABLES ALARM OUTPUT, 0 DISABLES ALARM OUTPUT. 16 Hz AND 1 Hz SIGNALS ARE NOT AFFECTED.			
→ TIMER STARTS COUNTING WHEN THE BIT IS 1 AND COUNTERS AFTER SECOND COUNTER STOP COUNTING WHEN THE BIT IS 0.				

1	20	R	D7	D6	D5	D4	D3	D2	D1	D0	Reads data of keys from the buffer register.
1	21	W	–	–	–	–	D3	D2	D1	D0	Writes 4-bit data (00-0A) using low bits D0-D3 in the key common register in the gate array. High bits (D4-D7) are not used.
0	20	R	UNDEFINED								This I/O address is used when auto-power-off occurs.
1	40	R	–	–	–	–	D3	–	–	–	Data from CMT or RS-232C port is input to bit D3 of the CPU accumulator.
1	40	W	–	–	–	–	–	–	–	D0	Data at bit D0 of the accumulator is transfered to the gate array to be transfered to CMT or RS-232C port.
1	41	R	–	–	E	R	–	–	–	–	If D4 is 1, the serial data control circuit in the gate array is ready. If D4 is 0, the circuit is not ready. If D5 is 1, an error has occurred in the control circuit. These statuses are output from the gate array each time a byte of data is transferred.
1	41	W	D7	D6	D5	D4	D3	D2	D1	D0	Arbitrary data in bits D0-D7 are output to the gate array as an acknowledge signal for synchronization with the start bit when data from a serial I/O device is input to the CPU.

SOD	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
1	43	W	—	—	—	0	0	M2	M1	M0	Bits D0-D2 are output from the CPU to the gate array to designate the status of port P1 and RMT in the gate array.
0	40	R	0	0	0	0	0	1	0	1	Read the device code of "05" from the mini-floppy disk drive unit (FP-1021FD) at power-on.
1	80	W	D7	D6	D5	D4	D3	D2	D1	D0	8-bit parallel data is output for the printer to the gate array once then output to the printer.
1	81	R	B	—	—	—	—	—	—	—	D7 is set to 1 to indicate that the line buffer of the Centronics standard printer is full, causing the CPU to temporarily stop transfer of 8-bit data to the printer.
0	80	R	RQM	DIO	NDM	CB	D3B	D2B	D1B	D0B	These indicate the read status of each bit of the status register in the FDC of the FP-1021FD. The CPU performs the appropriate disk operation according to this information. A bit set to 1 indicates there is a status, and a bit set to 0 indicates there is no status. D0B (D0): Drive 0 is executing a seek command or holding for an interrupt request for termination of the seek. D1B (D1): Same as for D0B except that it is drive 1 instead of drive 0.

M0 →

M STATUS AT ADDRESS 10	0		1	
M0 STATUS AT ADDRESS 43	0	1	0	1
REMOTE OF CMT	OFF	ON	OFF	OFF
RTS OF RS-232C PORT	OFF	OFF	OFF	ON

M1 →

0	OUTPUT MODE
1	INPUT MODE

M2 →

0	CMT MODE
1	RS-232C

SOD	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
											D2B (D2): Same as for D0B except that it is drive 2 instead of drive 0. D3B (D3): Same as for D0B except that it is drive 3 instead of drive 0.

SOD	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
											D2B (D2): Same as for D0B except that it is drive 2 instead of drive 0. D3B (D3): Same as for D0B except that it is drive 3 instead of drive 0. CB (D4): FDC is now executing the execution phase of the phase command or the result phase of the ready write command, and cannot accept other commands as long as this bit is 1. NDM (D5): FDC is now transferring data in the non-DMA mode and is requesting service from the CPU. DIO (D6): Designates direction of data flow D6 is 0 if flow is from the CPU to the FDC. D6 is 1 if the flow is from the FDC to the CPU. Status of the data register is designated by RQM bit D7. RQM (D7): Indicates data to be transferred to the CPU from the FDC is being loaded or that there is no data in the data register and data from the CPU can be loaded in.
0	81	R	D7	D6	D5	D4	D3	D2	D1	D0	Reads 8-bit data from the data register of the FDC.
0	81	W	D7	D6	D5	D4	D3	D2	D1	D0	Writes 8-bit data in the data register of the FDC.
0	82	W	D7	D6	D5	D4	D3	D2	D1	D0	Writes 8 bits of random data in the input terminal TC of the FDC informing the FDC that the read or write operation from the CPU has ended.
0	84	W	D7	D6	D5	D4	D3	D2	D1	D0	Transfers (writes) 8 bits of random data to the FD control circuit of FP-1021FD, which is decoded to form the MOTOR ON signal.
0	86	W	D7	D6	D5	D4	D3	D2	D1	D0	Transfers 8 bits of random data to the FD control circuit, which is decoded to form the RESET signal.
0	86	R	INT	–	–	–	–	–	–	R	Reads status bits D0 and D7 from the status register in the FDC. If D0 is 1, the FDC is ready to receive data, and if D7 is 1, an interrupt from the FDC has been made to the CPU.

5. DISASSEMBLY/ASSEMBLY

5-1. DISASSEMBLY

REMOVING UPPER HOUSING

1) Turn the power switch off and disconnect all peripheral devices. Also remove RAM ROM packs from their compartments.
2) Remove 4 screws at each corner of the lower housing.
3) Unhook the 4 hooks from the upper housing (2 at the front and 2 at the rear), then the upper housing straight up.
4) While holding the upper housing, unplug the 2 flexible green cables with your other hand.
5) Disconnect the 2 green ground wires from the power supply section.

REMOVING DISPLAY PCB (P1-E2)

1) Remove 4 screws from each corner of the display PCB (P1-E2).

WARNING: Never try to remove the LCD or the three LSI chips (two of which are underneath the LCD). You must replace the entire PCB with a new one when one of these components fails.

REMOVING CONDUCTIVE RUBBER SHEET AND KEYTOPS

1) Remove 17 screws from the tops of the P1-E4 and P1-E3 PCBs, then remove the plastic spacer and the conductive rubber sheet.
2) To remove a keytop, unhook the two diagonal hooks while the upper housing is lifted up so that the key top will drop down by itself when the two hooks are released as shown in Fig. 5-1.

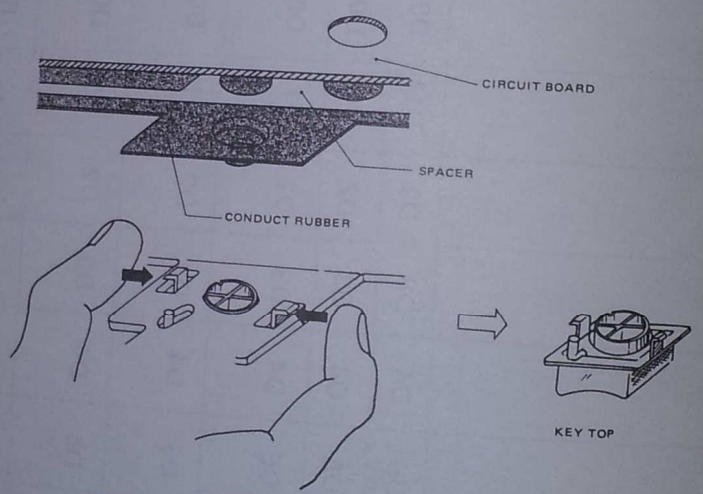


Fig. 5-1 REMOVING KEY TOP

REMOVING MAIN PCB (P1-1)

1) Remove the battery compartment for the operating battery, then remove 2 screws holding FDD connector on the chassis with a phillips screwdriver through the slot.
2) Remove 6 screws (4 on top of the main PCB and 2 on top of the power supply PCB (P1-1)). Disconnect the five-pin power connector and turn over the power supply PCB to the left as if you were opening a page in a book. Note the metal collars around the two shafts that sit on the power supply PCB. Take these collars away but not to loose.
3) Remove 3 screws holding the PCB (P1-B) that the printer connector, CMT connector, and RS-232C port connector are located on. Remove the PCB.

5-2. ASSEMBLY

Assembly is simple – just reverse all the steps in the disassembly procedure.

6. EXPLANATION OF CIRCUITS

6-1. CPU (MSM80C85A)

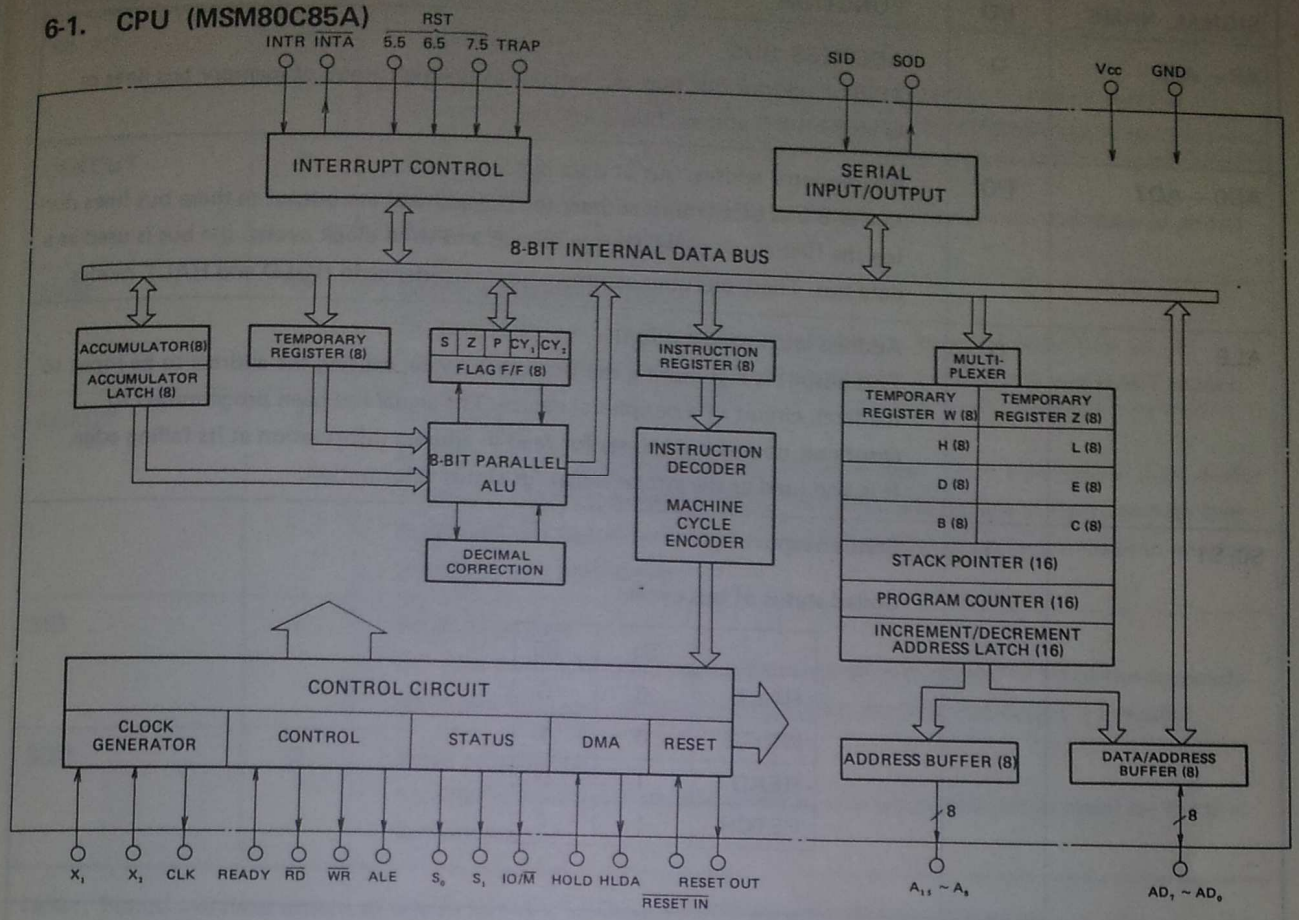


Fig. 6-1 CPU BLOCK DIAGRAM

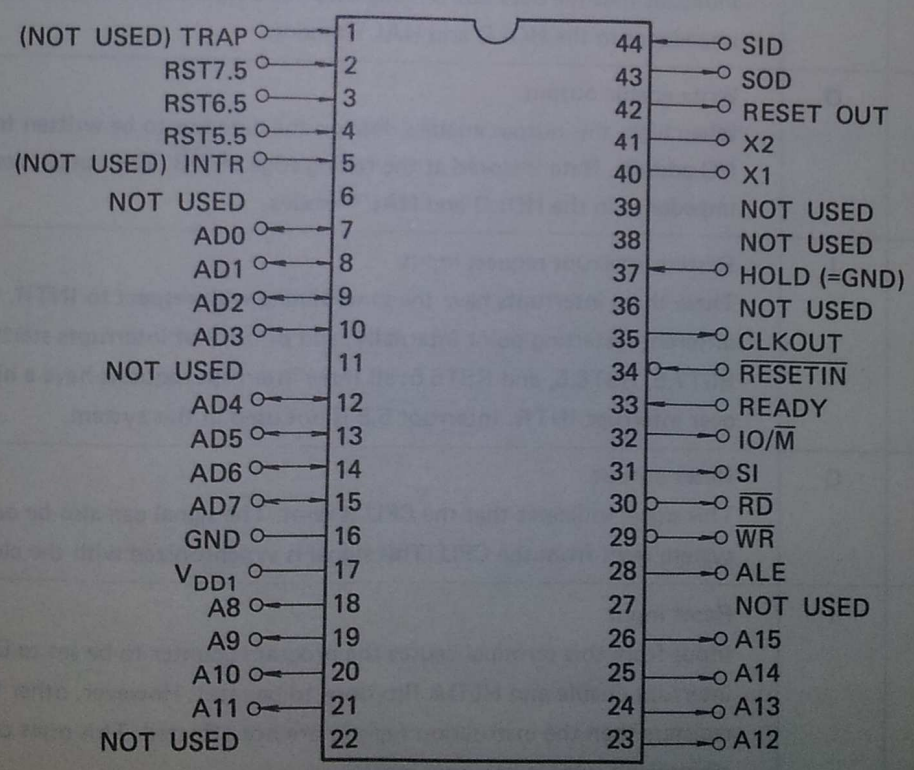


Fig. 6-2 PIN CONFIGURATION

SIGNAL NAME	I/O	FUNCTION
A8 – A15	O	ADDRESS BUS An 8-bit address bus that can be used as the high group of memory bus lines or as an 8-bit I/O address bus.
AD0 – AD7	I/O	Bidirectional address bus or data bus. Lower 8 bits of memory address (or I/O address) are output to these bus lines during the first clock cycle. During second and third clock cycles, the bus is used as a data bus. These bus lines assume a high impedance in HOLD and HALT modes.
ALE	O	Address latch enable output This output is high during the first clock cycle, causing the address to be input to the latch circuit of a peripheral device. The signal has been programmed to ensure set-up and hold times for read-in address information at its falling edge. It is also used as the strobe signal for status information.
S0, S1	O	Status output Coded status of bus cycle. HALT: S1 = 0, S0 = 0 WRITE: S1 = 0, S0 = 1 READ: S1 = 1, S0 = 0 FETCH: S1 = 1, S0 = 1
$\overline{RD}$	O	Read enable output When high, this output enables reading of selected memory or I/O address and indicates that the data bus is being used for data transfer. It assumes a high impedance in the HOLD and HALT modes.
$\overline{WR}$	O	Write enable output When high, this output enables data on the data bus to be written to a memory or I/O address. Data is stored at the falling edge of $\overline{WR}$. The output assumes a high impedance in the HOLD and HALT modes.
RST5.5 RST6.5 RST7.5	I	Restart interrupt request input These three interrupts have the same timing with respect to INTR. Each has different restarting point internally, and priority of interrupts starts from RST7.5, RST6.5, and RST5.5; all three interrupt requests have a higher priority over interrupt INTR. Interrupt 5.5 is not used in this system.
RESET OUT	O	Reset output This signal indicates that the CPU is reset. The signal can also be output as a system reset from the CPU. This signal is synchronized with the clock.
$\overline{RESET\ IN}$	I	Reset input Input from this terminal causes the program counter to be set to 0 and both the interrupt enable and HLDA flip-flops to be reset. However, other flags and registers than the instruction register are not affected. This reset condition is maintained until it becomes inactive.

SIGNAL NAME	I/O	FUNCTION
X1, X2	I/O	Clock input A crystal oscillator is connected to these two terminals, or a clock signal is generated and transferred by periphral device to the CPU through these terminals.
CLKOUT	O	Clock output Output of the clock from the CPU; it is used to synchronize operation of an I/O device with that of the CPU.
IO/$\overline{M}$	O	Data transfer cntrol output Output from this terminal designates read/write from/to memory or an I/O device. The terminal assumes a high impedance in the HOLD and HALT modes.
READY	I	Ready signal If this signal is 1 during the read/write cycle, memory or a peripheral (I/O) device is ready to transfer or receive data. The CPU waits for this signal to go high then completes the read or write cycle. This signal must be on long enough to ensure the set-up and hold times.
SID	I	Serial input data I/O data (in the FP-200, from the keyboard) is input to 7th bit of the accumulator in the CPU through this terminal when the RIM instruction is executed.
SOD	O	Serial output data Serial data is output from this terminal; it is controlled (set or reset) by the SIM instruction.

Note: Functional descriptions of signals not used in Casio FP-200 are omitted from this table.

OPERATIONAL TIMING CHART

CLOCK PULSE

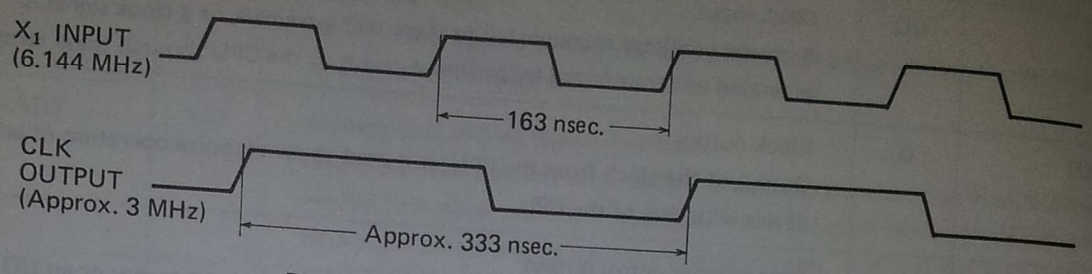


Fig. 6-3 CLOCK PULSE TIMING CHART

READ/WRITE CYCLE

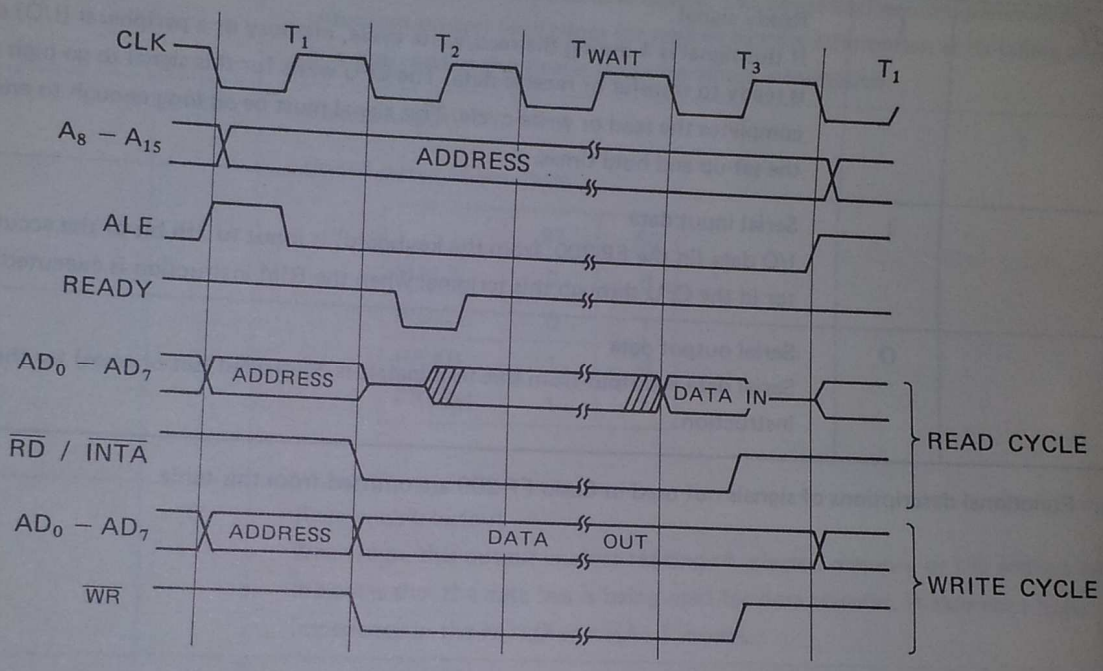


Fig. 6-4 READ/WRITE TIMING CHART INSTRUCTION FETCH CYCLE

INSTRUCTION FETCH CYCLE

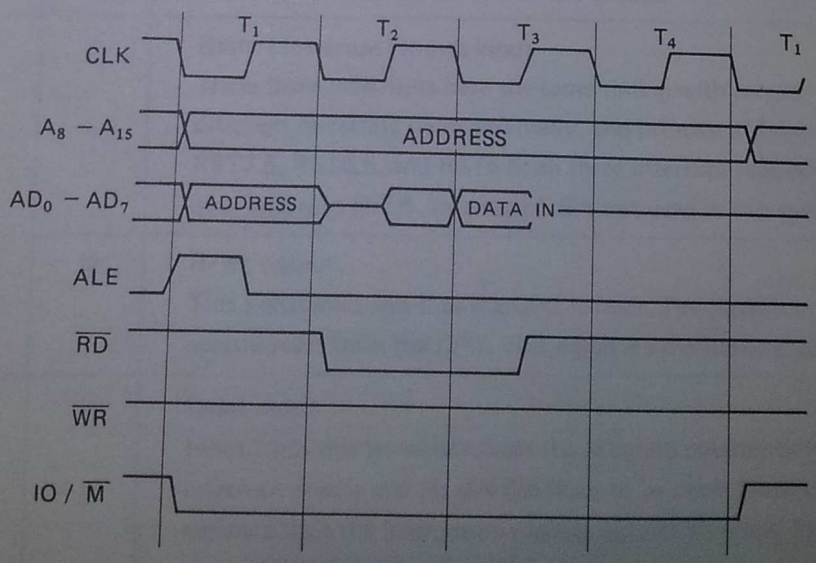


Fig. 6-5 TIMING CHART FOR INSTRUCTION FETCH CYCLE

6-2. GATE ARRAY (μPD65010G-030)

After the CPU, the next most important device in the FP-200 is the CMOS gate array. The gate array interfaces between the CPU and I/O devices such as a Centronics-compatible printer, RS-232C port, etc.; the gate array simplifies the entire system. The gate array programmed for FP-200 can access the LCD display, RS-232C port, printer, mini-plotter, CMT, and the keyboard.

PIN CONFIGURATION

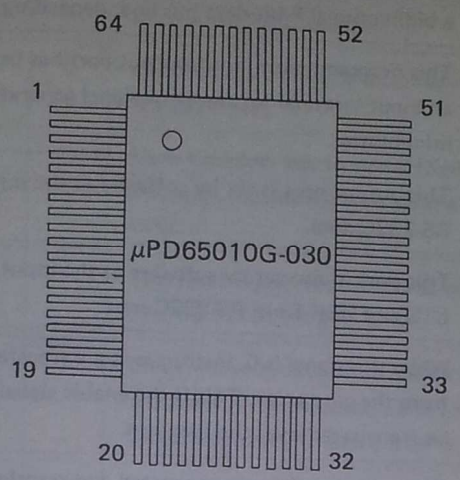


Fig. 6-6 PIN CONFIGURATION FOR GATE ARRAY μPD65010G-030

BLOCK DIAGRAM OF GATE ARRAY

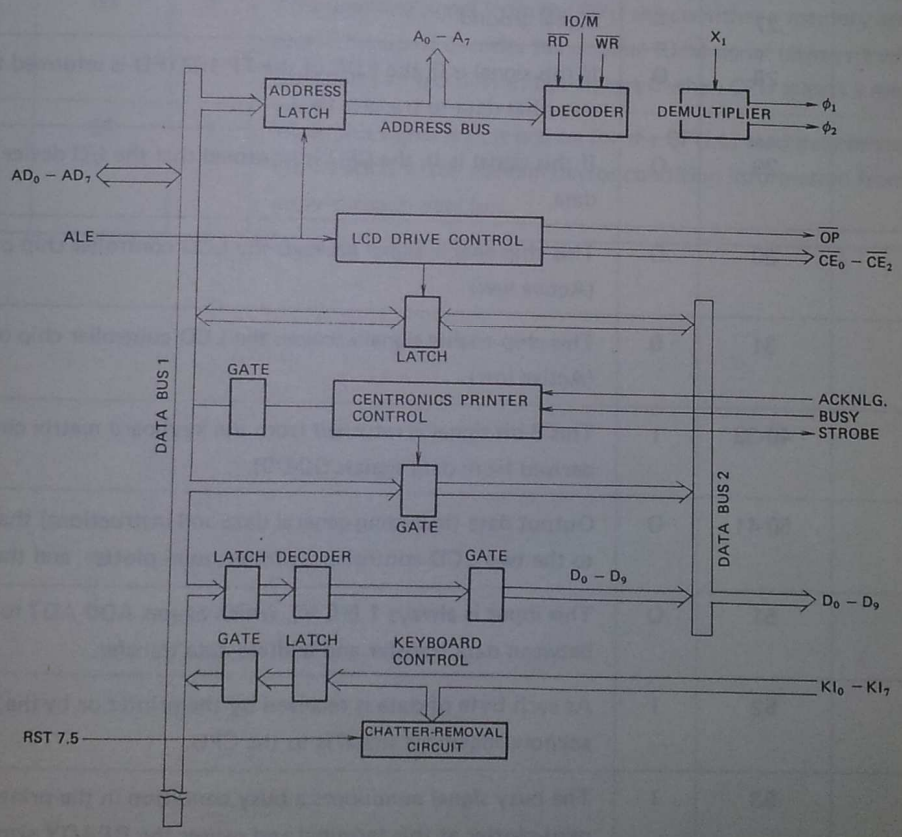


Fig. 6-7 BLOCK DIAGRAM OF GATE ARRAY

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
$\overline{WR}$	2	I	The write enable signal is generated by the CPU and causes the CPU to write data to the gate array when it is 0. (Active low)
A0 – A7	11-4	O	The low group of address bits are derived from address outputs AD0-AD7, which are latched by the ALE signal.
AD0 – AD7	19-12	I/O	This 8-bit bus line can be used as either a low-address bus lines (A0-A7) or a bidirectional 8-bit data bus line, depending on the clock state.
P2	20	I	This programmable input/output port has been programmed for use as an input terminal for the error signal generated by the printer or the mini-plotter.
P1	21	O	This output port is set by software as the output port for CMT data or RS-232C data.
P0	22	I	This port is also set by software as the input port for the decoded signal of CTS and DSR from RS-232C port.
$\overline{OP}$	23	O	When this signal is 0, instructions are transferred to the LCD controller from the gate array. This is the enable signal that allows instructions to be transferred over the data bus.
$\phi 1, \phi 2$	25, 24	O	These clock pulses are generated and transferred by the gate array to synchronize the LCD controller's operation.
VDD	26, 58	I	+5 V DC
GND	27	–	Signal ground
$\overline{CE4}$	28	O	If this signal is 0, the FDC of the FP-1021FD is informed that the gate array has data to transfer to it.
$\overline{CE3}$	29	O	If this signal is 0, the CPU is informed that the I/O device is ready for data.
$\overline{CE2}$	30	O	This chip enable signal accesses the LCD controller chip of the right half. (Active low)
$\overline{CE1}$	31	0	This chip enable signal accesses the LCD controller chip of the left half. (Active low)
KI0 – KI7	40-33	I	This 8-bit signal is returned from the keyboard matrix circuit (originally derived from data signals D0-D9).
D0 – D9	50-41	O	Output data (including general data and instructions) that is transferred to the two LCD controllers, printer, mini-plotter, and the keyboard.
CPUS	51	O	This input is always 1 (+5 V), which causes AD0-AD7 to be timeshared between data transfer and address data transfer.
ACKNLG	52	I	As each byte of data is received by the printer or by the mini-plotter, any acknowledgement signal is to the CPU.
BUSY	53	I	The busy signal announces a busy condition in the printer or in the mini-plotter at this terminal and causes the READY signal to reset (not active).

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
STROBE	54	O	This strobe signal is used to synchronize writing data to the printer buffer from the CPU.
RMT	55	O	If this signal is 1, the AND gate for the remote control circuit of CMT and the NAND gate circuit of RST for RS-232C port are enabled.
EAR	56	I	This input terminal is set for serial data for incoming port CMT and for the RS-232C port.
MIC	57	O	Output data from this terminal is serial data and is transferred to CMT or RS-232C port.
RST7.5	59	O	Each time low key-in signal (KI0-KI7) is input to the gate array, an interrupt request signal is generated and input to terminal RST7.5 of the CPU.
RST	60	I	This reset signal from the CPU initializes the registers, the counter, and the flag register in the gate array.
X1	61	I	Clock input derived from the CPU. This in the gate array signal is used to synchronize the functions and I/O derives controlled by the gate array. Clock frequency is about 3 MHz.
READY	62	O	This ready signal differs from the ready signal previously explained. This ready signal declares that the serial data control circuit of the gate array is ready to operate.
IO/$\overline{M}$	63	I	This selecting signal from the CPU selects either a memory area or I/O area. This signal decodes the original IO/$\overline{M}$ signal (always 1 when the CPU designates an I/O device, but always 0 when CPU selects a memory area).
$\overline{RD}$	64	I	When this signal is 0, it is time for the CPU to read data or status information which contain device condition information from the gate array through data bus.

6-3. TIMER (RP5C01)

A programmable timer used in this system, the RP5C01, can count time (hours, min and seconds), keep track of the date/month/year (including leap year), has two time [illegible] modes (12-hour with AM and PM or 24-hour), etc.
It has also non-volatile (26 x 4 bits) RAM memory protected by an external back-up batte[illegible]

PIN CONFIGURATION

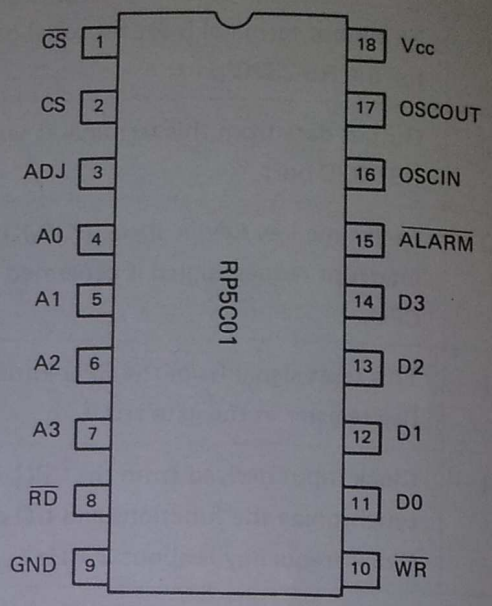


Fig. 6-8 PIN CONFIGURATION OF TIMER

BLOCK DIAGRAM OF TIMER

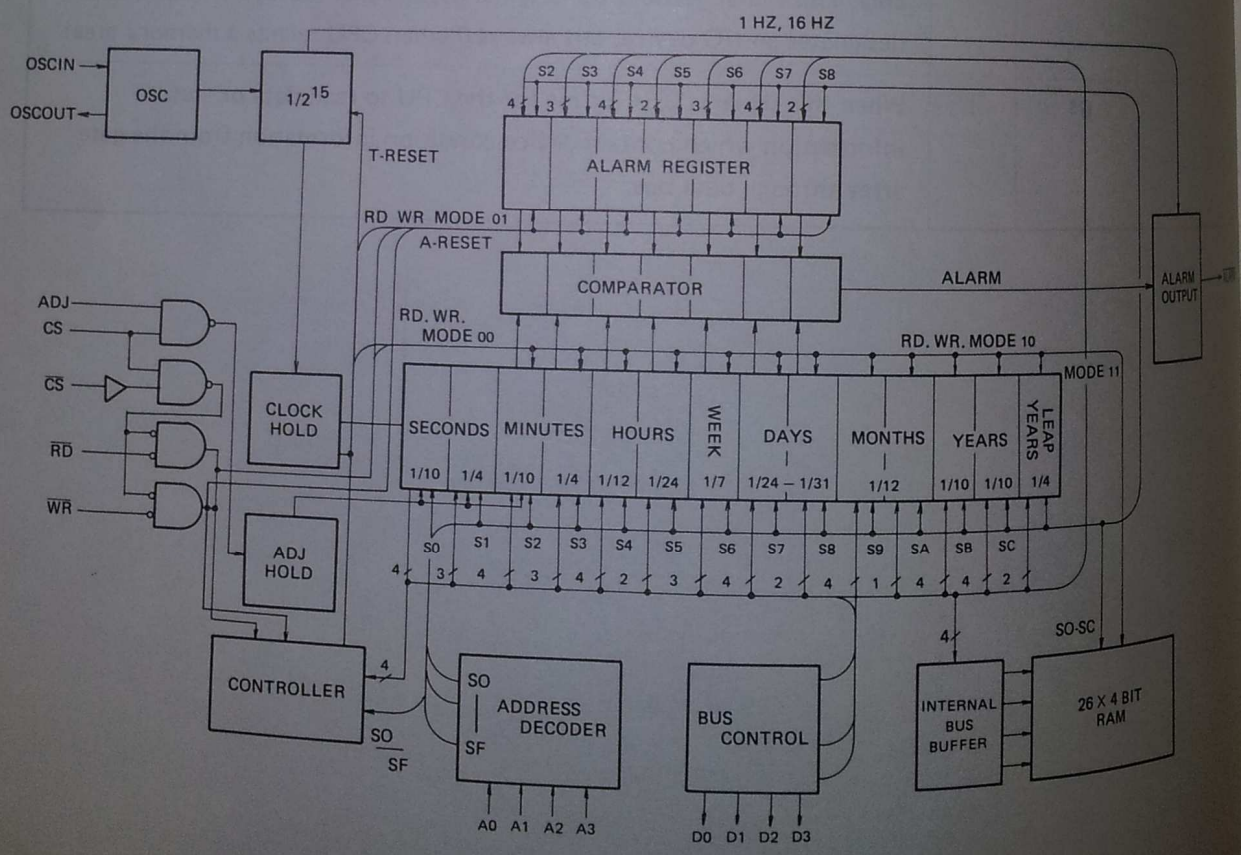


Fig. 6-9 BLOCK DIAGRAM OF TIMER

SIGNAL NAME	I/O	DESCRIPTION
$\overline{CS}$, CS	I	Both input signals are chip-select signals, which are used to select this device. Port $\overline{CS}$ (active low) interfaces the CPU and this device; port CS (active high) is connected to the power-down detector circuit (RESET circuit) to initialize the count when the power voltage becomes low and there is not enough power for all components.
A0 – A3	I	The 4-bit address bus supplied by the CPU can designate 16 address (0-F).
$\overline{RD}$	I	The read enable signal is from the CPU and is used by the CPU to read time and calendar data when it is 0.
$\overline{WR}$	I	Write enable signal. This signal is also from the CPU and is used by the CPU to write data that sets starting time.
D0 – D3	I/O	Bidirectional data bus. These data bus lines are connected directly to the CPU.
OSCIN, OSCOUT	I/O	Terminals to connect crystal oscillator. Clock frequency is 32.768 KHz.
Vcc	I	DC +5 V

Note: All functions not used in the FP-200 are omitted.

OPERATION TIME CHART

WRITE CYCLE (CS = "H")

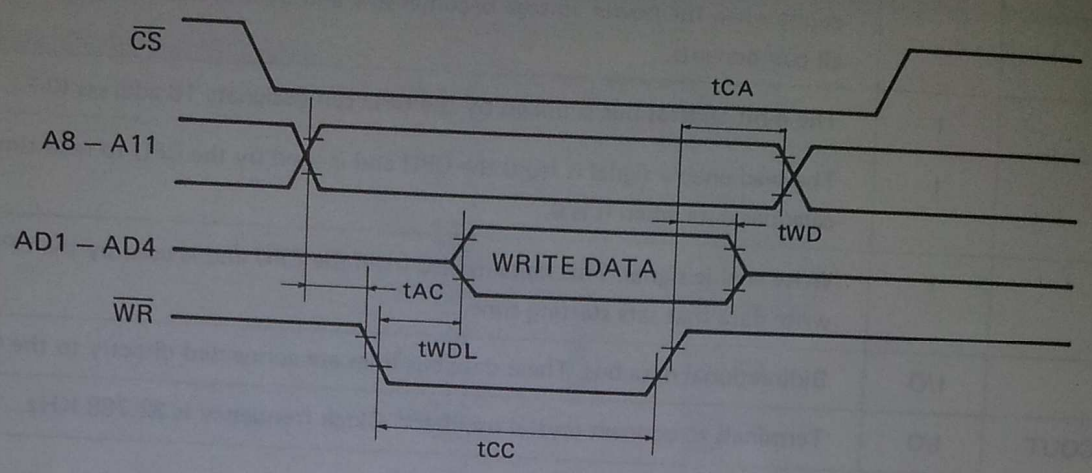


Fig. 6-10 WRITE OPERATION TIMING CHART

READ CYCLE (CS = "H")

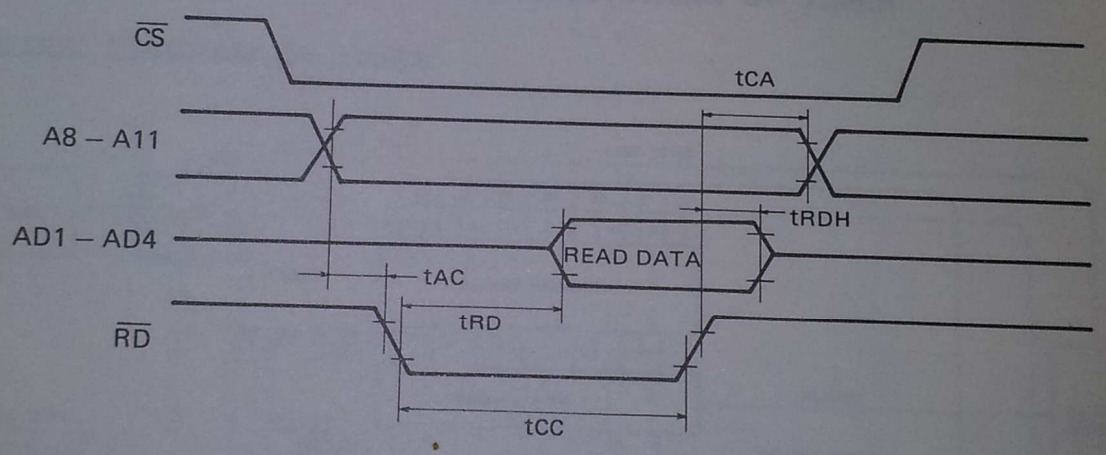


Fig. 6-11 READ OPERATION TIMING CHART

6-4. MEMORY INTERFACE

The circuit below can access, by enabling $\overline{CE1}$ and $\overline{CS}$, the built-in 8K RAM (each RAM has 2K) and a maximum of up to three optional 2K RAM packs or two 2K RAMs and one 8K ROM packs.

When $\overline{WR}$ or $\overline{RD}$ signal is 0 (the CPU can read or write data to memory), the output at inverting NOR gate G2 becomes active and simultaneously pin 3 of J2 is also active (caused by active address A15 and IO/$\overline{M}$ = 0). These two low-active inputs at gate J2 cause the output at pin 6 of the gate to be 0, and $\overline{CE1}$ enables all RAMs of the main memory; it can also enable them through gate E10 if the AUTO-POWER-OFF signal is off (active high) and inverter D10 for decoder H3. In the decoder, timesharingly seven different chip select ($\overline{CS}$) signals for four RAMs of the main memory and three optional memory packs, are output and each chip select signal corresponds to particular address allocation as shown in address table below.

LOCATION: MAIN PCB (P1-1)

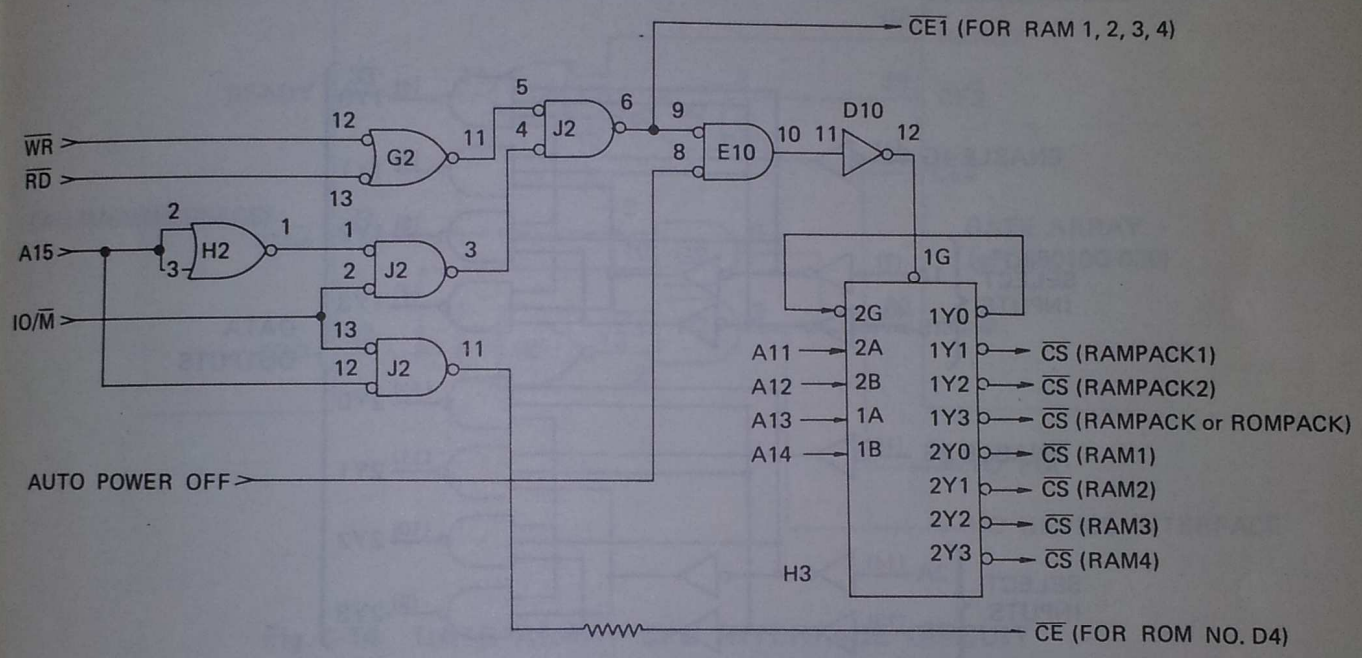


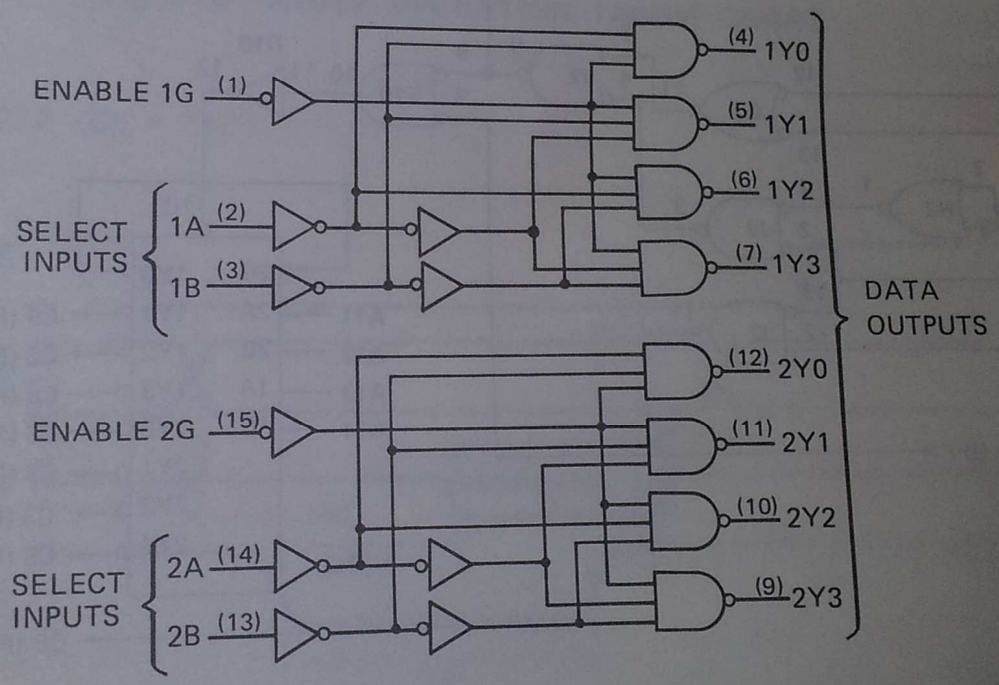
Fig. 6-12 MEMORY INTERFACE CIRCUIT

The memory areas between 8000H and FFFFH, between 32,768 and 65,535, from 0000H to 7FFFH (of 32K memory area) are selected by active or by non active address A15. That is, the ROM contains BASIC and CETL interpreters is selected when A15 is off. Gate J2 makes this possible with low signal of IO/$\overline{M}$ applied at input pin 13. The purpose of AUTO POWER OFF as an input to gate E10 is to protect memory (from destruction or invalid data due to low power). It does this by not letting the enable signal access the decoder H3. Refer to the explanation of AUTO POWER OFF for the theory function of this circuit.

MEMORY ADDRESS ALLOCATION TABLE

ADDRESS	DEVICE	CAPACITY
8000H – 87FFH	MAIN RAM CHIP 1	2K
8800H – 8FFFH	" 2	2K
9000H – 97FFH	" 3	2K
9800H – 9FFFH	" 4	2K
A000H – BFFFH	OPTIONAL RAM PACK 1	8K
C000H – DFFFH	" 2	8K
E000H – FFFFH	" 3 OR ROM PACK	8K

SN74LS139N (IC NO. H3) CIRCUIT DIAGRAM AND TRUTH TABLE



INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

6-5. GATE ARRAY (CPU INTERFACE)

Two ready signals, output from the gate array to the CPU, report the ready status. However, the output from pin 62 informs the CPU of the ready status in the control circuit of the gate array and the output from pin 29 declares the ready status in a peripheral device (such as a printer or mini-plotter).

The ready signal from pin 29 is NORed with the high-active IO/$\overline{M}$ signal to assume that the ready signal is generated only when the CPU accesses an I/O address.

AND gate G2 allows the CPU to access the gate array while both inputs (IO/$\overline{M}$ and SOD) are 1; the two H2 gates allow the CPU to access an I/O device while IO/$\overline{M}$ is 1 and SOD is 0.

In other words, gates H2s and G2 switch over between I/O addresses when SOD changes from 1 to 0. When output from SOD is 1, the I/O address map of left half on page 6 is chosen; when it is 0, the address map of right half is chosen.

LOCATION: MAIN PCB (P1-1)

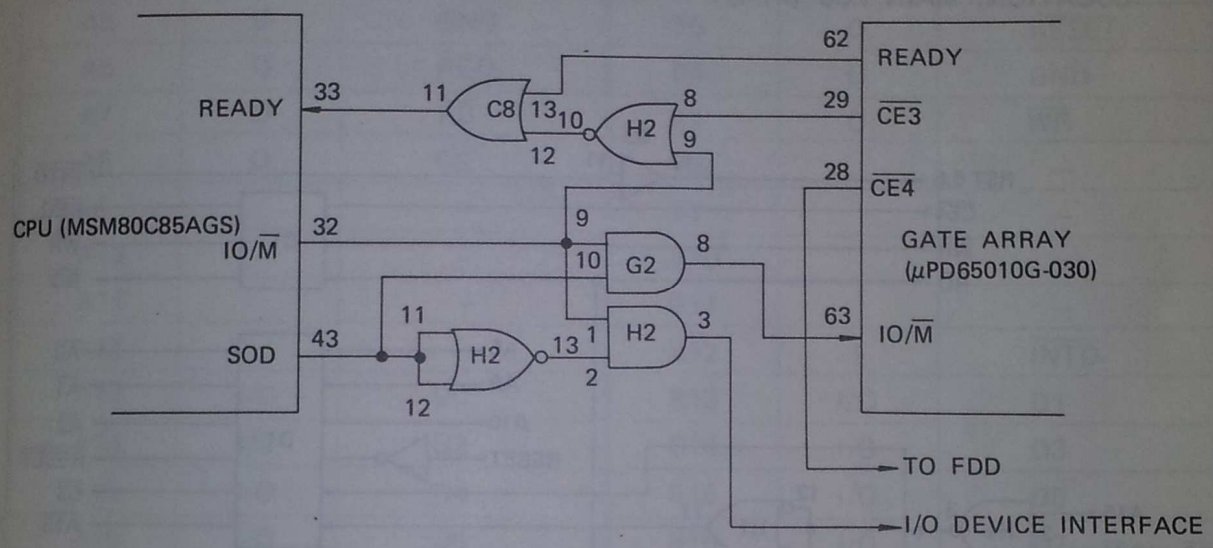


Fig. 6-14 GATE ARRAY CPU INTERFACE CIRCUIT

6-6. FDD INTERFACE

The following circuit is the interface for data and control signals between the gate array and FDD model FP-1021FD.

Address A15 is used for various accessing and enabling controls in the FDD. First A15 is NANDed with SOD•IO/$\overline{M}$ at gate H1. The A15 signal passes through the gate only when the condition is met. Then the signal is inverted by the gate H1.

Two other H1 gates and gate G3 apply the enable signal at buffer gates D2 and C2. Input at pin 4 of first gate H1 allows FDD operations in I/O address 80-8FH, and input pin 5 allows the CPU to read the allocated device code in the FDD at I/O address 40-4FH. The second NAND gate H1 assumes that buffers D2 and C2 pass data only when the CPU reads data from the FDD.

Signal S1 (active low) indicates the operating status of the CPU and lets buffers C1 and C3 pass data from the CPU to the FDD (refer to function description for the CPU on page 13.) C1, D2, D3, D1 and D2 are bus buffer ICs.

LOCATION: MAIN PCB (P1-1)

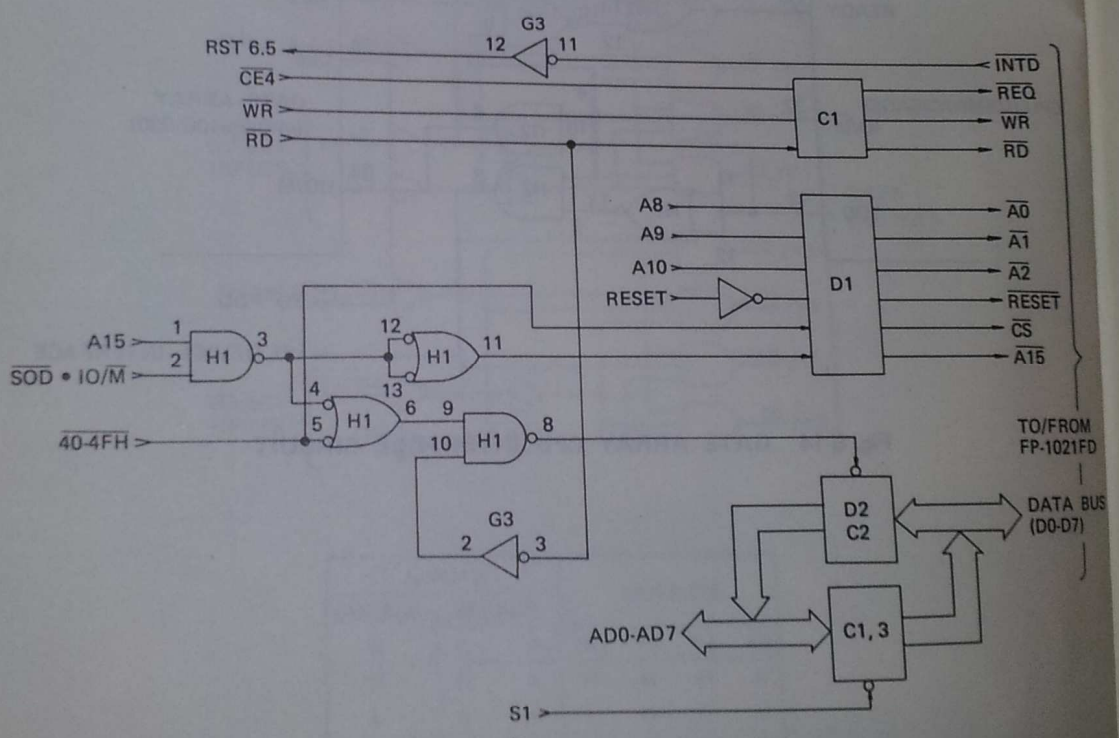
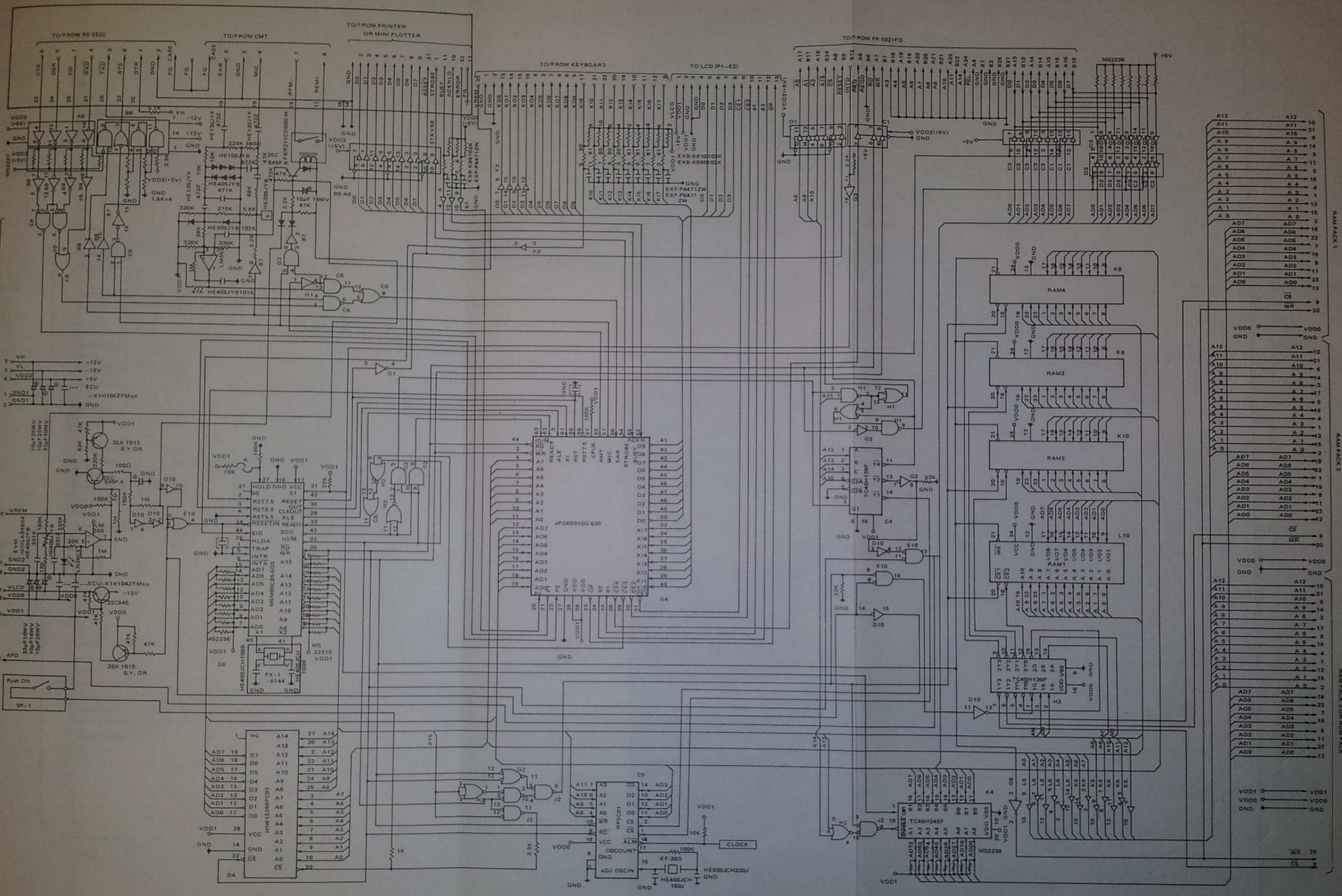
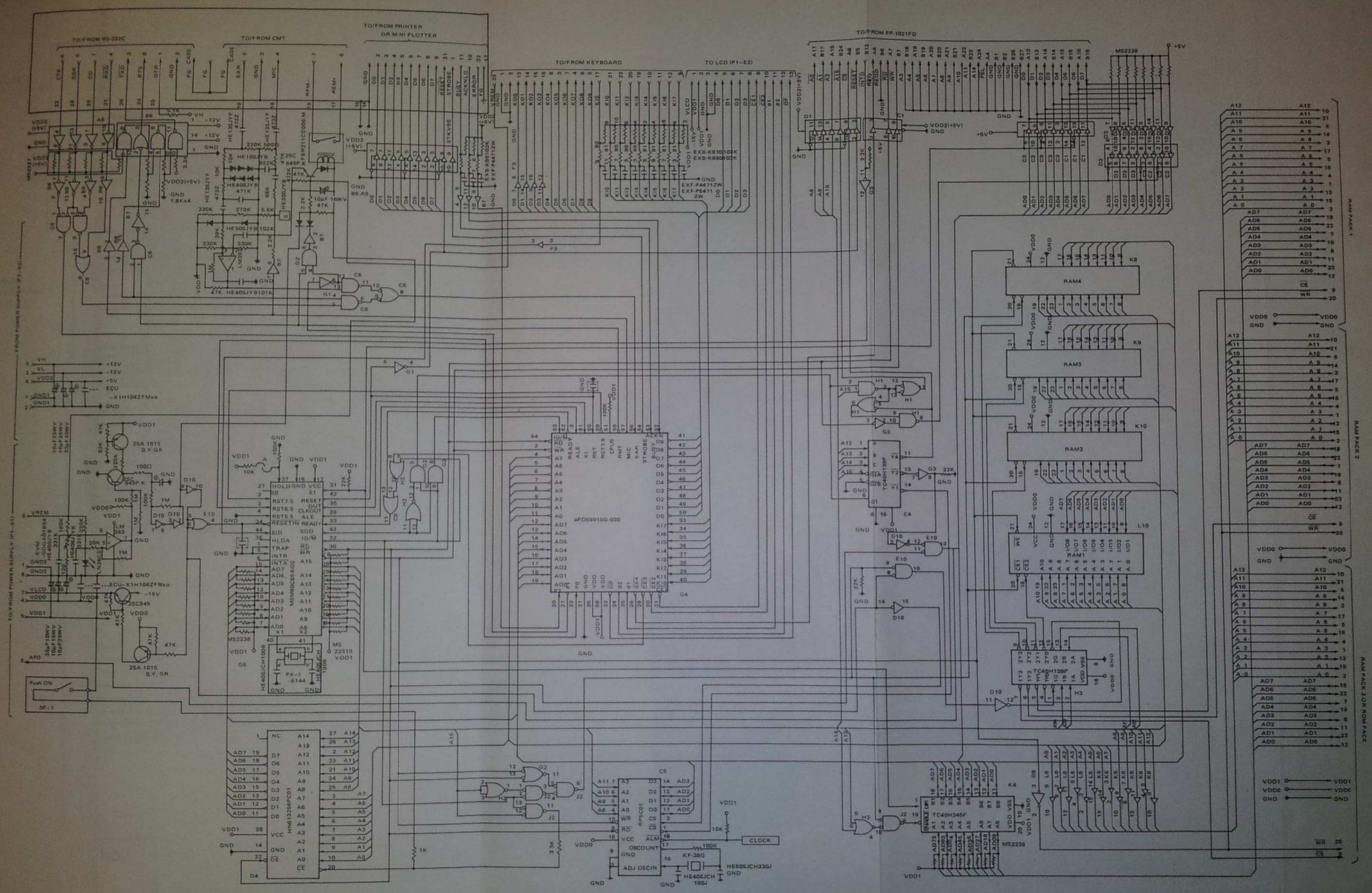


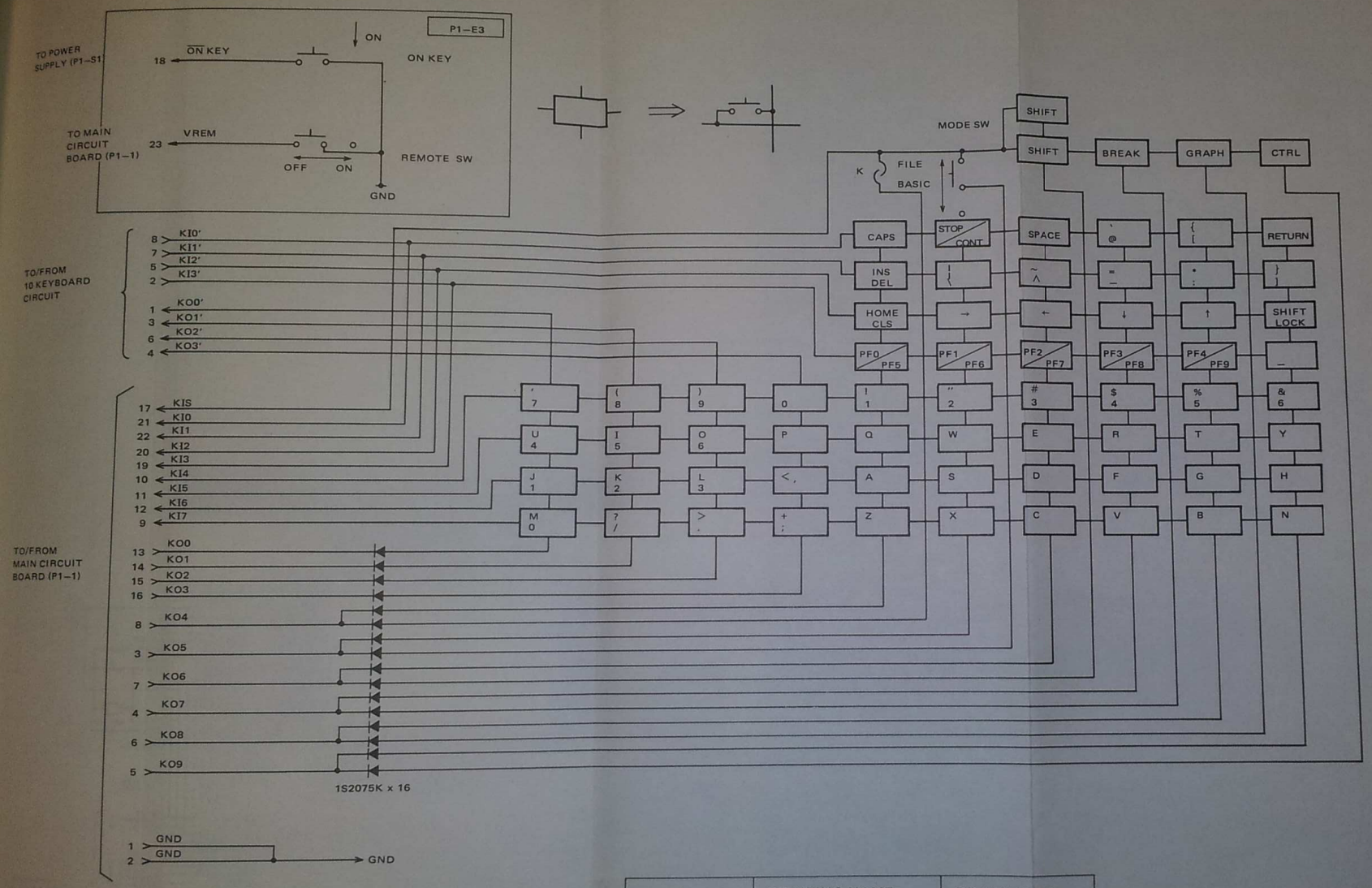
Fig. 6-15 FDD INTERFACE CIRCUIT



MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP-200	MAIN CIRCUIT	C141



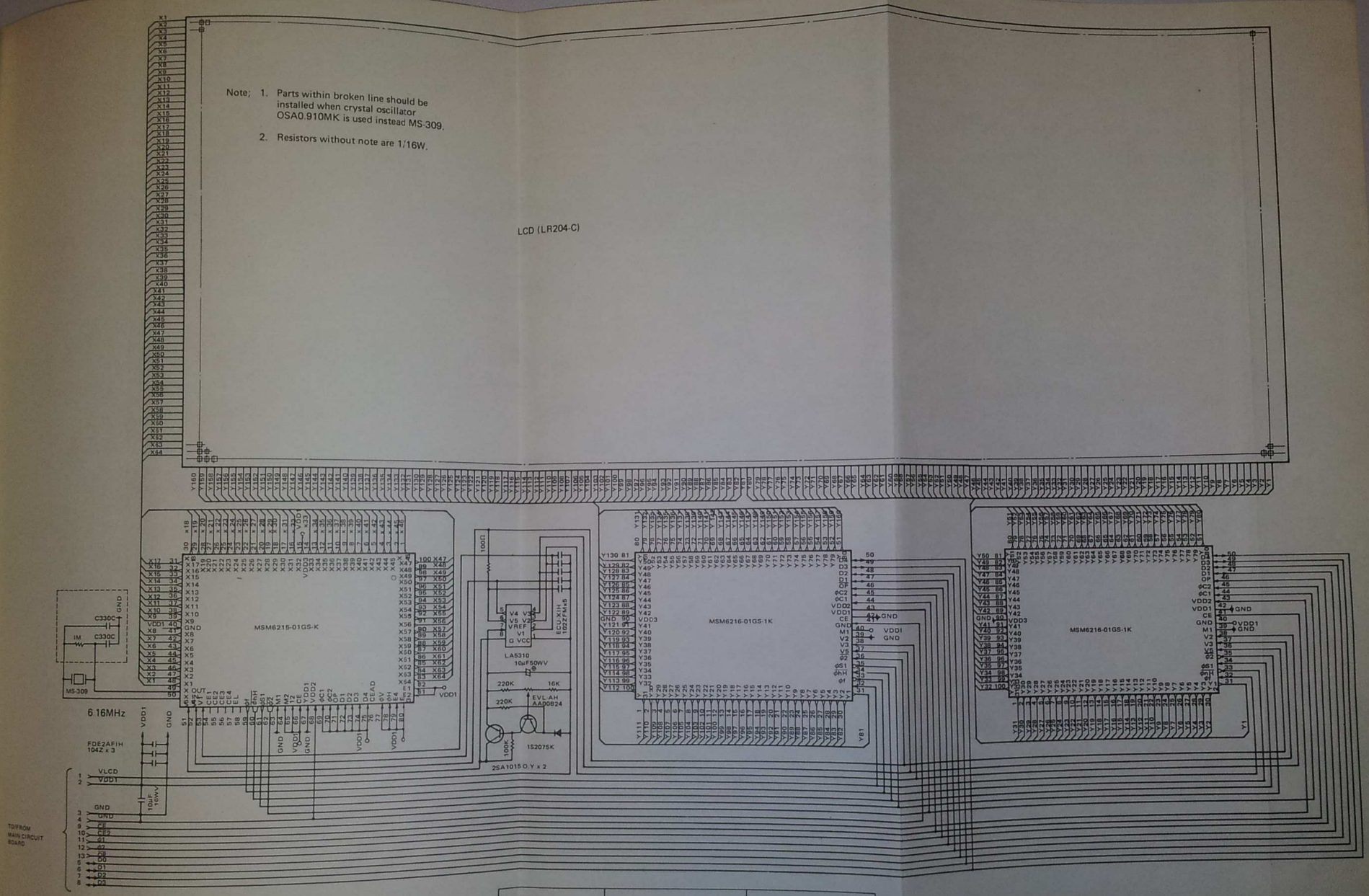
MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP-200	MAIN CIRCUIT	C141



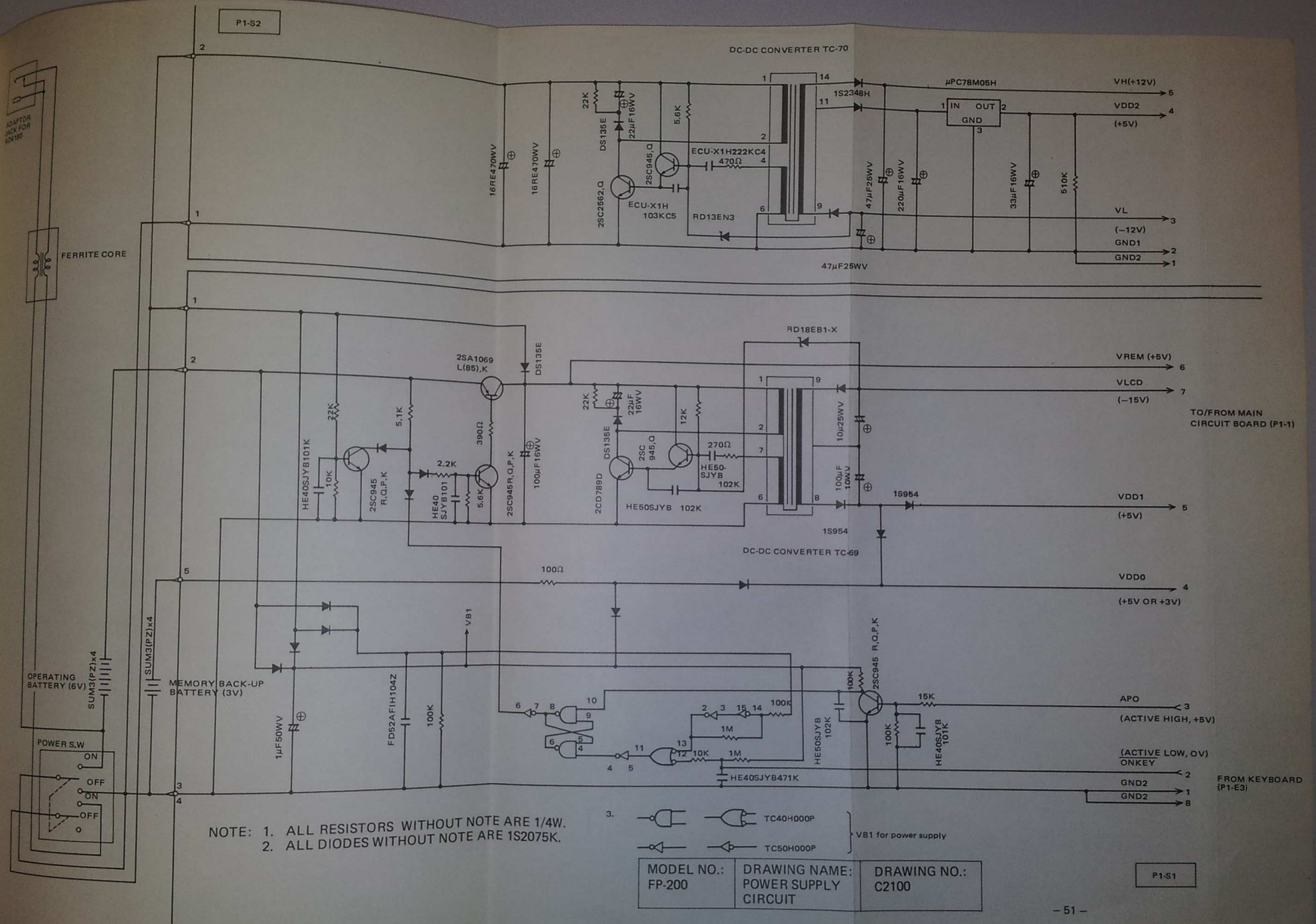
NOTE:
FOR ASCII KEYBOARD, SHORT PAD "K" AND OPEN IT FOR JIS KEYBOARD.

MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP–200	KEYBOARD CIRCUIT	C299 ASCII

P1–E4



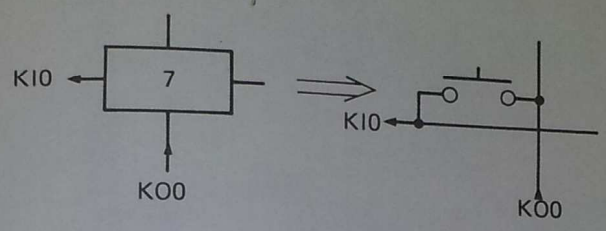
MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP-200	DISPLAY CIRCUIT	C145

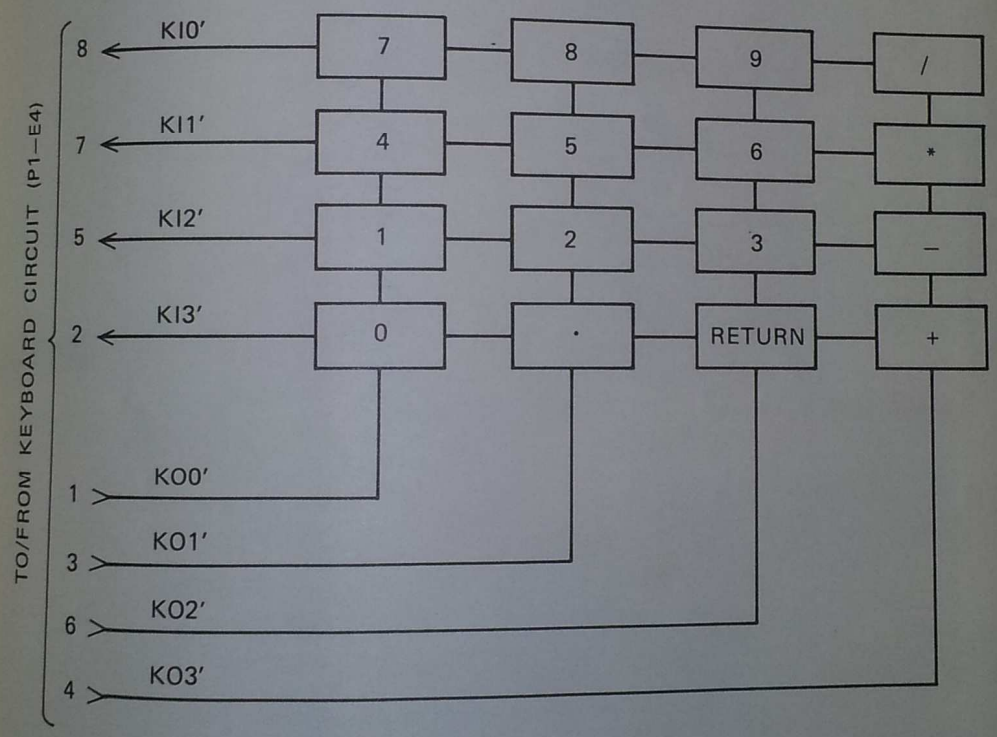


NOTE: 1. ALL RESISTORS WITHOUT NOTE ARE 1/4W.
2. ALL DIODES WITHOUT NOTE ARE 1S2075K.

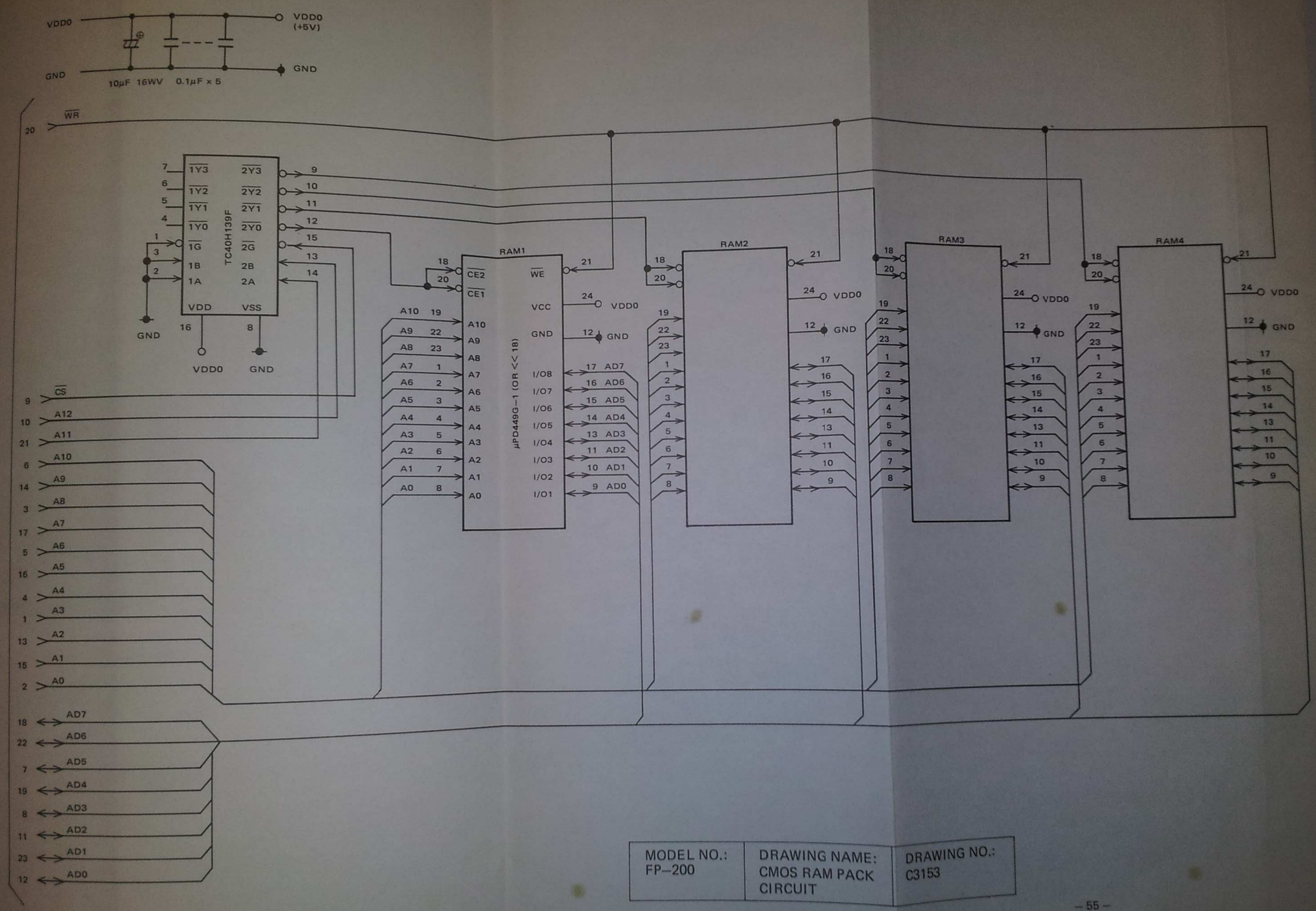
MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP-200	POWER SUPPLY CIRCUIT	C2100

EXAMPLE

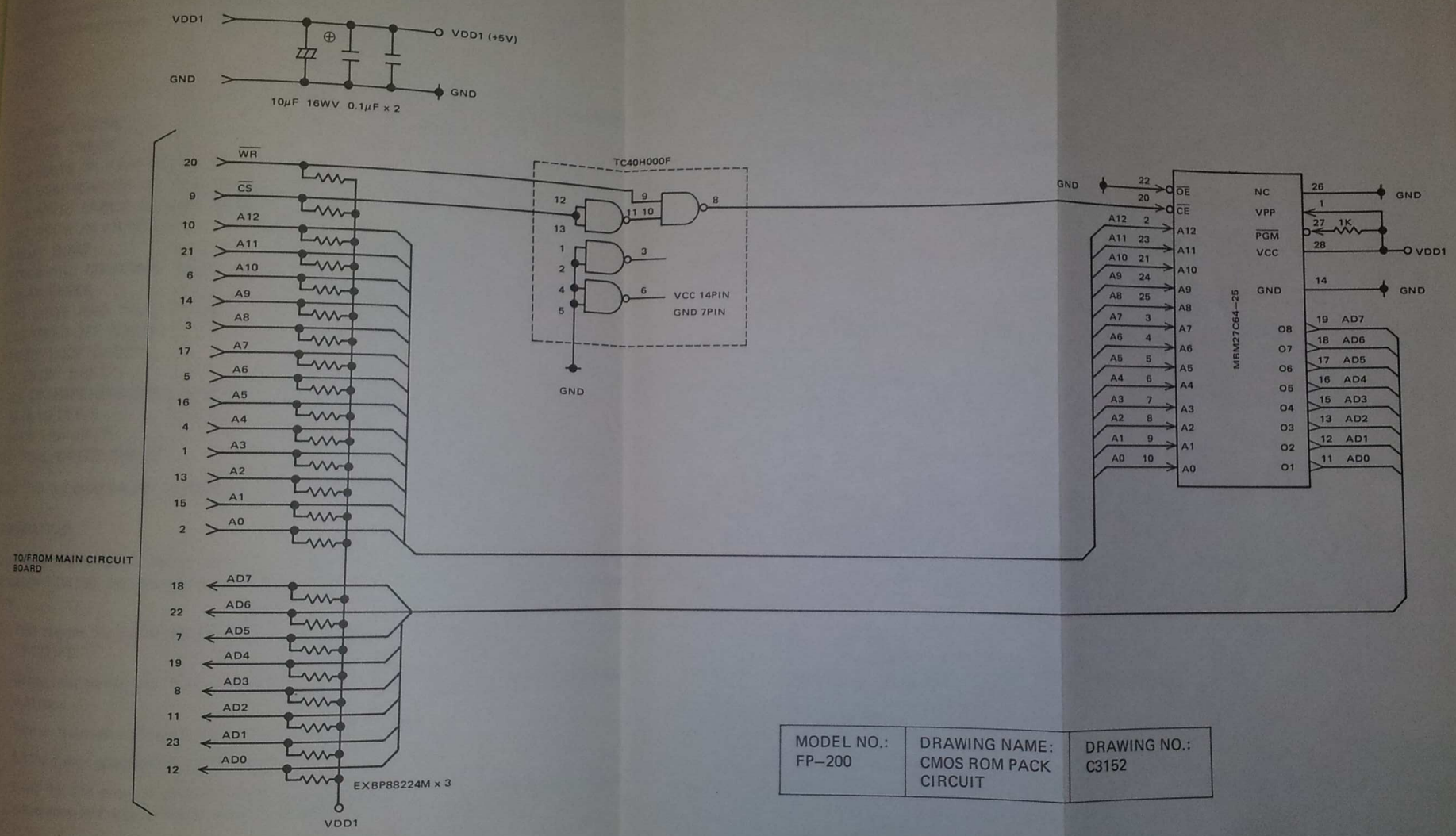




MODEL NO.: FP-200	DRAWING NAME: 10 KEYBOARD CIRCUIT	DRAWING NO.: C4184



MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP–200	CMOS RAM PACK CIRCUIT	C3153



MODEL NO.:	DRAWING NAME:	DRAWING NO.:
FP–200	CMOS ROM PACK CIRCUIT	C3152

8. TEST PROGRAM

The test program, its file name TP and loaded from the floppy diskette, can diagnose the following internal hardware circuits, components, and peripheral devices that are available to the FP-200. This program ability has, however, limitation to its capability and it cannot detect all kinds of trouble. The program can run under the conditions where the CPU and the gate array function normally, all power voltages are normally provided to all sections, and the FDD interface functions normally.

8-1. MENU

	COMMAND CODE (PROGRAM FILE NAME)
MASK ROM CHECK	MR
ROM PACK CHECK	ER
DATA WRITE IN RAM PACK	CW
DATA VERIFICATION IN RAM PACK	CR
DATA WRITE CHECK IN RAM PACK	RM
DATA WRITE IN PRINTER	LP
MEMORY DUMP	DM
SETTING AND COUNTING TIME	TM
DISPLAY CHECK	DP
DATA WRITE AND READ IN CMT	MT
AUTO-POWER-OFF CHECK	AP
MEMORY LOOP CHECK	AP Y
KEY ENTRY CHECK	KB
DATA TRANSFER/RECEIVE THROUGH RS-232C PORT	
DATA RECEIVE	ML
DATA TRANSFER	MS
FDD READ/WRITE CHECK	FD

Note: This test program cannot check the internal main RAM of 8K bytes.

8-2. PREPARATION

Before start this program, you must have a FP-200 to be checked, a working FP-1021FD, AC adaptor AD4180, and the diskette of the test program ready before proceeding to the steps below.

2-1. First remove the power battery pack from the unit and insert the pack from FDD unit FP-1021FD.

2-2. Connect the power jack from the adaptor into the unit. The female jack locates on your right hand.

2-3. Turn on the power of the FP-1021FD first, then the FP-200.

2-4. Set the dialect selection switch to BASIC.

2-5. Insert the test program diskette slowly into the drive unit. This diskette must remain in operation in the drive unit until the testing ends.

DATA WRITE CHECK IN RAM PACK

Enter RM ↵

This command writes formatted data in designated RAM pack by you and then verifies that data. After verification, regardless of its result, the indication shows the result of each RAM IC 1 to 4 in the RAM pack as shown in Fig. 6.

Fig. 6 shows erratic verification in RAM pack No. 3 and, RAM IC numbers, RAM address, erratic data, and original data.

```
PACK NO. = 3

RAM 1: E000 FF FF 00
RAM 2: E800 FF FF 00
RAM 3: F000 FF FF 00
RAM 4: F800 FF FF 00

PACK NO. = _
```

Fig. 6

DATA WRITE IN PRINTER

Enter LP ↵

This command outputs data, character code 20H-FFH and 0DH, to the printer FP-1012PR or FP-1011PL. One of printing out example is shown in Fig. 7. Of course, before executing this command, printer FP-1012PR or FP-1011PL must be connected while all units are turned off.

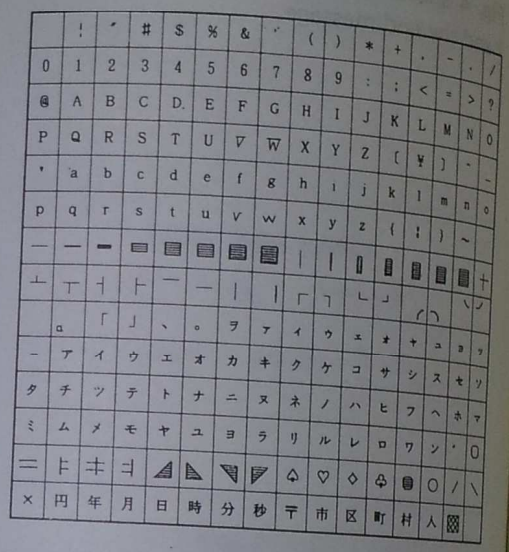


Fig. 7 PRINTING OUT ON FP-1011PL

MEMORY DUMP

1. Enter DM ↵
2. Enter starting address ↵
3. Enter end address ↵
4. Enter D or P ↵

This command is used to dump memory contents in memory address anywhere between 0000H and FFFFH. You can designate any memory address area and also select the output device, a display or printer. Data is printed by two digits hexadecimal notation.

First enter start address then end memory address, and D or P, referring as to the display or the printer, consecutively.

```
START ADDRESS = FFF0

END ADDRESS = FFFF

[D] OR [P] ?D

FFF0  FF  FF  FF  FF
FFF4  FF  FF  FF  FF
```

Fig. 8

SETTING AND COUNTING TIME

Enter TM ↵
Enter year (two digits) ↵
Enter month (two digits) ↵
Enter date (two digits) ↵
Enter hour (two digits) ↵
Enter minute (two digits) ↵
Enter second (two digits) ↵

After entering data for the year, month, date, hour, minute, and second, in proper number, be sure that indication shows all these data and counting of time on the LCD as shown in Fig. 10.

To terminate this counting mode, enter ↵ and Y.

Fig. 9

```
*** CLOCK CHECK ***
YY = 83
MO = 07
DD = 07
HH = 10
MM = 26
SS = 50
```

↓

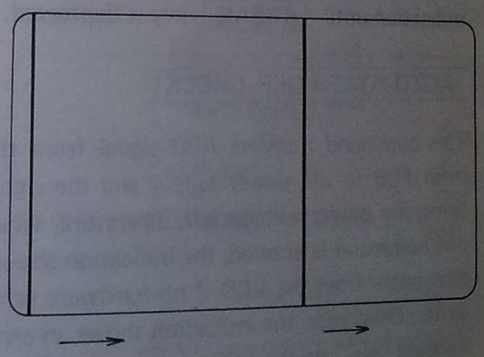
```
*** CLOCK CHECK ***
83 Y 07 M 07 D
10 H 26 M 50 S
```

Fig. 10

DISPLAY CHECK

Enter DP ↵

This command draws two vertical lines, one from left to the center and the other from the center to right, simultaneously first, then two horizontal lines, one from top to the center and the other from the center to bottom, simultaneously, so that each dot on the LCD can be checked, it takes about 40 seconds to complete the operation.



Lines move this way.

Fig. 11

DATA TRANSFER/RECEIVE THROUGH RS-232C PORT

This check is used for data transfer and receive between two RS232C ports of FP-200. The data, 1, 2, 4, 8, 10, 20, 40, 80H, is transferred by the command MS and is received by the command ML.
Configuration for this check mode is that you must have another FP-200 with the "ML" program loaded and the receive side must be in receive mode to load data in (the command ML must be executed) before transferring data. In addition to above setting, you must make wiring between the two cables, FP-280RSC as shown in Fig. 17.

RECEIVE SIDE

1. Enter ML ↵ and Y (if both sides are ready)

After receiving data at the receive side, data is verified with original data and its result is indicated by message "OK" or "ERROR."

TRANSFER SIDE

2. Enter MS ↵ and Y (if both sides are ready)

FDD READ/WRITE CHECK

This command firstly formats a diskette and then write and read data in all sectors and tracks, 0 – 34.
During the operation, sector and track numbers where data is written and is read are shown on the LCD. When the operation ends, the result is indicated by "OK" for correct, or "ERROR" for erratic read/write operation.

1. Enter FD ↵
2. After the program is loaded, remove the test program diskette from the drive and insert a work diskette instead.
3. Enter Y when it is ready for formatting. The formatting should end in 20 seconds.
4. Then data is automatically written.

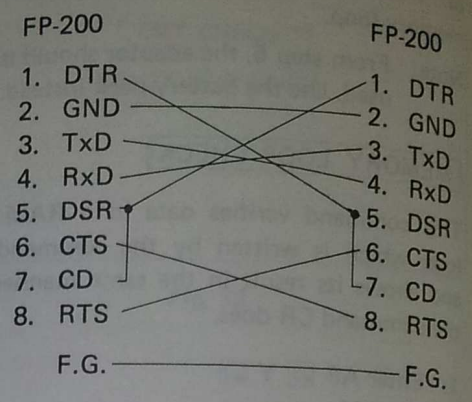


Fig. 17 WIRING FOR THE CHECK MODE

```
**** FDD CHECK ****
TRACK  = 34
SECTOR =  8
****** OK ******
END? Y OR N = _
```

Fig. 18