1. Description

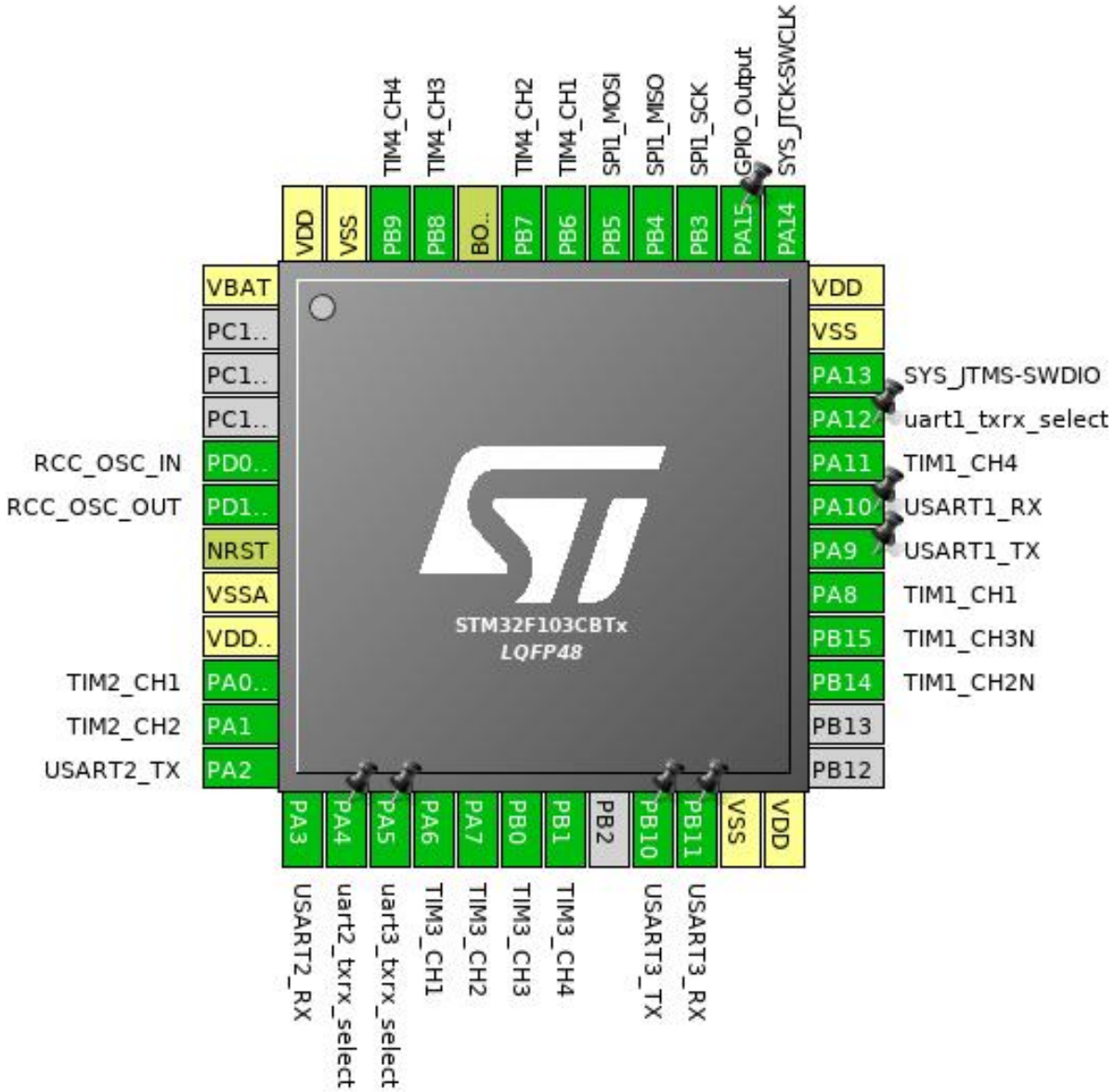
1.1. Project

Project Name	abry_controller
Board Name	abry_controller
Generated with:	STM32CubeMX 4.21.0
Date	09/04/2017

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103CBTx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration



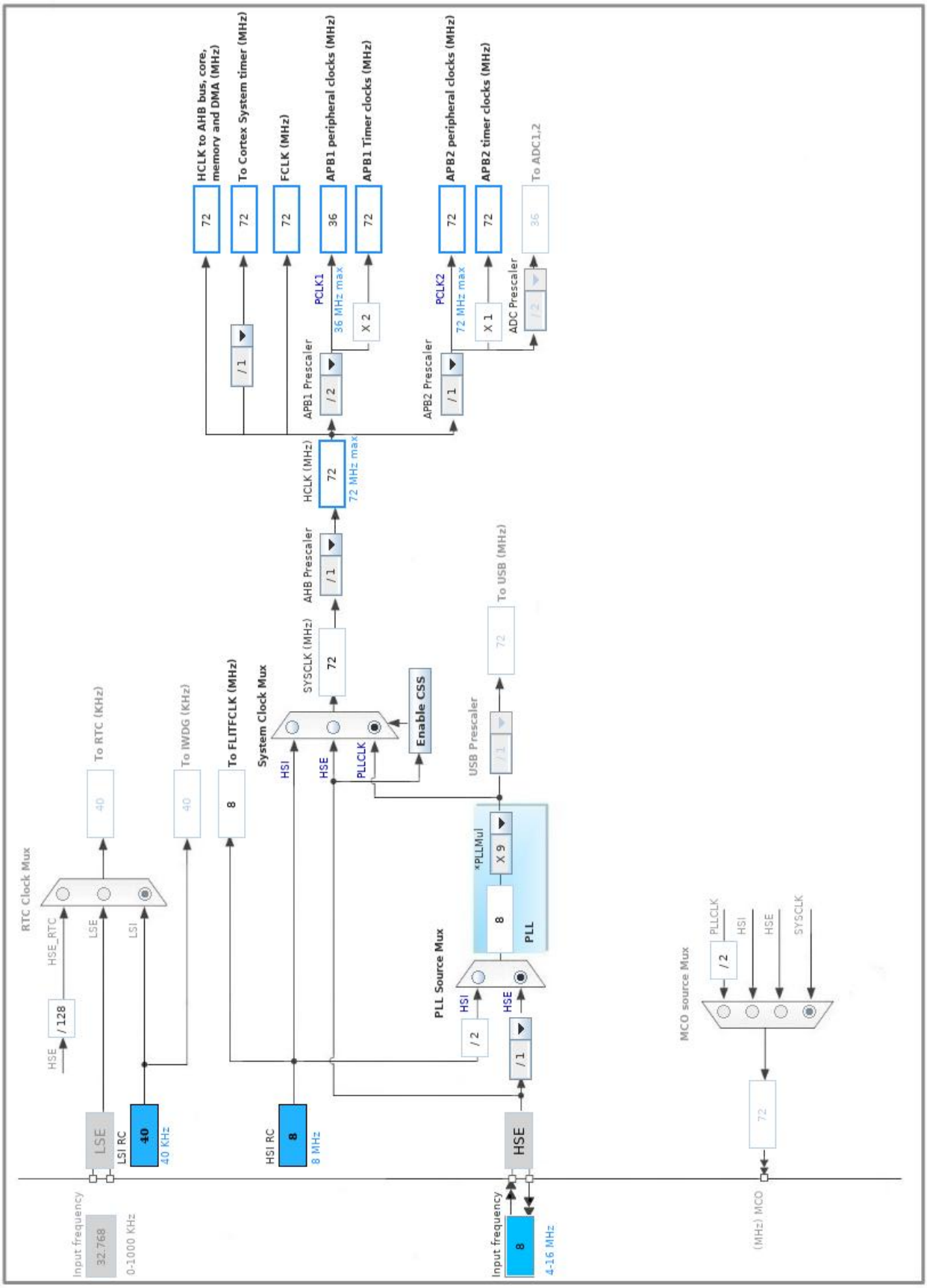
3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	TIM2_CH1	
11	PA1	I/O	TIM2_CH2	
12	PA2	I/O	USART2_TX	
13	PA3	I/O	USART2_RX	
14	PA4 *	I/O	GPIO_Output	uart2_txrx_select
15	PA5 *	I/O	GPIO_Output	uart3_txrx_select
16	PA6	I/O	TIM3_CH1	
17	PA7	I/O	TIM3_CH2	
18	PB0	I/O	TIM3_CH3	
19	PB1	I/O	TIM3_CH4	
21	PB10	I/O	USART3_TX	
22	PB11	I/O	USART3_RX	
23	VSS	Power		
24	VDD	Power		
27	PB14	I/O	TIM1_CH2N	
28	PB15	I/O	TIM1_CH3N	
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
32	PA11	I/O	TIM1_CH4	
33	PA12 *	I/O	GPIO_Output	uart1_txrx_select
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
38	PA15 *	I/O	GPIO_Output	
39	PB3	I/O	SPI1_SCK	
40	PB4	I/O	SPI1_MISO	
41	PB5	I/O	SPI1_MOSI	
42	PB6	I/O	TIM4_CH1	

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
43	PB7	I/O	TIM4_CH2	
44	BOOT0	Boot		
45	PB8	I/O	TIM4_CH3	
46	PB9	I/O	TIM4_CH4	
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.2. SPI1

Mode: Full-Duplex Master

5.2.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**18.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.4. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2N

Channel3: PWM Generation CH3N

Channel4: PWM Generation CH4

5.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0x5a ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2N:

Mode	PWM mode 1
Pulse (16 bits value)	0

Fast Mode	Disable
CHN Polarity	High
CHN Idle State	Reset

PWM Generation Channel 3N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CHN Polarity	High
CHN Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.5. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0

Fast Mode	Disable
CH Polarity	High

5.6. TIM3

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0

Fast Mode	Disable
CH Polarity	High

5.7. TIM4

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0

Fast Mode	Disable
CH Polarity	High

5.8. USART1

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	**1000000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.9. USART2

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**1000000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.10. USART3

Mode: Asynchronous

5.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**1000000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	n/a	**High ***	
	PB4	SPI1_MISO	Input mode	No pull-up and no pull-down	**n/a**	
	PB5	SPI1_MOSI	Alternate Function Push Pull	n/a	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PB14	TIM1_CH2N	Alternate Function Push Pull	n/a	Low	
	PB15	TIM1_CH3N	Alternate Function Push Pull	n/a	Low	
	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	
	PA11	TIM1_CH4	Alternate Function Push Pull	n/a	Low	
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	n/a	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	n/a	Low	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	n/a	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	n/a	Low	
	PB0	TIM3_CH3	Alternate Function Push Pull	n/a	Low	
	PB1	TIM3_CH4	Alternate Function Push Pull	n/a	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	n/a	Low	
	PB7	TIM4_CH2	Alternate Function Push Pull	n/a	Low	
	PB8	TIM4_CH3	Alternate Function Push Pull	n/a	Low	
	PB9	TIM4_CH4	Alternate Function Push Pull	n/a	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	**High ***	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	**High ***	
	PA3	USART2_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART3	PB10	USART3_TX	Alternate Function Push Pull	n/a	**High ***	
	PB11	USART3_RX	Input mode	No pull-up and no pull-down	**n/a**	
GPIO	PA4	GPIO_Output	Output Push Pull	n/a	Low	uart2_txrx_select
	PA5	GPIO_Output	Output Push Pull	n/a	Low	uart3_txrx_select

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA12	GPIO_Output	Output Push Pull	n/a	Low	uart1_txrx_select
	PA15	GPIO_Output	Output Push Pull	n/a	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low
USART3_TX	DMA1_Channel2	Memory To Peripheral	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
TIM2_CH1	DMA1_Channel5	Memory To Peripheral	Low
TIM3_CH1/TRIG	DMA1_Channel6	Memory To Peripheral	Low
TIM4_CH1	DMA1_Channel1	Memory To Peripheral	Low
TIM1_CH2	DMA1_Channel3	Memory To Peripheral	Low

USART2_TX: DMA1_Channel7 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

USART3_TX: DMA1_Channel2 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

TIM2_CH1: DMA1_Channel5 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable

Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	**Byte ***

TIM3_CH1/TRIG: DMA1_Channel6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

TIM4_CH1: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

TIM1_CH2: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	**Byte ***

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
USART1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
USART3 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103CBTx
Datasheet	13587_Rev17

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	abry_controller
Project Folder	/home/erakhorst/ecl_workspace/stm32/stm_workspace/abry_controller/docs
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F1 V1.4.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No