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|  | Experiment 5Hardware Verification of Seven Segment Decoder | Michael Ward Section 308 10/3/2019 |

# 10/3/2019

**Objective**

Upload code from the previous experiment to the Cyclone II and verify that it works.

**Equipment**

AlteraDE2 Board, Altera Cyclone II FPGA, Quartus II Software

## Procedure

1. Open the circuit design created in Experiment 4 in Quartus II and compile it.
2. Upload the code to the Cyclone II.
3. Test that all 16 cases work using the switches on the Quartus II.

**Questions** (if applicable)

1. **How many configurable logic elements does your design contain?**7
2. **What is the worst case propagation delay of your circuit in nanoseconds?**7.491
3. **Which path (specified as input pin to output pin) has the worst case delay?**y -> pin\_a

## Results & Conclusion

The lab was successful. Every segment worked fine. A small sample is shown in figures 1 and 2.

## Printouts, Tables, Figures

Figure 1: A displayed on seven segment display

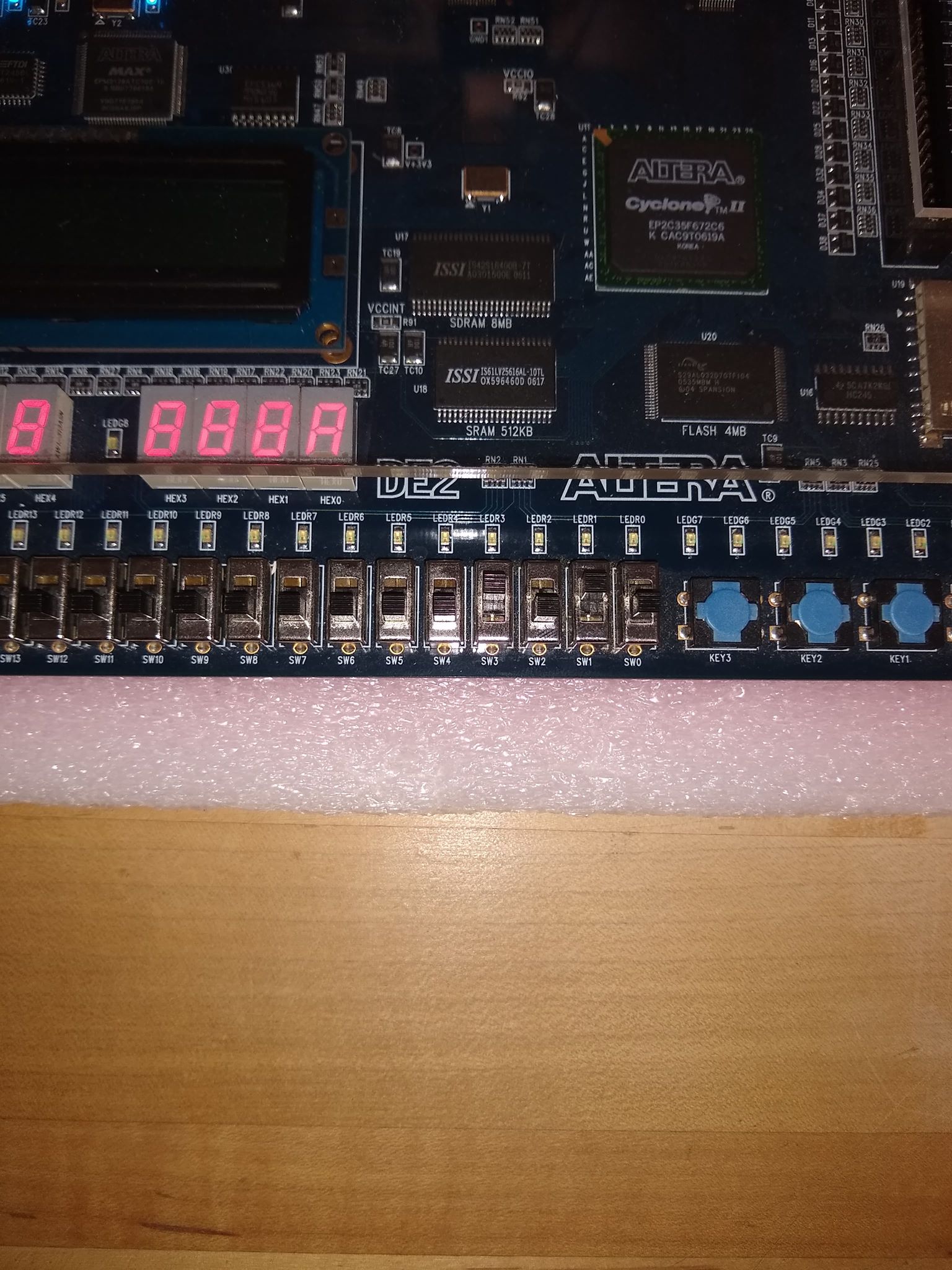


Figure 1: 6 displayed on seven segment display

