DCC commands

This description of DCC control orders is organized in 2 parts.

First an overview of the structure of the orders with a brief/short description of the byte and bit content. This include the total set of bits in a message.

Then we leave out the PreAmple, Separators and the XOR byte concentrating on a deeper explanation of the remaining bytes and bits.

The 2 parts are connected through the **RED TEXT**, which act as a kind of index. Bit Values in **Bold** indicate key values for that Byte, i.e. the interpretation of the remaining bits depend upon this key.

This document is based upon Jens Klarskovs text to the Embedded C-Programming course at KEA (Copenhagens School of Design and Technology). A text which is based upon:

General Packet Format:

https://www.nmra.org/sites/default/files/s-92-2004-07.pdf

Extended Package Format:

https://www.nmra.org/sites/default/files/s-9.2.1 2012 07.pdf

both kept at the National Model Railroad Associations, Inc. homepage.



		Loc	o * Sm	nall	Address * Speed	
Bit number	Byte number	Name	Bit value		Short Explanation Text in blue : see Glossary	
0			1			
1			1			
2			1			
3			1			
4	Ę	1				
5		PREAMPLE	1		A sequence of at least 10 bits set to 1.	
6		EAI	1		16 is a good choice.	
7		PR	1		To is a good enoise.	
8		_	1			
9			1			
10			1			
11			1			
12			0		Separating bit	
13			0		0 means 7 bit short address	
14		ш	A7			
15	1	37.1	A6			
16	Ę.	SSI	A5		Short loco address (7 bit)	
17	BYTE 1	ADDRESSBYTE	A4		A7 A6 A5 A4 A3 A2 A1 1 <= value <= 127	
18	Ш	αα	A3		0 is NOT allowed	
19		AI AI	A2		o is itel allowed	
20			A1			
21			0		Separating bit	
22			0		0	
23			1		1 means speed & direction command	
24	6	MAND	D		D = 0 backward = 1 forward	
25	Ë 2		C = S1		C = 0 (see Speed below)	
26	вуте	COMMA	S5		Loco speed :	
27	ш	<u> </u>	S4		S5 S4 S3 S2 S1	
28		O	S3		Easy version: 4 bits = 16 speed values	
29			S2		0 S4 S3 S2 S1	
30			0		Separating bit	
31			X8			
32		/TE	X7			
33	~	8	Х6			
34	Ë 3	JO NC	X5		All bits are binary XOR:	
35	ВУТЕ 3	ERROR DETECTION BYTE	X4		BYTE 1 XOR BYTE 2	
36		E	Х3			
37		Œ	X2			
38]	X!			
39			1		End of message bit	



Loco *	Small Address	*	Light & Sound

Bit number	Byte number	Name	Bit value	Short Explanation Text in blue : see Glossary
0			1	
1			1	
2			1	
3			1	
4		٣	1	A sequence of at least
5		₹	1	10 bits set to 1.
6		PREAMPLE	1	16 is a good choice.
7		PR	1	Identical to Loco * Small Address *Speed
8		_	1	
9			1	
10			1	
11			1	
12			0	Separating bit
13			0	0 means 7 bit (short) address
14		ш	A7	
15		ADDRESS BYTE	A6	Short loco address (7 bit)
16	Н	SS	A5	A7 A6 A5 A4 A3 A2 A1
17	ВУТЕ	ES .	A4	1 <= value <= 127
18	~	Ö	А3	0 is NOT allowed.
19		AC	A2	Identical to Loco * Small Address *Speed
20			A1	
21			0	Separating bit
22			T4	
23			Т3	Tn bits shows which
24	61	2	T2	set of Functions are on or off
25	Ë	¥ Z	T1 / U5	
26	ВУТ	8 ₹	U4	F0 - F4; F8 - F5; F12-F9; F16-F13
27	ш	COMI	U3	
28		0	U2	
29			U1	
30			0	Separating bit
31			X8	
32		Ë	X7	
33	BYTE 3	<u>9</u>	Х6	
34		Ö NO	X5	All bits are binary XOR:
35		ERROR DETECTION BYTI	X4	BYTE 1 XOR BYTE 2
36			Х3	
37		Ä	X2	
38			X1	
39			1	End of message bit



Accessory * Signal * Switch

Bit number	Byte number	Name	Bit value	Explanation Text in blue : see Glossary	
0			1		
1			1		
2			1		
3			1		
4		Ä	1		
5		Σ̈́	1	A sequence of at least	
6		EA	1	10 bits set to 1. 12 is a good choice.	
7		PREAMPLE	1	12 is a good choice.	
8			1		
9			1		
10			1		
11			1		
12			0	Separating bit	
13			1	10 means short 9 bit accessory address	
14	BYTE 1		0		
15		S1	A6	A9 A8 A7 A6 A5 A4 A3 A2 A1	
16		ES	A5	NOTE: ^A9 ^A8 ^A7 is in next byte	
17		DR	A4	Is calculated from the track layout address	
18		ADDRESS1	A3	See here	
19			A2		
20			A1		
21			0	Separating bit	
22			1		
23		્	^A9	NOTE:	
24	-	D S2	^A8	^A9 ^A8 ^A7	
25	É 2	AN	^A7	1 complement to the values used above	
26	BYT	COMMA	С	0 off 1 on	
27	•	AD A	D1	lead outstand U	
28		\mathbf{z}	D2	local register address	
29			Е	== 0 turn / red == 1 straight / green	
30			0	Separating bit	
31			X8		
32		Ë	X7		
33	•	~ 6	X6		
34	BYTE 3	P S	X5	All bits are binary XOR:	
35		R. T.	X4	BYTE 1 XOR BYTE 2	
36		m	BYTE 3 ERROR DETECTION BYTE	Х3	
37		Ĕ	X2		
38			X1		
39			1	End of message bit	



GLOSSARY

Ir	Index num		Bit value								
Loco *	Loco * Small Address * Speed & Registers										
	Small Ad	8	0	0 means 7 bit short address							
		7	A7								
	(0	6	A6	A7 A6 A5 A4 A3 A2 A1							
1	ES	5	A5	A7 A6 A5 A4 A3 A2 A1							
ВУТЕ	ADDRESS	4	A4	127 >= value >= 1							
—	ΑΓ	3	A3	0 is NOT allowed.							
		2	A2								
		1	A1								
Loco *	Small Ad	dress * Sı	peed								
		8	0	0							
	COMMAND	7	1	1 means Speed and Direction							
		6	D	D = 0 backward = 1 forward							
E 2		5	C = S1								
BYTE 2	Σ	4	S5	Easy Speed is 16 possible steps using S5 S4 S3 S2 and let S1=0.							
	00	3	S4	S5 S4 S3 S2 S1							
		2	S3	$0 \ 0 \ 0 \ 0 = stop$.							
		1	S2	0 0 0 1 0 = emergency stop							
Loco *	Small Ad	dress * R	egisters								
		8	1	1							
		7	0	0 means F registers							
	COMMAND	6	0								
E 2		5	F0	Light : 0 = off 1 = on							
BYTE		4	F4	Bell : 0 = off 1 = on							
_		3	F3	Horn2 : 0 = off 1 = on							
		2	F2	Horn1: 0 = off 1 = on							
		1	F1	Sound : 0 = off 1 = on							



Index		Bit number	Bit value									
Loco *	Small Ad	dress * Lig		ınd								
		8	0		0 mean	s 7 bit (sho	ort) loco ado	dress				
		7	A7									
	SS	6	A6									
Ë 1	RES	5	A5						A7 A6 A5 A4 A3 A2 A1			
ВУТЕ	ADDRESS	4	A4						127 >= valua >= 1			
		3	A3		127 >= value >= 1 0 is NOT allowed.							
		2	A2					Identio	al to Loco * Small Address *Speed			
		1	A1						·			
Loco *	Small Ad	dress * Lig	ght & Sou	ınd								
		8	T4		1	1	1	1				
	COMMAND	7	Т3		0	0	0	1				
		6	T2		0	1	1	0				
Ë 2		5	T1 / U5		F0	1	0	1				
BYTE		4	U4	7	F4	F8	F12	F16				
ш		3	U3		F3	F7	F11	F15	FO is Light on / off			
		2	U2		F2	F6	F10	F14	F1F15 are functionalities in the sound decoder			
		1	U1		F1	F5	F9	F13				



Index		Bit number	Bit value				
Accesso	ory * Si	gnal * Swi	itch				
		8	1				
		7	0				
1	SS	6	A6				
	Ř	5	A5	layoutAddr is the address (number), that is defined in the track layout			
ВУТЕ	ADDRESS	4	A4	(A. A. A			
ш	AE	3	А3	(AccAdr : Accessory Address A9 A8 A7 A6 A5 A4 A3 A2 A1) = ((layoutAddr / 4) + 1) & 63, Where / is an integer division (i.e. without remainder)			
		2	A2	where 7 is an integer division (i.e. without remainder)			
		1	A1				
Accesso	ory * Si	gnal * Swi	tch				
		8	1				
	∞	7	~A9				
	. ~	6	~A8	~A9 ~A8 ~A7			
BYTE 2	COMMAND ADDRESS2	5	~A7	Is the complementary values to the bits in AccAdr			
		4	С	= 0 off = 1 on Note: Send this order with C == 1 and then send it with C == 0			
	ON AC	3	D2	RegAdr: Register Address D2 D1) = (layoutAddr % 4) - 1			
	Ö	2	D1	RegAdr < 0 is NOT allowed If (RegAdr < 0) then {RegAdr = 3; AccAdr}			
		1	Е	if switch (== 0 turn == 1 straight) if signal (== 0 red == 1 green)			

