Experiment: 1 — Sum of N natural numbers

Experimental Procedure:

1. Design a digital block to compute the sum of first N natural numbers where N is the given 3-bit input.
2. Use a three state FSM to control the data flow. The states are IDLE, BUSY and DONE. The module has to wait till it receives an ack from the subsequent module to move to IDLE state and accept any new input.
3. Implement the design and develop a simple testbench for verifying the DUT.
4. Clearly draw the architecture, name all the intermediate signals, neatly divide combinational and sequential logic portions, write a readable Verilog code and report the results with waveforms and observations. Everything carries weightage.