Experiment: 3 — Sum of factorials

Experimental Procedure:

1. Design a digital block to compute the sum of factorials upto given input N, i.e.,

   Sum $= 1! + 2! + 3! + ... + N!$

   using the following three different approaches

   (a) Direct implementation using two down counters (for two "for" loops) and hand-shaking with factorial computation block and properly synchronising the data flow using a control FSM.

   (b) Refine your design to use a single up counter, sum and prod registers.

   (c) Fully optimize your design to use a single down counter and a single sum register.

   N is a 3-bit unsigned integer input. You can assume a simple interface with N_valid and Sum_valid for input and output respectively. In each case, comment on the critical path of the architecture and number of clock cycles to compute the sum in the worst case. Show the worst case computation in the waveform to verify your analysis.