Experiment: 2 GCD of two numbers

Experimental Procedure:

1. Design a digital block to compute the GCD of two given numbers. Assume inputs to be of 8-bit each.
2. Use a three state FSM to control the data flow. The states are IDLE, BUSY and DONE. The module has to wait till it receives an ack from the subsequent module to move to IDLE state and accept any new inputs.
3. Divide the design into control path and data path, clearly show the control/status hand-shake signals, implement the hierarchical design in Verilog (i.e., one module for control path, one module for data path and one top level module to connect them), develop a simple testbench to verify the DUT.