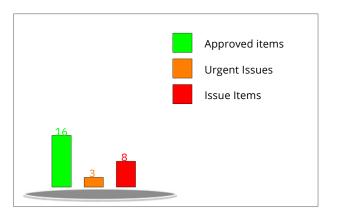


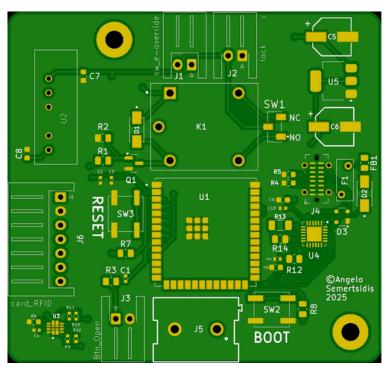
## HQDFM Design for Manufacture(DFM) Report

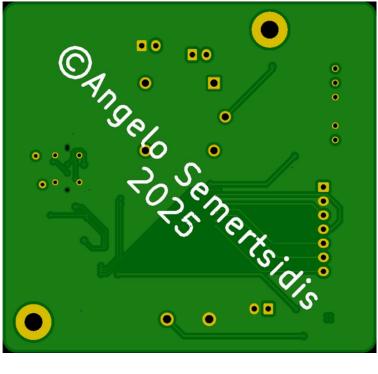
File name: 0000A542351\_1

Time: 2025-09-25Layer count:4 PCB Thickness: 1.60 Quantity: 5 mm



	Trace Width/Spacing	4.00/8.00mil
	Milling Density	62.7329m/m²
Basic Board Specs	Surface Finish Area	14.30%
	Test Point Count	221





## PASS WITH ERRORS

Туре	Category	No. of Checks	Result
	Smallest Trace Width	1	Pass 2 , Fail 2
	Smallest Trace Spacing	3	Pass 149 , Fail 41
	SMD Pad Spacing	2	Pass 66
	Pad Size	3	Pass 23 , <mark>Fail 1</mark>
	Hatched Copper Pour	2	Pass
PCB Trace Analysis	Annular Ring Size	2	Pass 4 , Fail 4
	Drill to Copper	5	Pass 178 , Fail 26
	Signal Integrity	4	Fail 12
	Copper-to-Board Edge	2	Pass 32
	Holes on SMD Pads	4	Fail 4
	Open/Shorts (IPC)	1	Fail
	Drill Diameter	8	Pass 78 , <mark>Fail 6</mark>
	Drill Hole Density	1	Pass
	Drill Diameter	8	Pass 78 , <mark>Fail 6</mark>
PCB Drilling Analysis	Drill Spacing	4	Pass 3
	Drill to Board Edge	4	Pass
	Drill Hole Density	1	Pass
	Special Drill Holes	2	Pass
DCD Coldon Marsh Arraharia	Solder Mask Dam	2	Pass 8 , Fail 25
PCB Solder Mask Analysis	Missing SMask Opening	1	Pass
PCB Silk Analysis	Silkscreen Spacing	1	Fail
PCBA Fiducial Analysis	Fiducial Count	1	Pass

ID	Check	Limits	Value	Issue	Image	Position	Qty	Level
1	Drill Diameter_ Aspect Ratio	12,10,8	0.10 mm	For most factories, the aspect ratio is 8:1 to 10:1 (Depth of hole/Diameter of hole). Smaller aspect ratios require higher throwing power to ensure the interior of the holes are fully plated. Failure to meet the factory's requirements could increase the risk of incomplete plating of the hole, which decrease manufacturing efficiency and yield, and affect the reliability of the boards. Aspect ratio of 16.00was detected in your design. The drill sizes and board thickness should be modified to reduce the aspect ratio to at least 8:1.		152.25,-97.75	24	Risk
2	Drill Diameter S mail Drill Size	est 2,0.25,0	0.10 0.3 mm	For most factories, the smallest (mechanical) drill hole size requirement is Smaller drill bits need to be replaced likely to result in misalignment and hole wall roughtest, which decrease manufacturing efficiency and yield rine appropriate the requirements. Drill holes require laser drilling and requirements. Drill holes requirements. Drill holes defected in your design it is advisable to increase the diameter want to avoid additional costs.		152.25,-97.75	24	Risk

3 W	Smallest Trace (idth_Sma llest Trace Width	3.5,4,5	0.10 mm	Traces 3.94mil in width were detected in your design. This could result in overetched traces, which decrease manufacturing efficiency and yield, and affect the reliability of the boards. It is recommended to increase the width to at least 6 mil for regular routing and at least 4 mil in high density areas, such as when routing fine pitch BGA s.	154.50,-104.50	2	Warnin g
4	Smallest Trace Spacing_S MD Pad Spacing	3.5,4,5	0.02 mil	For most factories, the minimum pad-to-pad spacing requirement is around 3-4 mil. Failure to meet the factory's requirement could result in incomplete solder mask dams between the pads, thereby increasing the risk of incomplete etching of the pads, which decrease manufacturing efficiency and yield, and affect the reliability of the boards. Pad-to-pad spacings of 1.97mil were detected in your design. The spacing should be at least 6 mil where possible. For solder mask covered pads, 4 mil spacing is sufficient.	160.50,-114.25	6	Risk

5	Smallest Trace Spacing_Tr ace-to-Pad Spacing		0.02 mil	For most factories, the minimum trace-to-pad spacing requirement is around 3.0-4.0 mil, with 3.5 mil or less requiring tighter quality control. Failure to meet the factory's requirement could result in insufficient solder mask covering the trace or excess solder mask covering the pad, which decrease manufacturing efficiency and yield, and affect the reliability of the boards. Trace-to-pad spacings of 0.02mil were detected in your design. The spacing should be at	118.58,-124.10	44	Risk
6	Pad Size_Long Pads	7,9,10	0,20 mm	Rectangular/Oblong pads of wighth U.20mm were detected in Jour design. Which were possible of the control of th	119.98,-123.25	11	Warnin

7	A nnular Ring Size_Via A nnular Ring	4,5,6	0,05 mm	Min via annular rings I ed in vour design. It detected in your design. It will affect production efficiency and electrical recommended that the rinimum ring size for via annular rings be ≥5 mils.	119.75,-122.85	5	Risk
8	Drill to Copper_Vi a-to-Trace [Outer]	8,10,12	5.91 mil	For most factories, the via to trace clearance requirement in outer copper layers is at least 8 mil. Failure to meet the factory's requirement could increase the risk of defects such as short circuits, which decrease manufacturing efficiency and yield, and affect the reliability of the boards. Via to trace spacing (outer layer) of 5.91mil was detected in your design. The spacing should should be at least 10 mil.	143.85,-106.44	76	Risk

9	Drill to Copper NP Copper	8,10,12	0.15 mm	NPTH to copper spacing of 9.86 mil was detected in 9.86 mil was detected in 9.86 mil was detected in 19.86 mil was detected in 19.86 mil was short circuits which deficiency manufacturing affect the reliability of the boards of the position of the spacing to at least 12 mil.	166.10,-93.32	8	Risk
10	Signal Integrity_U nconnecte d Vias	7,7,7	Error(s) detect	Isolated areas of copper (floating copper) were detected in your design, Leaving Isolated areas of copper unforced as of cause them to act as an earn as and can affect signal integrity. We suggest removing or grounding	143.85,-104.86	12	Risk

11	Holes on SMD Pads_PTH on SMD Pad	-,-,-	100,00	Holes on surface mount pads were detected in your design, buring SWI your assembly, solder could leak solder away from the SMD decrease manufacturing effects the reliability of the boards of the pads if possible.	164.35,-99.15	4	Warnin
12 [	Solder Mask Dam_Solde 1 r Mask-to- Trace	.5,2,2.5	0.00 mm	Solder mask opening to trace spacings less than 0.00mil were detected in your design. This could increase the risk of exposed traces and short circuits, which decrease manufacturing efficiency and yield. If the value is negative, exposed traces were detected in the design which are susceptible to shorts during assembly. The width should be increased to at least 0.08mm.	118.48,-124.09	26	Risk

13	Silkscreen Spacing _Solder Mask-to- Silkscreen	4,5,6	Error(s) detect ed	For most factories, the minimum silkscreen to solder mask spacing requirement is at least 8 mil. Failure to meet the factory's requirements could result in part of the silkscreen being removed or being printed directly on the pads, which decrease manufacturing efficiency and yield, and affect the reliability of the boards. Silkscreen to solder mask spacing of 0 mil were detected in your design. It is recommended to increase the spacing to at least 12 mil.		151.89,-93.67	1	Risk	
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