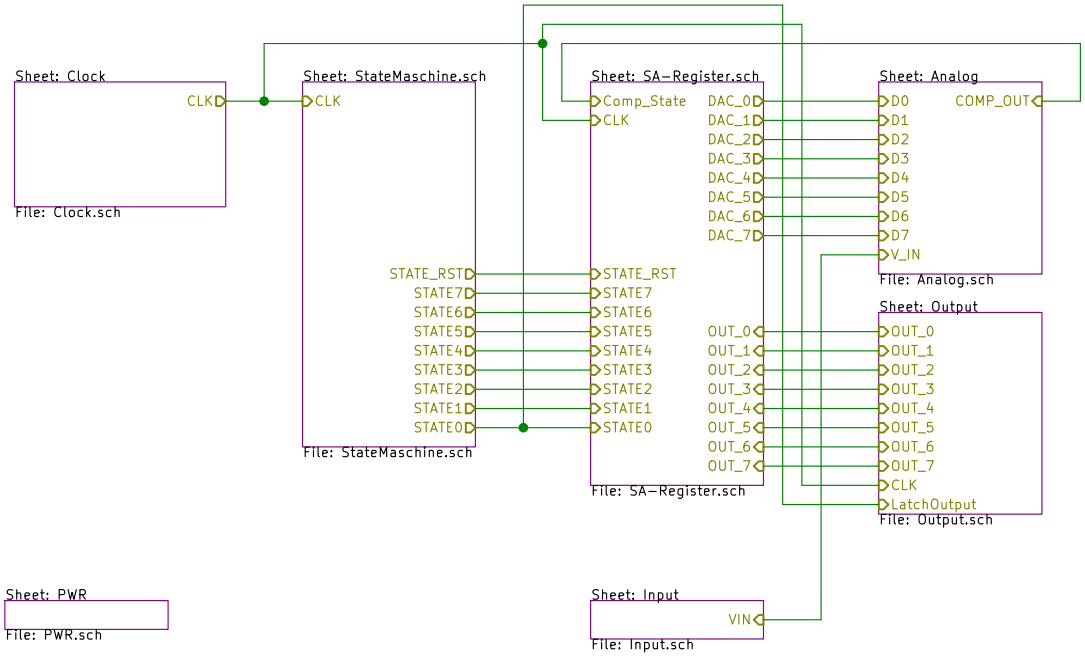


A Discrete Successive-Approximation-ADC

Implemented to learn about/demonstrate the workings of this ADC Architecture, not to design an effective ADC.

Sheets/Breakdown:

PWR:
Power Input & Voltage Regulation

Input:
Analog Voltage Input to the ADC

Clock:
NE555-based clock used to drive state machine. Adjustable in Frequency from approx. 1Hz to 170Hz

State Machine:
The State machine that sequences the conversion.

SA-Register:
The Successive-Approximation (SA) Register used during conversion.

Analog:
The Analog-domain section of the ADC. This includes the comparator and the DAC: An R2R DAC fed by the output of the SA-Register and the state machine.
?This output is buffered to remove switching noise.

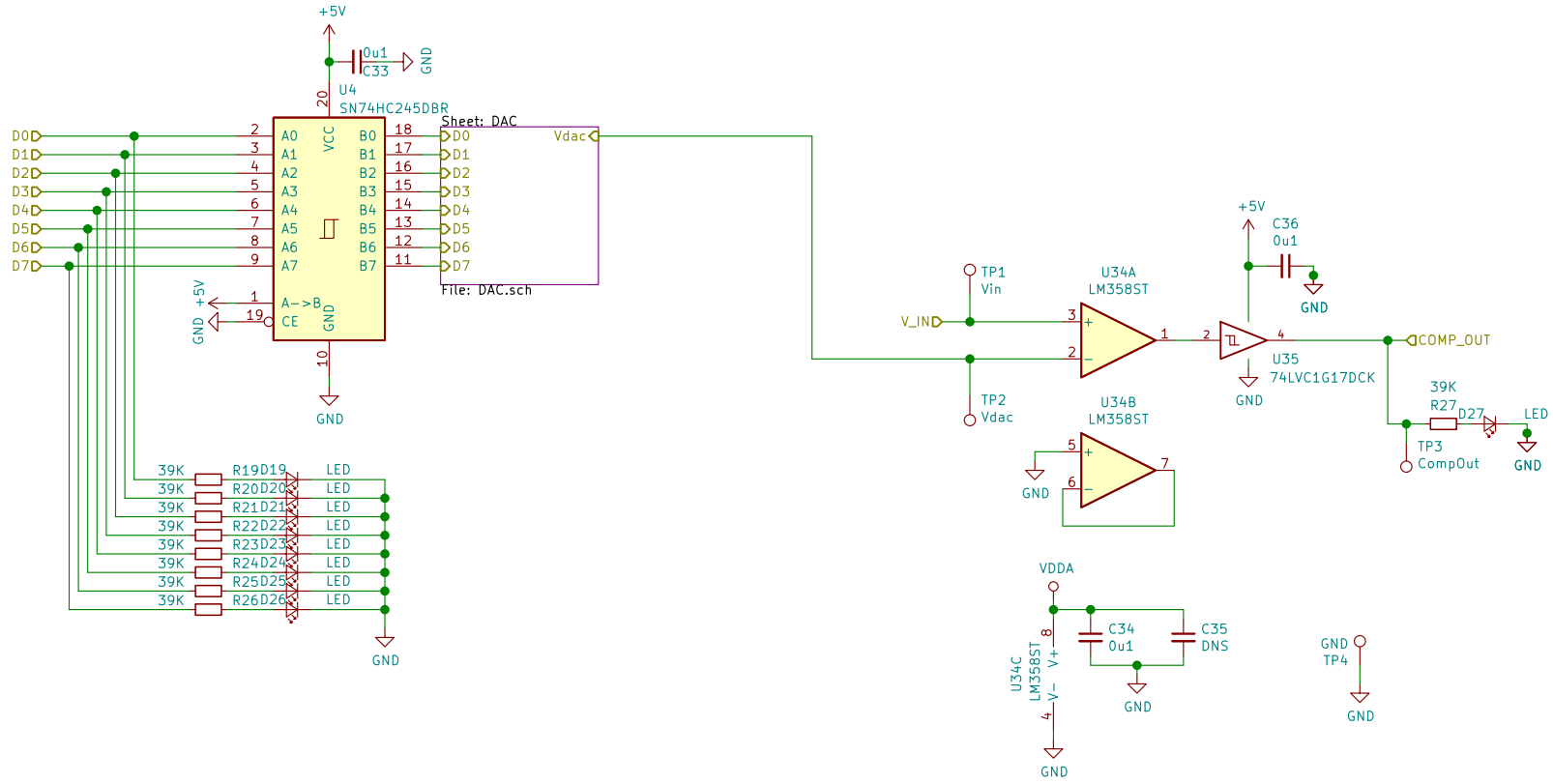
Output:
The output register into which the result is latched once a conversion finishes. Also contains a simple binary Display of the final conversion result.

Philipp Schilk

Sheet: /
File: SA-ADC.sch

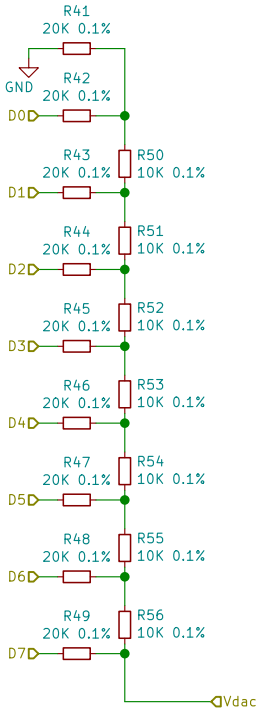
Title: Schilk_SA-ADC

Size: A4	Date: 2020-08-26	**Rev: v0.3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/9



R2R DAC generates the reference voltage dictated by the SA Register and state machine. This voltage is then compared to the input voltage.

Sheet: /Analog/		
File: Analog.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-08-26	**Rev: v0.3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/9

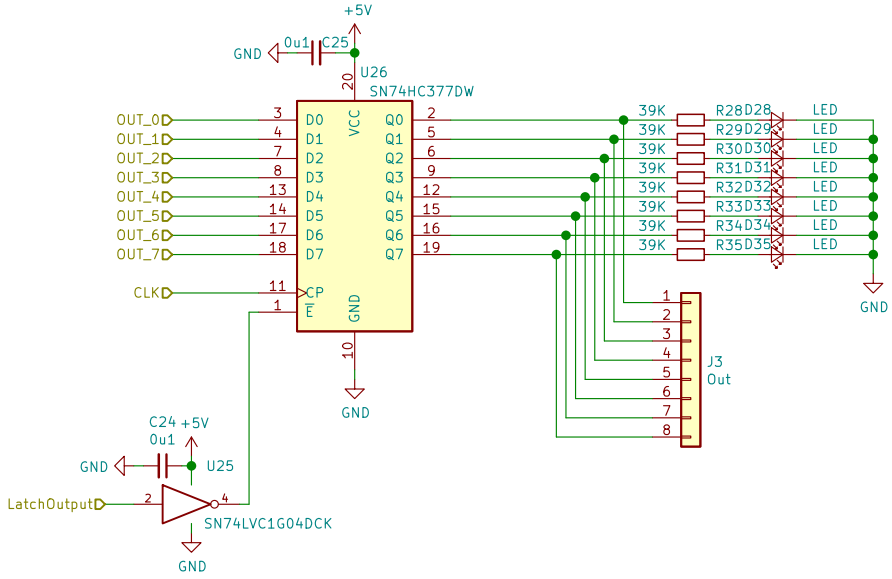


R2R DAC

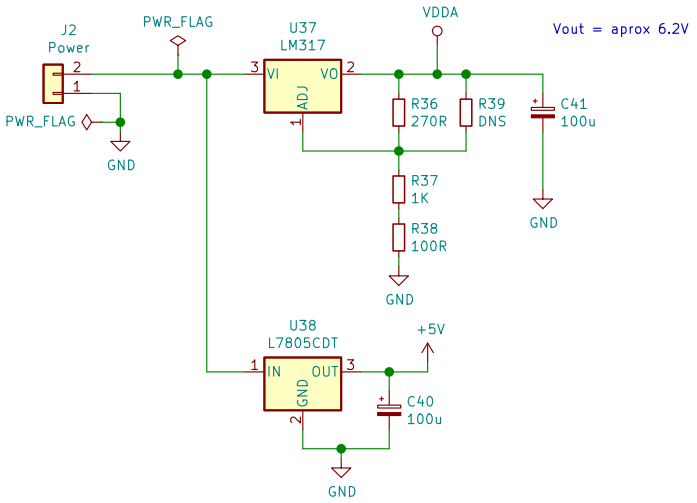
Use Precision Resistors, Optimally <0.5%

Sheet: /Analog/DAC/		
File: DAC.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-08-26	**Rev: v0.3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 3/9

Results are latched into this register to make space
in the SA Register for the next conversion.



Sheet: /Output/		
File: Output.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-08-26	**Rev: v0.3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/9



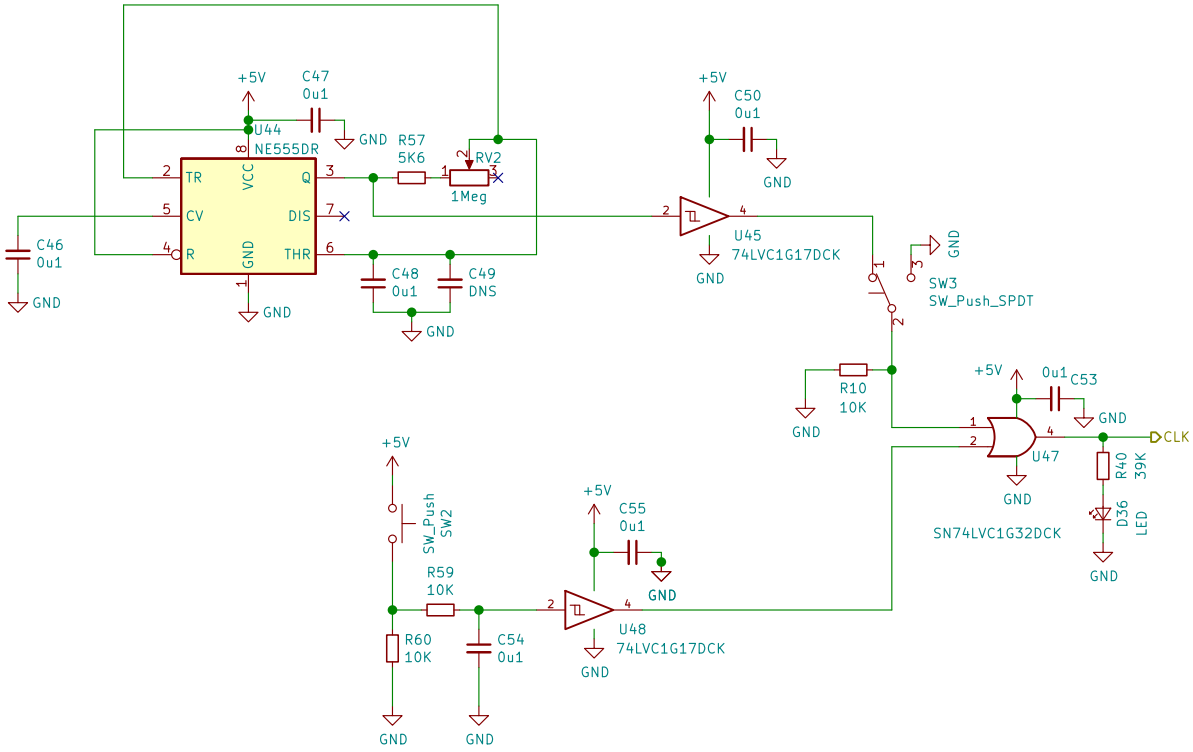
OpAmp used as comparator
needs supply slightly higher than 5v to compare signals close to / at 5v.

Specific voltage was choosen as it both enabled comparing accross
the whole 0–5v band, and resulted in the opamp outputing around 5V as
logic–high. (Output of Opamp ist at max aprox. 1.2–1.3 V lower than Supply Voltage)

H1
MountingHole

H2
MountingHole

Sheet: /PWR/		
File: PWR.sch		
Title: Schilk_SA–ADC		
Size: A4	Date: 2020–08–26	**Rev: v0.3**
KiCad E.D.A. kicad (5.1.5)–3		Id: 5/9

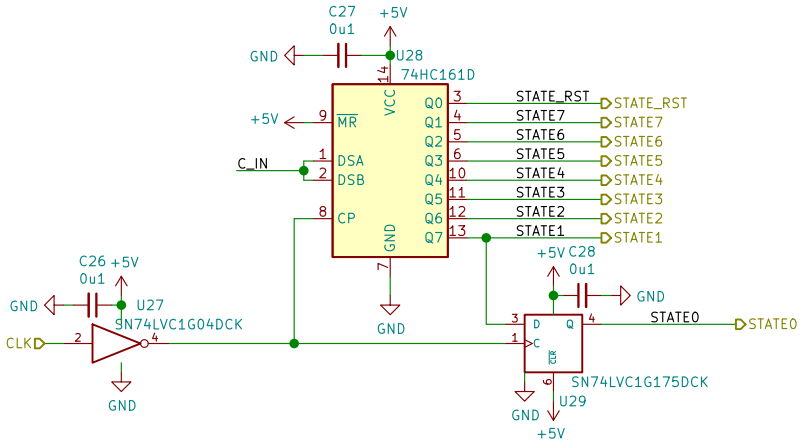


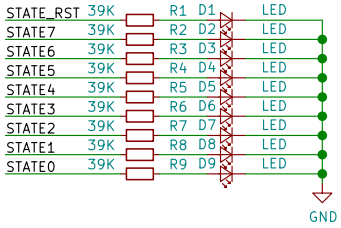
Clock derived from 555 timer may be enabled with JP1.

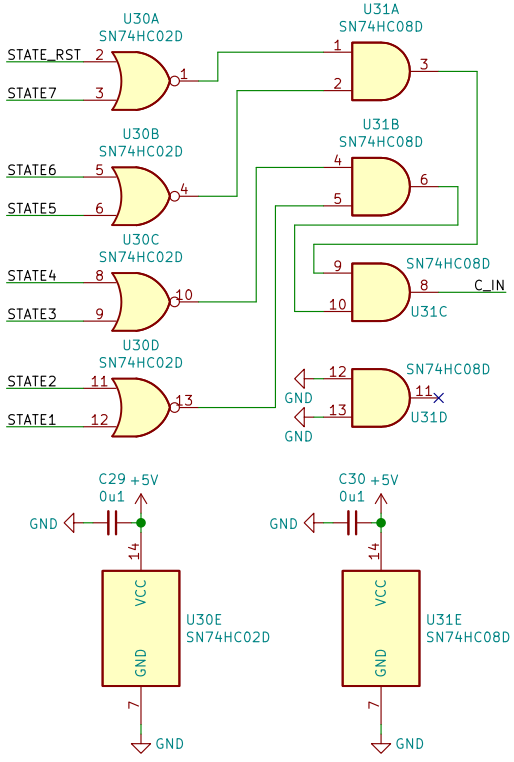
Frequency may be adjusted with RV2

SW2 may be used to manually generate a clock pulse regardless of the position of JP1.

Sheet: /Clock/ File: Clock.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-08-26	**Rev: v0.3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 6/9







Generates the Sequental Signals that decide the state of the converter.

D-FlipFlop U29 essentially provides a 9th stage to the shift register U28

NOR Gates U30 and U31 enable the shift-in signal of the register once the first 8 stages are empty.

During operation it would be sufficient to tie STATE0 to the shift-in, but this circuit ensures proper operation of the state machine after at most 1 cycle through all states, no matter what the initial value of the register after power up is.

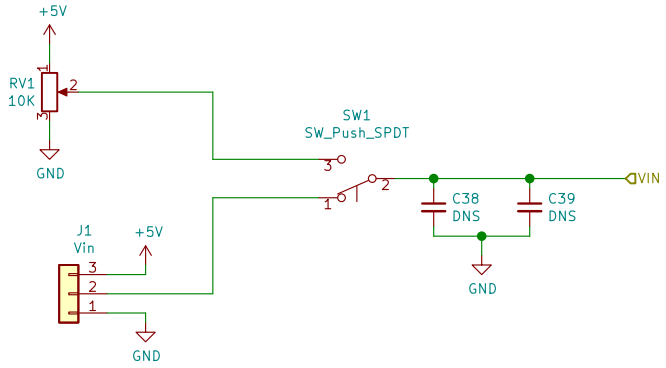
This shift register operates on the falling edge of the clock. This avoids race conditions:

All signals are set up by the state machine on the falling clock edge,
and are latched into the registers on the rising edge.

Sheet: /StateMaschine.sch/
File: StateMaschine.sch

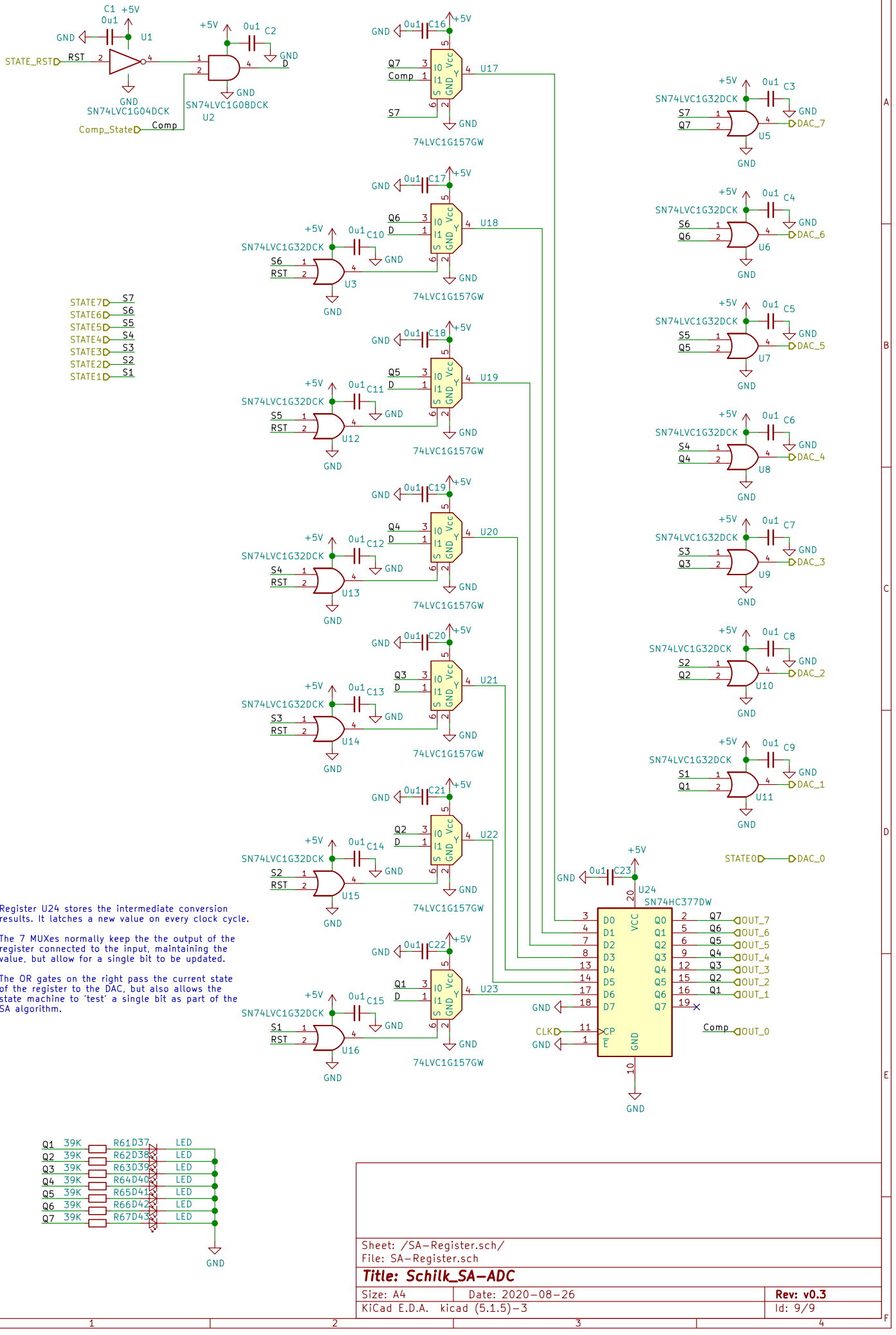
Title: Schilk_SA-ADC

Size: A4	Date: 2020-08-26	**Rev: v0.3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 7/9



SW1 Allows selection between the internal potentiometer or an external voltage input to be fed to the ADC.

Sheet: /Input/ File: Input.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-08-26	**Rev: v0.3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 8/9



Sheet: /SA-Register.sch/
File: SA-Register.sch

Title: Schilk_SA-ADC

Size: A4	Date: 2020-08-26	**Rev: v0.3**
KiCad E.D.A. kicad (5.1.5)-3		Id: 9/9