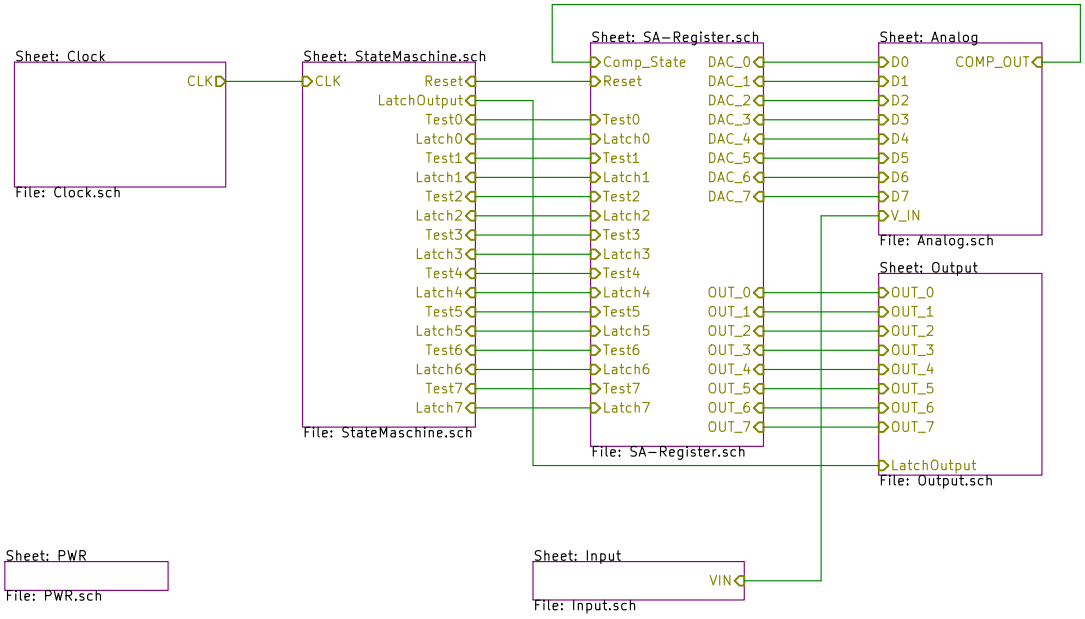


A Discrete Successive-Approximation-ADC

Implemented to learn about/demonstrate the workings of this ADC Architecture, not to design an effective ADC.

Sheets/Breakdown:

PWR:
Power Input & Voltage Regulation

Input:
Analog Voltage Input to the ADC

Clock:
NE555 based Clock used to drive State machine. Adjustable in Frequency from approx. 1Hz to 400Hz

State Machine:
The State machine that sequences the conversion. Consists of:
Counter: A simple binary counter
State Decode: A lookup that decodes the counter's output to the various control signals needed.

SA-Register:
Contains the Successive-Approximation (SA) Register used during conversion.

Analog:
The Analog-domain section of the ADC. This includes the comparator and the DAC: An R2R DAC fed by the binary output of the SA-Register. This output is buffered to remove switching noise.

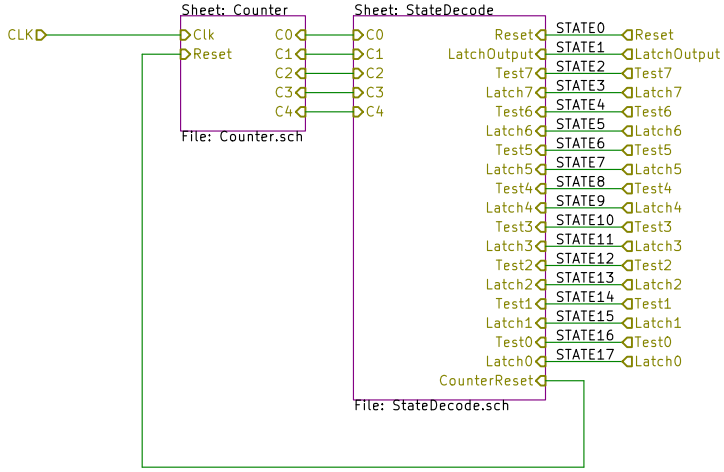
Output:
Contains the output register into which the result is latched once a conversion finishes. Also contains a simple binary Display of the final conversion result.

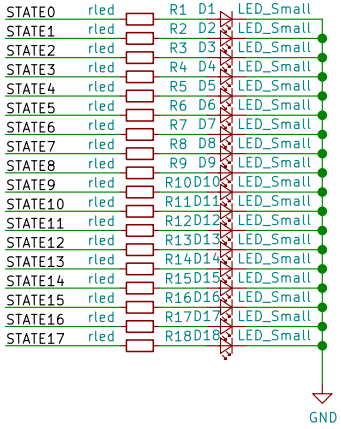
Philipp Schilk

Sheet: /
File: SA-ADC.sch

Title: Schilk_SA-ADC

Size: A4	Date: 2020-02-03	**Rev: v0.0 (Prod.)**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/11

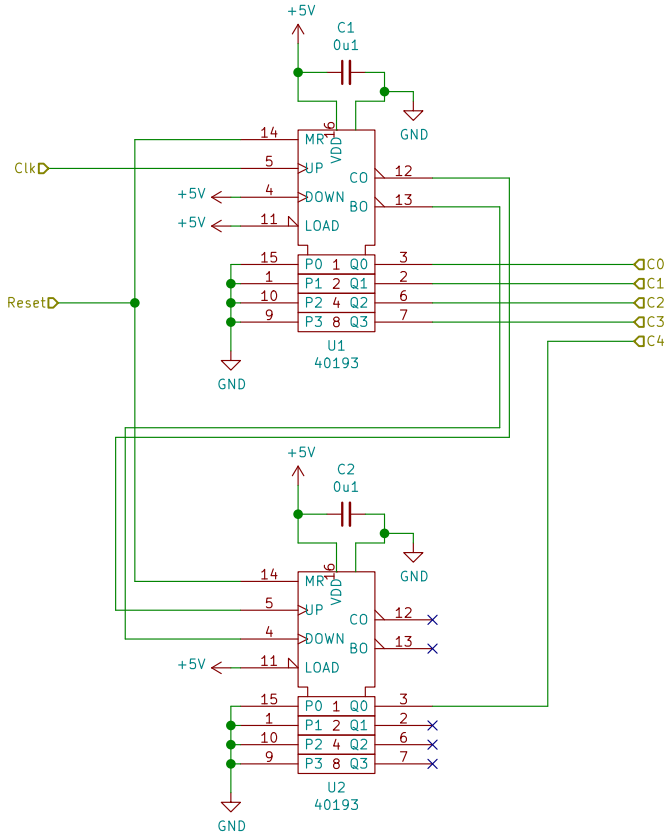




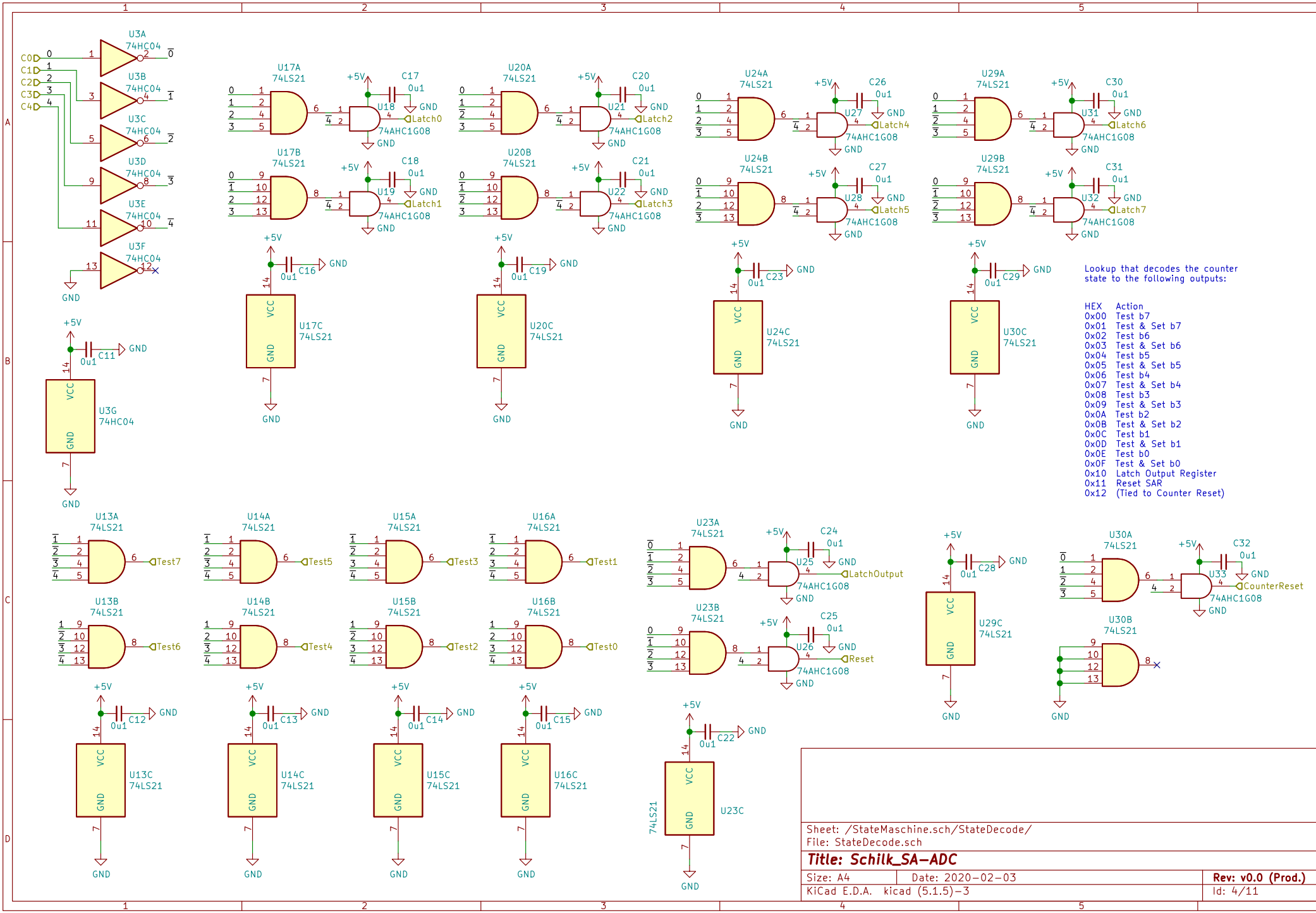
Sheet: /StateMaschine.sch/
File: StateMaschine.sch

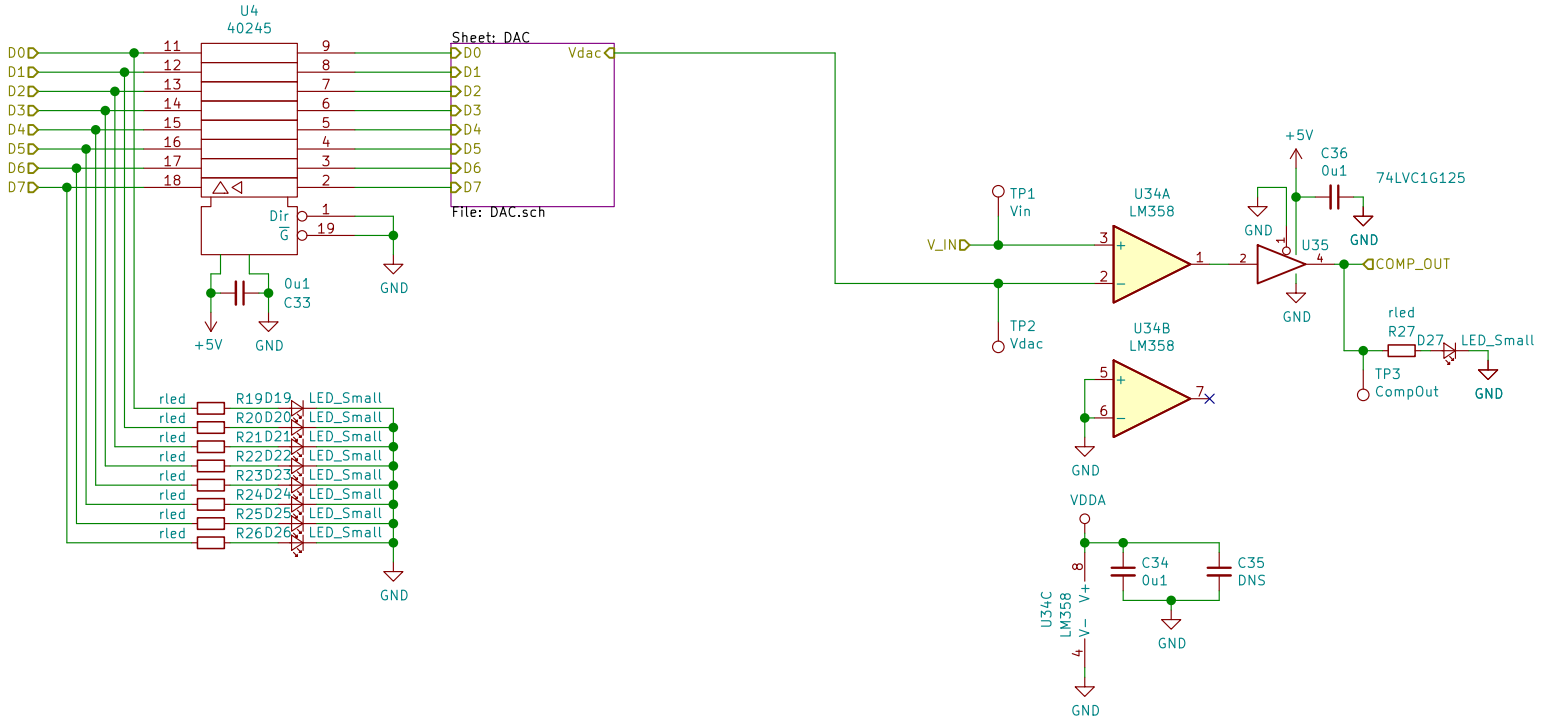
Title: Schilk_SA-ADC

Size: A4	Date: 2020-02-03	**Rev: v0.0 (Prod.)**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/11

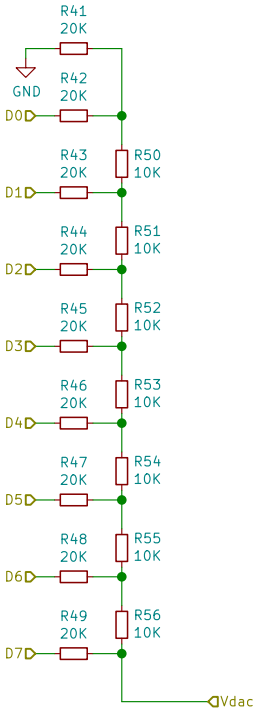


Sheet: /StateMaschine.sch/Counter/		
File: Counter.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-02-03	**Rev: v0.0 (Prod.)**
KiCad E.D.A. kicad (5.1.5)-3		Id: 3/11


U3A 74HC04
U3B 74HC04
U3C 74HC04
U3D 74HC04
U3E 74HC04
U3F 74HC04
C0
C1
C2
C3
C4
GND
U17A 74LS21
U17B 74LS21
U17C 74LS21
U18 74AHC1G08
U19 74AHC1G08
C16 0u1
C17 0u1
C18 0u1
+5V
Latch0
Latch1
U20A 74LS21
U20B 74LS21
U20C 74LS21
U21 74AHC1G08
U22 74AHC1G08
C19 0u1
C20 0u1
C21 0u1
Latch2
Latch3
U24A 74LS21
U24B 74LS21
U24C 74LS21
U27 74AHC1G08
U28 74AHC1G08
C23 0u1
C26 0u1
C27 0u1
Latch4
Latch5
U29A 74LS21
U29B 74LS21
U30C 74LS21
U31 74AHC1G08
U32 74AHC1G08
C29 0u1
C30 0u1
C31 0u1
Latch6
Latch7
U3G 74HC04
C11 0u1
Lookup that decodes the counter state to the following outputs:
HEX Action
0x00 Test b7
0x01 Test & Set b7
0x02 Test b6
0x03 Test & Set b6
0x04 Test b5
0x05 Test & Set b5
0x06 Test b4
0x07 Test & Set b4
0x08 Test b3
0x09 Test & Set b3
0x0A Test b2
0x0B Test & Set b2
0x0C Test b1
0x0D Test & Set b1
0x0E Test b0
0x0F Test & Set b0
0x10 Latch Output Register
0x11 Reset SAR
0x12 (Tied to Counter Reset)
U13A 74LS21
U13B 74LS21
U13C 74LS21
U14A 74LS21
U14B 74LS21
U14C 74LS21
U15A 74LS21
U15B 74LS21
U15C 74LS21
U16A 74LS21
U16B 74LS21
U16C 74LS21
Test7
Test6
Test5
Test4
Test3
Test2
Test1
Test0
C12 0u1
C13 0u1
C14 0u1
C15 0u1
U23A 74LS21
U23B 74LS21
U23C 74LS21
U25 74AHC1G08
U26 74AHC1G08
C22 0u1
C24 0u1
C25 0u1
LatchOutput
Reset
U29C 74LS21
C28 0u1
U30A 74LS21
U30B 74LS21
U33 74AHC1G08
C32 0u1
CounterReset
Sheet: /StateMaschine.sch/StateDecode/
File: StateDecode.sch
Title: Schilk_SA-ADC
Size: A4
Date: 2020-02-03
Rev: v0.0 (Prod.)
KiCad E.D.A. kicad (5.1.5)-3
Id: 4/11



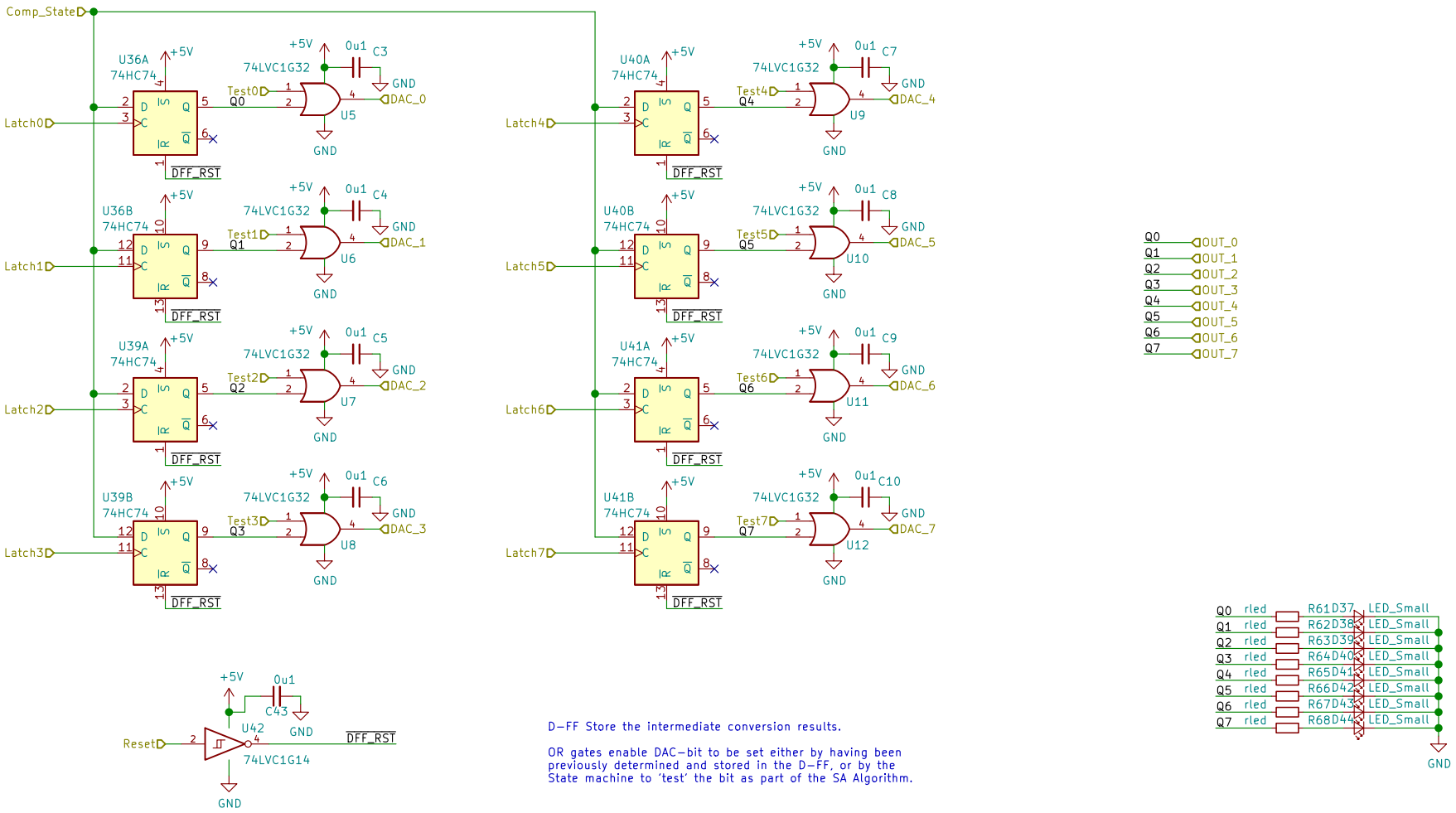
Sheet: /Analog/		
File: Analog.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-02-03	**Rev: v0.0 (Prod.)**
KiCad E.D.A. kicad (5.1.5)-3		Id: 5/11



R2R DAC

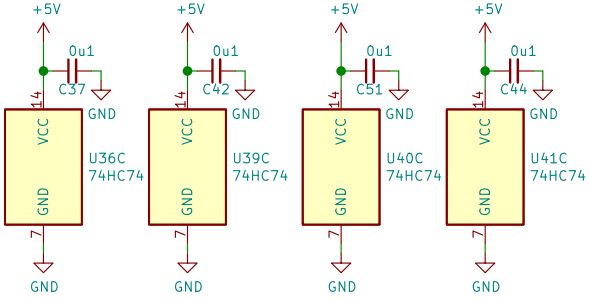
Use Precision Resistors, Optimally <0.5%

Sheet: /Analog/DAC/		
File: DAC.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-02-03	**Rev: v0.0 (Prod.)**
KiCad E.D.A. kicad (5.1.5)-3		Id: 6/11

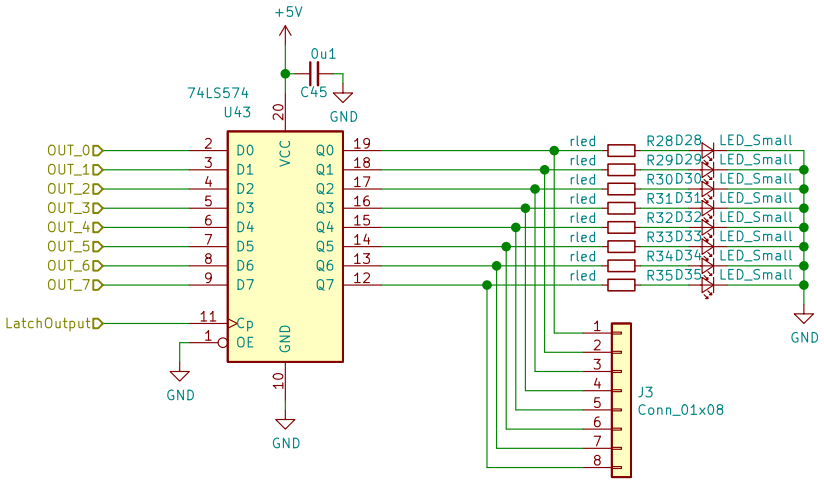


D-FF Store the intermediate conversion results.

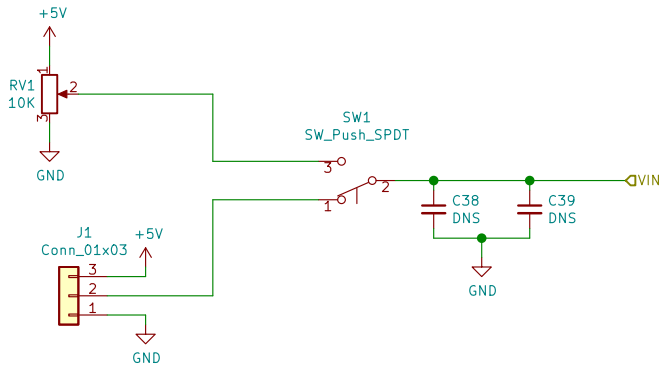
OR gates enable DAC-bit to be set either by having been previously determined and stored in the D-FF, or by the State machine to 'test' the bit as part of the SA Algorithm.



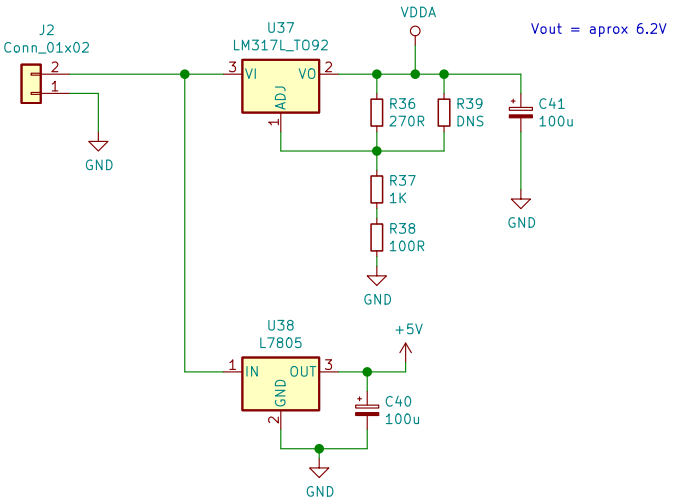
Sheet: /SA-Register.sch/		
File: SA-Register.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-02-03	**Rev: v0.0 (Prod.)**
KiCad E.D.A. kicad (5.1.5)-3		Id: 7/11



Sheet: /Output/		
File: Output.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-02-03	**Rev: v0.0 (Prod.)**
KiCad E.D.A. kicad (5.1.5)-3		Id: 8/11



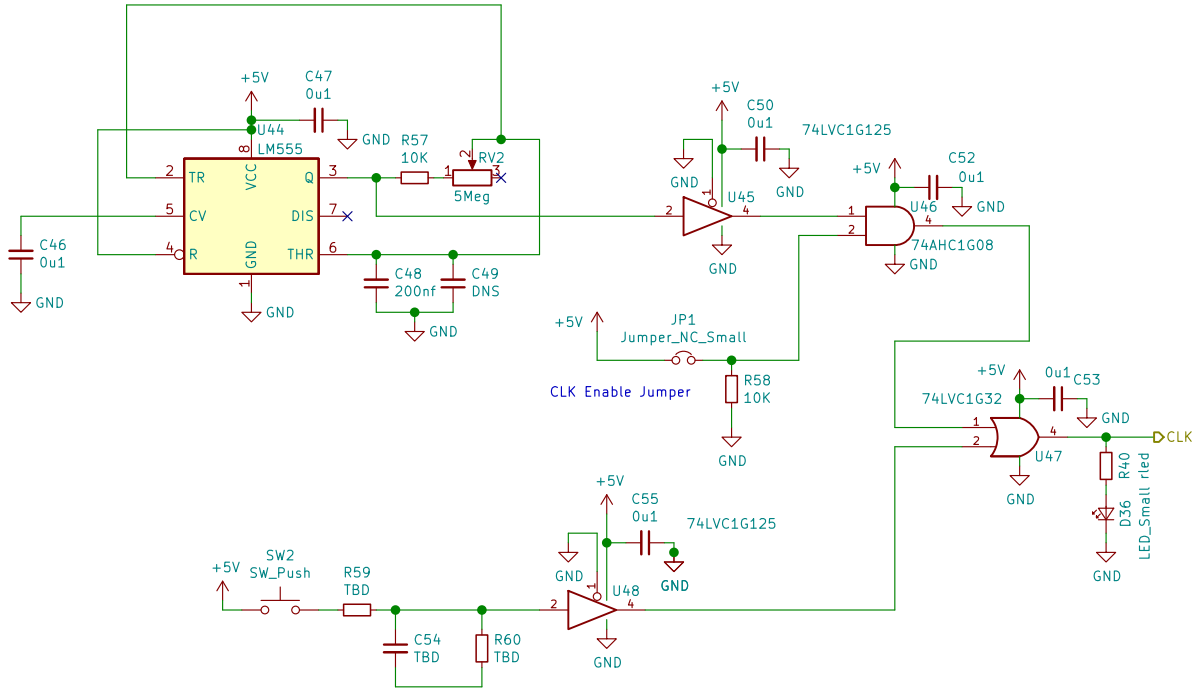
Sheet: /Input/		
File: Input.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-02-03	**Rev: v0.0 (Prod.)**
KiCad E.D.A. kicad (5.1.5)-3		Id: 9/11



OpAmp used as comparator
needs supply slightly higher than 5v to compare signals close / at 5v.

Specific voltage was choosen, as it both enabled comparing accross
the whole 0–5v band, and resulted in the opamp outputing around 5V as
logic–high. (Output of Opamp ist at max aprox. 1.2–1.3 V lower than Supply Voltage)

Sheet: /PWR/		
File: PWR.sch		
Title: Schilk_SA–ADC		
Size: A4	Date: 2020–02–03	**Rev: v0.0 (Prod.)**
KiCad E.D.A. kicad (5.1.5)–3		Id: 10/11



Clock derived from 555 timer may be connected to state machine using JP1.

SW2 may be used to manually generate a clock pulse regardless of the position of JP1.

Sheet: /Clock/ File: Clock.sch		
Title: Schilk_SA-ADC		
Size: A4	Date: 2020-02-03	**Rev: v0.0 (Prod.)**
KiCad E.D.A. kicad (5.1.5)-3		Id: 11/11