EE739A - Advanced Processor Design
Project I : Superscalar IITB RISC

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1 Fetch

2 Decode

3 Dispatch

3.1 Register Renaming

Registers are 16-bit. Carry and Zero Flag registers are 1-bit.

3.1.1 Architectural Register File

- They store tags of the corresponding rename regiser for every Architectural registers, along with non-speculative data.
- It will also have a valid bit. Whenver interrupt all valid bits are set to 1.
- If the AR is renamed, then it is invalid, else it is valid.
- It is set valid, only when the tag pointed by it, and the tag broadcasted by the ROB matches.
- It will take into account the interdependency bits and use the RRF queue to decide which tags to issue.

3.1.2 Rename Register File

- Execution will give the tag for the RR, and the corresponding register will update its value.
- This will also be broadcasted RS.

3.1.3 RRF Queue

- Queue of available rename registers, updated based on ROB tag broadcast.

3.2 Reservation Station

3.2.1 Allocation Policy

- Keep a queue (circular), to store the available RS entries for allocation.
- This has to check whether or not to stall.
- The register values are from the pipeline registers, valid bits from the ARF, and ROB tag from ROB.
- It also allocates to the ROB, and checks for stalls.

3.2.2 Issue Policy

- Top-down search for ready bits.
- Decides between alu, branch, memory, as well as memory branch Execution pipes.

3.2.3 Table

- Source Rename Register Tags.
- Immediate Data
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- ROB tag.

4 Execution

4.1 4 Pipes

5 Write Back

5.1 Reorder Buffer (ROB)