EE739A - Advanced Processor Design
Project I : Superscalar IITB RISC

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1 Fetch

1.1 Program Counter

- This register is the speculative program counter which is used to fetch from the instruction cache
- The actual permanent PC is stored in the ARF corresponding to register R7 as R7 == PC in the ISA
- It is updated by PC+2 every cycle, unless a branch misprediction correction is issued or the fetch stage is stalled

1.2 Branch Predictor

- Stores Target Address and Prediction History corresponding to BEQ and JAL
- JLR is not stores becuase its target address needs to always be computed and can be multitargeted which adds issues in checking whether the branch taken was to the right address or not
- Branches are by default assumed to be not taken so that PC+2 rule can be continually followed
- Planned to be implemented as a two bit predictor because the ISA does not allow from good prediction accuracy with small hardware

2 Decode

2.1 Decoders

- There are two paraller decoders which generate the necessary control signals for the future stages. This also includes the necessary reordering of the operands into source and destination registers
- They include necessary hardware to detect inter-dependencies between the two instructions fetched
- They generate inter-dependency bits which are later to be used in the renaming stage by the ARF and RRF to correctly generate and provide the tags
- The validity of the destination operand for the ARF as well as for the carry and zero flags are produced which is passed on as the invalid tag bits in the execution stage

2.2 LM/SM Handling Block

- It is responsible for replacing the decode block in case of arrival of an LM or SM
- It generates the necessary operands and addresses that are to be written to or read from. This is performed by generating signals similar to the load instruction and simply by incrementing the immediate field
- To ensure that the value read from Address Source Register does not change an isLM bit is generated which is a signal for harware in the dispatch stange which ensures correct execution of the instruction

3 Dispatch

3.1 Register Renaming

Registers are 16-bit. Carry and Zero Flag registers are 1-bit. Renaming is performed for both the registers individually.

3.1.1 Architectural Register File

- They store tags of the corresponding rename regiser for every Architectural registers, along with non-speculative data.
- It will also have a valid bit. Whenver interrupt all valid bits are set to 1.
- If the AR is renamed, then it is invalid, else it is valid.
- It is set valid, only when the tag pointed by it, and the tag broadcasted by the ROB matches.
- It will take into account the interdependency bits and use the RRF queue to decide which tags to issue and which to be provided to the reservation station in case of a intra RAW hazard.

3.1.2 Rename Register File

- Execution will give the tag for the RR, and the corresponding register will update its value.
- This will also be broadcasted RS.

3.1.3 RRF Queue

- Queue of available rename registers, updated based on ROB tag broadcast.

3.2 Reservation Station

3.2.1 Allocation Policy

- Keep a queue (circular), to store the available RS entries for allocation.
- This has to check whether or not to stall.
- The register values are from the pipeline registers, valid bits from the ARF, and ROB tag from ROB.
- It also allocates to the ROB, and checks for stalls.

3.2.2 Issue Policy

- Top-down search for ready bits.
- Decides between alu, branch, memory, as well as memory branch Execution pipes.

3.2.3 Table

- Source Rename Register Tags.
- Immediate Data
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- ROB tag.

4 Execution

4.1 4 Pipes

5 Write Back

5.1 Reorder Buffer (ROB)