Microprocessors Project 2 - IITB-RISC Pipeline

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List of Control Signals

NOP bit

NOP bit will be active low, so for each instruction, NOP is high. When NOP is low then that instruction will not be executed.

NOP bit controls the output of individual control decoders of each stage. If NOP bit is set, all control signals are disabled for that stage.

RR Control

Control Signal	Description
JLR	Controls stall for JLR instruction. Goes to PC load mux and sets NOP of previous stages.
A1c/A2c	Controls mux for A1/A2 input of Register File.
RDc	Controls mux for RD(destination register) address.
LM/SM	Controls ALUI2 mux for passing Zero-Padded-PE output to ALU.
Dmem	Controls mux for choosing Dmem and RM for store operations.

Exec Control

Control Signal	Description
BEQ	Controls stall for BEQ instruction if ALU gives zero. Goes to PC load mux and sets NOP of previous stages.
ALU_c	Controls operation to be done by ALU (ADD/NAND/XOR).
Flag	Enables flag forwarding block.
Imm	Controls mux for ALUI2 to choose Immediate data.
PC1	Controls mux for ALUI1 to choose constant "+1". Controls mux for ALUI2 to choose PC.
LHI	Controls mux for ADmem to send ALUO or Immediate data(for LHI).
C/Z	Controls flag muxes to pass flags from ALU if instruction sets them.

Mem Control

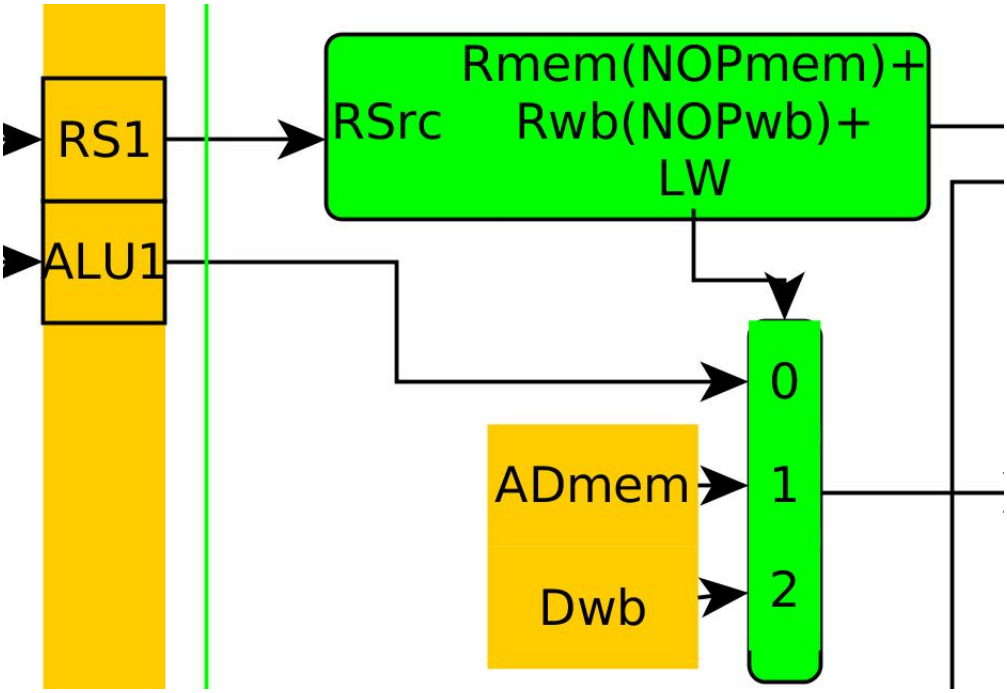
Control Signal	Description
LW	Goes to Register Forwarding blocks in Exec stage to determine LW stall.
MW/MR	Controls Read/Write enable of RAM.
Out_c	Controls mux to select RAM data output or ALU output.
Zc	Controls whether Z flag is updated by data read.

WB Control

Control Signal	Description
Wen	Enable data write for Register File
Cen/Zen	Enable write for C/Z registers.

Combinational Blocks

Forwarding Block



This block will compare **Rsrc** with **Rmem** and **Rwb** and output a control signal for mux to select the corresponding data.

Also, if **LW** is set for Mem stage and **Rsrc** matches, we need to stall.

Logic:

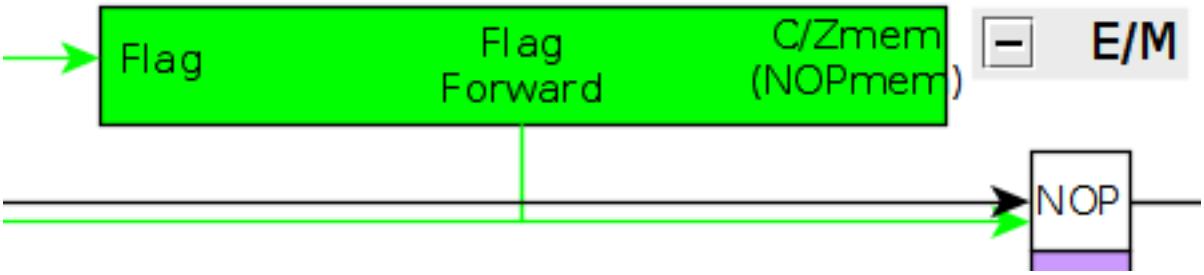
```
if(NOPmem == 1 && Rsrc == Rmem){
    if (LW == 1) {
        Stall;
    } else {
        Out = ADmem;
    }
} else if(NOPwb == 1 && Rsrc == Rwb){
    if (LW == 1) {
        Stall;
    } else {
        Out = Dwb;
    }
}
```

LW Stall Block

It takes input from the 3 forwarding blocks and if we want to stall, it disables write of all previous pipeline registers(and PC) so they stay in same state, and sets **NOP** bit of **E/M** pipeline register to send **NOP** instruction (i.e. stall) to Mem stage.

Current instruction in Exec stage will be recomputed using the forwarding values obtained from WB stage(which now has **LW** instruction).

Flag Forwarding Block



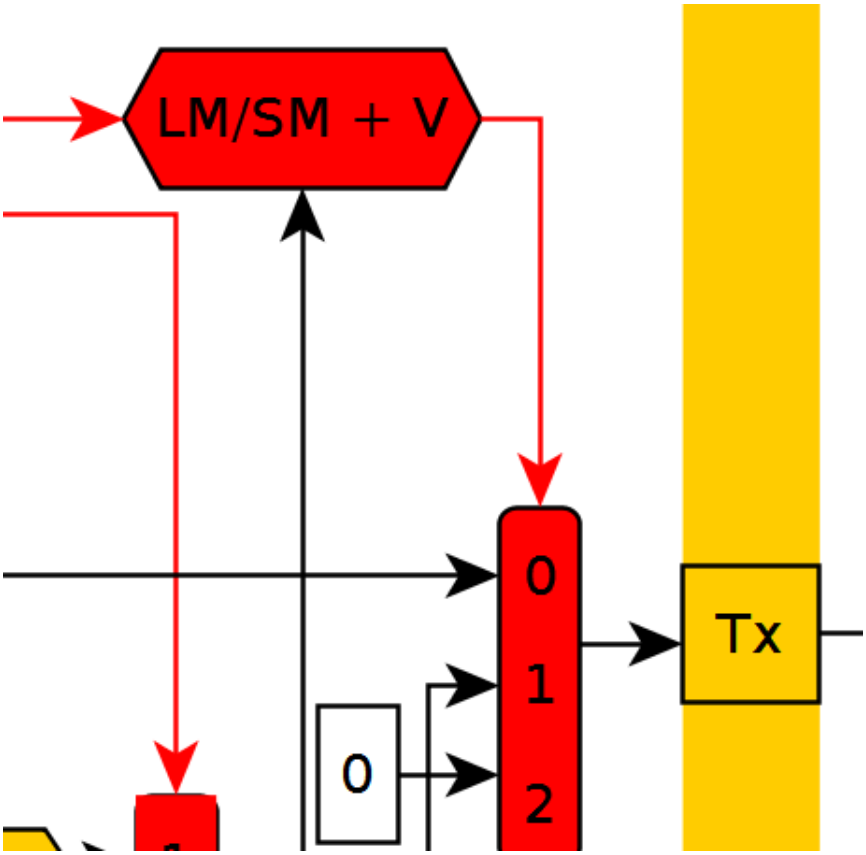
Used by **ADC/ADZ/NDC/NDZ** instructions to determine whether to execute or change to **NOP**.

Logic:

```
if(NOPmem == 1){
    if(Flag == C && Cmem == 0){
        Dont execute;
    } else if(Flag == Z && Zmem == 0){
        Dont execute;
    }
}
```

If we decide to not execute, the Exec state's control decoder is disabled, and **NOP** bit is set in **E/M** pipeline register to send **NOP** instruction. This means the instruction will not execute further.

LM/SM Initialisation and Freeze logic



Initialisation logic:

```
if(LM/SM == 0 && V == 0){
    Tx = 0;
} else if(LM/SM == 1 && V == 0){
    Tx = Immediate;
} else if(V == 1){
    Tx = Txn;
}
```

When V = 1, then **Wdis** is on for previous two pipeline registers and PC so write is disabled and hence the next two instructions loaded are frozen in fetch and decode stage.

Control signals for each instruction

ADD/NDU

Stage	Signals
Decode	–
Reg Read	A1c = ra A2c = rb RDc = rc
Exec	ALU_c = add/nand Z = 1 C = 1(for add)
Mem	–
Write Back	Wen = 1 Cen = 1(for add) Zen = 1

ADC/ADZ/NDC/NDZ

Stage	Signals
Decode	–
Reg Read	A1c = ra A2c = rb RDc = rc
Exec	ALU_c = add/nand Z = 1 C = 1(for add) Flag = C/Z
Mem	–
Write Back	Wen = 1 Cen = 1(for add) Zen = 1

ADI

Stage	Signals
Decode	–
Reg Read	A1c = ra RDc = rb
Exec	ALU_c = add Z = 1 C = 1 Imm = 1
Mem	–
Write Back	Wen = 1 Cen = 1(for add) Zen = 1

LHI

Stage	Signals
Decode	LHI = 1
Reg Read	RDc = ra
Exec	LHI = 1
Mem	–
Write Back	Wen = 1

LW

Stage	Signals
Decode	–
Reg Read	A1c = rb RDc = ra
Exec	ALU_c = add Imm = 1
Mem	LW = 1 MR = 1 Out_c = 1 Zc = 1
Write Back	Wen = 1 Zen = 1

SW

Stage	Signals
Decode	–
Reg Read	A1c = rb A2c = ra Dmem = D2 RM = A2
Exec	ALU_c = add Imm = 1
Mem	MW = 1
Write Back	–

BEQ

Stage	Signals
Decode	–
Reg Read	A1c = ra A2c = rb
Exec	BEQ = 1 ALU_c = xor
Mem	–
Write Back	–

JAL

Stage	Signals
Decode	JAL = 1
Reg Read	RDc = ra
Exec	ALU_c = add PC1 = 1
Mem	–
Write Back	Wen = 1

JLR

Stage	Signals
Decode	–
Reg Read	RDc = ra A1c = rb JLR = 1
Exec	ALU_c = add PC1 = 1
Mem	–
Write Back	Wen = 1

LM

Stage	Signals
Decode	LM/SM = 1
Reg Read	LM/SM = 1 RDc = pe A1c = ra
Exec	ALU_c = add
Mem	MR = 1 Out_c = 1
Write Back	Wen = 1

SM

Stage	Signals
Decode	LM/SM = 1
Reg Read	LM/SM = 1 A2c = pe A1c = ra
Exec	ALU_c = add
Mem	MW = 1
Write Back	–