Computer Architecture – ESP – Exercise 2
Q1
For the following C statement, write a minimal sequence of MIPS assembly instructions that does the identical operation. Assume $t1 = A, $t2 = B, and $s1 is the base address of C.
A = C[0] << 4;

Q2
Assume $t0 holds the value 0x00101000. What is the value of $t2 after the following instructions?

```
        slt $t2, $0, $t0
        bne $t2, $0, ELSE
                j DONE
        ELSE: addi $t2, $t2, 2
        DONE:
```


Q3
Suppose the program counter (PC) is set to 0x2000 0000. Is it possible to use the jump (j) MIPS assembly instruction to set the PC to the address as 0x4000 0000? Is it possible to use the branch-on-equal (beq) MIPS assembly instruction to set the PC to this same address?

Q4
The following instruction is not included in the MIPS instruction set:
rpt $t2, loop # if(R[rs]>0) R[rs]=R[rs]−1, PC=PC+4+BranchAddr
Q4.1 If this instruction were to be implemented in the MIPS instruction set, what is the most appropriate instruction format?
Q4.2 What is the shortest sequence of MIPS instructions that performs the same operation?

Q5
Implement the following C code in MIPS assembly. What is the total number of MIPS instructions needed to execute the function?

```
        int fib(int n){
                if (n==0)
                        return 0;
                else if (n == 1)
                        return 1;
                else
                return fib(n−1) + fib(n−2);
```