HOME WORK #4

MULTI-CYCLE

Question 1)
Relate to the Multi-Cycle diagram of the MIPS processor.
Add to the processor the following new instruction: **addm**

This instruction adds to a register a value stored in memory. The instruction is I-type. The symbolic representation of the command is the following
addm RT, offset(RS)
the action it accomplishes is RT =RT + MEM[RS+offset]
for example: addm $1 , 32($2) means $1 = $1 + MEM[$2+32]
Describe:
1) What physical changes you would make to the diagram (adding elements, control lines)
2) What are the values of the control lines for this command in each and every cycle.
3) If you have added a control line, specify what its value will be for all other commands in all other cycles.

Question 2)
Relate to the Multi-Cycle diagram of the MIPS processor.
Add to the processor the following new instruction: **jal**

To understand the instruction, please read the MIPS Instruction Reference found on moodle or the internet (http://www.mrc.uidaho.edu/mrc/people/jff/digital/MIPSir.html) .
Describe:
1) What physical changes you would make to the diagram (adding elements, control lines)
2) What are the values of the control lines for this command in each and every cycle.
3) If you have added a control line, specify what its value will be for all other commands in all other cycles.

Question 3)
Relate to the Multi-Cycle diagram of the MIPS processor.
For this instruction update if necessary the data path and the control lines.
 Do not change the Register File.
The command is **swap Rs, Rt**
The instruction exchanges the values of Rs and Rt
Assume the command is R-Type

Question 4)

An error has occurred in a MIPS multicycle processor. The error is in the multiplexor which is controlled by the PCSource control lines. Line-in 0 was accidently connected to ALU Target register and line-in 1 was connected directly to the output of the ALU. In other words, input lines 0 and 1 were reversed.

Which instructions will no longer work correctly?

Working correctly means its actions produce the expected results and the program continues to run as expected.

Question 5)

In the multi-cycle MIPS diagram we have seen, there is a multiplexor D which is controlled by PCSource. (The same multiplexor as in question 4) The following error has occurred: line-in 1 was completely severed. This line normally comes from the Target register. Which commands will be affected?

    a) Just Jump
    b) All instructions because we can longer do PC =PC + 4
    c) Just Branch
    d) All instructions that have an immediate value
    e) All instructions because the result of the ALU will be lost before it can be used.

Much Success!!