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Implementing a TMDS Video Interface in the Spartan-6 FPGA

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Summary

Transition Minimized Differential Signaling (TMDS) is a standard used for transmitting video data over the Digital Visual Interface (DVI) and High-Definition Multimedia Interface (HDMI). Both interfaces are popular in a wide range of market segments including consumer electronics, audio/video broadcasting, industrial surveillance, and medical imaging systems. They are commonly seen in flat panel TVs, PC monitors, blue-ray players, video camcorders, and medical displays.

This application note describes a set of reference designs able to transmit and receive DVI and HDMI data streams up to 1080 Mb/s using the native TMDS I/O interface featured by Spartan®-6 FPGAs.

Introduction

The DVI and HDMI protocols use TMDS at the physical layer. The TMDS throughput is a function of the serial data rate of the video screen mode being transmitted. This in turn determines the FPGA speed grade that must be used to support this throughput.

After the Spartan-3A family, Xilinx has offered embedded electrically-compliant TMDS I/O allowing implementation of DVI and HDMI interfaces inside the FPGA. The operation theory for this is detailed in *Video Connectivity Using TMDS I/O in Spartan-3A FPGAs* [Ref 1]. The data throughput in that application note was maximized at 666 Mb/s in the fastest speed grade.

The Spartan-6 FPGA on the other hand has made significant speed improvements. Table 1 shows the maximum throughput for each speed grade of the Spartan-6 FPGA.

Table 1: **Spartan-6 Family TMDS I/O Throughput**

Speed Grade	Throughput (Mb/s)
-4	1080
-3	1050
-2	945
-1L	500

Common video screen modes corresponding to these data rates are listed in Table 2.

Table 2: **Common Video Screen Modes**

Screen Mode	Pixel Rate (MHz)	Serial Data Rate (Mb/s)	Color Depth
VGA(1) (640x480 @ 60 Hz)	25	250	24b
480p(2) (720x480 @ 60 Hz)	27	270	24b
SVGA(1) (800x600 @ 60 Hz)	40	400	24b
XGA(1) (1024x768 @ 60 Hz)	65	650	24b
HD(1) (1366x768 @ 60 Hz)	85.5	855	24b
WXGA(1) (1280x800 @ 60 Hz)	71	710	24b

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在Spartan-6 FPGA中实现TMDS视频接口

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总结

过渡最小化差分信令（TMDS）是一种通过数字视频接口（DVI）和高清多媒体接口（HDMI）传输视频数据的标准技术。这两种接口广泛适用于消费电子、影音广播、工业监控和医疗成像系统等多个细分市场，常见应用场景包括平板电视、电脑显示器、蓝光播放器、摄像机和医疗显示设备等终端产品。

本应用说明介绍了一组参考设计，能够通过Spartan®-6 FPGA原生支持的TMDS I/O接口，实现高达1080 Mb/s的DVI和HDMI数据流传输与接收。

简介

DVI和HDMI协议在物理层使用TMDS。TMDS吞吐量是所传输视频屏幕模式的串行数据速率的函数。这进而决定了必须用来支持该吞吐量的FPGA速度等级。

继Spartan-3A系列之后，赛灵思公司推出了嵌入式电气兼容TMDS I/O，支持在FPGA内部实现DVI和HDMI接口。其工作原理详见《在Spartan-3A FPGA中使用TMDS I/O实现视频连接》[参考文献1]。该应用指南中，在最快速度等级下数据吞吐量最高可达666 Mb/s。

另一方面，Spartan-6 FPGA在速度上有了显著提升。表1显示了Spartan-6 FPGA各速度等级的最大吞吐量。

表 1：Spartan-6 系列 TMDS I/O 吞吐量

Speed Grade	Throughput (Mb/s)
-4	1080
-3	1050
-2	945
-1L	500

与这些数据速率{v*}相对应的常见视频屏幕模式列于表2中。

表 2: 常见视频屏幕模式

Screen Mode	Pixel Rate (MHz)	Serial Data Rate (Mb/s)	Color Depth
VGA(1) (640x480 @ 60 Hz)	25	250	24b
480p(2) (720x480 @ 60 Hz)	27	270	24b
SVGA(1) (800x600 @ 60 Hz)	40	400	24b
XGA(1) (1024x768 @ 60 Hz)	65	650	24b
HD(1) (1366x768 @ 60 Hz)	85.5	855	24b
WXGA(1) (1280x800 @ 60 Hz)	71	710	24b

Table 2: **Common Video Screen Modes *(Cont'd)***

Screen Mode	Pixel Rate (MHz)	Serial Data Rate (Mb/s)	Color Depth
HDTV 720p(2) (1280x720 @ 60 Hz)	74.25	742.5	24b
HDTV 1080i(2) (1920x1080 @ 60 Hz interlaced)	74.25	742.5	24b
HD(1) (1366x768 @ 60 Hz)	85.5	855	24b
SXGA(1) (1280x1024 @ 60 Hz)	108	1080	24b

Notes:

1. Refer to the Video Electronics Standards Association (VESA) Coordinated Video Timing Generator [Ref 2].
2. Refer to the Consumer Electronics Association's Consumer Video Timing Specification [Ref 3].

The throughput offered by the fastest Spartan-3A device can be achieved by the slowest speed grade of the Spartan-6 device. For the first time, the most popular 720p and 1080i resolution is achievable in most Spartan-6 devices (except the -1L speed grade).

In addition to the speed enhancement, the Spartan-6 FPGA possesses some unique hardened I/O features ideal for implementing video interfaces. Compared to what is described in *Video Connectivity Using TMDS I/O in Spartan-3A FPGAs* [Ref 1] for the Spartan-3A FPGA, this application note focuses on leveraging the new I/O features to achieve higher performance with fewer resources.

Logic Construct

One of the major advancements in the Spartan-6 FPGA is its I/O architecture. This is represented by the addition of new advanced I/O logic and clocking resources, namely, IODELAY2, IOSERDES2, and the phase-locked loop (PLL) and I/O clock distribution network. As detailed in *Spartan-6 FPGA SelectIO™ Resources User Guide* [Ref 4], IODELAY2 provides calibrated delay taps for the TMDS video stream to deskew and phase align on a per-pair basis. IOSERDES2 helps with serialization and deserialization of video pixels using dedicated and hardened circuitry. The PLL synthesizes a high-speed bit rate matching clock, and the I/O distribution routes the clock to designated IODELAY2 and IOSERDES2 elements via a dedicated path with the finest resolution. This not only gives a higher performance improvement over the Spartan-3A family but allows the actual DVI/HDMI transmitter and receiver to be built in a much easier manner.

Transmitter Design

For each of three data pairs in a DVI or HDMI link, the transmitter design is logically divided into two parts: TMDS encoding and 10-bit parallel-to-serial conversion. Figure 1 illustrates the topology of the DVI/HDMI transmitter design in the Spartan-6 FPGA.

表2：常见视频屏幕模式（续表）

Screen Mode	Pixel Rate (MHz)	Serial Data Rate (Mb/s)	Color Depth
HDTV 720p(2) (1280x720 @ 60 Hz)	74.25	742.5	24b
HDTV 1080i(2) (1920x1080 @ 60 Hz interlaced)	74.25	742.5	24b
HD(1) (1366x768 @ 60 Hz)	85.5	855	24b
SXGA(1) (1280x1024 @ 60 Hz)	108	1080	24b

备注：

1. 请参考视频电子标准协会（VESA）协调视频时序发生器 [Ref 2]。2. 请参阅消费电子协会的《消费类视频时序规范》[Ref 3]。

性能最快的Spartan-3A器件提供的吞吐量可通过速度等级最慢的Spartan-6器件实现。首次在多数Spartan-6器件（除-1L速度等级外）中实现了最主流的720p和1080i分辨率。

除了速度提升外，Spartan-6 FPGA还具备独特的硬化I/O特性，非常适合实现视频接口。相较于《在Spartan-3A FPGA中使用TMDS I/O实现视频连接》[Ref 1]中针对Spartan-3A FPGA的描述，本应用指南重点介绍如何利用这些新型I/O特性以更少资源实现更高性能。

逻辑构造

Spartan-6 FPGA的主要进步之一是其I/O架构。这体现在新增了先进的I/O逻辑和时钟资源，即IODELAY2、IOSERDES2、锁相环（PLL）以及I/O时钟分配网络。如《Spartan-6 FPGA SelectIO™资源用户指南》[参考文献4]所述，IODELAY2为TMDS视频流提供校准延迟抽头，实现基于信号对的去歪斜和相位对齐。IOSERDES2通过专用且硬化的电路，协助完成视频像素的串行化与解串行化。PLL可合成匹配高速比特率的时钟，而I/O分配网络通过高精度专用路径，将时钟路由至指定的IODELAY2和IOSERDES2元件。这不仅相较Spartan-3A系列实现了更高的性能提升，还使实际DVI/HDMI发射器与接收器的构建更为简便。

发射机设计

对于DVI或HDMI链路中的三组数据对，发射器设计在逻辑上分为两个部分：TMDS编码和10位并行至串行转换。图1展示了Spartan-6 FPGA中DVI/HDMI发射器设计的拓扑结构。

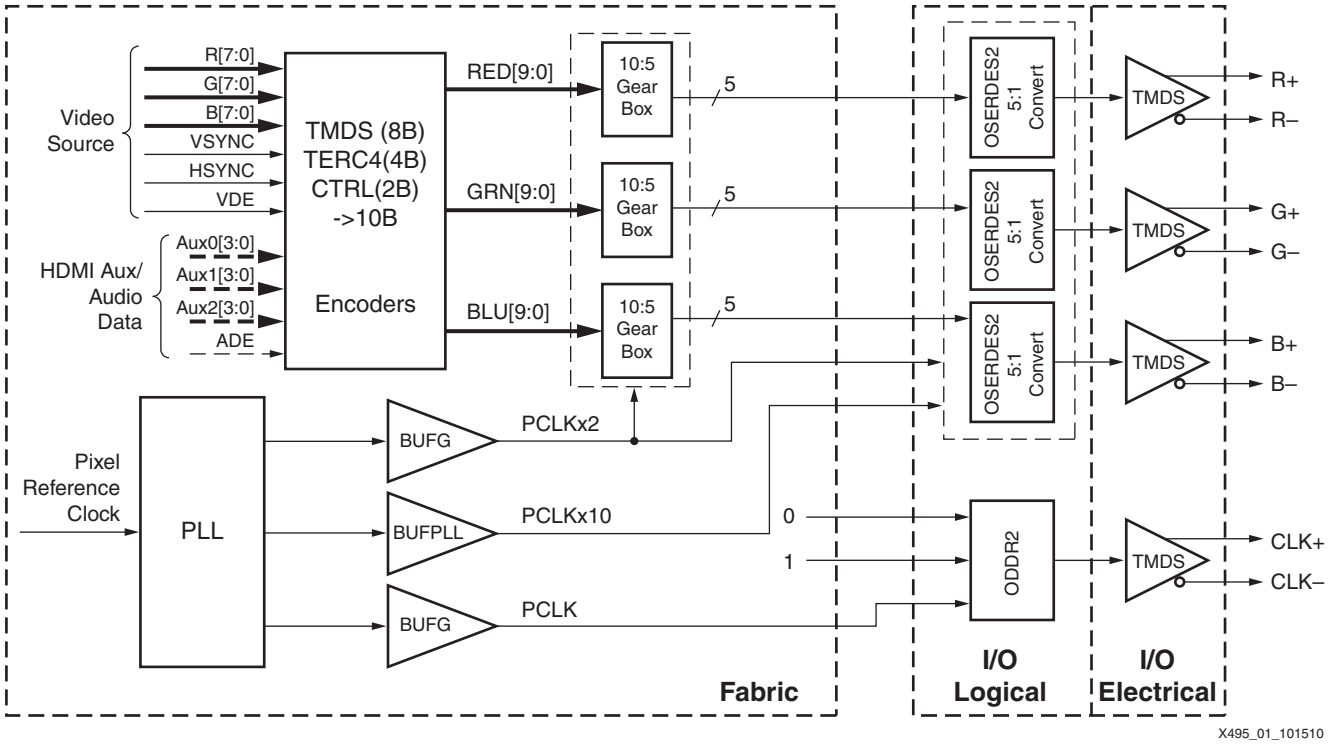

Figure 1: **TMDS Transmitter Design**

The TMDS encoder in the Spartan-6 FPGA is identical to that in the Spartan-3A FPGA, and is thoroughly discussed in *Video Connectivity Using TMDS I/O in Spartan-3A FPGAs* [Ref 1]. However, the serializer and its clocking scheme are significantly different in the Spartan-6 FPGA.

10:1 Serializer

Compared to the Spartan-3A FPGA soft solution [Ref 1], the serializer design in the Spartan-6 FPGA is completely based on hardened circuitry. Each output pin in the Spartan-6 FPGA comes with a built-in OSERDES2 block that converts a maximal 4-bit parallel bus to a 1-bit serial stream. By cascading with another OSERDES2 block within its adjacent output pin, the hardened circuitry is able to perform serialization with a maximal 8:1 ratio. This is typically obtained by default when the output is operating in a differential pair like the TMDS. The OSERDES2 blocks are fully configurable to work in either cascading or non-cascading mode with any ratio ranging from 1 to 8. A detailed description of the OSERDES2 block can be found in *Spartan-6 FPGA SelectIO Resources User Guide* [Ref 4].

To perform the required 10:1 serialization for both DVI and HDMI, two stages of conversion must be made: a 2:1 soft gear box and 5:1 OSERDES2 cascading.

Clocking Scheme

Compared to the transmitter in the Spartan-3A FPGA, the clocking scheme in the Spartan-6 FPGA design is much more simplified. There is no longer the need to implement DDR based high-speed soft multiplexing logic [Ref 1].

Leveraging the built-in high-performance PLL and dedicated I/O clock network, both the soft 2:1 gear box and the hard 5:1 OSERDES2 block work in single data rate (SDR) mode. The PLL takes the pixel rate reference as its input and synthesizes three clocks: a pixel clock, a 10x pixel clock, and a 2x pixel clock.

The 10x pixel clock is used to match the serial data bit rate. It is routed to the OSERDES2 clock through a dedicated BUFPLL driver. This is named as an I/O Clock. The clock runs as fast as

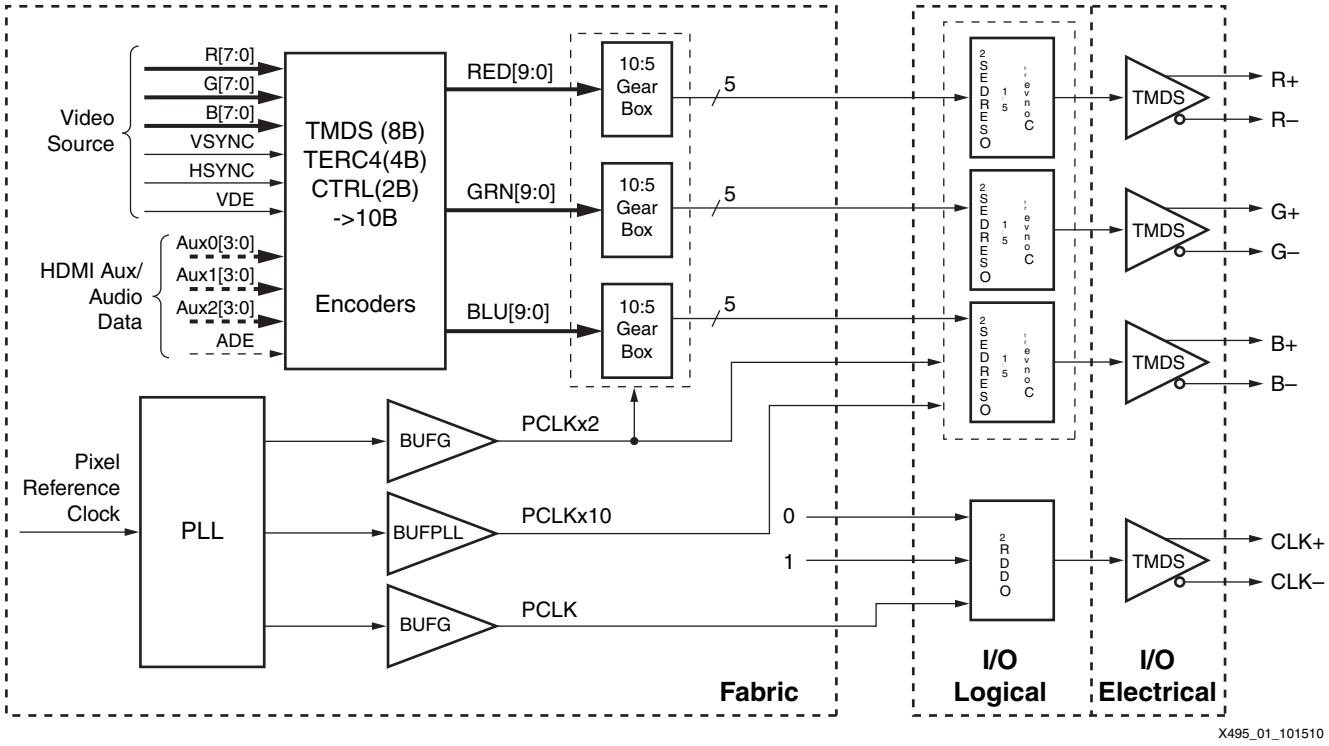

图 1：TMDS 发送器设计

Spartan-6 FPGA中的TMDS编码器与Spartan-3A FPGA中的完全相同，其在《使用Spartan-3A FPGA的TMDS I/O实现视频连接》[参考文献1]中已有详尽论述。然而，Spartan-6 FPGA中的串行器及其时钟方案存在显著差异。

10:1 串行器

与Spartan-3A FPGA软核解决方案[参考文献1]相比，Spartan-6 FPGA中的串行器设计完全基于硬化电路。Spartan-6 FPGA的每个输出引脚均内置OSERDES2模块，可将最大4位并行总线转换为1位串行数据流。通过与其相邻输出引脚内的另一个OSERDES2模块级联，该硬化电路可实现最高8:1的串行化比率。当输出端采用差分对（如TMDS）工作时，该配置通常为默认实现方式。OSERDES2模块完全可配置，能以1至8任意比率在级联或非级联模式下工作。有关OSERDES2模块的详细说明可参阅《Spartan-6 FPGA SelectIO资源用户指南》[参考文献4]。

为了对DVI和HDMI实现所需的10:1串行化，必须进行两个转换阶段：2:1的软变速器和5:1的OSERDES2级联。

时钟方案

与 Spartan-3A FPGA 中的发射器相比，Spartan-6 FPGA 设计中的时钟方案更为简化，不再需要实现基于 DDR 的高速{v*}软复用逻辑 [Ref 1]。

利用内置的高性能PLL和专用I/O时钟网络，软2:1齿轮箱和硬5:1 OSERDES2模块均工作于单数据速率（SDR）模式。该PLL将像素速率参考时钟作为输入，生成三个时钟信号：一个像素时钟、一个10倍像素时钟和一个2倍像素时钟。

10倍像素时钟用于匹配串行数据比特率。它通过专用的BUFPLL驱动器路由到OSERDES2时钟，这种时钟被命名为I/O时钟。该时钟的运行速度最高可达

945 MHz in the -2 speed grade, 1050 MHz in the -3 speed grade, and 1080 MHz in the -4 speed grade [Ref 5]. The OSERDES2 block also takes the 2x pixel clock as its 5-bit parallel data input reference.

The 2:1 soft gear box, however, takes both the pixel clock and the 2x pixel clock. It converts the 10-bit TMDS encoded data into a 5-bit data stream. The logic here is extremely insignificant. The only requirement is separate sampling of a 5-bit MSB and 5-bit LSB in the 2x pixel clock domain. The sampling is controlled by a toggle flip-flop generated framing signal.

Timing Analysis and Constraint

Other than resource saving with the help of hardened serialization circuitry, another major advantage of the Spartan-6 FPGA solution is the ease of FPGA logic timing.

The FPGA logic has only two timing domains: pixel clock and x2 pixel clock. By setting the PERIOD constraint on the PLL reference input, the ISE® Design Suite automatically derives appropriate constraints for the 2x and 10x pixel clocks. The latter only applies to hardened clocks and datapaths and has no impact on any of the soft logic running through the FPGA logic. The PERIOD constraint can be set in this manner:

```
NET "pclk" TNM_NET = DVI_CLOCK0;
TIMESPEC TS_DVI_CLOCK0 = PERIOD "DVI_CLOCK0" 100 MHz HIGH 50%;
```

In the code above, pclk represents the PLL input running at the video pixel rate.

Receiver Design

The receiver typically needs to recover the bit sampling clock using the incoming pixel clock and then apply the bit clock to recover the serial data stream back into 10-bit word aligned symbols. This process is known as clock and data recovery (CDR). The second step involves a channel deskew circuit to remove allowed skews among the three data channels. Finally, the 10-bit symbol is decoded into one of these three formats:

- 8-bit video pixel data through the DVI or HDMI decoder
- 4-bit auxiliary data, i.e., information and audio frames through the HDMI decoder only
- 2-bit control data, e.g., the HSYNC and VSYNC through the DVI or HDMI decoder

The second decoder step in the Spartan-6 FPGA is identical to that in the Spartan-3A FPGA, and is thoroughly discussed in *Video Connectivity Using TMDS I/O in Spartan-3A FPGAs* [Ref 1]. The first step CDR and deserialization segment, however, has changed significantly to leverage all the new Spartan-6 FPGA I/O features for higher performance with less resources. Figure 2 illustrates the topology of the DVI/HDMI receiver design in the Spartan-6 FPGA.

-2速度等级下为945 MHz，-3速度等级下为1050 MHz，-4速度等级下为1080 MHz[参考文献5]。OSERDES2模块还采用2倍像素时钟作为其5位并行数据输入参考。

然而，2:1软齿轮箱同时接收像素时钟和2倍像素时钟。其将10位TMDS编码数据转换为5位数据流。该逻辑设计极为简单，唯一要求是在2倍像素时钟域中对5位最高有效位（MSB）和5位最低有效位（LSB）进行独立采样。采样过程由触发器生成的帧同步信号控制。

时序分析与约束

除了借助硬化串行化电路{v*}实现的资源节约优势外，Spartan-6 FPGA解决方案的另一主要优势在于其FPGA逻辑时序的简便性。

FPGA逻辑仅包含两个时序域：像素时钟和x2像素时钟。通过在PLL参考输入上设置PERIOD约束，ISE® Design Suite可自动推导出适用于2倍和10倍像素时钟的相应约束。后者仅适用于硬化的时钟和数据路径，且对运行于FPGA逻辑中的任何软逻辑均无影响。PERIOD约束可按如下方式设置：

```
NET "pclk" TNM_NET = DVI_CLOCK0; TIMESPEC TS_DVI_CLOCK0 = PERIOD "DV
I_CLOCK0" 100 MHz 高电平 50%;
```

在上述代码中，pclk代表以视频像素速率运行的PLL输入。

接收机设计

接收器通常需要利用输入的像素时钟恢复比特采样时钟，随后应用该比特时钟将串行数据流恢复为10比特字对齐的符号。这个过程称为时钟数据恢复（CDR）。第二步需要通过通道去斜电路消除三个数据通道之间允许的偏移。最终，10比特符号将被解码为以下三种格式之一：

- 8位视频像素数据通过DVI或HDMI解码器• 4位辅助数据（即信息与音频帧仅通过HDMI解码器）• 2位控制数据（如HSYNC和VSYNC）通过DVI或HDMI解码器

Spartan-6 FPGA 中的第二个解码器步骤与 Spartan-3A FPGA 中的相同，并在《Spartan-3A FPGA 中使用 TMDS I/O 实现视频连接》[Ref 1] 中进行了详尽讨论。然而，首步时钟数据恢复（CDR）与解串行化模块已发生显著变化，以充分利用 Spartan-6 FPGA 所有新型 I/O 特性，从而以更少资源实现更高性能。图 2 展示了 Spartan-6 FPGA 中 DVI/HDMI 接收器设计的拓扑结构。

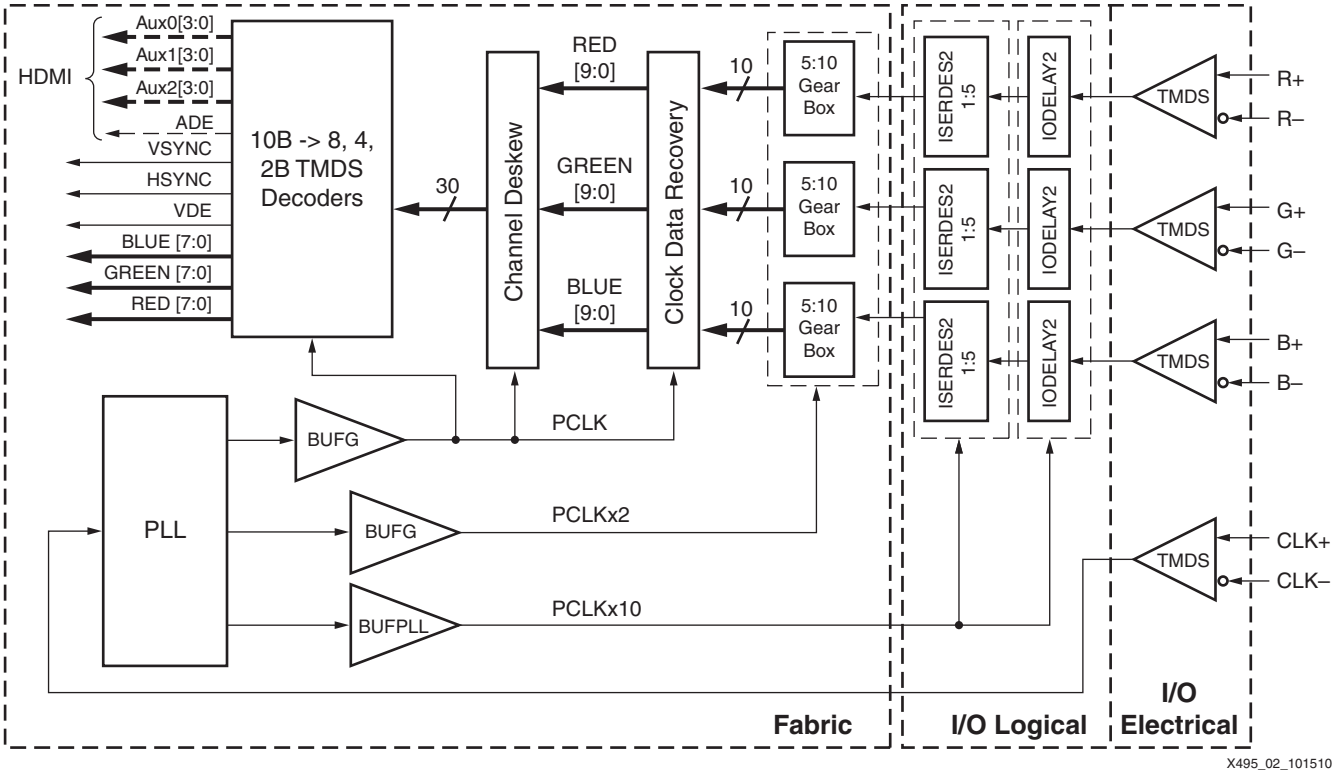

Figure 2: **TMDS Receiver Design**

1:10 Deserialization

Like the transmitter serialization design, deserialization is also based on hardened circuitry working in SDR mode. Each input pin in the Spartan-6 FPGA comes with a built-in ISERDES2 block that converts a 1-bit serial stream to a maximal 4-bit parallel bus. By cascading with another ISERDES2 block within its adjacent input pin, the hardened circuitry is able to perform serialization with a maximal 1:8 ratio. This is typically obtained by default when the input is operating in a differential pair like the TMDS. The ISERDES2 blocks are fully configurable to work in either cascading or non-cascading mode with any ratio ranging from 1 to 8. A detailed description of the ISERDES2 block can be found in *Spartan-6 FPGA SelectIO™ Resources User Guide* [Ref 4].

Similar to the transmitter serialization design, two stages of conversion must be undertaken to obtain the required 1:10 deserialization: 1:5 ISERDES2 cascading and 1:2 FPGA logic gear box.

Clock and Data Recovery

The TMDS clock channel carries a character rate frequency reference from which the receiver reproduces a bit rate sample clock for the incoming serial streams. The reproduced bit rate clock, however, does not have a guaranteed phase relationship associated with any of the three data lanes. In addition, both DVI [Ref 6] and HDMI specifications [Ref 7] allow certain skew between any two data lanes. As a result, the clock phase must be adjusted individually for each data lane to correctly sample the incoming serial bit. This involves aligning the clock rising edge to the middle sampling window of each data lane. Like the serialization and deserialization steps, the CDR work here is mostly done through hardened circuitry.

The bit sampling clock is reproduced through a PLL using the incoming TMDS pixel clock as a reference. The TMDS clock is multiplied by 10 to match the bit rate and then fed to a BUFPLL that routes the 10x clock to designated ISERDES2 and IODELAY2 blocks. This clock is named IOCLK. Figure 2 illustrates the clock connections.

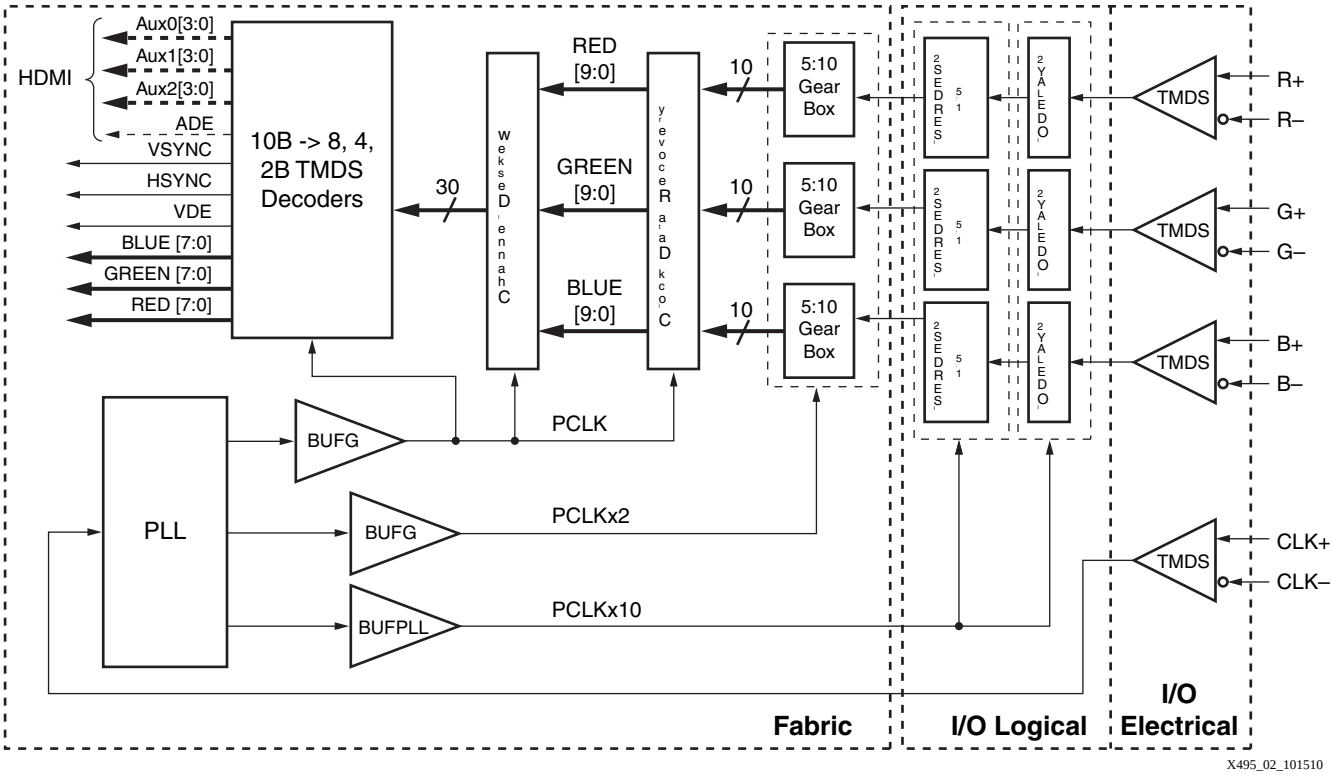

图2: TMDS 接收器设计

1:10 反序列化

与发送端串行化设计类似，解串化同样基于采用SDR模式工作的硬化电路。Spartan-6 FPGA的每个输入引脚均配置内置ISERDES2模块，可将1位串行流转换为最大4位并行总线。通过与相邻输入引脚的另一个ISERDES2模块级联，该硬化电路可实现最高1:8的串行化比率。当输入采用TMDS等差分对工作时，该配置通常为默认实现。ISERDES2模块可完全配置为级联或非级联模式，支持1至8任意比率工作模式。ISERDES2模块的详细说明可参阅《Spartan-6 FPGA SelectIO™ 资源用户指南》[参考文献4]。

与发射机串行化设计类似，为获得所需的1:10解串比，需进行两级转换：1:5 ISERDES2级联和1:2 FPGA逻辑齿轮箱。

时钟与数据恢复

TMDS 时钟通道承载字符速率频率参考，接收器据此为输入串流再生比特率采样时钟。然而再生的比特率时钟与三个数据通道之间并不存在保证的相位关系。此外，DVI [参考文献6] 和 HDMI 规范 [参考文献7] 均允许任意两个数据通道之间存在特定偏移。因此，必须为每个数据通道单独调整时钟相位以实现正确的串行比特采样。这涉及将时钟上升沿对齐到每个数据通道的中间采样窗口。与串行化/反串行化步骤类似，此处的时钟数据恢复（CDR）工作主要通过硬化电路完成。

位采样时钟通过使用输入的TMDS像素时钟作为参考源的PLL再生。TMDS时钟被乘以10以匹配比特率后，输入至BUFPLL模块，该模块将10倍频时钟路由至指定的ISERDES2和IODELAY2模块。该时钟被命名为IOCLK。图2展示了时钟连接关系。

Other than deserialization of serial bits into a parallel bus, the ISERDES2 block in the Spartan-6 FPGA possesses a unique “phase detector” function when operating in cascading mode. By sampling and comparing the incoming serial data samples using the two ISERDES2 blocks residing in two adjacent differential input pins, the phase detector is able to determine the phase relationship between the current IOCLK rising edge and the serial data transition edge. Subsequent validation and control signals are sent to the FPGA logic for a soft controller state machine to adjust the IODELAY2 accordingly.

The IODELAY2, on the other hand, provides a dynamically adjustable delay line to the incoming serial data bit. Upon receiving the control signals from the controller state machine, the IODELAY2 is able to align the rising edge of IOCLK to the middle of the data sampling window.

A detailed operation theory of the phase detector together with the IODELAY2 and its controller state machine can be found in *Spartan-6 FPGA SelectIO™ Resources User Guide* [Ref 4] and *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* [Ref 8].

To accommodate the unknown clock to data phase relationship, the phase detector and the IODELAY2 together must be able to shift the data window either to the left or right for up to 0.5 UI. This is determined by the DIFF_PHASE_DETECTOR operation mode of the IODELAY2 and its relevant calibration routine. The calibration process:

- Measures the number of taps in one bit time (UI). This becomes the maximum length of the IDELAY line and is stored as a MAX value into an internal register.
- Presets the master IDELAY to the HALF_MAX (half of the MAX value) position.
- Presets the slave IDELAY to the ZERO position.

Five cases can occur depending on the various clock-to-data initial phase positions. Figure 3 to Figure 7 illustrate how the phase detector works together with the IDELAY blocks and moves the data to align with the clock rising edge.

Case 1

The master IDELAY settles around HALF_MAX and the slave IDELAY settles around ZERO. There might be a bounce of ±2 taps over voltage and temperature changes (Figure 3).

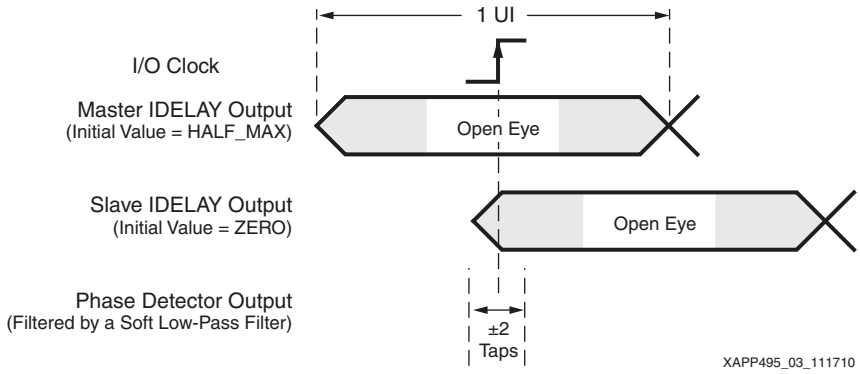

Figure 3: **Case 1: IOCLK Initially Falls into the Middle of the Data Window**

除了将串行比特反序列化为并行总线外，Spartan-6 FPGA中的ISERDES2模块在级联模式下运行时还具备独特的"相位检测器"功能。通过利用两个相邻差分输入引脚中的ISERDES2模块对输入的串行数据样本进行采样和比较，相位检测器能够确定当前IOCLK上升沿与串行数据转换边沿之间的相位关系。后续的验证和控制信号会被发送至FPGA逻辑，供软控制器状态机据此调整IODELAY2。

另一方面，IODELAY2为输入的串行数据位提供了动态可调延迟线。在接收到来自控制器状态机的控制信号后，IODELAY2能够将IOCLK的上升沿{v*}对准数据采样窗口的中间位置{v*}。

相位检测器与IODELAY2及其控制器状态机的详细操作理论可在《Spartan-6 FPGA SelectIO™资源用户指南》[参考文献4]和《源同步串行化与反串行化（速率高达1050 Mb/s）》[参考文献8]中找到。

为了适应未知时钟与数据相位的关系，相位检测器与IODELAY2必须能够将数据窗口向左或向右移动最多0.5 UI。这由IODELAY2的{DIFF_PHASE_DETECTOR}操作模式及其相关校准例程决定。校准过程：

- 测量单位间隔（UI）内的抽头数量。该值即为IDELAY线的最大长度，并以MAX值的形式存储到内部寄存器中。• 将主IDELAY预设到HALF_MAX（MAX值的一半）位置。• 将从IDELAY预设到ZERO位置。

根据不同的时钟与数据初始相位位置，可能会出现五种情况。图3至图7展示了相位检测器如何与IDELAY模块协同工作，并将数据移动以与时钟上升沿对齐。

案例 1

主IDELAY稳定在HALF_MAX附近，从IDELAY则稳定在ZERO附近。随电压和温度变化可能会有±2个抽头的跳变（图3）。

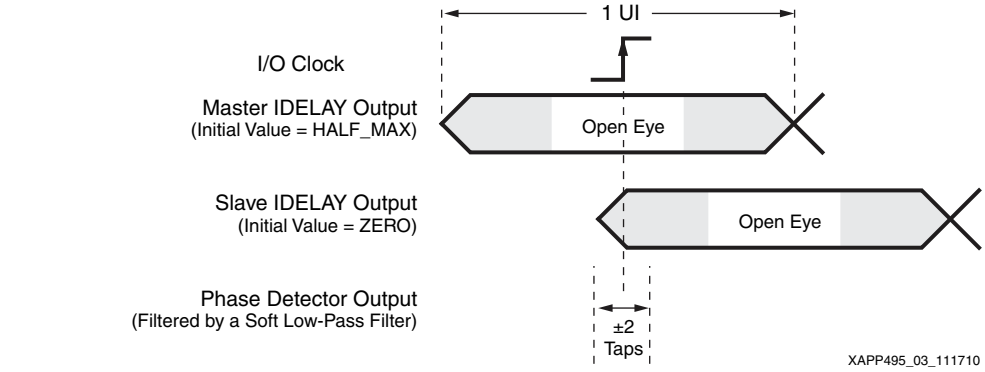

图3：案例1：IOCLK初始位于数据窗口中间

Case 2

The master IDELAY settles around HALF_MAX + n, and the slave IDELAY settles around n, where n < HALF_MAX (Figure 4).

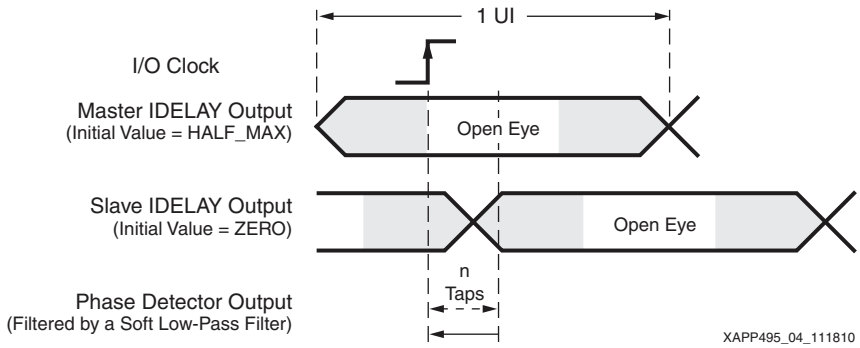

Figure 4: **Case 2: IOCLK Initially Falls into the Left Side of the Data Window**

Case 3

The master IDELAY settles around HALF_MAX – n and the slave IDELAY settles around –n or MAX – n, where n < HALF_MAX (Figure 5).

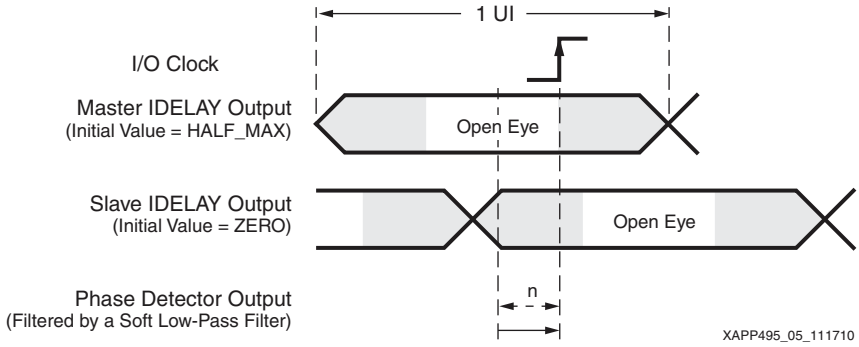

Figure 5: **Case 3: IOCLK Initially Falls into the Right Side of the Data Window**

Case 4

The master IDELAY settles around MAX and the slave IDELAY settles around HALF_MAX (Figure 6).

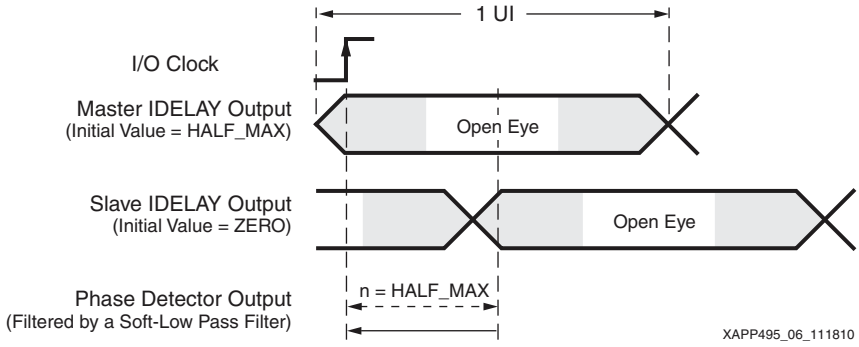

Figure 6: **Case 4: IOCLK Initially Falls by the Left Data Transition Edge**

案例2

主IDELAY稳定在HALF_MAX + n附近，从IDELAY稳定在n附近，其中n < HALF_MAX（图4）。

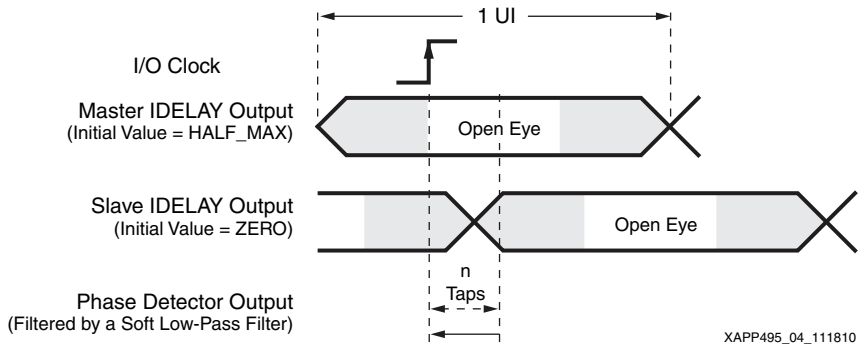

图4：案例2：IOCLK初始位于数据窗口的左侧

案例3

主IDELAY大致稳定在HALF_MAX – n附近，从IDELAY大致稳定在–n或MAX – n附近，其中n < HALF_MAX（图5）。

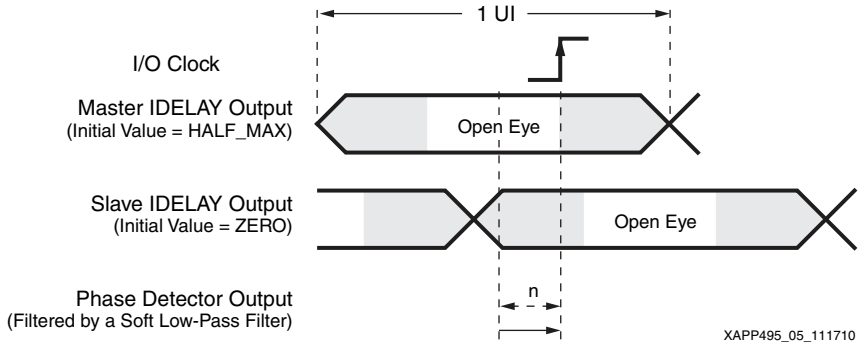

图5：案例3：IOCLK初始位于数据窗口右侧

案例 4

主IDELAY稳定在最大值（MAX）附近，而从IDELAY则稳定在半最大值（HALF_MAX）附近（图6）。

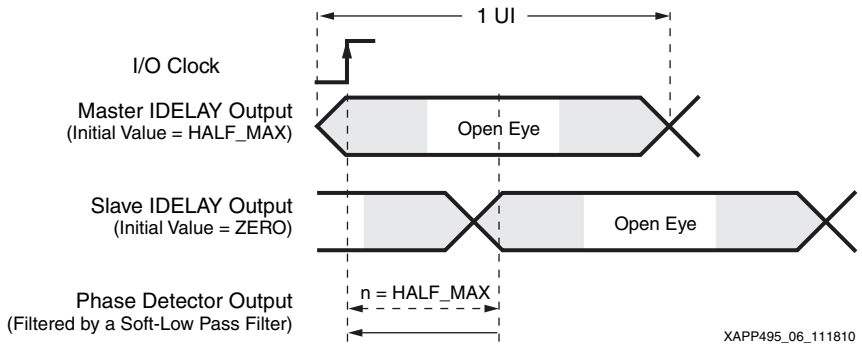

图6: 案例4: IOCLK初始由左侧数据转换边沿下降

Case 5

The master IDELAY settles around ZERO and the slave IDELAY settles around HALF_MAX (Figure 7).

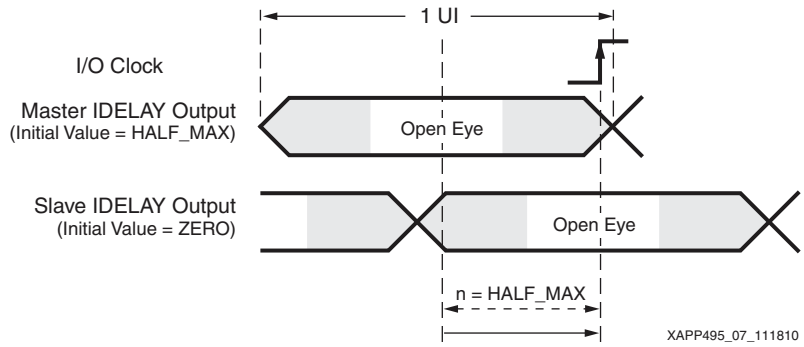

Figure 7: **Case 5: IOCLK Initially Falls by the Right Data Transition Edge**

In Case 4 and Case 5, because the master IDELAY settles either at ZERO or MAX, its IODELAY2 attribute COUNTER_WRAPAROUND must be set to STAY_AT_LIMIT to prevent the IDELAY from underflow or overflow. This is important because the clock and data jitter cause the phase detector to issue extra decrement or increment commands.

This usage is different from that described in *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* [Ref 8], where WRAP_AROUND is suggested when clock and data are roughly pre-aligned. For the cases with unknown initial clock to data phase described in this application note, the use of WRAP_AROUND leads the master sampling window to accidently draft one bit and subsequently cause bit errors.

Word Boundary Detection

Instead of building a soft barrel shifter in the FPGA logic as described in *Video Connectivity Using TMDS I/O in Spartan-3A FPGAs* [Ref 1], another hardened ISERDES2 feature is used in the Spartan-6 FPGA design: the bitslip function. In brief, the ISERDES2 block has the barrel shifter built-in. Upon receiving a one cycle long control pulse, the ISERDES2 block shifts one bit in its deserialized parallel data. *Spartan-6 FPGA SelectIO™ Resources User Guide* [Ref 4] has a detailed description of the bitslip operation. Figure 8 illustrates a possible controller state machine that appropriately issues the bitslip control pulse to determine the word boundary.

案例5

主IDELAY稳定在ZERO附近，从IDELAY稳定在HALF_MAX附近（图7）。

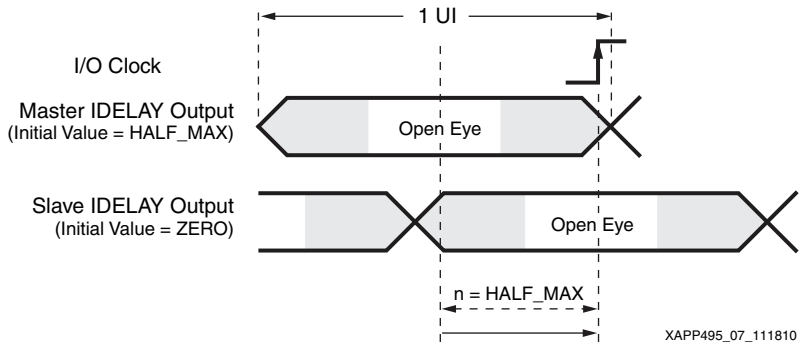

图7: 案例5: IOCLK初始下降沿位于右侧数据转换边沿

在案例4和案例5中，由于主IDELAY会稳定在ZERO或MAX状态，其IODELAY2属性COUNTER_WRAPAROUND必须设置为STAY_AT_LIMIT，以防止IDELAY发生下溢或上溢。这一点至关重要，因为时钟和数据抖动会导致相位检测器发出额外的递减或递增命令。

此用法与源同步串行化与解串行化（最高1050 Mb/s）[Ref 8]中描述的方式不同，后者建议在时钟与数据已大致预对齐时使用WRAP_AROUND。对于本应用说明中描述的初始时钟与数据相位关系未知的情况，使用WRAP_AROUND会导致主采样窗口意外偏移一个比特位，继而引发比特错误。

词边界检测

与《使用TMDS I/O实现Spartan-3A FPGA视频连接》[参考文献1]中描述的通过FPGA逻辑构建软核桶形移位器不同，Spartan-6 FPGA设计中采用了另一个硬件实现的ISERDES2特性：位滑动功能。简而言之，ISERDES2模块内置了桶形移位器。当接收到一个周期宽度的控制脉冲时，ISERDES2模块会对其解串后的并行数据进行单比特移位操作。《Spartan-6 FPGA SelectIO™资源用户指南》[参考文献4]详细描述了位滑动操作机制。图8展示了一种可能的控制器状态机实现方案，该状态机通过适时发出位滑动控制脉冲来判定字边界。

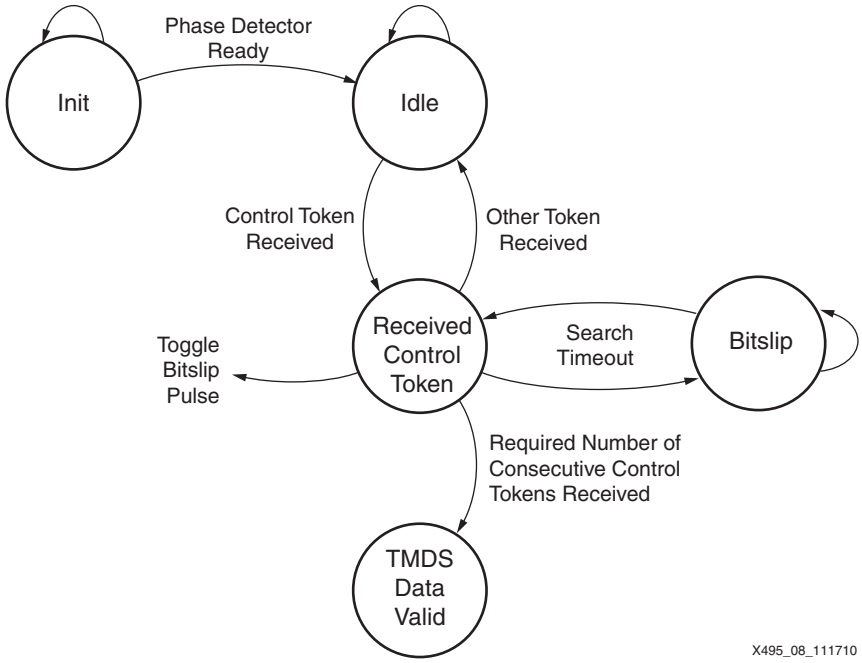

Figure 8: **State Machine to Determine TMDS Word Boundary**

Data Lane Deskew

To remove the allowed data lane skew (up to 0.6 pixel time [Ref 6], [Ref 7]), FIFO-based deskew logic is built. Each data lane hosts a FIFO that is capable of holding data before the other two lanes are aligned to the same timing sequence. The detailed operation of the deskew logic is discussed in *Video Connectivity Using TMDS I/O in Spartan-3A FPGAs*. The design module in the Spartan-3A FPGA can be dropped into the Spartan-6 FPGA with no modification.

Timing Analysis and Constraint

Like the transmitter design, the receiver also operates in three different clock domains:

- Pixel clock: Applicable to most of the FPGA logic, including the ISERDES2/IODELAY2 controller and TMDS decoder
- Pixel clock x2: Applicable to the 1:2 gear box and ISERDES2/IODELAY2 internal
- Pixel clock x10: Applicable only to the ISERDES2/IODELAY2 internal

By setting the appropriate PERIOD constraint to the TMDS clock feeding into the PLL input, the ISE software automatically derives constraints for all three clocks. The PERIOD constraint can be set in this manner:

```
NET "TMDS_CLK" TNM_NET = DVI_CLOCK0;
TIMESPEC TS_DVI_CLOCK0 = PERIOD "DVI_CLOCK0" 100 MHz HIGH 50%;
```

In the code above, TMDS_CLK represents the TMDS clock coming from the DVI or HDMI cable.

Implementation

The hardware evaluation of the Spartan-6 FPGA TMDS capability underwent two stages. An initial feasibility study was performed on the Spartan-6 FPGA SP601 Evaluation Kit. A standard DVI cable was cut into half and the conductors soldered to a 68-pin FMC male connector that was mated with the female FMC connector on the SP601 board. Figure 9 demonstrates the connections, together with a color bar successfully displayed on a standard DVI monitor with resolution up to 1280x1024 @ 60 Hz.

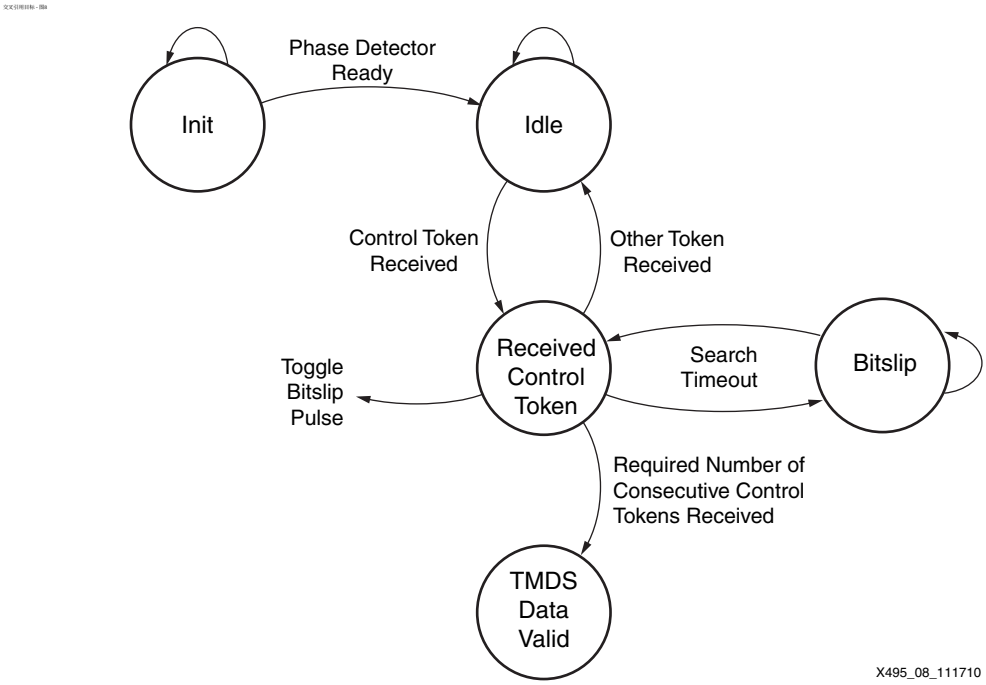

图8: 确定TMDS字符边界的状态机

数据通道去偏移

为消除允许的数据通道偏移（最多0.6像素时间[Ref 6]、[Ref 7]），系统构建了基于FIFO的去偏移逻辑。每个数据通道均配置一个FIFO，该FIFO能够在另两条通道同步至相同时序前暂存数据。去偏移逻辑的详细操作可参考《Spartan-3A FPGA中基于TMDS I/O的视频连接技术》。Spartan-3A FPGA中的设计模块无需修改即可直接应用于Spartan-6 FPGA。

时序分析与约束

就像trans　　发射机设计中，接收机也工作在三种不同的　　t时钟　领域：

- 像素时钟：适用于大部分FPGA逻辑，包括ISERDES2/IODELAY2控制器和TMDS解码器
- 像素时钟2：适用于1:2齿轮箱及ISERDES2/IODELAY2内部
- 像素时钟10：仅适用于ISERDES2/IODELAY2内部

通过为输入 PLL 的 TMDS 时钟设置适当的 PERIOD 约束，ISE 软件会自动推导出所有三个时钟的约束。PERIOD 约束可以按以下方式设置：

```
网络 "TMDS_CLK" TNM_NET = DVI_CLOCK0;  时间规范 TS_DVI_CLOCK0 = 周期 "
DVI_CLOCK0" 100 MHz 高50%;
```

在上面的代码中，TMDS_CLK 表示来自 DVI 或 HDMI 电缆的 TMDS 时钟。

实现

斯巴达-6 FPGA的TMDS功能硬件评估分为两个阶段实施。首先在Spartan-6 FPGA SP601评估套件上进行了初步可行性研究：将标准DVI线缆截为两段，将导线焊接至68针FMC公头连接器，再与SP601开发板的FMC母座进行对接。如图9所示连接方案，配合标准DVI显示器成功实现了最高可达1280x1024 @ 60 Hz分辨率的彩条显示。

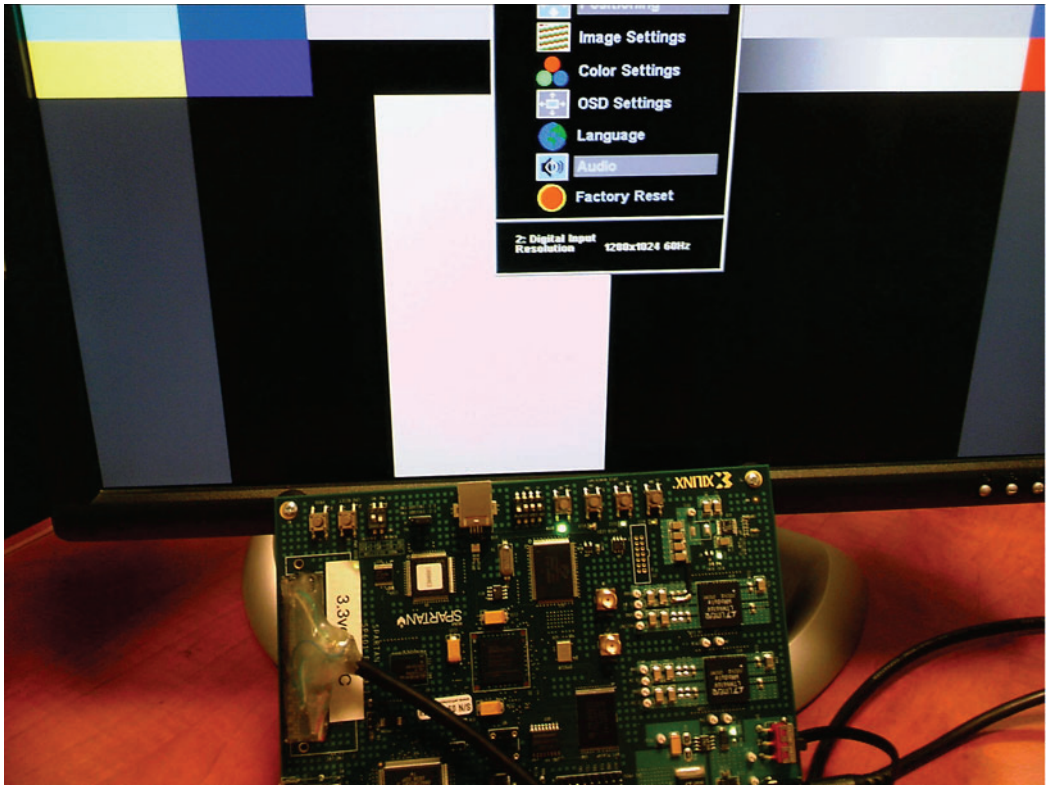

Figure 9: **Spartan-6 DVI Transmission on SP601 Board**

The success of this proof-of-concept justified the further pursuit of both the transmitter and receiver designs in a more refined hardware platform.

Validation Hardware

Video Connectivity Using TMDS I/O in Spartan-3A FPGAs [Ref 1] has a thorough discussion of the electrical considerations for transmitting and receiving TMDS signals through the use of the TMDS_33 SelectIO™ interface mode in the Spartan-3A FPGA. The Spartan-6 FPGA shares the same concepts:

- TMDS_33 outputs are supported only on banks 0 and 2 (top and bottom).
- TMDS_33 outputs require VCCO = 3.3V and VCCAUX = 2.5V/3.3V.
- TMDS_33 inputs require VCCO = 2.5V/3.3V and VCCAUX = 3.3V.
- TMDS_33 signals require 50Ω termination to 3.3V at the receiver.

For a simple design that both transmits and receives TMDS signals (such as an evaluation board), it is easiest to use 3.3V for VCCAUX and VCCO on all four banks of the device.

In addition, other considerations described in *Video Connectivity Using TMDS I/O in Spartan-3A FPGAs* [Ref 1] are also applicable here for the Spartan-6 FPGA. These include 100Ω differential impedance matching on PCB trace lines, display data channel (DDC)/hot plug detect (HDP) compatibility, and use of the low-cost TMDS buffer TMDS141 from Texas Instruments to offer additional signal clean-up and ESD protection up to 6 kV. Figure 10 shows an evaluation board named Atlys built with these concepts and considerations in mind.

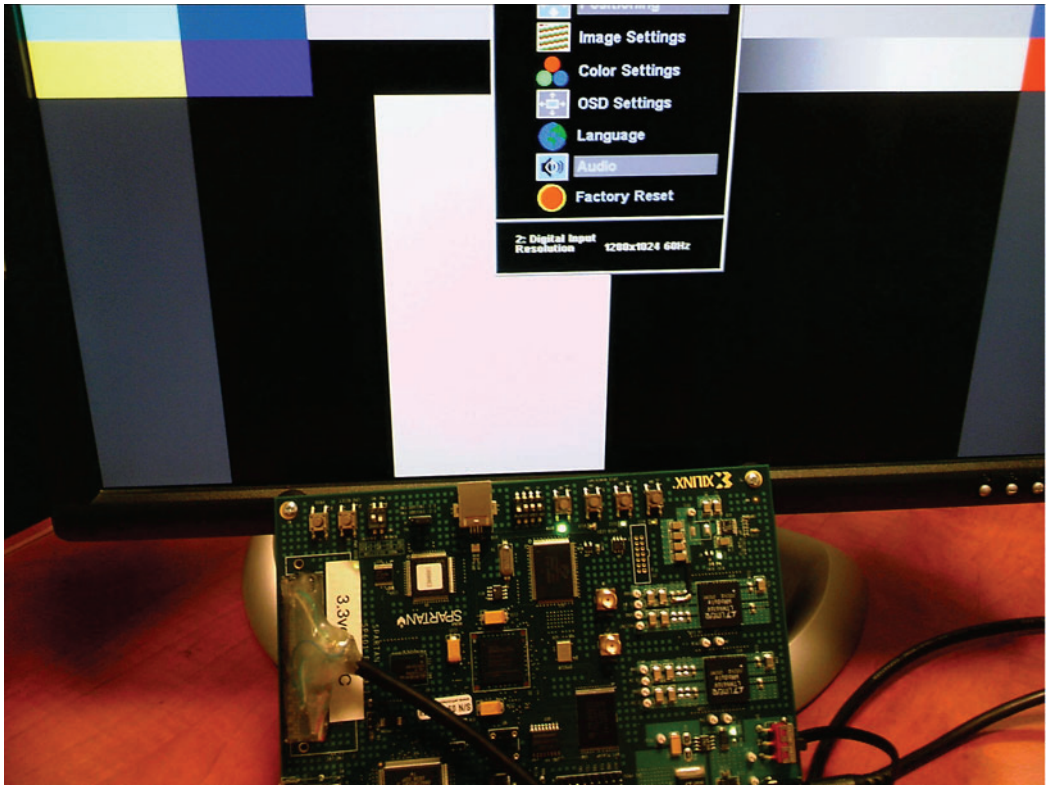

图9：Spartan-6 DVI在SP601开发板上的传输

这一概念验证的成功证明了在更完善的硬件平台上进一步研发发射器和接收器两者设计的合理性。

验证硬件

使用TMDS I/O在Spartan-3A FPGA中实现视频连接[参考文献1] 详细探讨了通过Spartan-3A FPGA的TMDS_33 SelectIO™接口模式传输与接收TMDS信号时的电气注意事项。Spartan-6 FPGA延续了相同的设计理念：

- TMDS_33输出仅支持在组0和组2（顶部和底部）上。• TMDS_33输出需要VCCO = 3.3V及VCCAUX = 2.5V/3.3V。• TMDS_33输入需要VCCO = 2.5V/3.3V及VCCAUX = 3.3V。• TMDS_33信号在接收端需要50Ω端接至3.3V。

对于同时传输和接收TMDS信号的简单设计（例如评估板），在器件的全部四个Bank上使用{v*}为VCCAUX和VCCO供电最为简便。

此外，Spartan-3A FPGA中《使用TMDS I/O实现视频连接》[参考文献1]所述的其他设计考量同样适用于Spartan-6 FPGA。这些考量包括PCB走线上的100Ω差分阻抗匹配、显示数据通道(DDC)/热插拔检测(HDP)兼容性，以及采用德州仪器的低成本TMDS缓冲器TMDS141来提供额外的信号净化功能和高达6 kV的ESD保护。图10展示了基于这些设计理念开发的Atlys评估板。

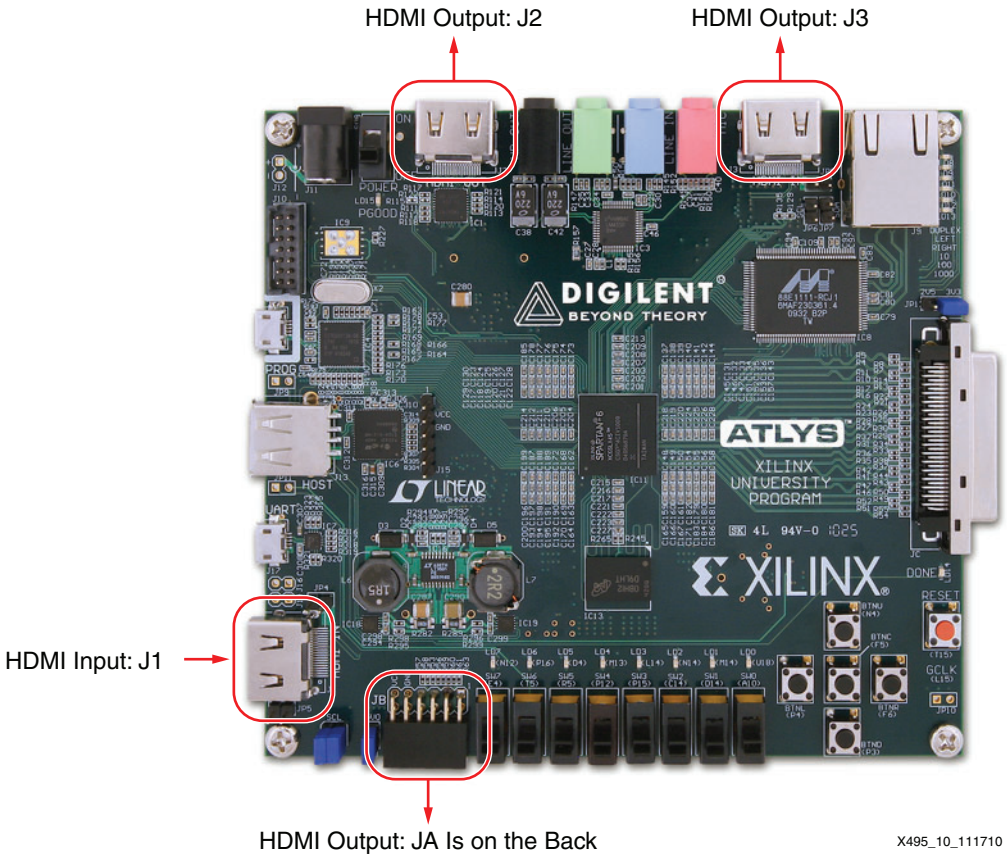

Figure 10: **Atlys TMDS Evaluation Board**

The Atlys board comes with 2x HDMI input ports and 2x HDMI output ports. The two inputs are both based on standard type-A [Ref 7] HDMI connectors located on J1 and J3. The two outputs, in contrast, are configured into two different types of HDMI connectors: type-A [Ref 7] (located at J2) and type-D [Ref 7] (located at JA). All three type-A ports are buffered through the TI TMDS141 buffers. The signals through the type-D connector, however, are connected directly to the Spartan-6 FPGA. One of the two input ports is connected to FPGA I/O bank 0 and the other is connected to bank 1. The type-A output port is connected to bank 0, and the type-D port is connected to bank 2.

The Atlys board is ideal for showcasing the superior capability of the Spartan-6 FPGA at simultaneously receiving, driving, and processing multiple TMDS HD video streams in a single device. The board is available through the Xilinx University Program or can be ordered from Digilent at http://www.digilentinc.com.

Reference Designs

Two reference designs have been built on the Atlys board. For the transmitter alone, a color bar generator is designed to work in various dynamically configurable video timing modes. To demonstrate both the transmitter and receiver, a 2 x 2 DVI matrix is implemented.

Programmable Video Timing Controller

To validate whether the TMDS I/O in the Spartan-6 FPGA is able to transmit video across different screen modes, a color bar generator is built to work with a dynamically configurable pixel clock, as shown in Figure 11. The pixel clock is generated in real time using another new feature in the Spartan-6 FPGA: DCM_CLKGEN. This synthesizes different CLKFX frequencies with variable M/D values using the dynamically configurable system packet interface (SPI)

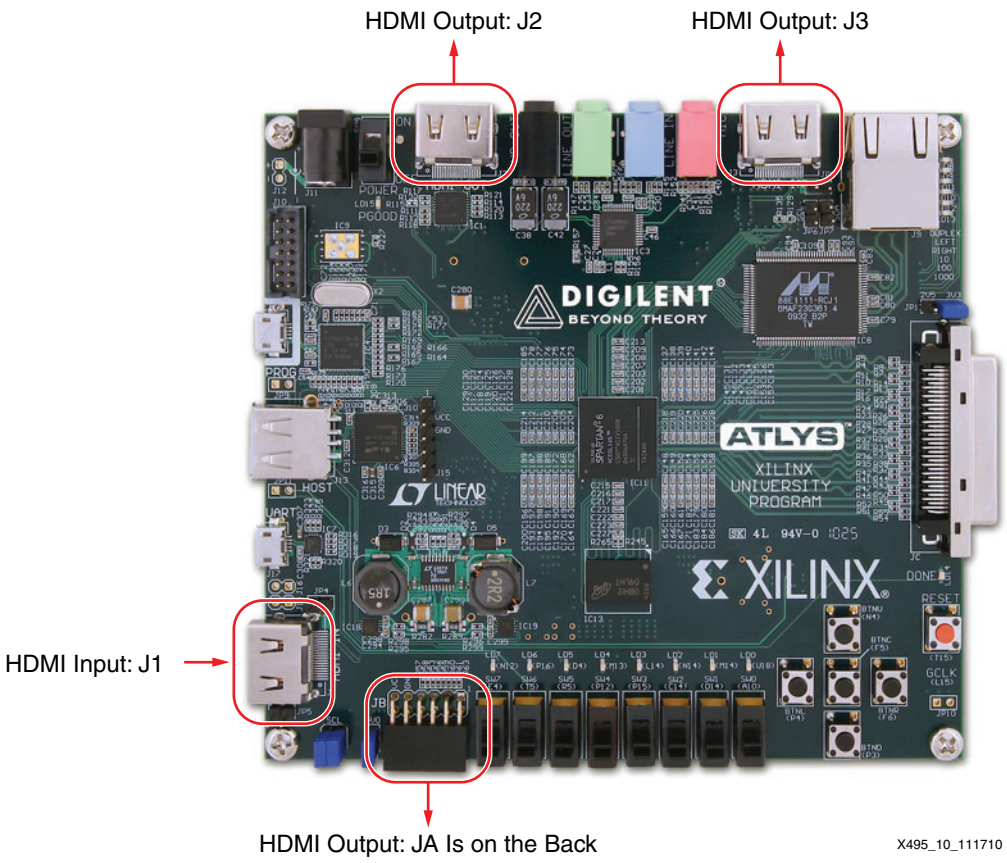

图 10：Atlys TMDS 评估板

Atlys开发板配备2个HDMI输入端口和2个HDMI输出端口。两个输入端口均采用标准type-A型[Ref 7] HDMI接口，分别位于J1和J3位置。而两个输出端口则配置为不同类型的HDMI接口：type-A型[Ref 7]（位于J2位置）和type-D型[Ref 7]（位于JA位置）。所有三个type-A型接口均通过TI TMDS141缓冲器进行信号缓冲。然而，type-D型接口的信号直接连接至Spartan-6 FPGA。两个输入端口中的一个连接至FPGA的I/O Bank 0，另一个连接至Bank 1。type-A型输出端口连接至Bank 0，而type-D型端口则连接至Bank 2。

Atlys开发板是展示Spartan-6 FPGA在单一设备中同时接收、驱动和处理多个TMDS高清视频流卓越性能的理想选择。该开发板可通过赛灵思大学计划获取，或从Digilent公司网站http://www.digilentinc.com订购。

参考设计

在Atlys板上构建了两个参考设计。针对单独的发射器，设计了一个可在多种动态可配置视频时序模式下工作的彩条发生器。为了同时演示发射器和接收器，实现了一个2x2 DVI矩阵。

可编程视频时序控制器

为了验证Spartan-6 FPGA中的TMDS I/O是否能够跨不同屏幕模式传输视频，我们构建了一个与动态可配置像素时钟协同工作的彩条发生器，如图11所示。该像素时钟通过Spartan-6 FPGA的另一新特性DCM_CLKGEN实时生成。该模块通过动态可配置系统数据包接口(SPI)，利用可变的M/D值合成了不同CLKFX频率。

based on a stable incoming clock reference. *Spartan-6 FPGA Clocking Resources User Guide* [Ref 9] contains a detailed discussion about the DCM_CLKGEN feature.

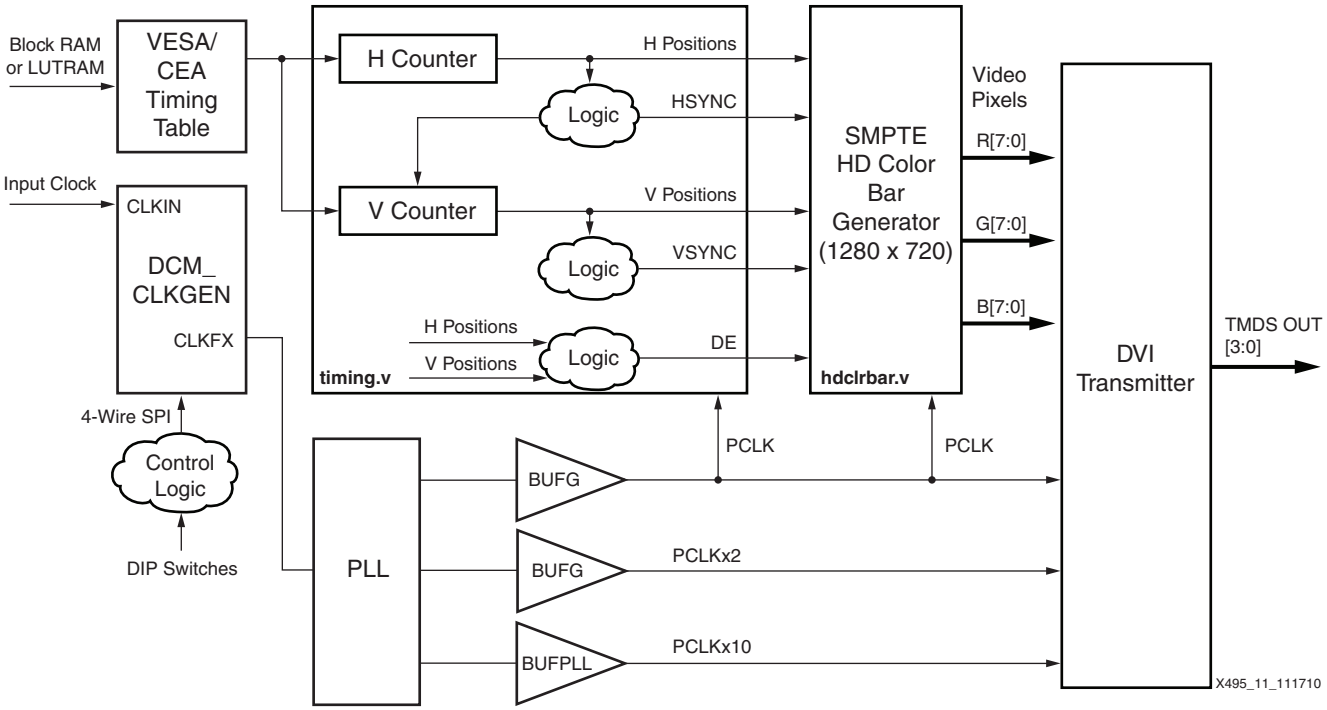

Figure 11: **SMPTE HD Color bar Generation with Programmable Video Timing**

In this design, using three DIP switches on the board (SW0, SW1, and SW3), the user is able to switch among five different screen modes:

- 640x480 @ 60 Hz
- 800x600 @ 60 Hz
- 1024x768 @ 60 Hz
- 1280x720 @ 60 Hz
- 1280x1024 @ 60 Hz

2 x 2 DVI Matrix

The best way to validate the receiver is to pass the video it receives to an output, based on the idea of what you see is what you get. To demonstrate the multi-port capability of the design, all four ports on the Atlys board are used to provide two inputs and two outputs concurrently. Figure 12 illustrates the design topology.

基于稳定的输入时钟参考。Spartan-6 FPGA 时钟资源用户指南 [Ref 9] 包含有关 DCM_CLKGEN 功能的详细讨论。

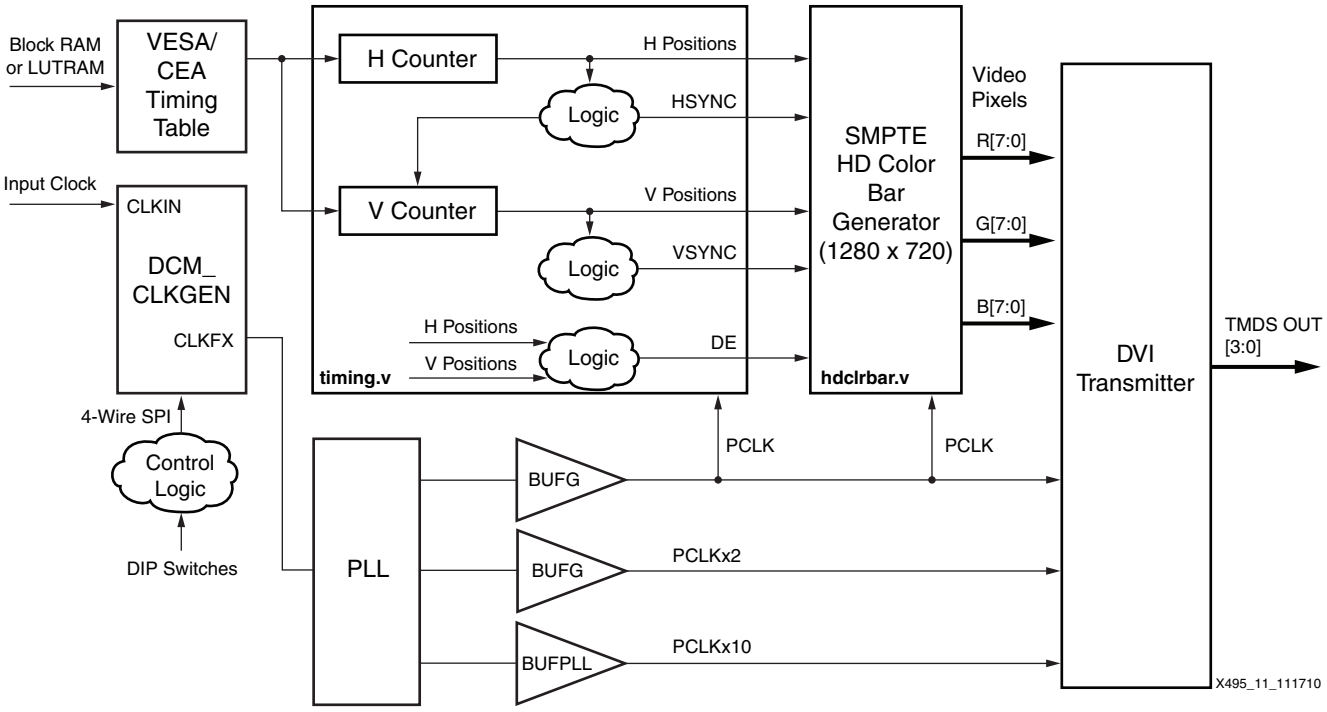

图11：采用可编程视频时序的SMPTE HD彩条生成

在此设计中，通过板载的三个DIP开关（SW0、SW1和SW3），用户可在五种不同的屏幕模式间切换：

- 640x480 @ 60 Hz • 80

0x600 @ 60 Hz • 1024x76

8 @ 60 Hz • 1280x720 @

60 Hz • 1280x1024 @ 60

Hz

2×2 DVI矩阵

验证接收器的最佳方法是将接收到的视频传输至输出端，基于"所见即所得"理念进行验证。为展示设计的多端口功能，Atlys开发板上的全部四个端口被同时用于提供两路输入和两路输出。

图12展示了设计拓扑。

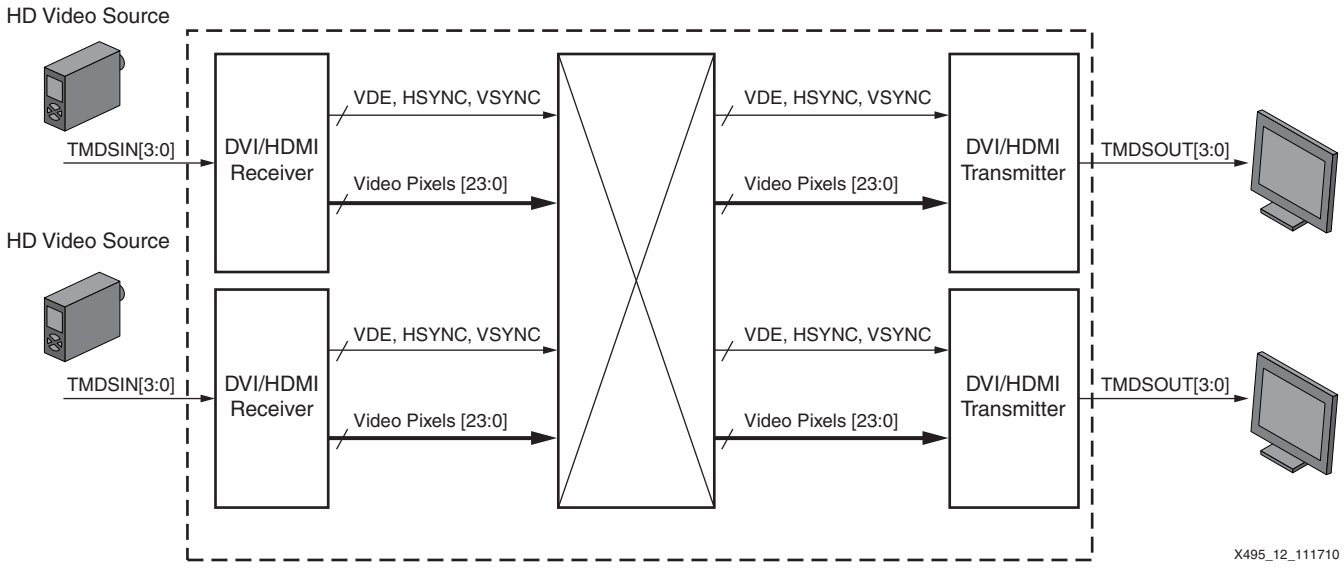

Figure 12: **2 x 2 DVI Matrix**

Using two on-board DIP switches (SW0 and SW1), the design is able to route the two video inputs to its outputs with four possible configurations. Figure 13 shows that the two video inputs are routed to the two video outputs at the same time.

Figure 13: **2 x 2 DVI Matrix Operating**

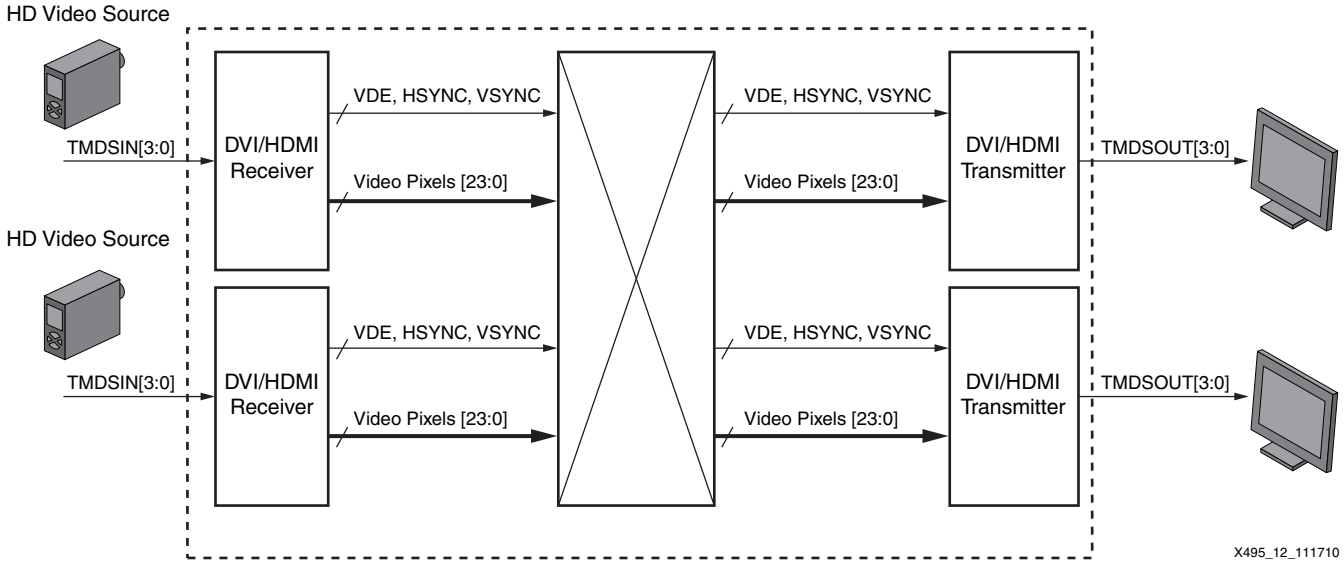

图12: 2 x 2 DVI矩阵

通过两个板载DIP开关（SW0和SW1），该设计能够以四种可能的配置将两个视频输入{v*}路由到其输出端。图13显示两个视频输入{v*}可同时路由至两个视频输出端。

图13: 2 x 2 DVI矩阵运行

Reference Design

Reference Design Files

The reference design files for this application note can be downloaded from:

https://secure.xilinx.com/webreg/clickthrough.do?cid=154258.

The ZIP file contains the following design files:

DVI Transmitter

- `dvi_demo/rtl/tx/dvi_encoder.v`: DVI transmitter top module without instantiation of clocking resources
- `dvi_demo/rtl/tx/dvi_encoder_top.v`: DVI transmitter wrapper with instantiation of clocking resources
- `dvi_demo/rtl/tx/encode.v`: DVI encoder
- `dvi_demo/rtl/tx/serdes_n_to_1.v`: Deconfigurable to 5:1 serializer
- `dvi_demo/rtl/tx/convert_30to15_fifo.v`: 30-bit 2:1 gear box
- `dvi_demo/rtl/tx/vtc_demo.v`: Color bar generator with programmable timing controller

DVI Receiver

- `dvi_demo/rtl/tx/dvi_decoder.v`: DVI receiver top wrapper
- `dvi_demo/rtl/tx/decode.v`: DVI decoder instantiating the CDR and channel deskew circuits
- `dvi_demo/rtl/tx/chnlbond.v`: Channel deskew module
- `dvi_demo/rtl/tx/phsaligner.v`: Bitslip and TMDS data validation state machine
- `dvi_demo/rtl/tx/ serdes_1_to_5_diff_data.v`: 1:5 de-serializer

DVI Common Modules

- `dvi_demo/rtl/common/DRAM16XN.v`: Width configurable distributed RAM
- `dvi_demo/rtl/common/timing.v`: Video Timing Controller
- `dvi_demo/rtl/common/hdclrbar.v`: SMPTE HD color bar generator
- `dvi_demo/rtl/common/debnce.v`: DIP switch debouncer
- `dvi_demo/rtl/common/dcmspi.v`: DCM_CLKGEN SPI controller
- `dvi_demo/rtl/common/synchro.v`: Clock boundary synchronizer

DVI Evaluation

- `dvi_demo/rtl/dvi_demo.v`: 2 x 2 DVI Matrix design

The reference design checklist is shown in Table 3.

Table 3: **Reference Design Checklist**

Parameter	Description
General	
Developer Name	Xilinx
Target Devices (Stepping Level, ES, Production, Speed Grades)	Spartan-6 FPGA
Source Code Provided	Yes
Source Code Format	Verilog

参考设计

参考设计文件

本应用笔记的参考设计文件可从以下位置下载：

高度：https://secure.xilinx.com/webreg/点击通过.do?cid=154258.

ZIP 文件中包含以下设计文件：

DVI发射器

• dvi_demo/rtl/tx/dvi_encoder.v: 未实例化时钟资源的DVI发射器顶层模块 • dvi_demo/rtl/tx/dvi_encoder_top.v: 含时钟资源实例化的DVI发射器封装模块 • dvi_demo/rtl/tx/encode.v: DVI编码器 • dvi_demo/rtl/tx/serdes_n_to_1.v: 可配置为5:1的串行器 • dvi_demo/rtl/tx/convert_30to15_fifo.v: 30位2:1变速器 • dvi_demo/rtl/tx/vtc_demo.v: 带可编程时序控制器的彩条发生器

DVI接收器

• dvi_demo/rtl/tx/dvi_decoder.v：DVI接收器顶层封装• dvi_demo/rtl/tx/decode.v：DVI解码器，实例化CDR和通道去歪斜电路• dvi_demo/rtl/tx/chnlbond.v：通道去歪斜模块• dvi_demo/rtl/tx/phs aligner.v：Bitslip和TMDS数据验证状态机• dvi_demo/rtl/tx/ serdes_1_to_5_diff_data.v：1:5解串器

DVI通用模块

• dvi_demo/rtl/common/DRAM16XN.v: 宽度可配置的分布式RAM • dvi_demo/rtl/common/timing.v: 视频时序控制器 • dvi_demo/rtl/common/hdclrbar.v: SMPTE高清彩条发生器 • dvi_demo/rtl/common/debnce.v: DIP开关消抖器 • dvi_demo/rtl/common/dcmspi.v: DCM_CLKGEN SPI控制器 • dvi_demo/rtl/common/synchro.v: 时钟域同步器

DVI 评估

• dvi_demo/rtl/dvi_demo.v: 2 x 2 DVI矩阵设计 参考设计检查表如表3所示。

表3：参考设计清单

Parameter	Description
General	
Developer Name	Xilinx
Target Devices (Stepping Level, ES, Production, Speed Grades)	Spartan-6 FPGA
Source Code Provided	Yes
Source Code Format	Verilog

Table 3: **Reference Design Checklist *(Cont'd)***

Parameter	Description
Design Uses Code/IP from Existing Application Note, Reference Designs, Third Party, or CORE Generator™ Software	Yes, *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* [Ref 8]
Simulation	
Functional Simulation Performed	Yes
Timing Simulation Performed	No
Testbench Used for Functional and Timing Simulations	No
Testbench Format	Verilog
Simulator Software/Version Used	Cadence IUS 8.2
SPICE/IBIS Simulations	No
Implementation	
Synthesis Software Tools/Version Used	XST, version 12.3
Implementation Software Tools/Versions Used	ISE software, version 12.3
Static Timing Analysis Performed	Yes
Hardware Verification	
Hardware Verified	Yes
Hardware Platform Used for Verification	Digilent Spartan-6 FPGA Atlys Board

Table 4 shows the resource utilization for the DVI transmitter alone.

Table 4: **Resource Utilization for DVI Transmitter**

Resource	Quantity
LUT6	408
Flip-Flops	402
BUFG	2
BUFIO2	1
BUFPLL	1
PLL	1
RAMB	0

Table 5 shows the resource utilization for the DVI receiver alone.

Table 5: **Resource Utilization for DVI Receiver**

Resource	Quantity
LUT6	478
Flip-Flops	453
BUFG	2
BUFIO2	1
BUFPLL	1

表3：参考设计检查清单（续）

Parameter	Description
Design Uses Code/IP from Existing Application Note, Reference Designs, Third Party, or CORE Generator™ Software	Yes, *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* [Ref 8]
Simulation	
Functional Simulation Performed	Yes
Timing Simulation Performed	No
Testbench Used for Functional and Timing Simulations	No
Testbench Format	Verilog
Simulator Software/Version Used	Cadence IUS 8.2
SPICE/IBIS Simulations	No
Implementation	
Synthesis Software Tools/Version Used	XST, version 12.3
Implementation Software Tools/Versions Used	ISE software, version 12.3
Static Timing Analysis Performed	Yes
Hardware Verification	
Hardware Verified	Yes
Hardware Platform Used for Verification	Digilent Spartan-6 FPGA Atlys Board

标签表4显示了DVI发射器的资源利用率{v*}独自。

表4：DVI发送器的资源利用率

Resource	Quantity
LUT6	408
Flip-Flops	402
BUFG	2
BUFIO2	1
BUFPLL	1
PLL	1
RAMB	0

表5展示了单独DVI接收器的资源利用率{v*}。

表 5：DVI 接收器的资源利用率

Resource	Quantity
LUT6	478
Flip-Flops	453
BUFG	2
BUFIO2	1
BUFPLL	1

Table 5: **Resource Utilization for DVI Receiver *(Cont'd)***

Resource	Quantity
PLL	1
RAMB	0

The final resource usage is application or design dependent. For instance, in some pass-through designs, the transmitter and receiver might be able to share the same clocking resources for pixel clock, pixel clock x2, and pixel clock x10. This typically happens when the transmitter and receiver are fully synchronized and both use bank 0 or bank 2 TMDS I/Os. Thus, the actual BUFG, BUFPLL, and PLL count for the transmitter is the same as the receiver alone.

Conclusion

This application note successfully demonstrates a high-definition TMDS video connectivity solution featuring the processing of multiple HD channels in parallel. The design demonstrates the Spartan-6 FPGA in DVI or HDMI applications (including the 480p, 1080i, and 720p video formats).

References

1. XAPP460, *Video Connectivity Using TMDS I/O in Spartan-3A FPGAs*.
2. *VESA Coordinated Video Timing Generator, Revision 1.1*, Video Electronics Standards Association, http://www.vesa.org.
3. CEA-861-D, *A DTV Profile for Uncompressed High Speed Digital Interfaces*, Consumer Electronics Association, http://www.ce.org.
4. UG381, *Spartan-6 FPGA SelectIO Resources User Guide*.
5. DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*.
6. *Digital Visual Interface*, *Revision 1.0*, Digital Display Working Group, http://www.ddwg.org.
7. *High-Definition Multimedia Interface Specification Version 1.3a*, HDMI Licensing, LLC, http://www.hdmi.org.
8. XAPP1064, *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)*.
9. UG382, *Spartan-6 FPGA Clocking Resources User Guide*.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
12/13/10	1.0	Initial Xilinx release.

Notice of Disclaimer

表5：DVI接收器资源利用率（续）

Resource	Quantity
PLL	1
RAMB	0

最终的资源使用情况取决于具体应用或设计。例如，在某些直通设计中，发射器和接收器可能能够共享相同的像素时钟、像素时钟x2和像素时钟x10的时钟资源。这种情况通常发生在发射器和接收器完全同步且均使用组0或组2 TMDS I/O时。因此，发射器实际使用的BUFG、BUFPLL和PLL数量与单独使用接收器时相同。

结论

本应用说明成功演示了一种高清TMDS视频连接解决方案，其特点在于可并行处理多个高清通道。该设计展示了Spartan-6 FPGA在DVI或HDMI应用中的性能（支持480p、1080i和720p视频格式）。

参考文献

1. XAPP460，在Spartan-3A FPGA中使用TMDS I/O实现视频连接。 2. VESA协调视频时序生成器，版本1.1，视频电子标准协会，http://www.vesa.org。 3. CEA-861-D，未压缩高速数字接口的DTV规范，消费电子协会，http://www.ce.org。 4. UG381，Spartan-6 FPGA SelectIO资源用户指南。 5. DS162，Spartan-6 FPGA数据手册：直流与开关特性。 6. 数字视觉接口，版本1.0，数字显示工作组，http://www.ddwg.org。 7. 高清多媒体接口规范版本1.3a，HDMI许可管理公司，http://www.hdmi.org。 8. XAPP1064，源同步串行化与解串行化（最高1050 Mb/s）。 9. UG382，Spartan-6 FPGA时钟资源用户指南。

修订历史

下表显示了本文档的修订历史。

Date	Version	Description of Revisions
12/13/10	1.0	Initial Xilinx release.

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