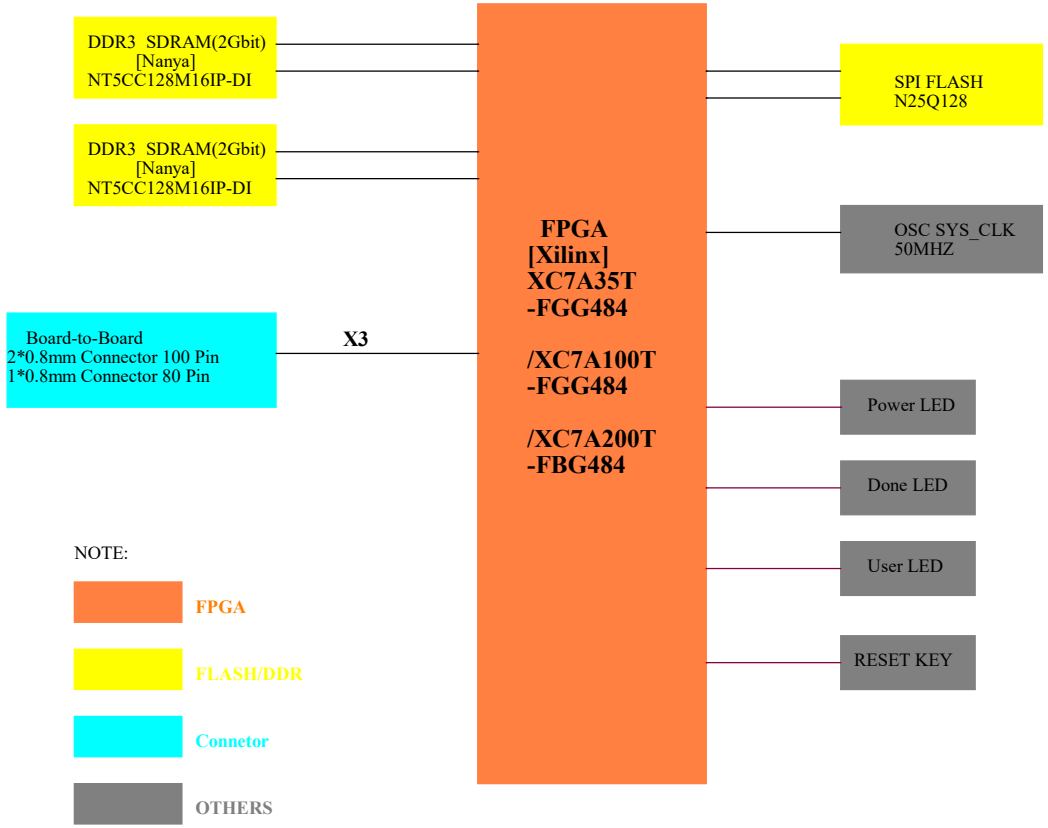
REV	DATE	PAGES	DESCRIPTION
V3.9	2021/10/13	All	初始版本管理
V4.0	2023/12/05	All	兼容紫光PG2L系列型号，升级V4.0丝印以便区分

Title: XC7A35_100_200T_FXG484_4V2_0223	
Author: ALIENTEK	Date: Friday, February 23, 2024
Version: V4.0	File: 00_Revision
Size: A4	Sheet 00 of 12

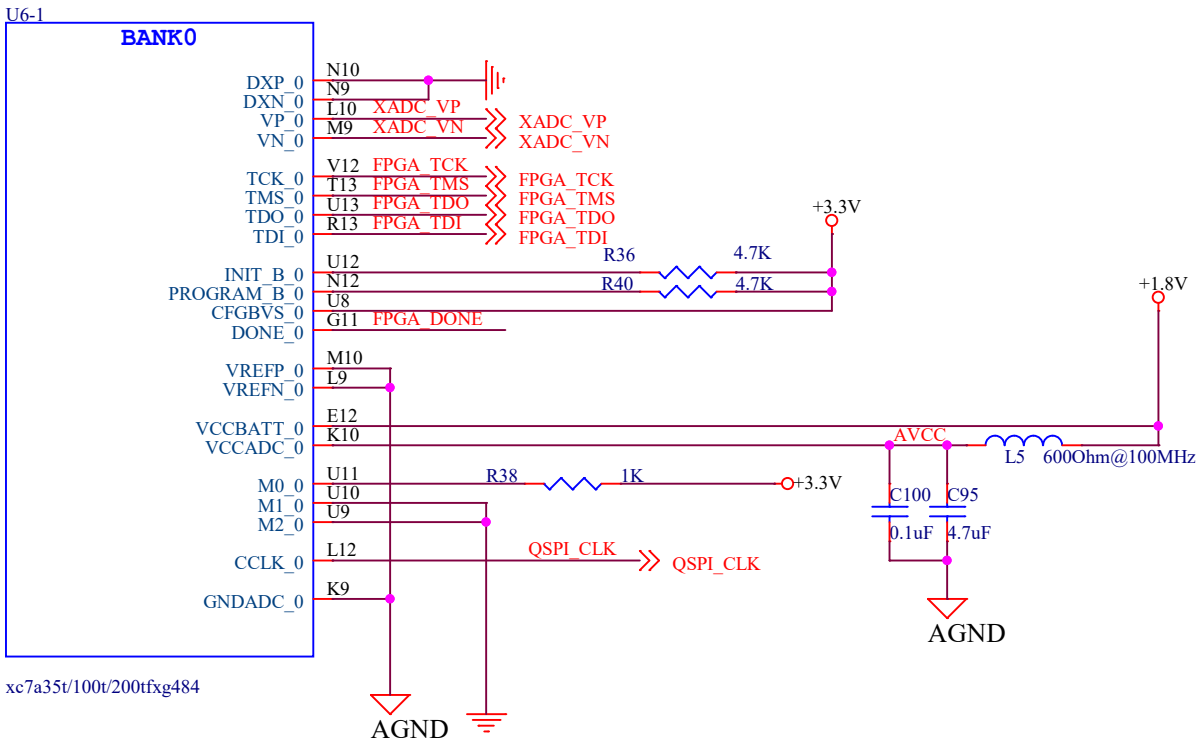
正点原子



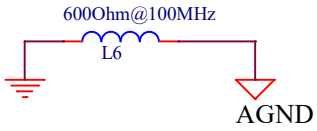
PAGE	Content
00	Revision
01	Block Diagram
02	02_FPGA Bank0
03	03_FPGA Bank13,Bank14
04	04_FPGA Bank15,Bank16
05	05_FPGA Bank34,Bank35
06	06_FPGA Bank216
07	07_FPGA Power
08	08_DDR3 SDRAM
09	09_Flash,Clock
10	10_Power
11	11_Connector
12	12_PHY

Title:	XC7A35_100_200T_FXG484_4V2_0223
Author: ALIENTEK	Date: Friday, February 23, 2024
Version: V4.0	File: 01_Block Diagram
Size: A3	Sheet 01 of 12

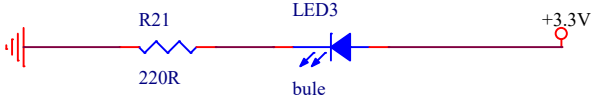
正点原子



MASTER SPI x4
M[2:0] = 001

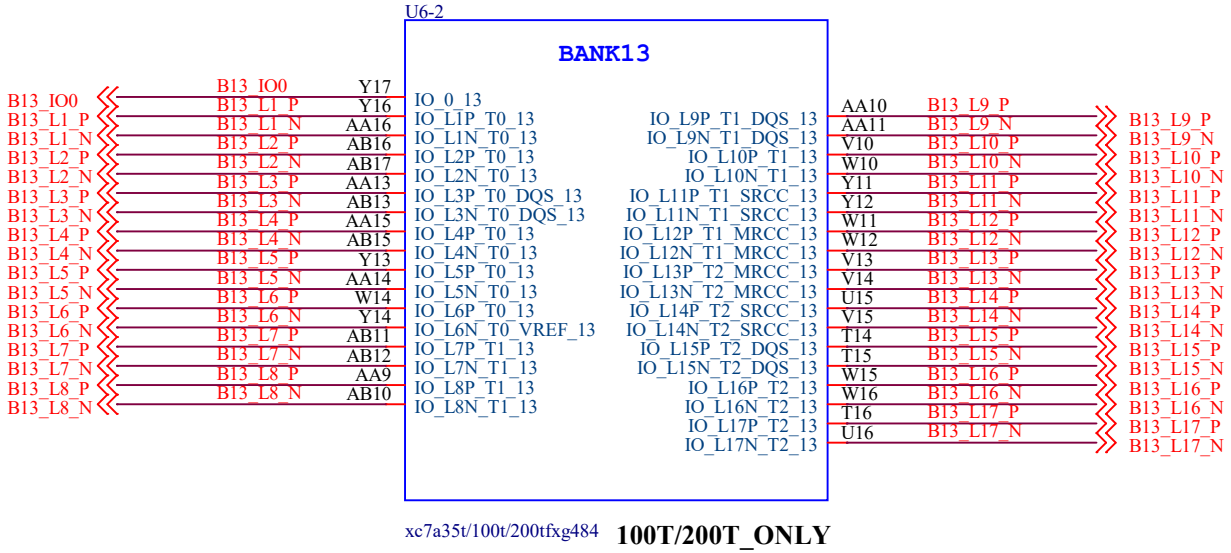


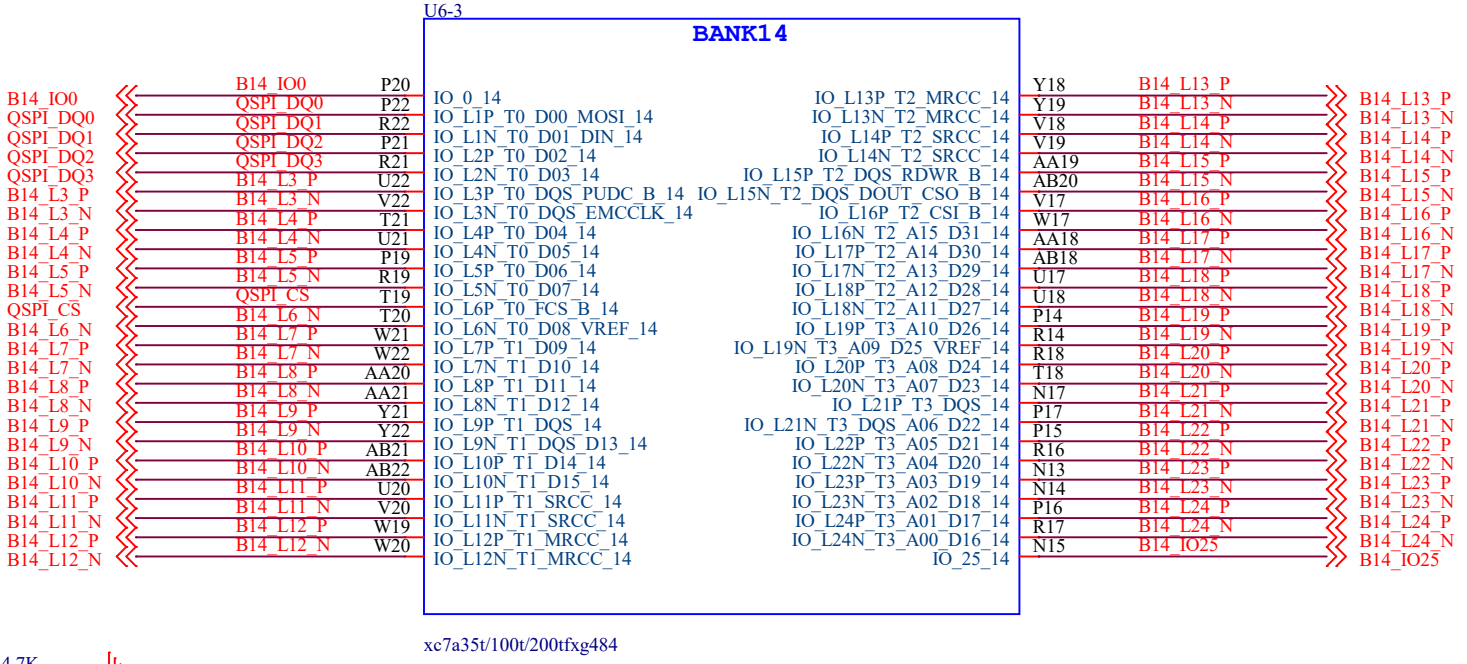
POWER LED

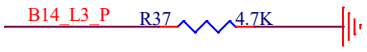


Title: XC7A35_100_200T_FXG484_4V2_0223	
Author: ALIENTEK	Date: Friday, February 23, 2024
Version: V4.0	File: 02_FPGA Bank0
Size: A4	Sheet 02 of 12

正点原子



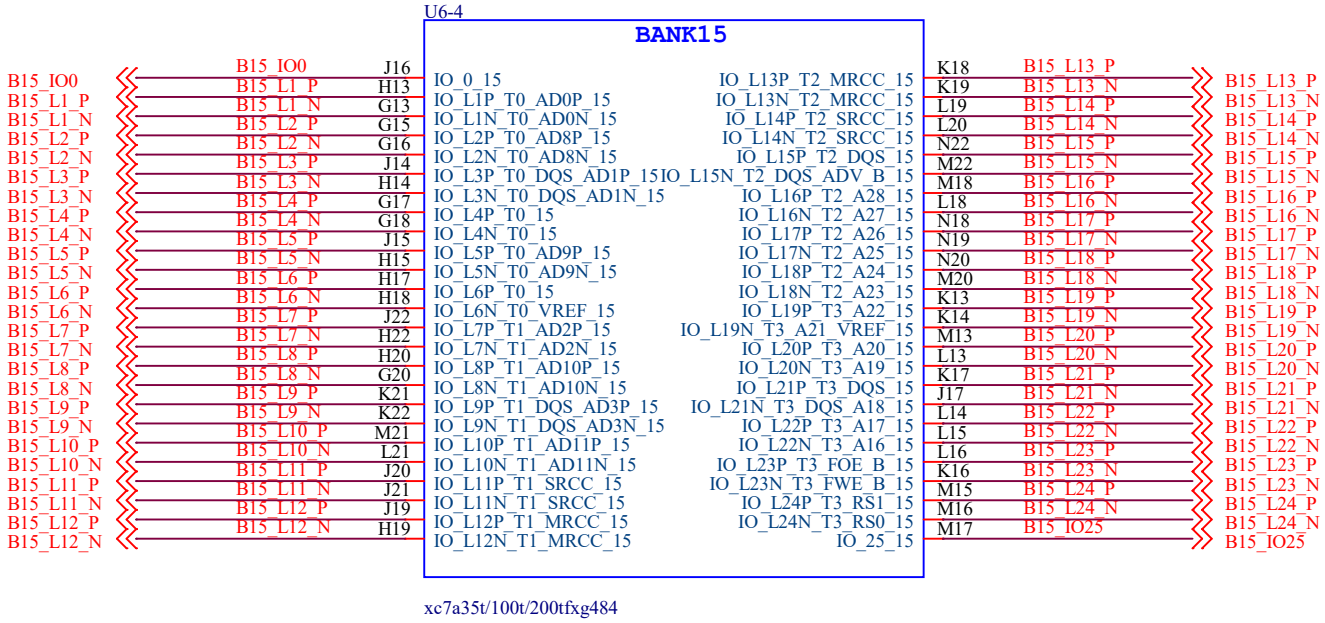


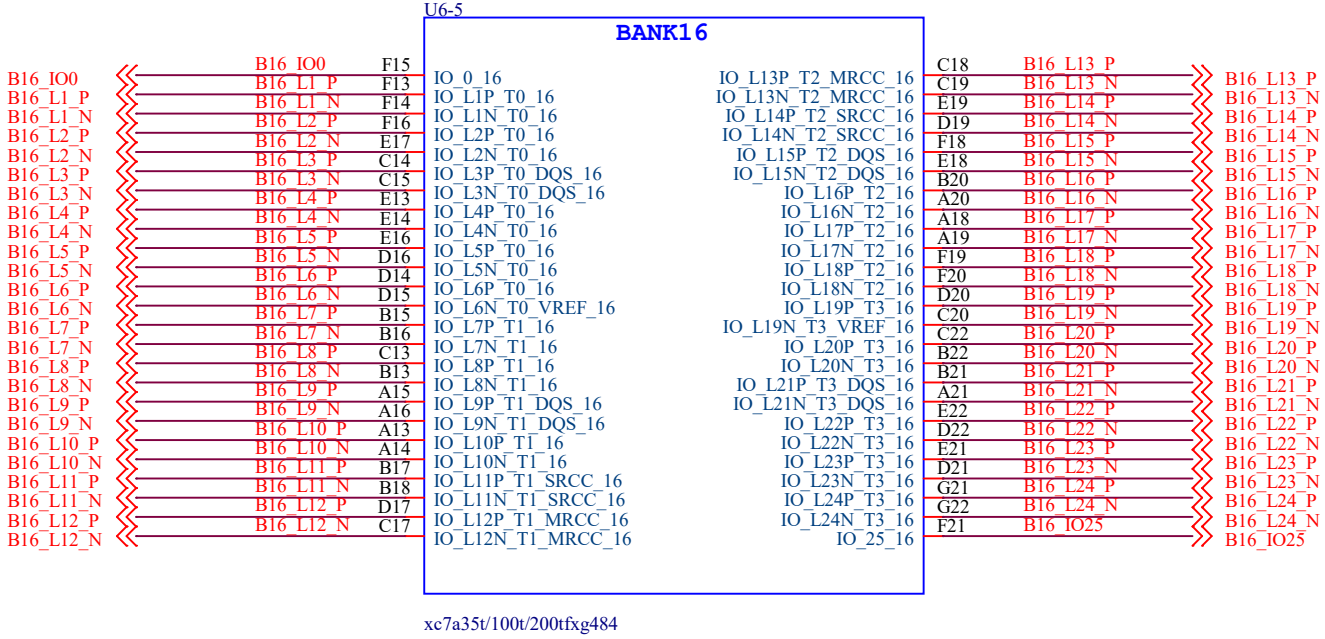


PUDC_B=0: Active internal Pull up Resister

Title: XC7A35_100_200T_FXG484_4V2_0223	
Author: ALIENTEK	Date: Friday, February 23, 2024
Version: V4.0	File: 03_FPGA Bank13,Bank14
Size: A4	Sheet 03 of 12

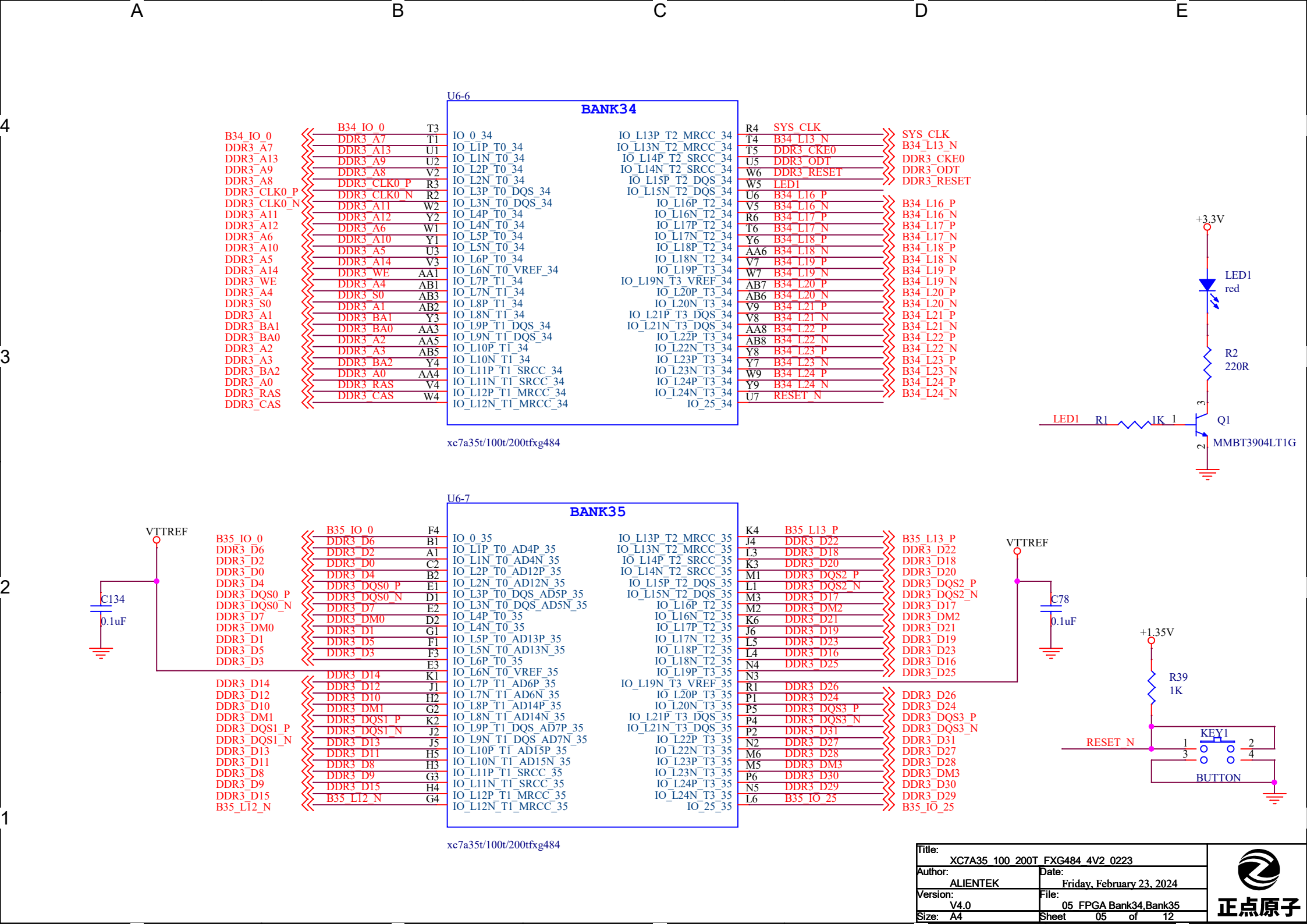
正点原子

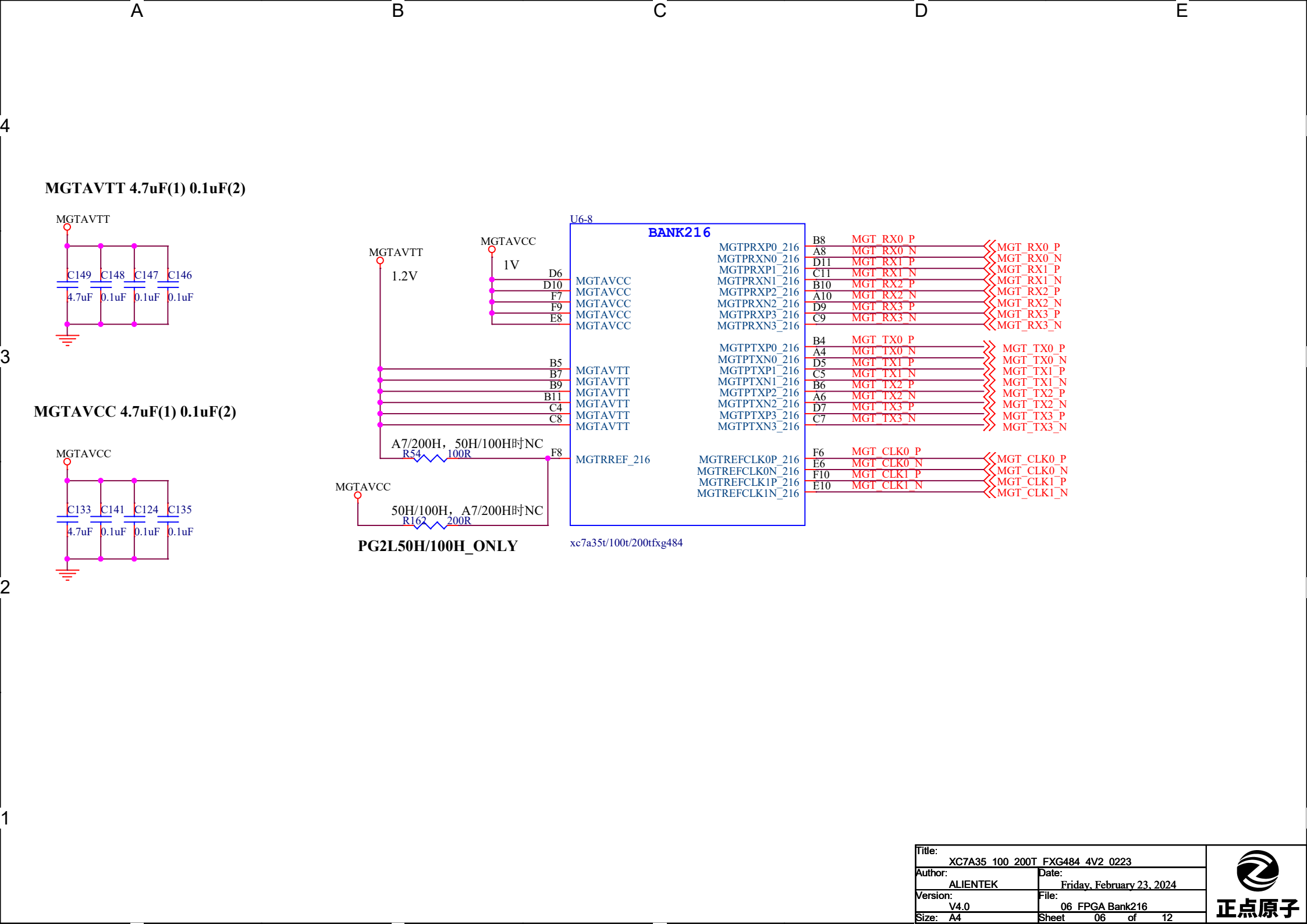




Title: XC7A35_100_200T_FXG484_4V2_0223	
Author: ALIENTEK	Date: Friday, February 23, 2024
Version: V4.0	File: 04_FPGA Bank15,Bank16
Size: A4	Sheet 04 of 12

正点原子


A
B
C
D
E
4
3
2
1
U6-6
BANK34
B34_IO_0
DDR3_A7
DDR3_A13
DDR3_A9
DDR3_A8
DDR3_CLK0_P
DDR3_CLK0_N
DDR3_A11
DDR3_A12
DDR3_A6
DDR3_A10
DDR3_A5
DDR3_A14
DDR3_WE
DDR3_A4
DDR3_S0
DDR3_A1
DDR3_BA1
DDR3_BA0
DDR3_A2
DDR3_A3
DDR3_BA2
DDR3_A0
DDR3_RAS
DDR3_CAS
T3 T1 U1 U2 V2 R3 R2 W2 Y2 W1 Y1 U3 V3 AA1 AB1 AB3 AB2 Y3 AA3 AA5 AB5 Y4 AA4 V4 W4
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
R4 T4 T5 U5 W6 W5 U6 V5 R6 T6 Y6 AA6 V7 W7 AB7 AB6 V9 V8 AA8 AB8 Y8 Y7 W9 Y9 U7
SYS_CLK
B34_L13_N
DDR3_CKE0
DDR3_ODT
DDR3_RESET
LED1
B34_L16_P
B34_L16_N
B34_L17_P
B34_L17_N
B34_L18_P
B34_L18_N
B34_L19_P
B34_L19_N
B34_L20_P
B34_L20_N
B34_L21_P
B34_L21_N
B34_L22_P
B34_L22_N
B34_L23_P
B34_L23_N
B34_L24_P
B34_L24_N
RESET_N
xc7a35t/100t/200tfxg484
+3.3V
LED1
red
R2
220R
LED1
R1
1K
Q1
MMBT3904LT1G
U6-7
BANK35
B35_IO_0
DDR3_D6
DDR3_D2
DDR3_D0
DDR3_D4
DDR3_DQS0_P
DDR3_DQS0_N
DDR3_D7
DDR3_DM0
DDR3_D1
DDR3_D5
DDR3_D3
DDR3_D14
DDR3_D12
DDR3_D10
DDR3_DM1
DDR3_DQS1_P
DDR3_DQS1_N
DDR3_D13
DDR3_D11
DDR3_D8
DDR3_D9
DDR3_D15
B35_L12_N
F4 B1 A1 C2 B2 E1 D1 E2 D2 G1 F1 F3 E3 K1 J1 H2 G2 K2 J2 J5 H5 H3 G3 H4 G4
IO_0_35
IO_L1P_T0_AD4P_35
IO_L1N_T0_AD4N_35
IO_L2P_T0_AD12P_35
IO_L2N_T0_AD12N_35
IO_L3P_T0_DQS_AD5P_35
IO_L3N_T0_DQS_AD5N_35
IO_L4P_T0_35
IO_L4N_T0_35
IO_L5P_T0_AD13P_35
IO_L5N_T0_AD13N_35
IO_L6P_T0_35
IO_L6N_T0_VREF_35
IO_L7P_T1_AD6P_35
IO_L7N_T1_AD6N_35
IO_L8P_T1_AD14P_35
IO_L8N_T1_AD14N_35
IO_L9P_T1_DQS_AD7P_35
IO_L9N_T1_DQS_AD7N_35
IO_L10P_T1_AD15P_35
IO_L10N_T1_AD15N_35
IO_L11P_T1_SRCC_35
IO_L11N_T1_SRCC_35
IO_L12P_T1_MRCC_35
IO_L12N_T1_MRCC_35
IO_L13P_T2_MRCC_35
IO_L13N_T2_MRCC_35
IO_L14P_T2_SRCC_35
IO_L14N_T2_SRCC_35
IO_L15P_T2_DQS_35
IO_L15N_T2_DQS_35
IO_L16P_T2_35
IO_L16N_T2_35
IO_L17P_T2_35
IO_L17N_T2_35
IO_L18P_T2_35
IO_L18N_T2_35
IO_L19P_T3_35
IO_L19N_T3_VREF_35
IO_L20P_T3_35
IO_L20N_T3_35
IO_L21P_T3_DQS_35
IO_L21N_T3_DQS_35
IO_L22P_T3_35
IO_L22N_T3_35
IO_L23P_T3_35
IO_L23N_T3_35
IO_L24P_T3_35
IO_L24N_T3_35
IO_25_35
K4 J4 L3 K3 M1 L1 M3 M2 K6 J6 L5 L4 N4 N3 R1 P1 P5 P4 P2 N2 M6 M5 P6 N5 L6
B35_L13_P
DDR3_D22
DDR3_D18
DDR3_D20
DDR3_DQS2_P
DDR3_DQS2_N
DDR3_D17
DDR3_DM2
DDR3_D21
DDR3_D19
DDR3_D23
DDR3_D16
DDR3_D25
DDR3_D26
DDR3_D24
DDR3_DQS3_P
DDR3_DQS3_N
DDR3_D31
DDR3_D27
DDR3_D28
DDR3_DM3
DDR3_D30
DDR3_D29
B35_IO_25
xc7a35t/100t/200tfxg484
VTTREF
C134
0.1uF
VTTREF
C78
0.1uF
+1.35V
R39
1K
KEY1
RESET_N
BUTTON
Title:
XC7A35_100_200T_FXG484_4V2_0223
Author:
ALIENTEK
Date:
Friday, February 23, 2024
Version:
V4.0
File:
05_FPGA Bank34,Bank35
Size: A4
Sheet 05 of 12
正点原子


A
B
C
D
E
4
3
2
1
MGTAVTT 4.7uF(1) 0.1uF(2)
MGTAVTT
C149 C148 C147 C146
4.7uF 0.1uF 0.1uF 0.1uF
MGTAVCC 4.7uF(1) 0.1uF(2)
MGTAVCC
C133 C141 C124 C135
4.7uF 0.1uF 0.1uF 0.1uF
U6-8
BANK216
MGTAVTT
1.2V
MGTAVCC
1V
D6
D10
F7
F9
E8
MGTAVCC
MGTAVCC
MGTAVCC
MGTAVCC
MGTAVCC
B5
B7
B9
B11
C4
C8
MGTAVTT
MGTAVTT
MGTAVTT
MGTAVTT
MGTAVTT
MGTAVTT
A7/200H，50H/100H时NC
R54 100R
F8
MGTRREF_216
MGTAVCC
50H/100H，A7/200H时NC
R162 200R
PG2L50H/100H_ONLY
xc7a35t/100t/200tfxg484
MGTPRXP0_216
MGTPRXN0_216
MGTPRXP1_216
MGTPRXN1_216
MGTPRXP2_216
MGTPRXN2_216
MGTPRXP3_216
MGTPRXN3_216
B8 MGT_RX0_P
A8 MGT_RX0_N
D11 MGT_RX1_P
C11 MGT_RX1_N
B10 MGT_RX2_P
A10 MGT_RX2_N
D9 MGT_RX3_P
C9 MGT_RX3_N
MGT_RX0_P
MGT_RX0_N
MGT_RX1_P
MGT_RX1_N
MGT_RX2_P
MGT_RX2_N
MGT_RX3_P
MGT_RX3_N
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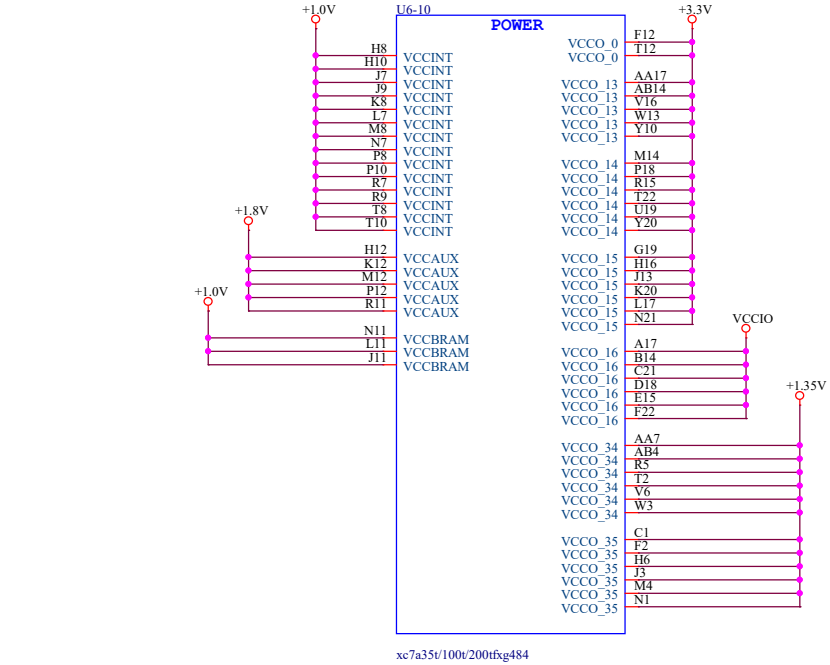
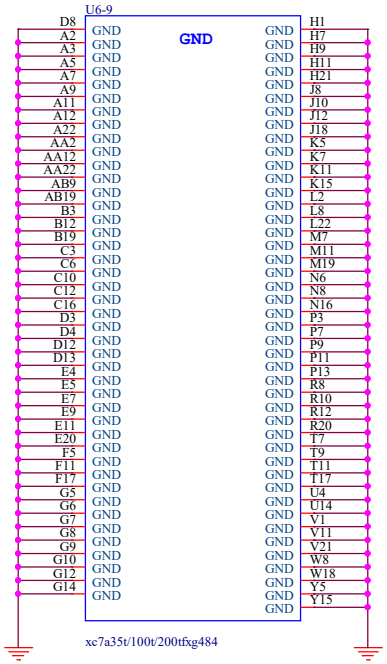
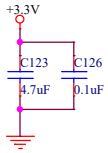
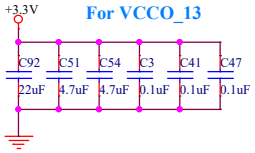
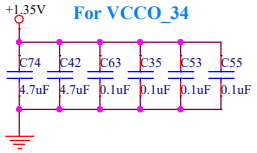
MGTPTXN0_216
MGTPTXP1_216
MGTPTXN1_216
MGTPTXP2_216
MGTPTXN2_216
MGTPTXP3_216
MGTPTXN3_216
B4 MGT_TX0_P
A4 MGT_TX0_N
D5 MGT_TX1_P
C5 MGT_TX1_N
B6 MGT_TX2_P
A6 MGT_TX2_N
D7 MGT_TX3_P
C7 MGT_TX3_N
MGT_TX0_P
MGT_TX0_N
MGT_TX1_P
MGT_TX1_N
MGT_TX2_P
MGT_TX2_N
MGT_TX3_P
MGT_TX3_N
MGTREFCLK0P_216
MGTREFCLK0N_216
MGTREFCLK1P_216
MGTREFCLK1N_216
F6 MGT_CLK0_P
E6 MGT_CLK0_N
F10 MGT_CLK1_P
E10 MGT_CLK1_N
MGT_CLK0_P
MGT_CLK0_N
MGT_CLK1_P
MGT_CLK1_N
Title: XC7A35_100_200T_FXG484_4V2_0223
Author: ALIENTEK
Date: Friday, February 23, 2024
Version: V4.0
File: 06_FPGA Bank216
Size: A4
Sheet 06 of 12
正点原子

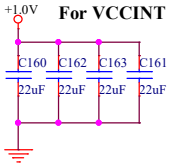


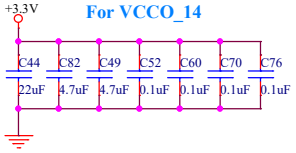


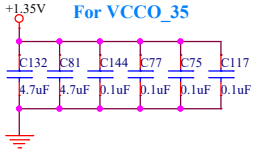


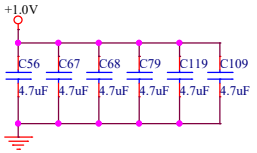


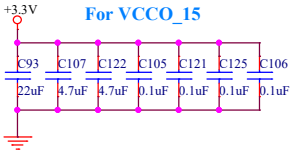


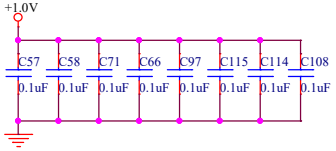


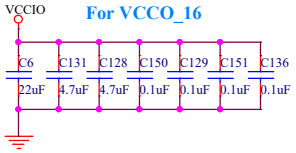


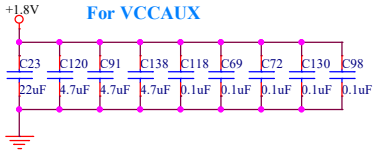


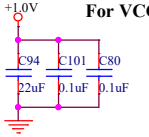






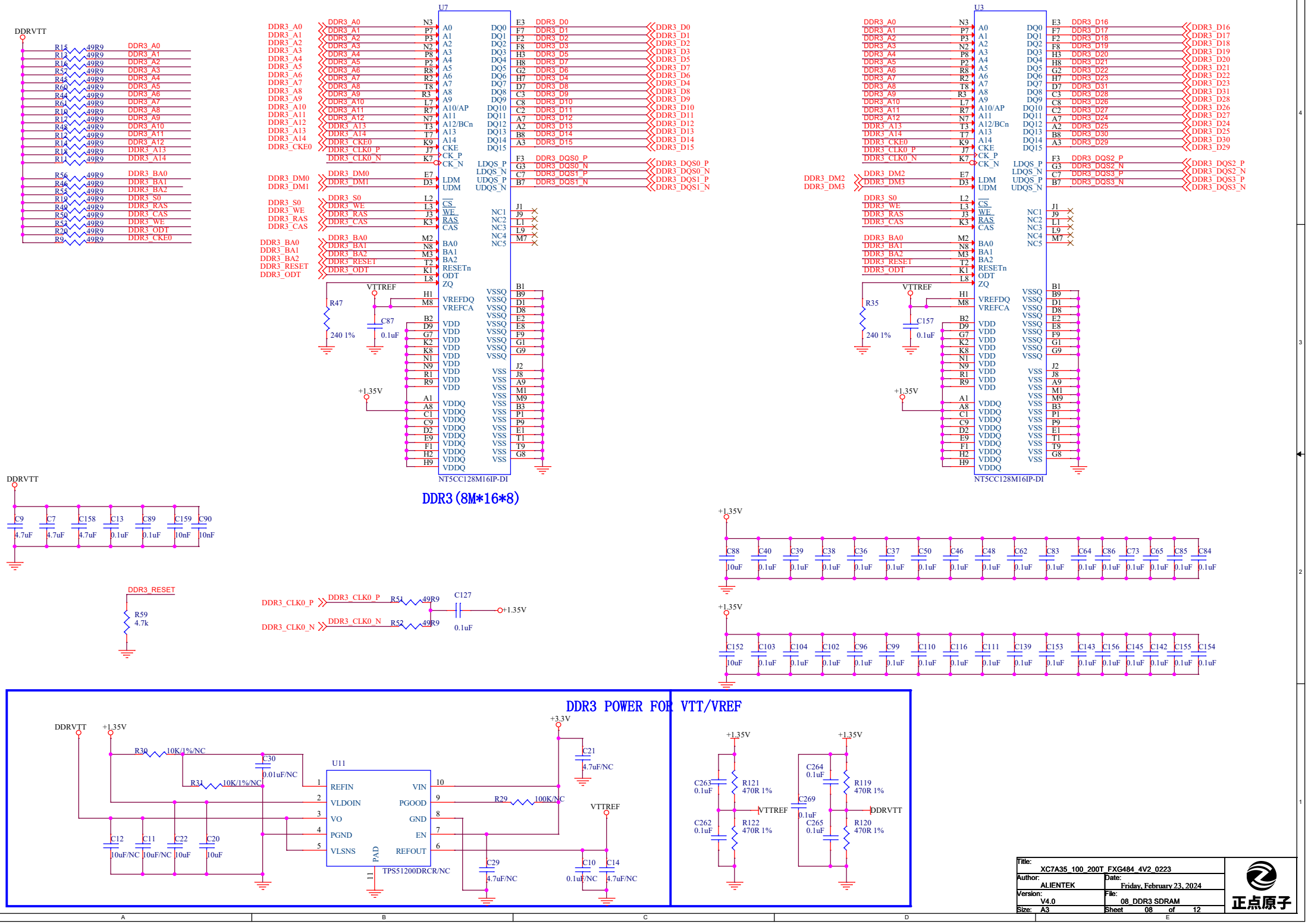


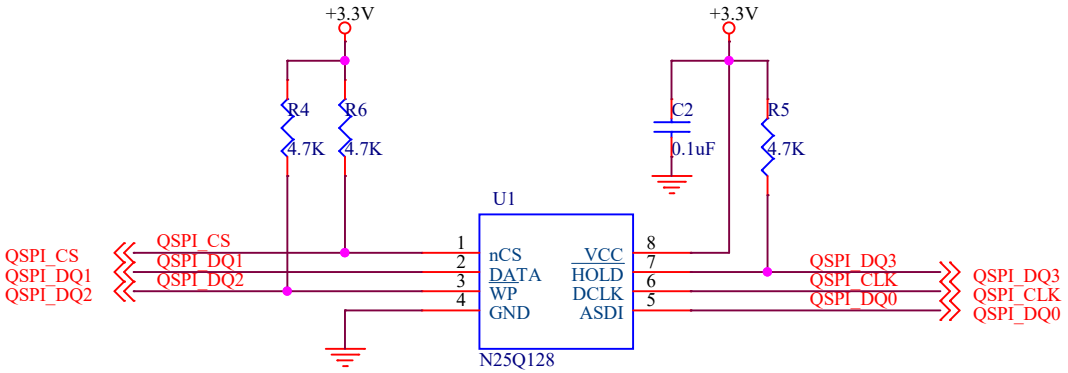




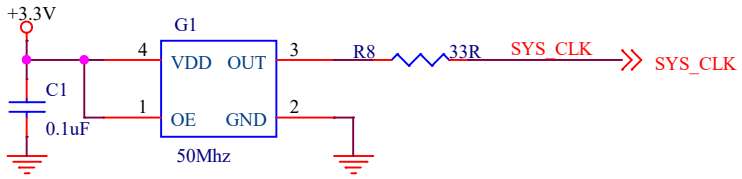
Title: XC7A35_100_200T_FXG484_4V2_0223	
Author: ALIENTEK	Date: Friday, February 23, 2024
Version: V4.0	File: 07_FPGA Power
Size: A3	Sheet 07 of 12

正点原子

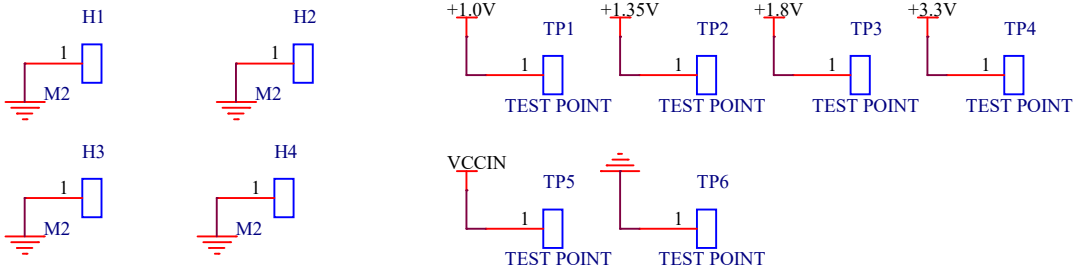

DDRVTT
R15 49R9 DDR3_A0
R12 49R9 DDR3_A1
R16 49R9 DDR3_A2
R52 49R9 DDR3_A3
R42 49R9 DDR3_A4
R60 49R9 DDR3_A5
R44 49R9 DDR3_A6
R61 49R9 DDR3_A7
R10 49R9 DDR3_A8
R12 49R9 DDR3_A9
R43 49R9 DDR3_A10
R13 49R9 DDR3_A11
R14 49R9 DDR3_A12
R15 49R9 DDR3_A13
R11 49R9 DDR3_A14
R56 49R9 DDR3_BA0
R46 49R9 DDR3_BA1
R55 49R9 DDR3_BA2
R19 49R9 DDR3_S0
R49 49R9 DDR3_RAS
R50 49R9 DDR3_CAS
R53 49R9 DDR3_WE
R20 49R9 DDR3_ODT
R9 49R9 DDR3_CKE0
U7
NT5CC128M16IP-DI
DDR3 (8M*16*8)
U3
NT5CC128M16IP-DI
VTTREF
R47 240 1%
C87 0.1uF
R35 240 1%
C157 0.1uF
+1.35V
DDRVTT
C9 4.7uF
C7 4.7uF
C158 4.7uF
C13 0.1uF
C89 0.1uF
C159 10nF
C90 10nF
DDR3_RESET
R59 4.7k
DDR3_CLK0_P
DDR3_CLK0_N
R51 49R9
R52 49R9
C127 0.1uF
C88 10uF
C40 0.1uF
C39 0.1uF
C38 0.1uF
C36 0.1uF
C37 0.1uF
C50 0.1uF
C46 0.1uF
C48 0.1uF
C62 0.1uF
C83 0.1uF
C64 0.1uF
C86 0.1uF
C73 0.1uF
C65 0.1uF
C85 0.1uF
C84 0.1uF
C152 10uF
C103 0.1uF
C104 0.1uF
C102 0.1uF
C96 0.1uF
C99 0.1uF
C110 0.1uF
C116 0.1uF
C111 0.1uF
C139 0.1uF
C153 0.1uF
C143 0.1uF
C156 0.1uF
C145 0.1uF
C142 0.1uF
C155 0.1uF
C154 0.1uF
DDR3 POWER FOR VTT/VREF
+3.3V
U11
REFIN
VLDOIN
VO
PGND
VLSNS
VIN
PGOOD
GND
EN
REFOUT
PAD
TPS51200DRCR/NC
R30 10K/1%/NC
R31 10K/1%/NC
C30 0.01uF/NC
R29 100K/NC
C21 4.7uF/NC
C12 10uF/NC
C11 10uF/NC
C22 10uF
C20 10uF
C29 4.7uF/NC
C10 0.1uF/NC
C14 4.7uF/NC
C263 0.1uF
R121 470R 1%
R122 470R 1%
C262 0.1uF
C264 0.1uF
R119 470R 1%
C269 0.1uF
R120 470R 1%
C265 0.1uF
Title: XC7A35_100_200T_FXG484_4V2_0223
Author: ALIENTEK
Date: Friday, February 23, 2024
Version: V4.0
File: 08_DDR3 SDRAM
Size: A3
Sheet 08 of 12
正点原子



FPGA CONFIG SPI

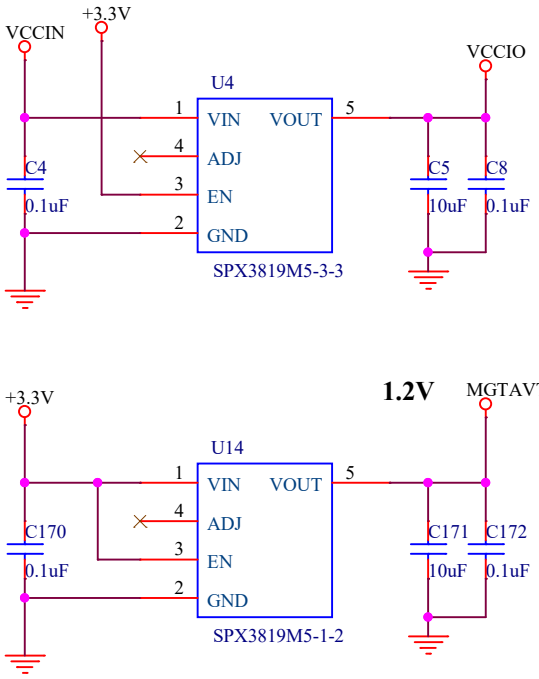


SYSTEM CLOCK



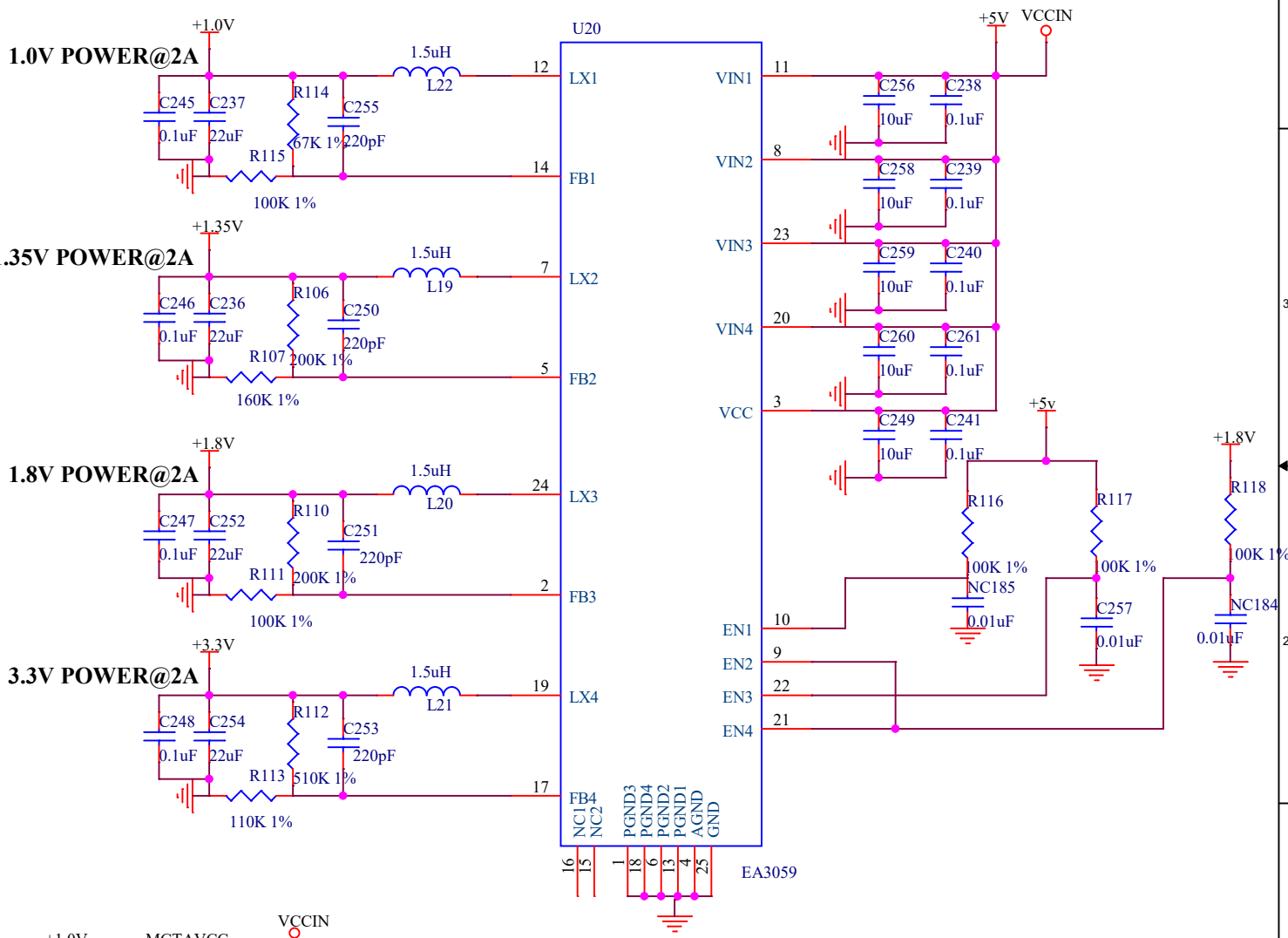
Title: XC7A35_100_200T_FXG484_4V2_0223	
Author: ALIENTEK	Date: Friday, February 23, 2024
Version: V4.0	File: 09_Flash,Clock
Size: A4	Sheet 09 of 12

正点原子



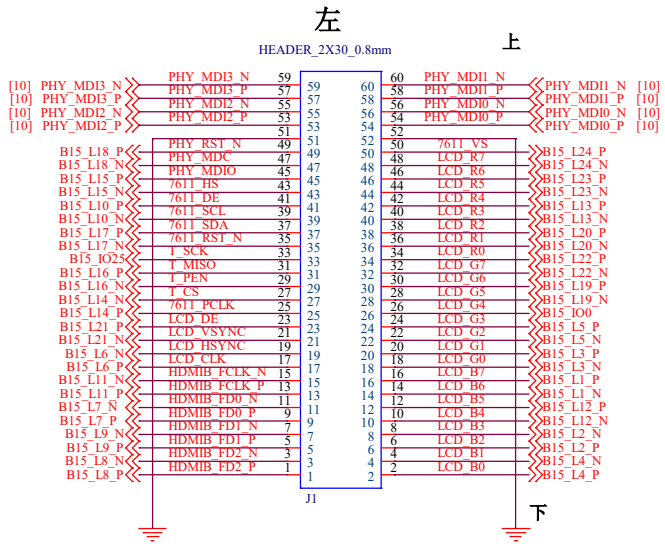
Power On Sequnce:
1.0V -> 1.8V -> 1.35V & 3.3V -> VCCIO

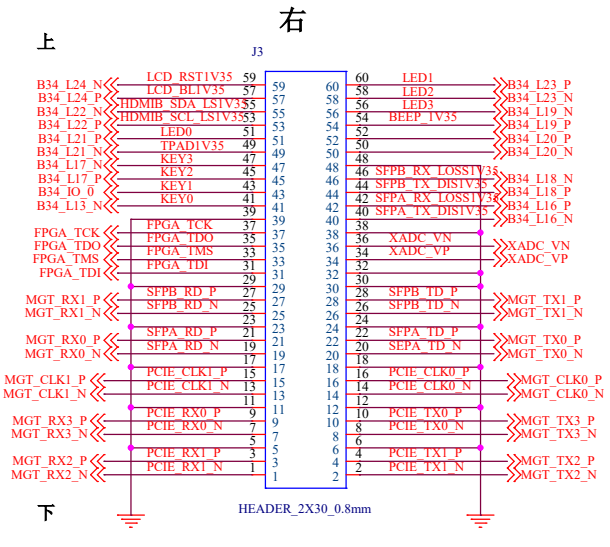
Vout=0.6*R1/R2+0.6



Title: XC7A35_100_200T_FXG484_4V2_0223	
Author: ALIENTEK	Date: Friday, February 23, 2024
Version: V4.0	File: 10_Power
Size: A4	Sheet 10 of 12

正点原子





X2 L5 singal must equal and not in lvds layout ,singal must 2W.

These IOs are on R5&R4, Voltage is 1.5V!!!

L5 IO total num is 45!

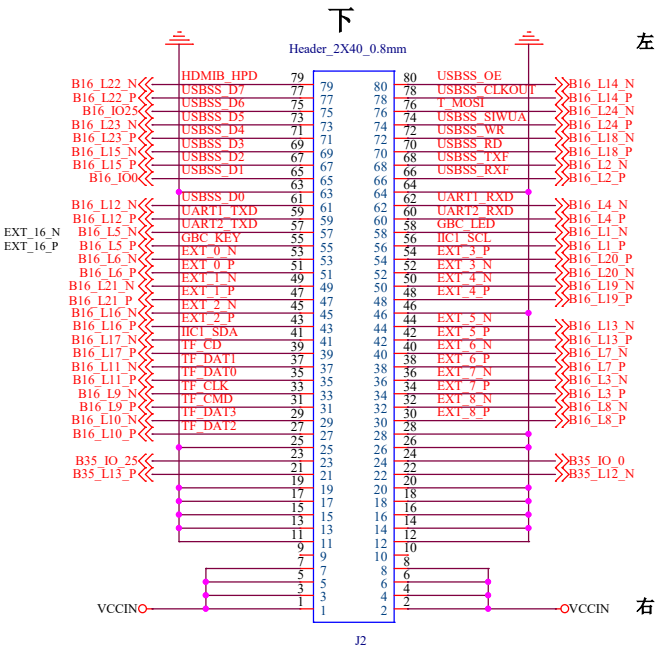
L6 IO total num is 35, only A100T has bank 13!

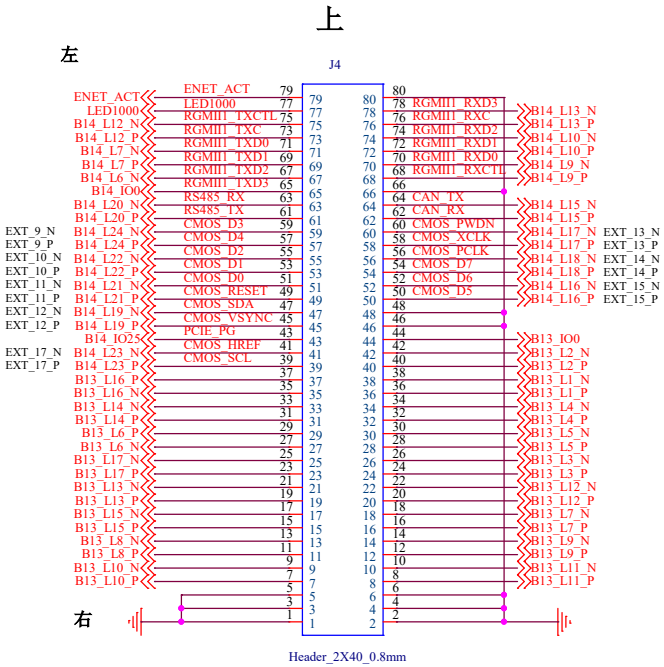
L4 IO total num is 50!

L3 IO total num is 50!

R5 IO total num is 20!

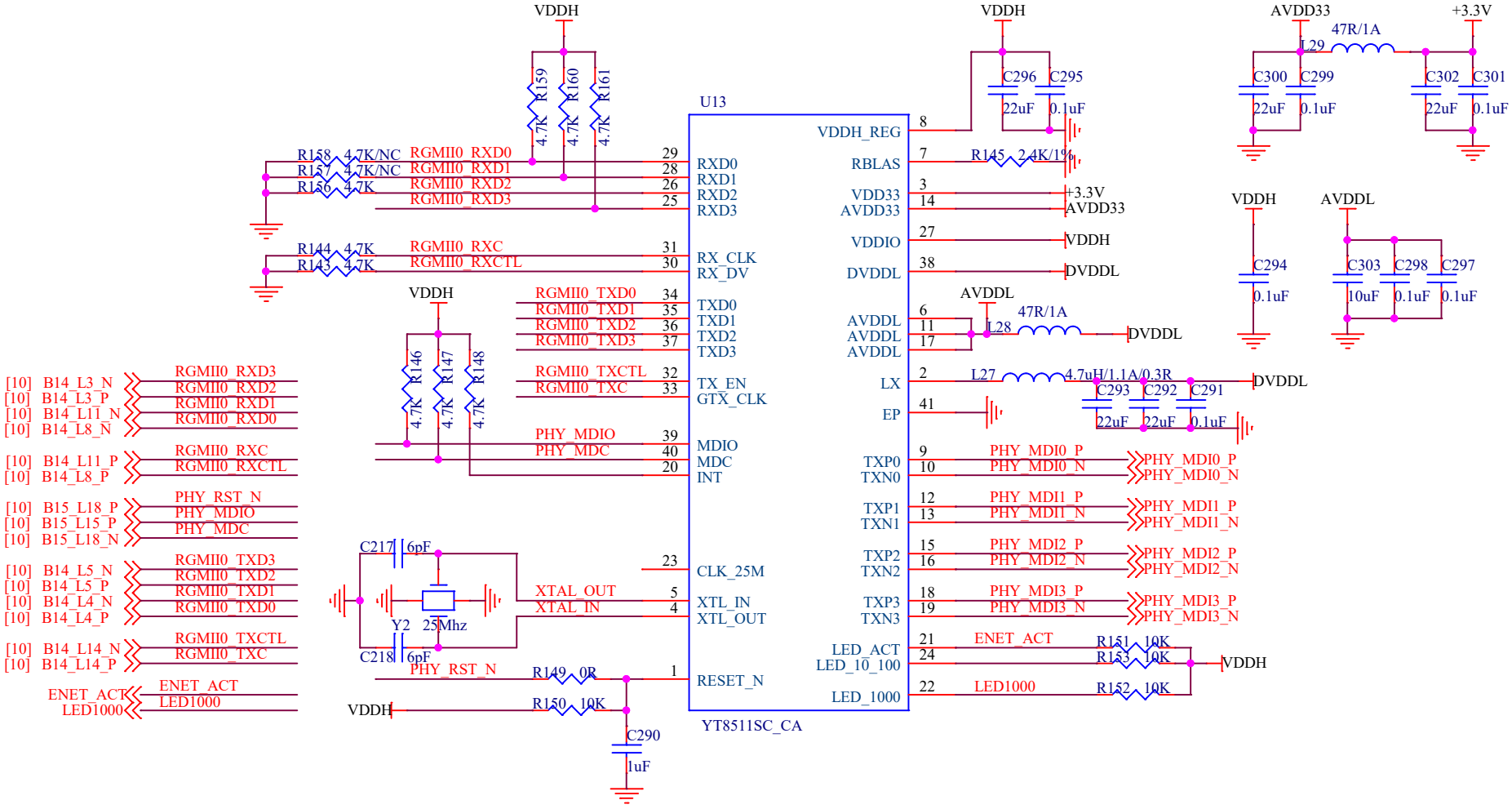
R4 IO total num is 4!





Title:	XC7A35_100_200T_FXG484_4V2_0223
Author: ALIENTEK	Date: Friday, February 23, 2024
Version: V4.0	File: 11_Connector
Size: A3	Sheet 11 of 12

正点原子



Title: XC7A35_100_200T_FXG484_4V2_0223	
Author: ALIENTEK	Date: Friday, February 23, 2024
Version: V4.0	File: 12_PHY
Size: A4	Sheet 12 of 12

正点原子