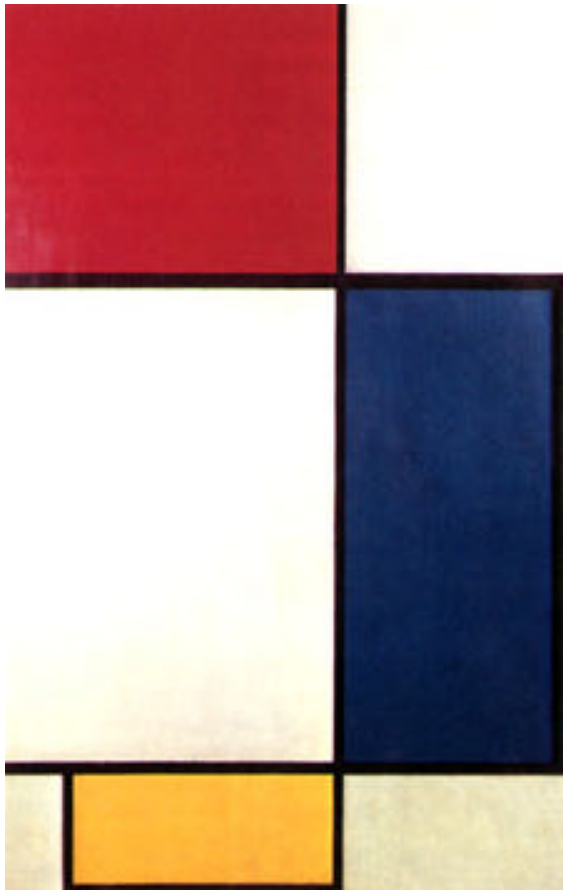
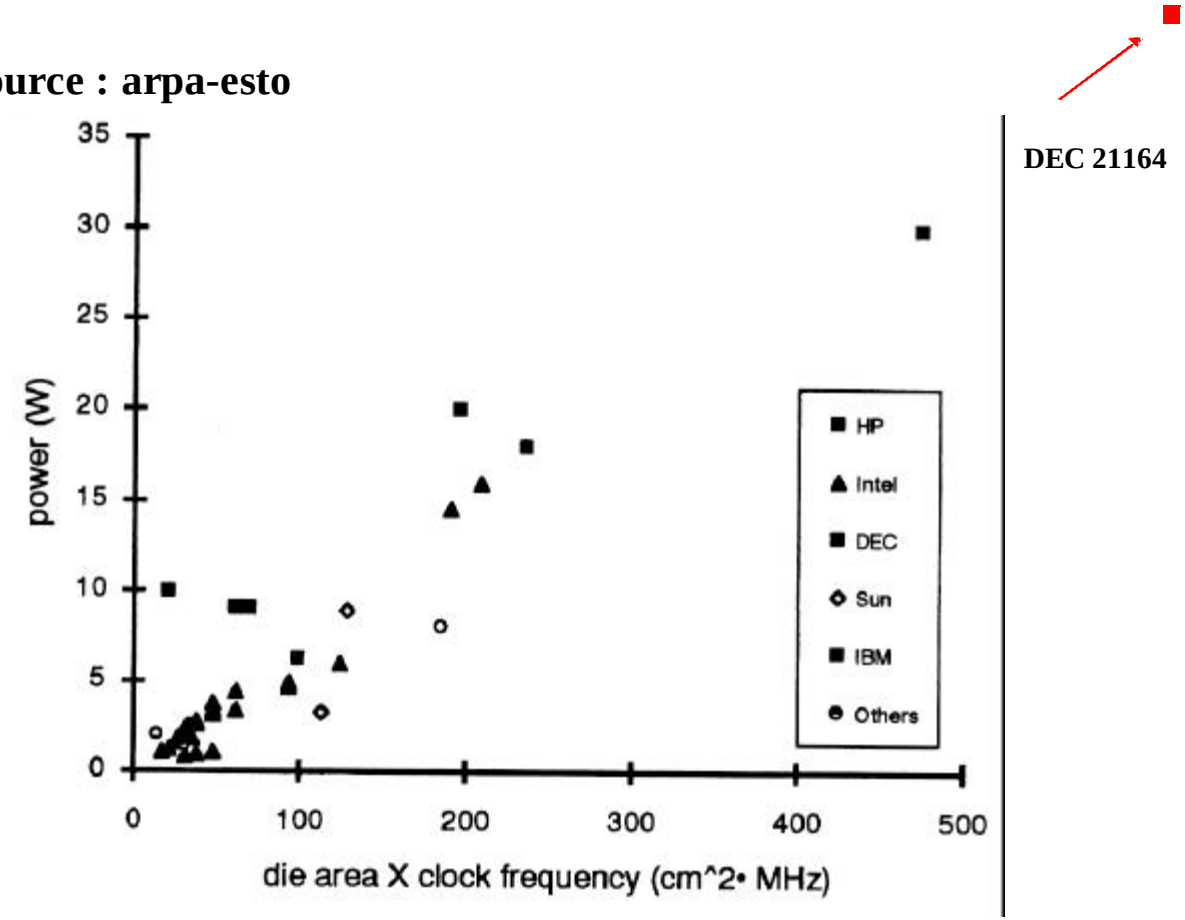
Low Power Design in CMOS



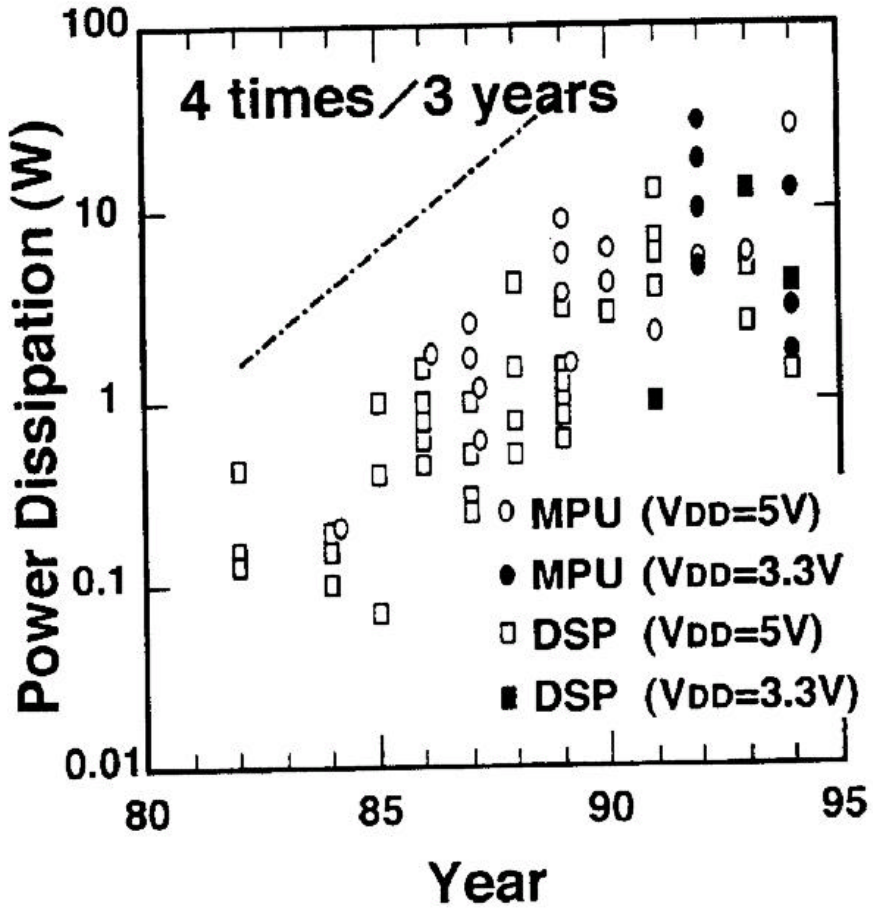
Why worry about power?
-- Heat Dissipation

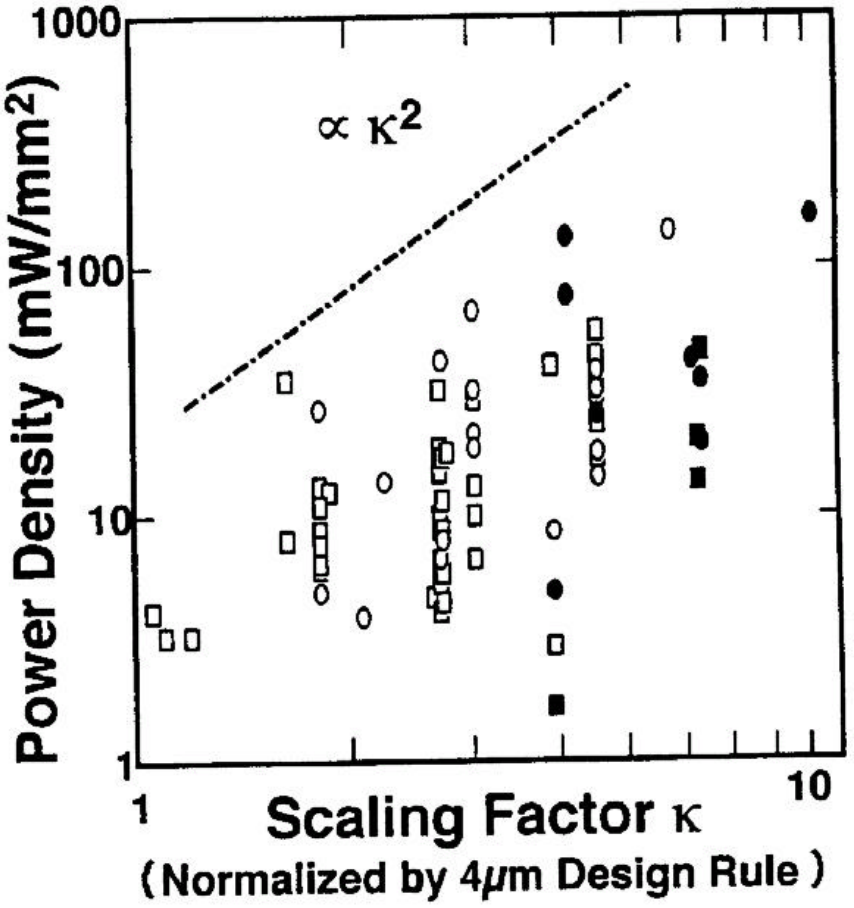
microprocessor power dissipation

source : arpa-esto

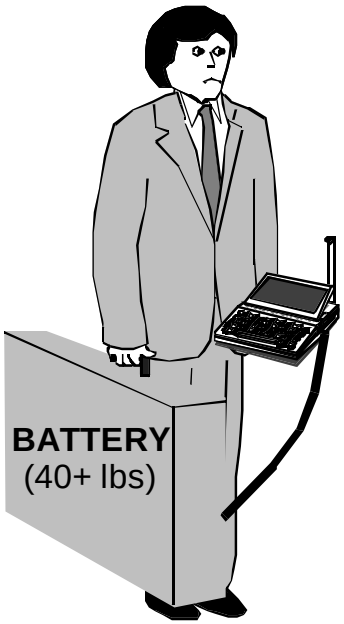


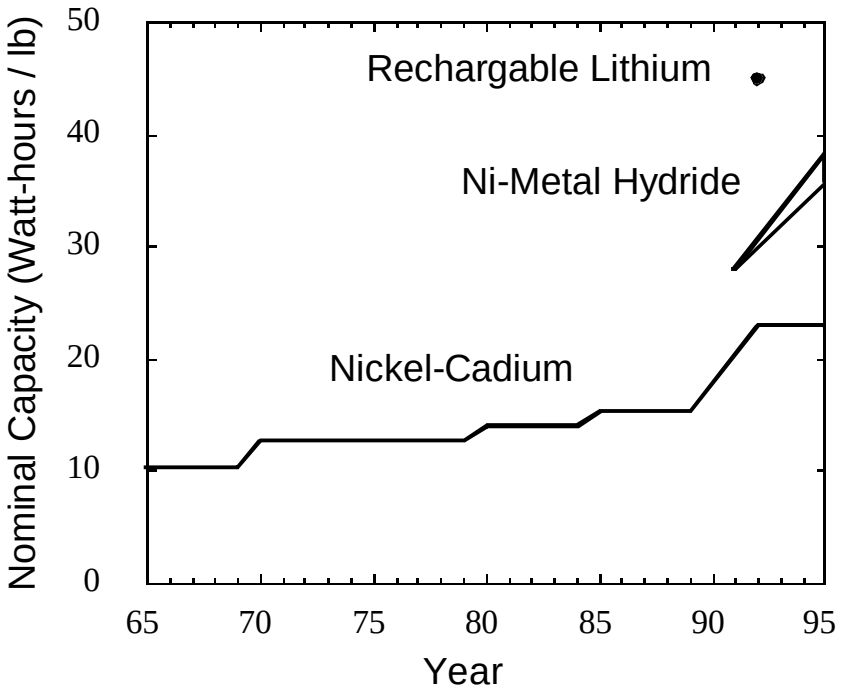
Evolution in Power Dissipation





Why worry about power – Portability





Multimedia Terminals

Laptop Computers

Digital Cellular Telephony

Expected Battery Lifetime increase over next 5 years: 30-40%

Where Does Power Go in CMOS?

- **Dynamic Power Consumption**

  Charging and Discharging Capacitors

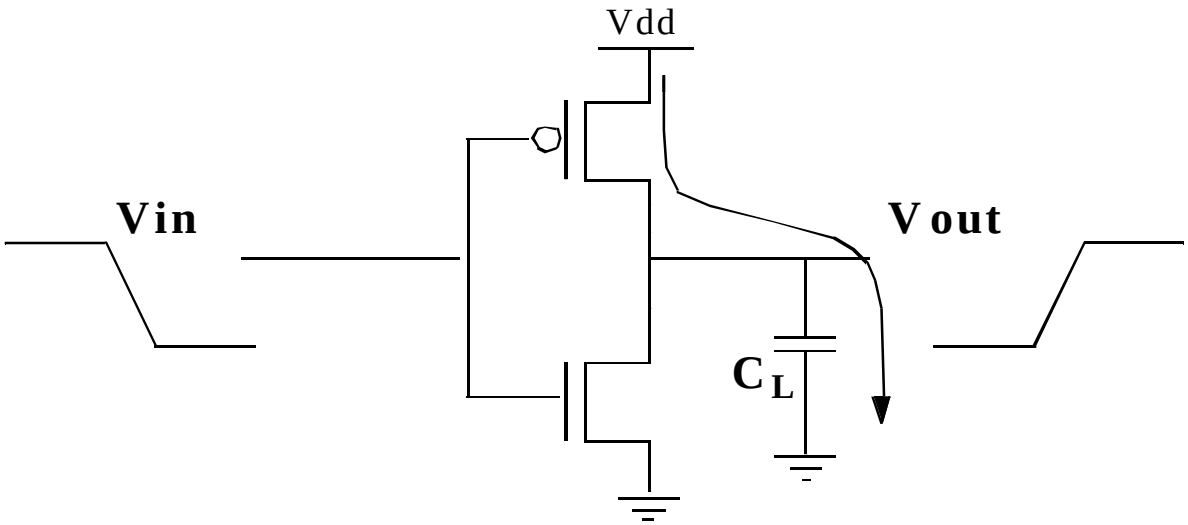
- **Short Circuit Currents**

  Short Circuit Path between Supply Rails during Switching

- **Leakage**

  Leaking diodes and transistors

Dynamic Power Consumption



$$\text{Energy/transition} = C_L * V_{dd}^2$$

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

- Not a function of transistor sizes!
- Need to reduce C_L, V_{dd}, and f to reduce power.

Dynamic Power Consumption - Revisited

Power = Energy/transition * transition rate

$$= C_L * V_{dd}^2 * f_{0\rightarrow 1}$$

$$= C_L * V_{dd}^2 * P_{0\rightarrow 1} * f$$

$$= C_{EFF} * V_{dd}^2 * f$$

Power Dissipation is Data Dependent
Function of *Switching Activity*

$$C_{EFF} = \text{Effective Capacitance} = C_L * P_{0\rightarrow 1}$$

Power Consumption is Data Dependent

Example: Static 2 Input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of 2 input NOR gate

Assume:

P(A=1) = 1/2

P(B=1) = 1/2

Then:

P(Out=1) = 1/4

P(0→1)

= P(Out=0).P(Out=1)

= 3/4 × 1/4 = 3/16

$$C_{EFF} = 3/16 * C_L$$

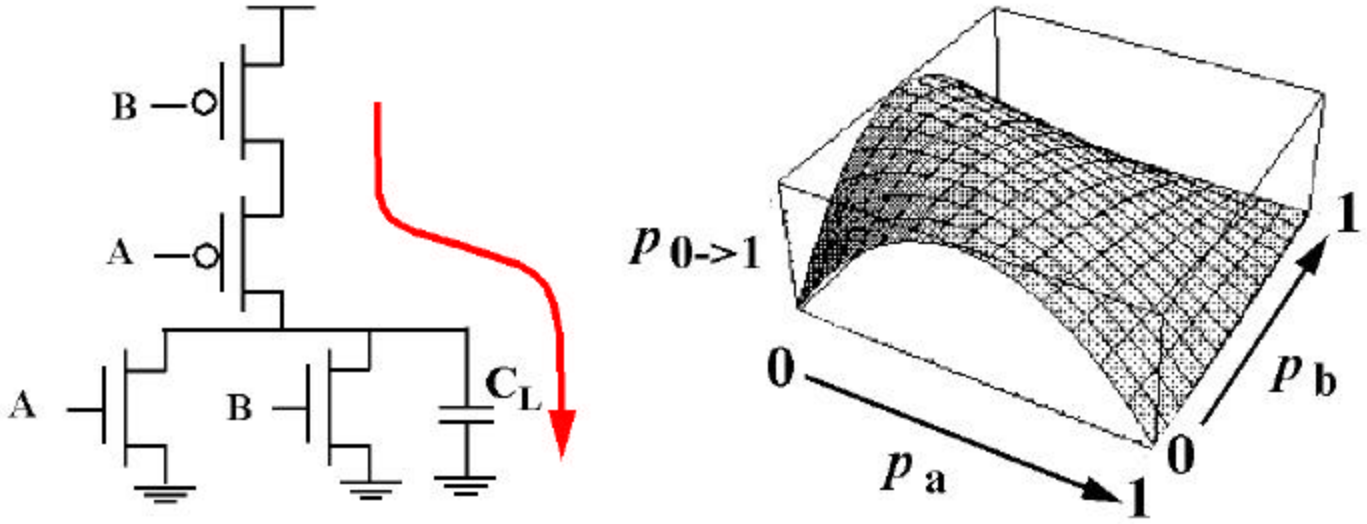
Transition Probabilities for Basic Gates

	$P_{0\rightarrow 1}$
AND	$(1-P_A P_B)P_A P_B$
OR	$(1-P_A)(1-P_B)(1-(1-P_A)(1-P_B))$
EXOR	$(1 - (P_A + P_B - 2P_A P_B))(P_A + P_B - 2P_A P_B)$

Switching Activity for Static CMOS

$$P_{0\rightarrow 1} = P_0 \cdot P_1$$

Transition Probability of 2-input NOR Gate

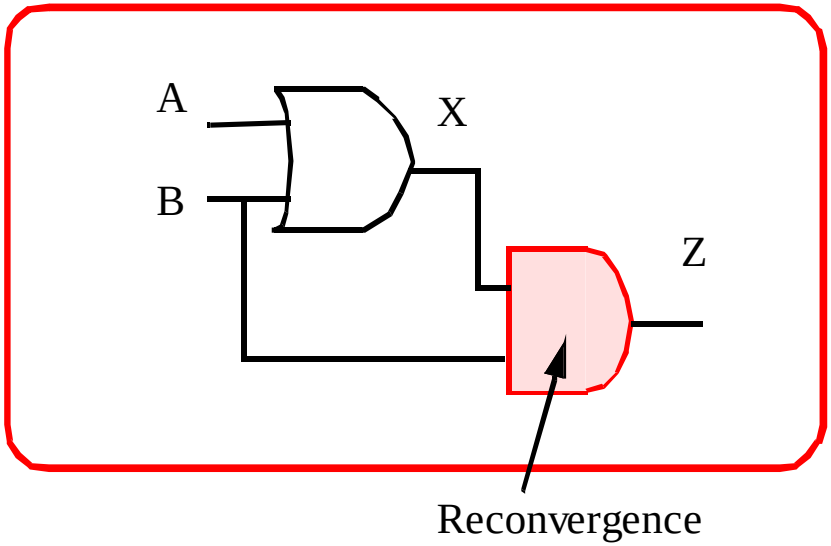


$$p_1 = (1-p_a)\,(1-p_b)$$

$$p_{0->1} = p_0\,p_1 = (1-(1-p_a)\,(1-p_b))\,(1-p_a)\,(1-p_b)$$

- $\alpha_{0->1}$ is a strong function of signal statistics

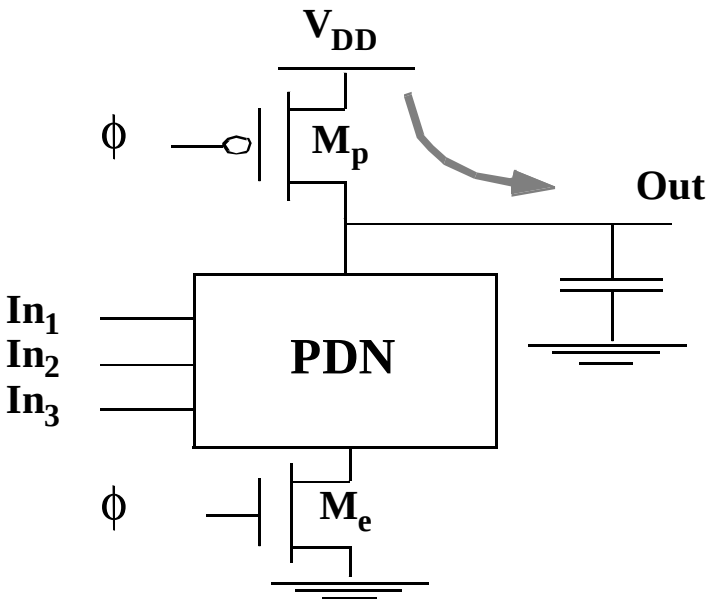
Problem: Reconvergent Fanout



$$P(Z=1) = P(B=1) \cdot P(X=1 \mid B=1)$$

Becomes complex and intractable real fast

How about Dynamic Circuits?



Power is Only Dissipated when Out=0!

$$C_{EFF} = P(Out=0).C_L$$

4-input NAND Gate

Example: Dynamic 2 Input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of 2 input NOR gate

Assume:

P(A=1) = 1/2

P(B=1) = 1/2

Then:

P(Out=0) = 3/4

$$C_{EFF} = 3/4 * C_L$$

Switching Activity Is Always Higher in Dynamic Circuits

Transition Probabilities for Dynamic Gates

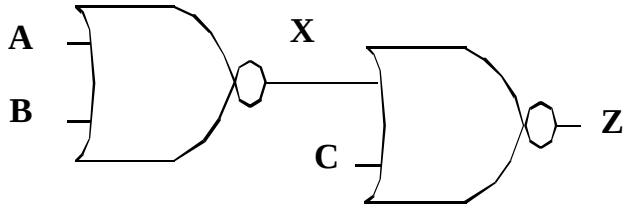
	$P_{0\rightarrow1}$
AND	$(1-P_A P_B)$
OR	$(1-P_A)(1-P_B)$
EXOR	$(1 - (P_A + P_B - 2P_A P_B))$

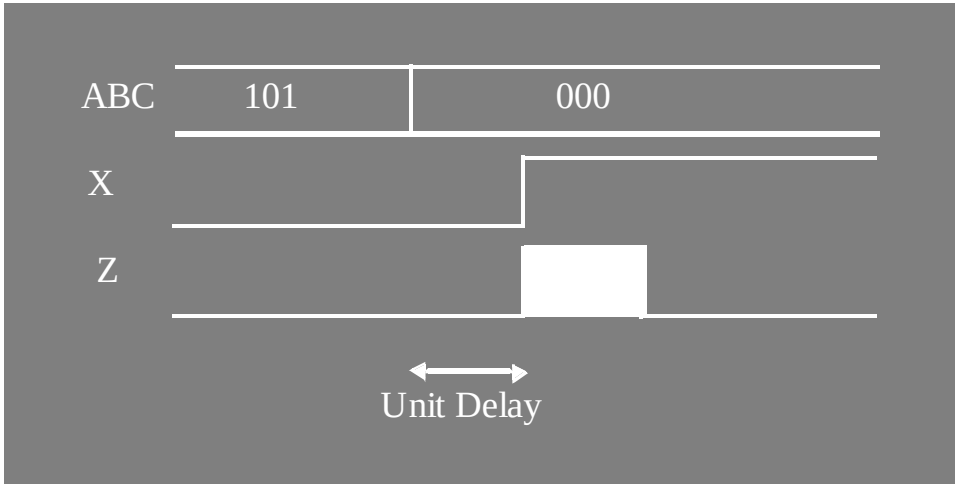
Switching Activity for Precharged Dynamic Gates

$$\mathbf{P_{0\rightarrow1} = P_0}$$

Glitching in Static CMOS

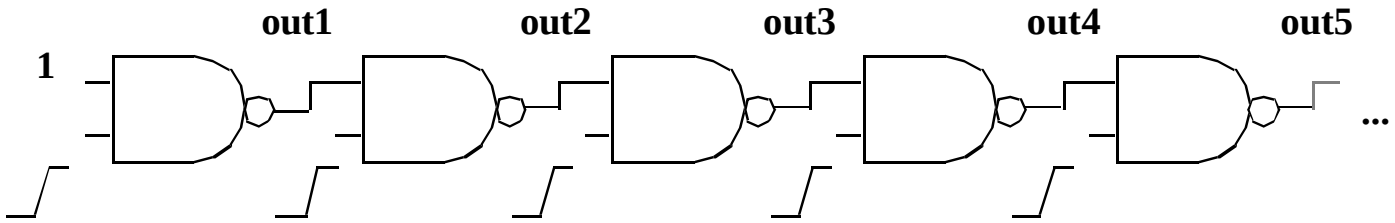
also called: dynamic hazards

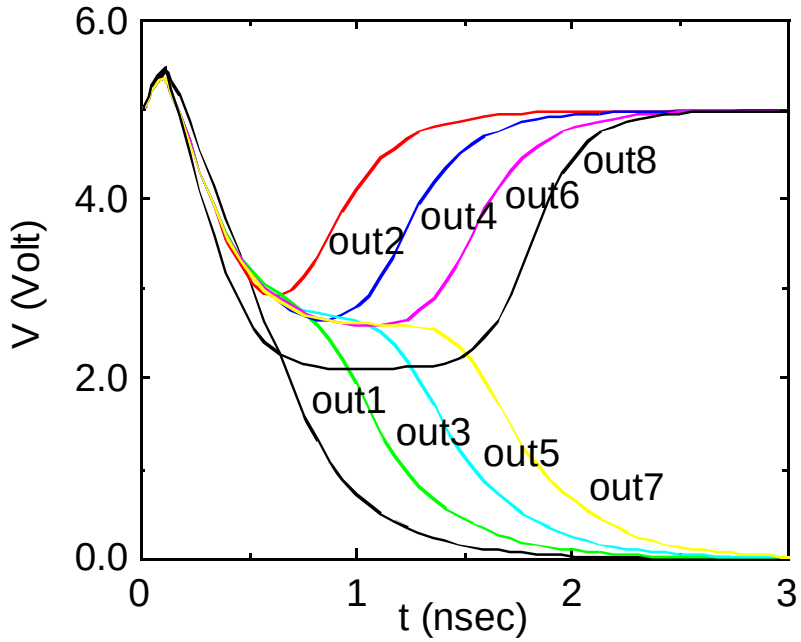




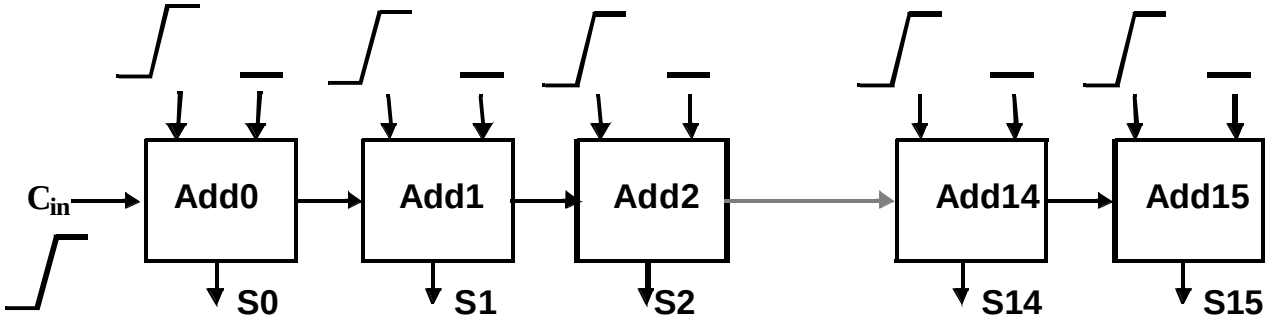
Observe: No glitching in dynamic circuits

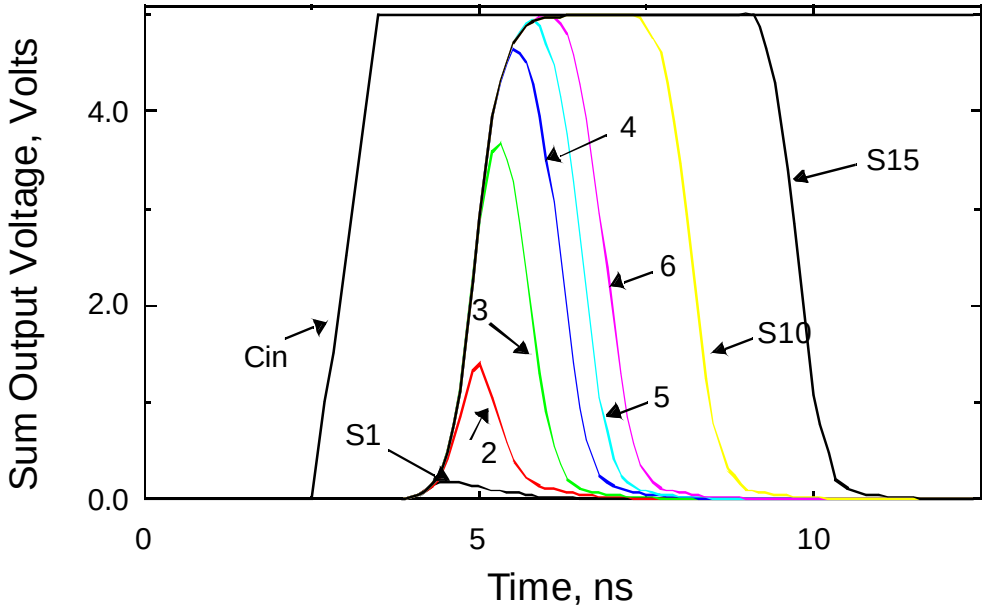
Example 1: Chain of NOR Gates



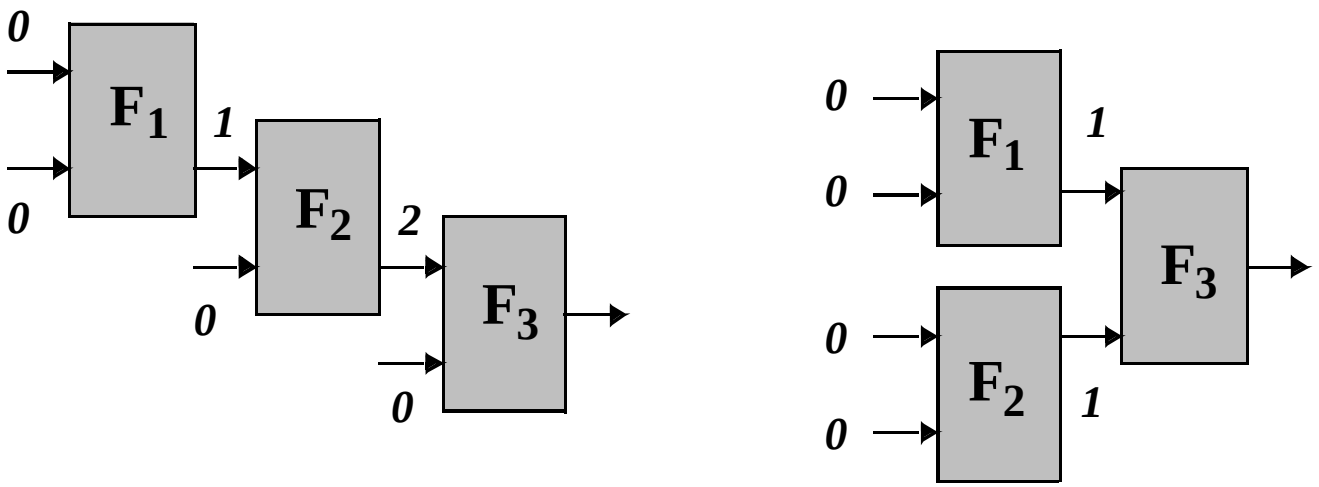


Example 2: Adder Circuit



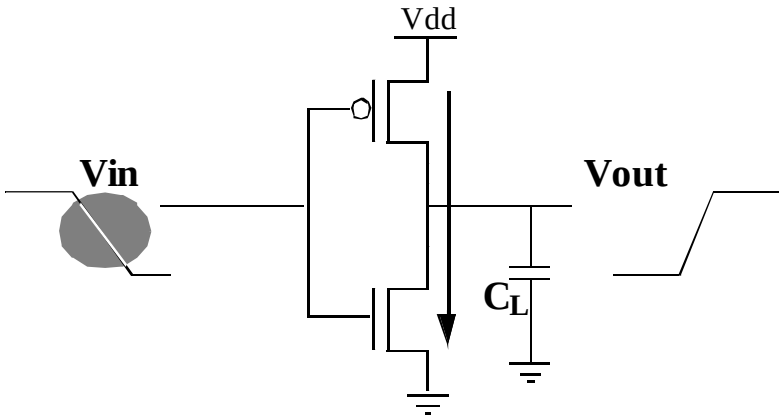


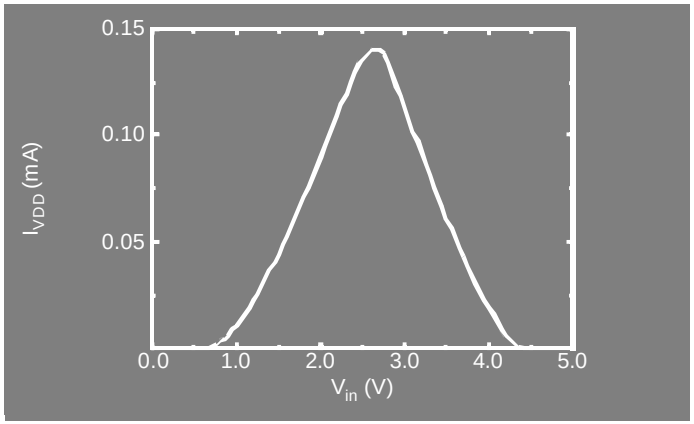
How to Cope with Glitching?



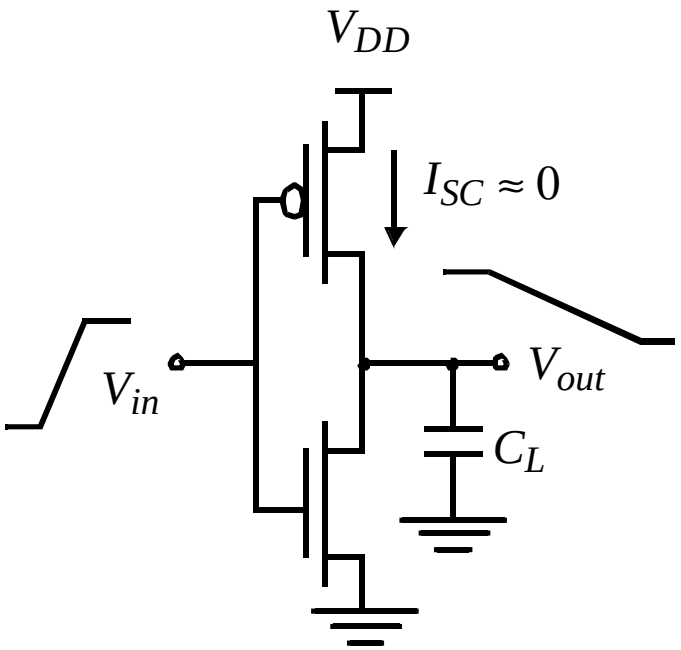
Equalize Lengths of Timing Paths Through Design

Short Circuit Currents

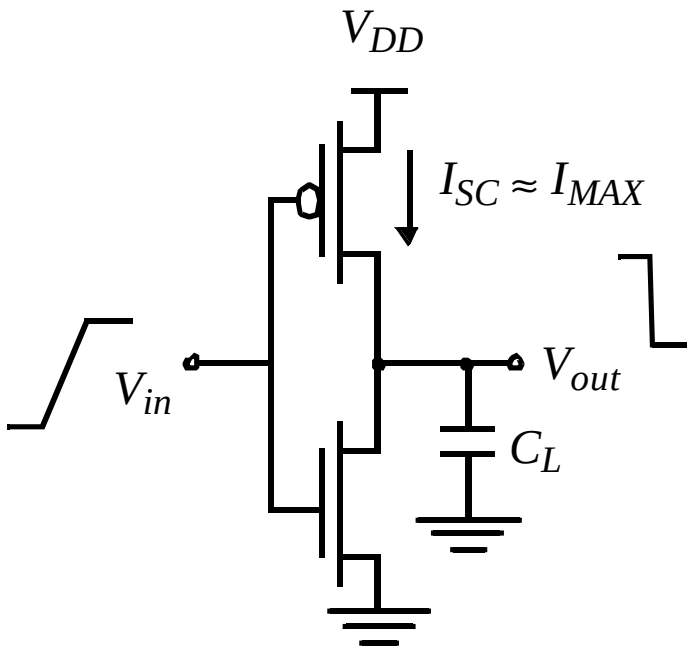




Impact of rise / fall times on short-circuit currents

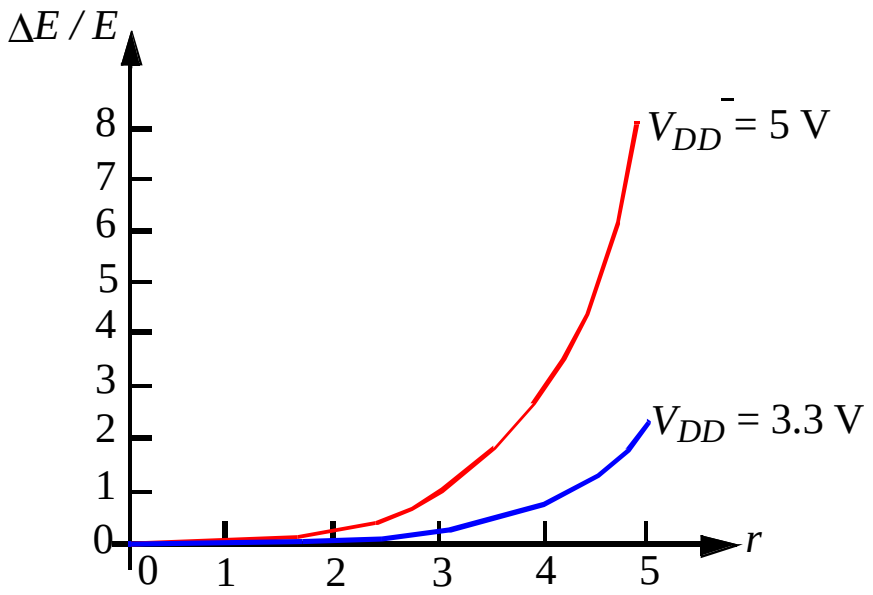


Large capacitive load



Small capacitive load

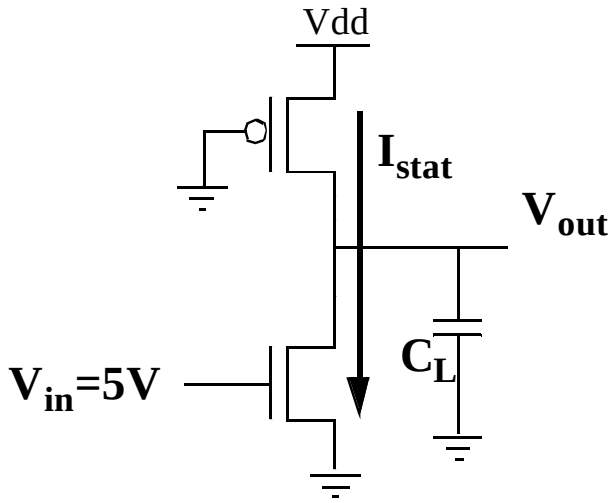
Short-circuit energy as a function of slope ratio



$W/L|_P = 7.2\mu m/1.2\mu m$
$W/L|_N = 2.4\mu m/1.2\mu m$

The power dissipation due to short circuit currents is minimized by matching the rise/fall times of the input and output signals.

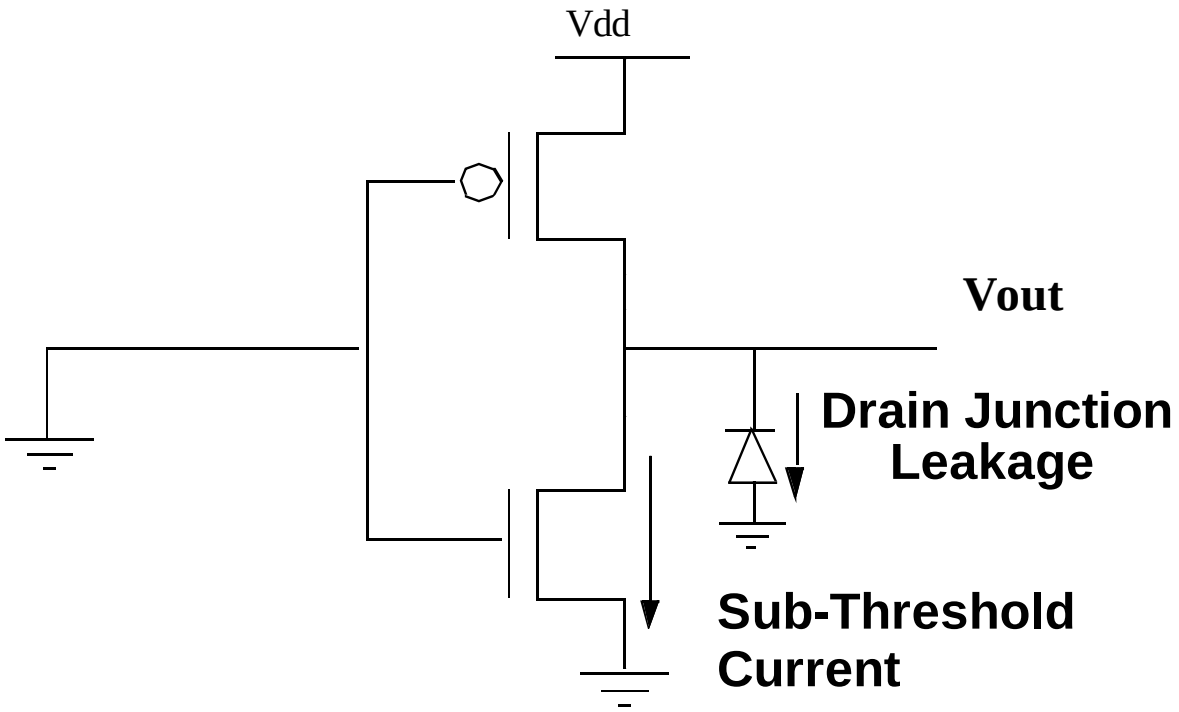
Static Power Consumption



$$P_{stat} = P_{(In=1)} \cdot V_{dd} \cdot I_{stat}$$

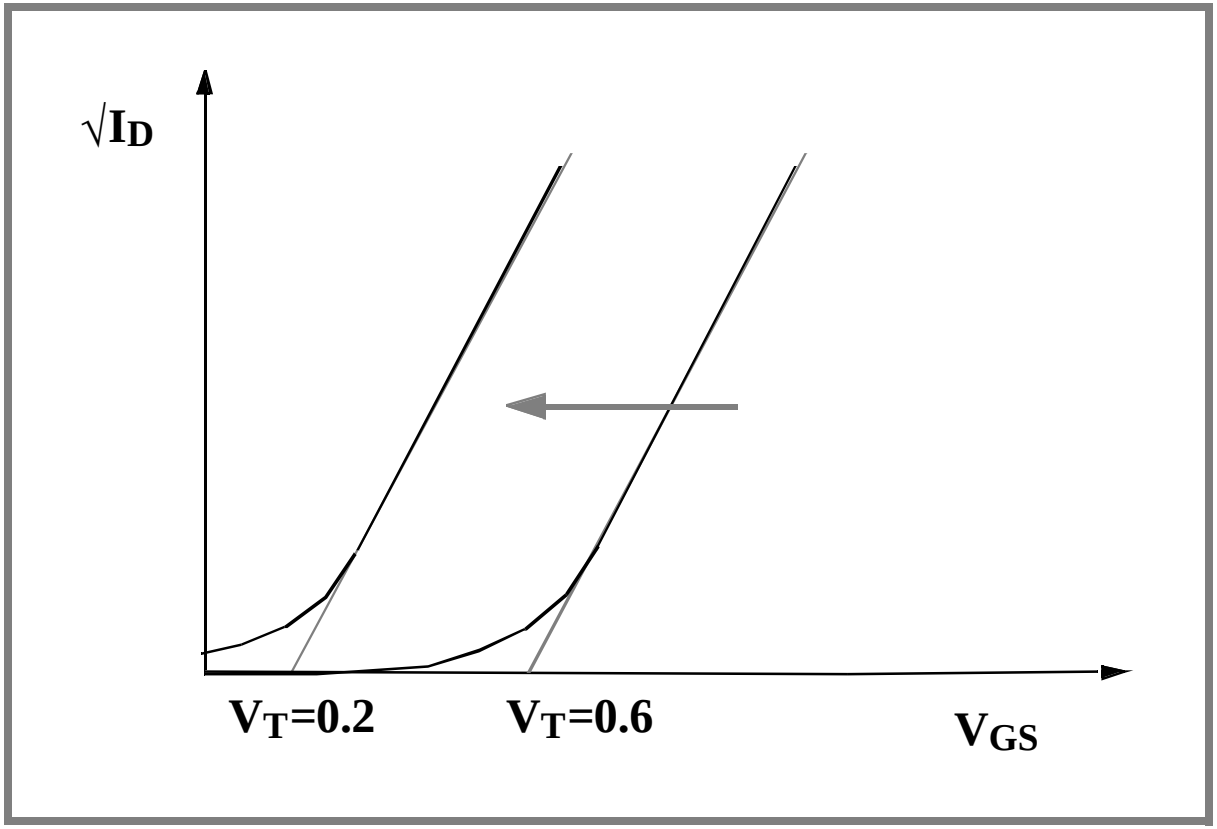
- **Dominates over dynamic consumption**
- **Not a function of switching frequency**

Leakage



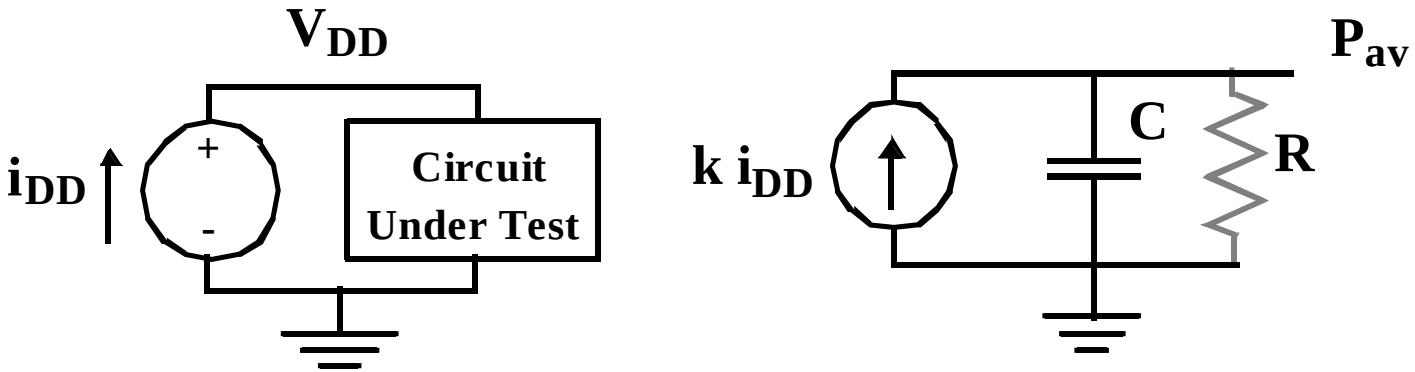
Sub-Threshold Current Dominant Factor

Sub-Threshold in MOS



Lower Bound on Threshold to Prevent Leakage

Power Analysis in SPICE



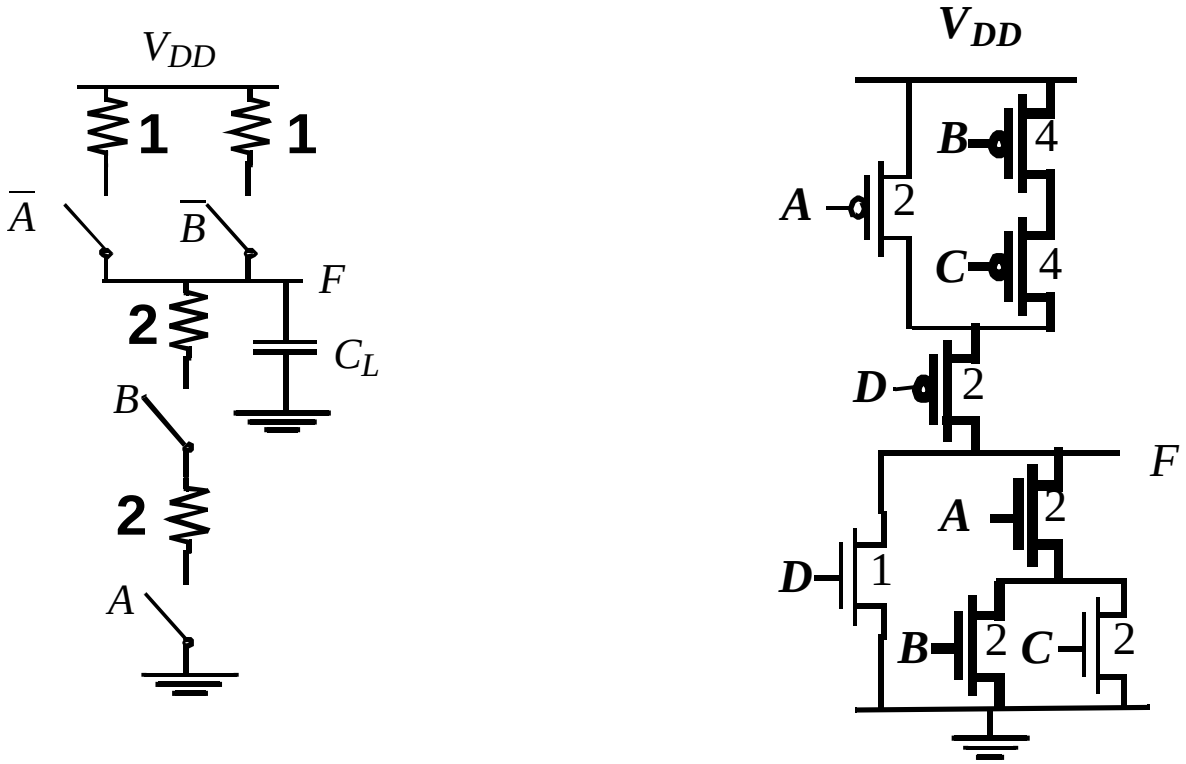
Equivalent Circuit for Measuring Power in SPICE

$$C\frac{dP_{av}}{dt} = ki_{DD}$$

$$or$$

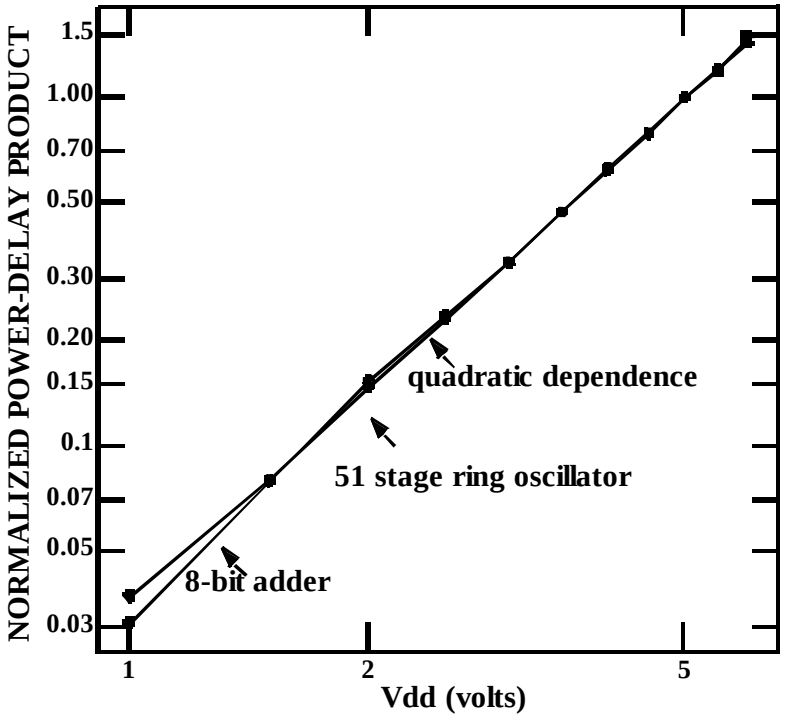
$$P_{av} = \frac{k}{C}\int_0^T i_{DD}dt$$

Design for Worst Case



Here it is assumed that $R_p = R_n$

Reducing V_{dd}



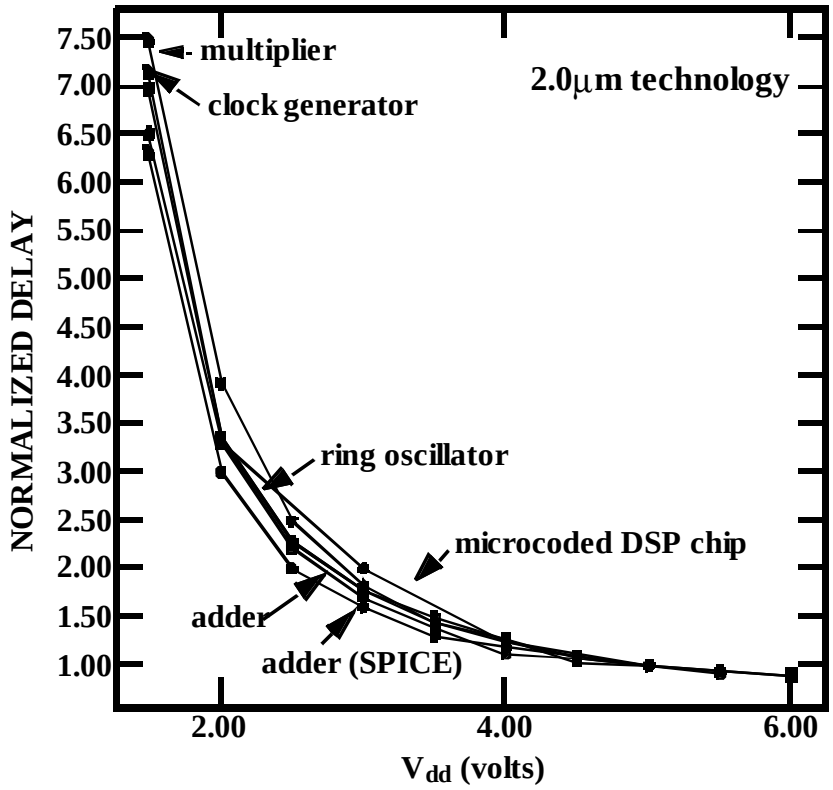
$$P \times t_d = E_t = C_L * V_{dd}^2$$

$$\frac{E_{(Vdd=2)}}{E_{(Vdd=5)}} = \frac{(C_L) * (2)^2}{(C_L) * (5)^2}$$

$$E_{(Vdd=2)} \approx 0.16\ E_{(Vdd=5)}$$

- Strong function of voltage (V^2 dependence).
- Relatively independent of logic function and style.
- Power Delay Product Improves with lowering V_{DD}.

Lower V_{dd} Increases Delay



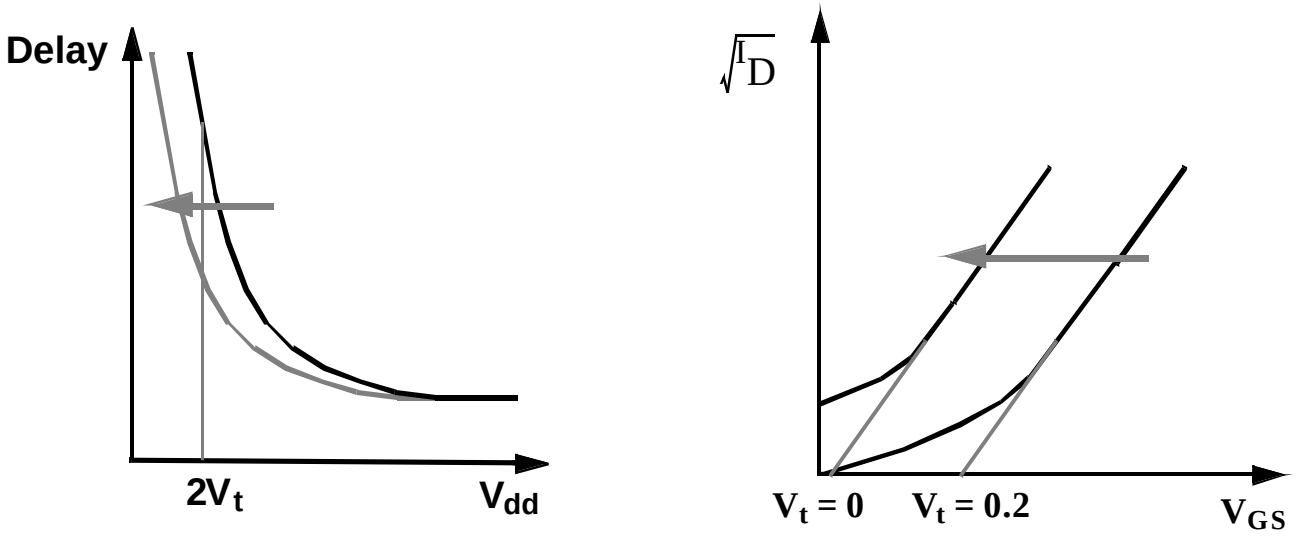
$$T_d = \frac{C_L * V_{dd}}{I}$$

$$I \sim (V_{dd} - V_t)^2$$

$$\frac{T_{d(Vdd=2)}}{T_{d(Vdd=5)}} = \frac{(2) * (5 - 0.7)^2}{(5) * (2 - 0.7)^2} \approx 4$$

- **Relatively independent of logic function and style.**

Lowering the Threshold

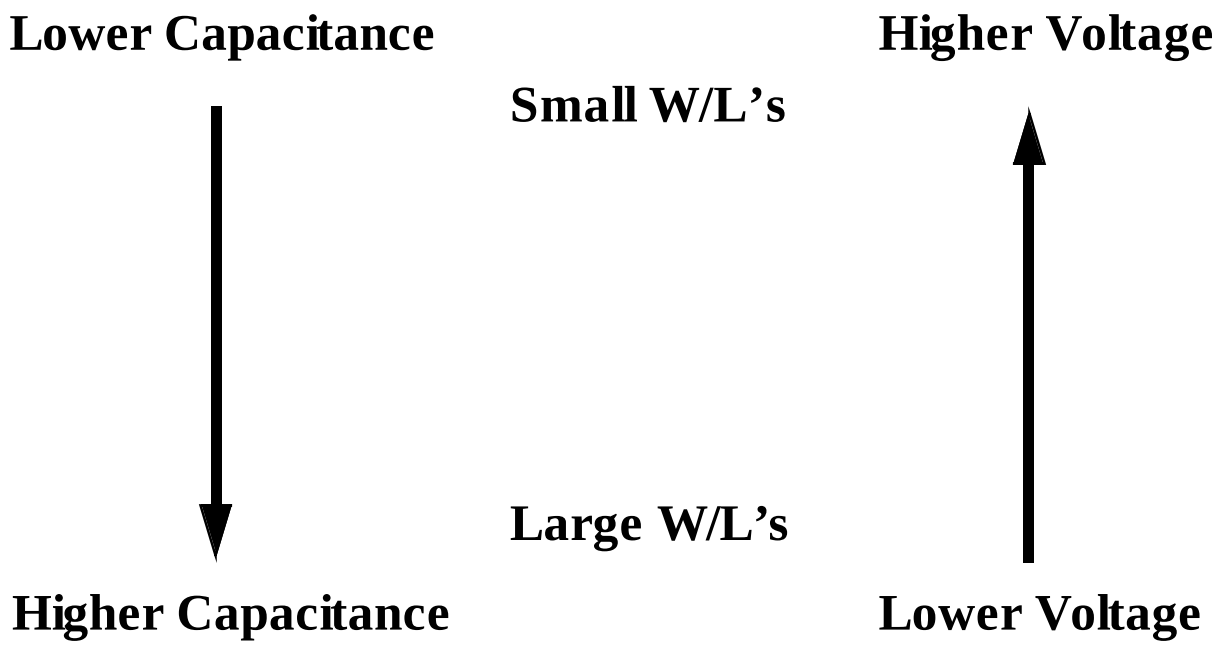


Reduces the Speed Loss, But Increases Leakage

Interesting Design Approach:

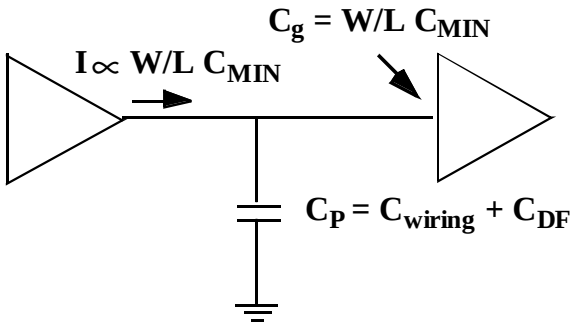
DESIGN FOR $P_{Leakage} == P_{Dynamic}$

Transistor Sizing for Power Minimization



- Larger sized devices are useful only when interconnect dominated.
- Minimum sized devices are usually optimal for low-power.

Transistor Sizing for Fixed Throughput



C_{MIN} = Minimum sized gate (W/L=1)

W /L after sizing

$\alpha = C_P / (K\ C_{MIN})$

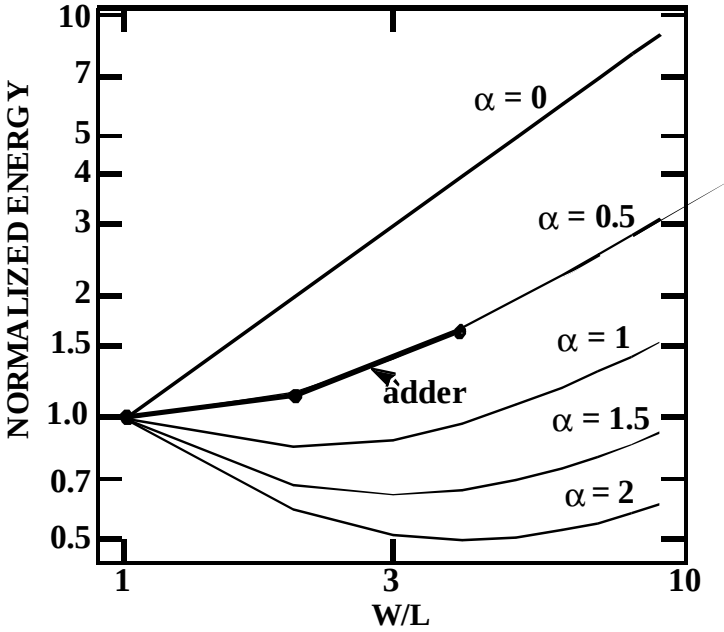
HIGH PERFORMANCE

$W/L >> C_P / (K\ C_{MIN})$

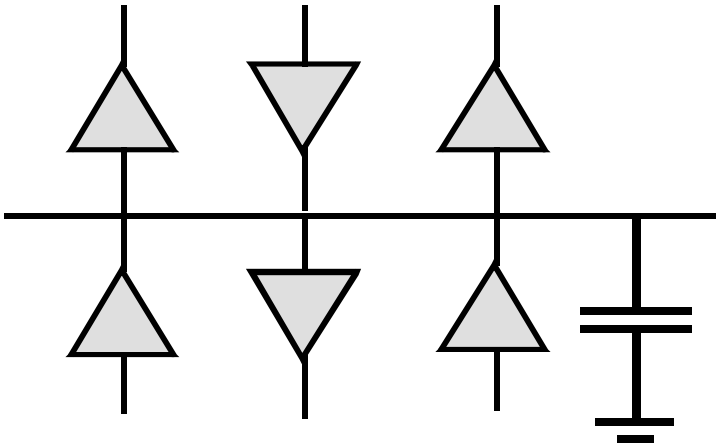
LOW POWER

$W/L = 2\ C_P / (K\ C_{MIN})$
$(\text{if } C_P \geq K\ C_{MIN})$

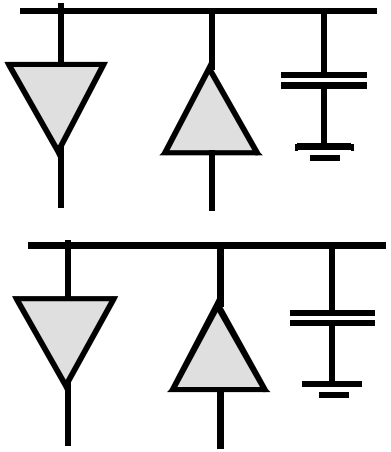
ELSE W/L = 1



Reducing Effective Capacitance



Global bus architecture



Local bus architecture

Shared Resources incur Switching Overhead

Summary

- **Power Dissipation is becoming Prime Design Constraint**
- **Low Power Design requires Optimization at all Levels**
- **Sources of Power Dissipation are well characterized**
- **Low Power Design requires operation at lowest possible voltage and clock speed**