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Assignment : Error Detection

1) A bit stream of 11001101 is transmitted using a standard CRC method. The generator polynomial is x^3+1. Show the actual bit string transmitted. Suppose the fourth bit from left is inverted during the transmission. Show how the error is detected at the receiver's end.

Ans: Given,

Data = 11001101

Polynomial eqn = x^3+1

$= 1 \cdot x^3 + 0 \cdot x^2 + 0 \cdot x^1 + 1 \cdot x^0$

CRC = 1001

Let, the redundant bit be 000.

CRC Generation: Sender Side:

```
        11010111
    ____________
1001 ) 11001101000
       -1001
        1011
       -1001
         0101
        -0000
         1010
        -1001
         0111
        -0000
         1110
        -1001
         1110
        -1001
         1110
        -1001
           111
```

Here, 111 is remainder ie CRC for receiver side

Case I: Actual bit transmitted

CRC check: Receiver side

```
          11010111
     ----------------
1001 ) 11001101111
       -1001
        1011
       -1001
         0101
        -0000
          1010
         -1001
           0111
          -0000
            1111
           -1001
             1101
            -1001
              1001
             -1001
              0000
```

∴ Remainder is zero, hence the transmission has no error.

Case II: If 4th bit from left is inverted during the transmission

CRC check: Receiver side

```
        11000101
     ___________
1001 ) 1101110111
       -1001
        1001
       -1001
         0001
        -0000
          0010
         -0000
           0101
          -0000
            1011
           -1001
             0101
            -0000
              1011
             -1001
               010
```

∴ Remainder is non-zero, hence the transmission has some error.

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2) Suppose the following block of 16 bits is sent using a checksum of 8 bits. 1001010000110001. Compute the checksum & verify the transmission without any error. Suppose the LSB of first segment is inverted: Show how the error is detected at the receiver's end.

Ans:

Sender Side

Two 8 bits numbers are added.

$$\begin{array}{r} 10010100 \\ +\ 00110001 \\ \hline 11000101 \end{array}$$

1's complement of 11000101 = 00111010

∴ The pattern sent is :

1001010000110001 = 00111010 + checksum

Receiver side

The received data along with checksum is added.

$$\begin{array}{r} 10010100 \\ 00110001 \\ +\ 00111010 \\ \hline 11111111 \end{array}$$

1's complement of 11111111 = 00000000

∴ There is no error in transmission.

Again,

If LSB of first segment is inverted during transmission,

Sender side

The block of 16 bits to be sent using a checksum of 8 bits : 10010100 00110001

The two 8 bit numbers are added:

```
  10010100
+ 00110001
  11000101
```

1's complement of 11000101 = 00111010

∴ The pattern sent is:

10010100 00110001 00111010

Receiver side:

The received data alongwith checksum is added:

```
  10010100 1
  00110001
+ 00111010
  100000000
```

Ignoring carry over : Sum = 00000000

1's complement of 00000000 = 11111111

∴ The result is non-zero ie. there exists some error in transmission.