**6. Design a simple pulse-width modulation PWM signal generator, where user can control the width of the pulse**

* Output clock period = 100ns
* Input duty\_cycle can be given from 0 to 100%
* Based on that output PWM is generated
* I used a counter approach to divide the clock and made divisor as input from user
* Post-synthesis might seem big because the design can output duty cycle from 0 to 100%

**TEST STIMULUS**

* I gave duty cycle values as 80,10,50,20,75 and 100
* Accordingly, we can observe the output pulse width varying.