**7. Suppose you have a 1-bit serial binary data stream synchronized with system clock. Now design a circuit that will count the number of times a user defined 4-bit sequence is occurred in the entire data stream. For simplicity you can defined the sequence while designing.**

* First I used FSM for this design.
* I used 4 states, as this is the minimum states required and I wanted to keep the design as minimum hardware as possible
* Next state switching logic is sequential and rest of logic is combinational. This reduces the number of Flip-flops.
* I drew a state diagram as explained and wrote the logic for the pattern of 0110

**TEST STIMULUS**

* I gave a stream of 01101100110
* The pattern “ 0110 ”comes 3 times in this stream
* So, output goes high 3 times at respective places.

**ANOTEHR APPROACH**

* While I was coding FSM, I wanted to make it generalised for any sequence.
* Then I got idea of second approach.
* It works fine when I tested for few patterns.