

swerv\_wrapper\_verilog\_0

clk  
rst  
nmi\_int  
nmi\_vec[31:0]  
timer\_int  
dmi\_reg\_en  
dmi\_reg\_addr[6:0]  
dmi\_reg\_wr\_en  
dmi\_reg\_rdata[31:0]  
dmi\_hard\_reset

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ifu\_axi\_araddr[31:0]  
ifu\_axi\_arlen[7:0]  
ifu\_axi\_arsize[2:0]  
ifu\_axi\_arburst[1:0]  
ifu\_axi\_arlock  
ifu\_axi\_arcache[3:0]  
ifu\_axi\_arprot[2:0]  
ifu\_axi\_arregion[3:0]  
ifu\_axi\_arqos[3:0]  
ifu\_axi\_arvalid  
ifu\_axi\_arready  
ifu\_axi\_rid[2:0]  
ifu\_axi\_rdata[63:0]  
ifu\_axi\_rresp[1:0]  
ifu\_axi\_rlast  
ifu\_axi\_rvalid  
ifu\_axi\_rready  
lsu\_axi\_araddr[31:0]  
lsu\_axi\_arlen[7:0]  
lsu\_axi\_arsize[2:0]  
lsu\_axi\_arburst[1:0]  
lsu\_axi\_arlock  
lsu\_axi\_arcache[3:0]  
lsu\_axi\_arprot[2:0]  
lsu\_axi\_arregion[3:0]  
lsu\_axi\_arqos[3:0]  
lsu\_axi\_arvalid  
lsu\_axi\_arready  
lsu\_axi\_wdata[63:0]  
lsu\_axi\_wstrb[7:0]  
lsu\_axi\_wlast  
lsu\_axi\_wvalid  
lsu\_axi\_wready  
lsu\_axi\_bid[3:0]  
lsu\_axi\_bresp[1:0]  
lsu\_axi\_bvalid  
lsu\_axi\_bready  
lsu\_axi\_araddr[31:0]  
lsu\_axi\_arlen[7:0]  
lsu\_axi\_arsize[2:0]  
lsu\_axi\_arburst[1:0]  
lsu\_axi\_arlock  
lsu\_axi\_arcache[3:0]  
lsu\_axi\_arprot[2:0]  
lsu\_axi\_arregion[3:0]  
lsu\_axi\_arqos[3:0]  
lsu\_axi\_arvalid  
lsu\_axi\_arready  
lsu\_axi\_rid[3:0]  
lsu\_axi\_rdata[63:0]  
lsu\_axi\_rresp[1:0]  
lsu\_axi\_rlast  
lsu\_axi\_rvalid  
lsu\_axi\_rready  
sb\_axi\_araddr[31:0]  
sb\_axi\_arlen[7:0]  
sb\_axi\_arsize[2:0]  
sb\_axi\_arburst[1:0]  
sb\_axi\_arlock  
sb\_axi\_arcache[3:0]  
sb\_axi\_arprot[2:0]  
sb\_axi\_arregion[3:0]  
sb\_axi\_arqos[3:0]  
sb\_axi\_arvalid  
sb\_axi\_arready  
sb\_axi\_wdata[63:0]  
sb\_axi\_wstrb[7:0]  
sb\_axi\_wlast  
sb\_axi\_wvalid  
sb\_axi\_wready  
sb\_axi\_bid[0:0]  
sb\_axi\_bresp[1:0]  
sb\_axi\_bvalid  
sb\_axi\_bready  
sb\_axi\_arid[0:0]  
sb\_axi\_araddr[31:0]  
sb\_axi\_arlen[7:0]  
sb\_axi\_arsize[2:0]  
sb\_axi\_arburst[1:0]  
sb\_axi\_arlock  
sb\_axi\_arcache[3:0]  
sb\_axi\_arprot[2:0]  
sb\_axi\_arregion[3:0]  
sb\_axi\_arqos[3:0]  
sb\_axi\_arvalid  
sb\_axi\_arready  
sb\_axi\_rid[0:0]  
sb\_axi\_rdata[63:0]  
sb\_axi\_rresp[1:0]  
sb\_axi\_rlast  
sb\_axi\_rvalid  
sb\_axi\_rready  
dmi\_reg\_rdata[31:0]

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