

IMAGINATION UNIVERSITY PROGRAMME

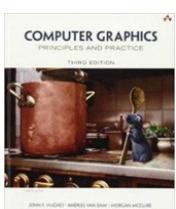
Let us empower you to use our technologies in your teaching labs and student projects! We have 27 years' experience of helping teachers around the world..

The four vital components in our teaching packages:

- Tools: free to download software tools such as PowerVR Software Development Kit ("SDK"). Full versions with no code size or time limits!
- Hardware: low-cost, robust, and effective hardware from our platform partners
- Materials: genuine teaching materials written by academics who are respected experts in their field. These are not in-house or commercial training materials. With licensing that allows sharing with students, editing, translation and unrestricted academic use
- Effective support through our forums, online video tutorials, and online/on-campus workshops

- Computer Science/Engineering ("CS"/"CE")
- Games Design/Engineering/Programming
- Electrical & Electronic Engineering ("EE")
- Automotive Engineering
- Computer Architecture
- System-on-Chip ("SoC") Design
- Graphics
- GPU Acceleration & Compute
- AI: Artificial Intelligence
- Autonomous Vehicles and In-Vehicle Systems

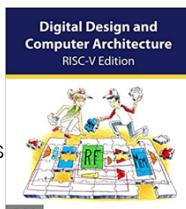
Textbooks



*Computer Graphics:
Principles and Practice*
(3rd Edition)

John F. Hughes & Andries van Dam

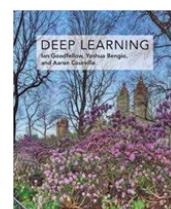
Available in:



*Digital Design &
Computer Architecture*
(RISC-V Edition)

Sarah Harris & David Harris - Sept'21

Available in:



Deep Learning (Adaptive Computation and Machine Learning series)

Ian Goodfellow, Yoshua Bengio, Aaron Courville

Available in:

Hardware Tools



Digilent Nexys A7

Nexys A7 incorporates a Xilinx Artix®-7 FPGA which could download the Western Digital RISC-V based SweRV softcore onto it. The 7-segment digital display and rich I/O make it a great fit for computer architecture labs.



Pumpkin i300 EVK

Based on the Mediatek i300B SoC, ARM Quad-Core A35 1.3GHz processor, PowerVR 8XE GPU which supports OpenGL, OpenGL ES and OpenCL. Together with the Nervual Compute SDK Academic version, it could become an ideal platform for you to run Edge AI applications.



BeagleBone® Black

The BeagleBone Black from beagleboard.org is based on the TI AM335x Arm Cortex-A8 processor 512MB DDR3 RAM, PowerVR SGX530 GPU with 3D graphics accelerator, microSD card, HDMI, Ethernet, USB 2.0, 2x PRU 32-bit microcontrollers

Teaching Materials

Our teaching material packages include presentation slides, an instructor's guide, a student manual, lab exercises, test questions and reference guides, supplied in both PDF and source PowerPoint & Word formats.

(1) Introduction to Mobile Graphics v2.2 ("2020 Edition")

Scope	The first full semester course on Mobile Graphics, with Lectures and Labs	Partners	BeagleBoard.org
Audience	3rd year BSc/MSc Gaming and CS Students	Tool-Chain	PowerVR SDK
Author	Darren McKie, University of Hull, UK	Videos	7 modules incl: Architecture, PVR framework, Open GL ES 2.0, Debugging with PVR Trace
Hardware	Chromebook, Android phones / tablets, BeagleBone Black OR: Software Emulator	Support	PowerVR Developer's Forum & IUP Course Forum
Video Tutorials	Online workshop package & video available	Language	English, Simplified / Traditional Chinese
Request & Download	https://university.imgtec.com/teaching-download/#MG		

Contents

Lecture Topic	Week	Details
Introduction to mobile graphics technologies	1	Introduction to the different graphics APIs available and how they compare.
Basics of the PowerVR Framework, and simple Object Orientated Design	1-2	How the simple triangle graphics program has been written using the PowerVR SDK. How to separate the triangle code out of the main drawing function and into its own class.
Introduction to mobile graphics architectures	2-3	Comparison of mobile's dominant graphics hardware, an introduction to the concerns relating to power consumption and performance, and to understand the cross-platform/cross-compilation benefits of OpenGL ES. The PowerVR Graphics architecture case study will be outlined.
Introduction to graphics SDKs and forums	3-4	Learn about the main technologies used in mobile graphics SDKs up to OpenGL ES 3.2 and to learn how to use some of the SDK utilities and how to use forums for help.
Texturing	4-5	How texturing works, including the coordinate system and performance concerns.
Transformations	5	How transformations and lighting can be applied to vertices, including translations, rotations, and how to apply lighting.
OpenGL ES basics	6-7	Learn the basics of the OpenGL ES commands and Shader Language.
OpenGL ES lighting	7-8	Learn how to use different lighting models to illuminate objects in a scene.
Reflection and Refraction	9	Learn how cubemaps can be created and how they are used for calculating reflections and refractions.
Introduction to Vulkan	9-10	Introduction to Vulkan and a comparison with OpenGL ES.

(2) RVfpga:

The Complete Course in Understanding Computer Architecture

Scope:

During 2021, this will build into three one-semester courses which fully illustrate the fundamentals of computer architecture, the inner workings of a RISC processor, and the process to get from a CPU to a System-on-Chip Design.

Audience

BSc Digital Design & Microarchitectures, Computer Organisation & Architecture, BSc/MSc Advanced Computer Architecture, MSc SoC design, MSc Design Verification, BSc/MSc Embedded Systems projects and MSc/PhD Processor Architecture

Request & Download

<https://university.imgtec.com/rvfga/>

Authors

Dr. Sarah Harris, University of Nevada, Las Vegas (U.S.) , Dr. Daniel Chaver-Martínez, Universidad Complutense de Madrid (Spain), Zubair Kakakhel (AKZY Ltd; UK)

Support

RVfpga Forum:
<https://university.imgtec.com/forums/rvfga/>

Languages:

English, Chinese (simplified & Traditional), Japanese, Spanish and Turkish

Global Team

This project is a global team effort advised and inspired by David Patterson who developed the original RISC processor and more recently, invented RISC-V!

Academic Adviser:

Prof. David Patterson
University of California, Berkeley

Contributor:

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AZKY Tech Ltd. Birmingham, UK

Reviewer:

Prof. Roy Kravitz
Portland State University, U.S.

Sponsors and Supporters



Tools Required & Contents

Software

- Xilinx Vivado 2019.2 WebPACK
- Microsoft's Visual Studio Code
- PlatformIO with Chips Alliance platform, which includes: RISC-V Tool-chain, OpenOCD, Verilator HDL Simulator, WD Whisper ISS

Hardware

- Digilent Nexys A7 or Nexys 4 DDR FPGA Board
- RISC-V Core & SoC
 - Core: Western Digital's SweRV EH1
 - SoC: Chips Alliance's SweRVolf

Lecture Details		
Topic		
Lab 0	Introduction <ul style="list-style-type: none"> - Direct to Quick Start Guide or Getting Started Guide - Overview of Tools - Overview of Labs 	Lab 8 <ul style="list-style-type: none"> Interrupt-driven GPIO <ul style="list-style-type: none"> - Introduction to SweRVolf's interrupt support - Overview of the main changes to the controller - Examples in C and assembly
Lab 1	Vivado Project <ul style="list-style-type: none"> - Simulation (Verilator). - Creating a Vivado project using SweRVolf RTL (Verilog), generating a bitfile and downloading it onto the Nexys A7 FPGA board. 	Lab 9 <ul style="list-style-type: none"> Timers <ul style="list-style-type: none"> - Understand the timer controller obtained from Opencores an online community for the development of gateware IP (Intellectual Properties) Cores in the spirit of Free and Open Source collaboration. - Examples in C and assembly
Lab 2	C Programming <ul style="list-style-type: none"> - Example C program 	Lab 10 <ul style="list-style-type: none"> Serial Buses <ul style="list-style-type: none"> - SPI, I2C, and UART - Understand the serial bus controllers obtained from OpenCores. - Examples in C and assembly
Lab 3	Assembly Programming <ul style="list-style-type: none"> - Simulation - using Whisper, the SweRV-ISS, Instruction Set Simulator 	Lab 11-15 <ul style="list-style-type: none"> Understanding and Modifying the RISC-V Datapath <ul style="list-style-type: none"> - Diagram of the core structure - Instruction flow through the pipeline - Hazards and how to deal with them - Implement new instructions and execute them on the board (use - Understand the Branch Predictor and make some changes to it - Understand superscalar processing
Lab 4	Function Calls <ul style="list-style-type: none"> - RISC-V ABI - Procedure Calling Convention 	Lab 16-20 <ul style="list-style-type: none"> Understanding and Modifying the RISC-V Memory Hierarchy - Understand the operation of the memory hierarchy including cache hits and misses. - Test different cache sizes, configurations and management policies - Understand the cache controller - Understand the ICCM and DCCM
Lab 5	C with Assembly Code <ul style="list-style-type: none"> - Embedding assembly code with C 	Lab 21+ <ul style="list-style-type: none"> + potential additional lab(s)
Lab 6	Introduction to I/O <ul style="list-style-type: none"> - Program-driven GPIO - Overview of Nexys A7 I/O - C and Assembly Programs 	
Lab 7	7-Segment Displays <ul style="list-style-type: none"> - Build 7-segment display decoder for driving Nexys A7's built-in 7-segment displays Examples in C and assembly 	

(3) Guide to RISC-V

A quick guide for teachers, students and developers to RISC-V licencing, software and hardware

The Guide to RISC-V

Imagination use RISC-V as the firmware processor inside our latest GPUs, and we decided to lead the way in Education to popularise the teaching of this important technology.

As part of our "IUP" Imagination University Programme we teamed up with Digi-Key to help them create a technology guide focused on RISC-V. It is short, easy to understand, and hands-on.

Written by Richard J. Sikora, it draws on his 35 years' experience in embedded systems development!

Contents

- RISC-V: its history and unique features
- Licencing
- Where the technology is going...
- Early examples of implementations
- Hands-on with three implementations:
 - (1) MPU microprocessor running Linux using the Kendryte CPU on the Seeed Technologies Maix BiT board
 - (2) MCU microcontroller using the SiFive SoC on the SparkFun RED-V "Red Board".
 - (3) And a "soft core" – implementing Western Digital's "SweRV" EH1 core on an FPGA from Xilinx.

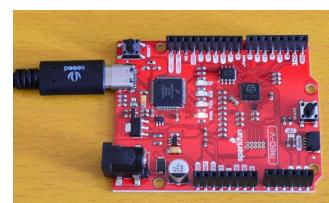
This project is called "RVfpga" and is being rapidly adopted as an under-graduate course in Computer Architecture.

Download

<https://university.imgtec.com/teaching-download/#RVGuide>



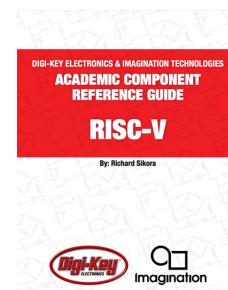
1. SiPeed Maix Bit



2. SparkFun RED-V



3. Digilent Nexys A-7



4. Cover – Guide to RISC-V

(4) Fun with Beagle – Exploring the GPU

Explore Open CL on the popular BeagleBone Black

The BeagleBone® Black

The BeagleBone® Black is a favourite development platform for millions of users: Students, Hobbyists, and Developers. As its popularity grew, it became a preferred Single Board Linux Computer for industrial developers.

The TI (Texas Instruments) "Sitara™ system-on-chip at the heart of Beagle contains an Imagination SGX530 GPU. Until now, this has been just a block on the system diagram and was a "black box" to most Beagle users. In recognition of Beagle's popularity, we are lifting the lid on its GPU...

Dr. Iain Hunter was at TI when the Sitara SoCs first appeared, and since then he has become a leading independent developer on this platform. Few people know Beagle so well!

Graphics

Almost all of the materials from "Introduction to Mobile Graphics, 2020 Edition" will run on Beagle, and we reprise a few of the basic examples in these materials.

Running Open CL

In a practical way, Dr. Hunter takes you through this interesting and quite complex part of the BeagleBone Black system. He shows you how to implement Open CL on the GPU and run an application.

- For the first time, we are releasing an Open CL driver which runs on the SGX530 allowing parallel compute activities to be run on the GPU.
- The package includes the Open CL driver along with a detailed and practical explanation about getting it running and how it can be used.
- The example demonstrated is Audio Sample Rate Conversion, running on the GPU – a first for the Beagle Board!

Request & Download

<https://university.imgtec.com/teaching-download/#FWB>

Video Tutorials

- The content list of Fun with Beagle videos:
- Preparation
- Boot BeagleBone Black
- Configure SDK
- Compile SDK
- Build BeagleBone Black OpenCL Examples
- Run BeagleBone Black OpenCL
- Build OpenCL audio
- Run ALSA OpenCL



Fig - BeagleBone Black

<https://university.imgtec.com/fun-with-beagle-video/>

(5) Edge AI – Principles and Practices

Rigorous and complete. A foundation course for under-graduates
In development - release Q4'21

Scope

The course is based on the development of 9 laboratory units, which will cover most of the fundamental algorithms and typical applications in Edge AI , following a case-study format and fitting a typical semester course.

Audience & Languages

3rd year BSc EE and CS Students
English, Simplified & Traditional Chinese ...

Platform:
SEED Studio "Pumpkin" i300 board running
Imagination's Neural Compute Software
Development Kit

Course syllabus

Module	Unit	Course
Module 1. Introduction to Edge AI	1. Introduction and Getting Started	Lecture 1: Introduction to Edge AI. Lab 1: Getting started with the Pumpkin platform and NCSDK
	2. Data acquisition and processing on the Edge	Lecture 2: Image processing fundamentals Lab 2: Image acquisition and processing with OpenCV
	3. Introduction to Machine Learning on the Edge	Lecture 3: Introduction to Machine Learning Lab 3: Basic Machine Learning on the Pumpkin board
Module 2. Image vision	4.Image classification	Lecture 4: Image classification on edge devices Lab 4: Developing an image classifier on the Pumpkin board with NCSDK
	5.Object detection	Lecture 5: Object detection on Edge devices Lab 5: Object detection for autonomous vehicles
	6. Image segmentation	Lecture 6: Image Segmentation Lab 6: Image Segmentation for Security Cameras on the Edge.
Module 3. Speech and natural language processing	7. Automatic Speech Recognition (ASR)	Lecture 7: Automatic Speech Recognition for Edge Devices Lab 7: Voice control of an Edge device
	8. Natural Language Processing (NLP)	Lecture 8: NLP Fundamentals Lab 8: Automatic question answering on Edge devices
Module 4. Advanced topics	9: Advanced NCSDK and OpenCL usage.	Lecture 9: Advanced NCSDK and OpenCL usage. Lab 9: OpenCL-based pre- and post-processing

Authors

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- Universidad Complutense de Madrid (Spain)

Prof. Xiaohui Duan - Peking University (China)

Support

IUP Forum:

<https://university.imgtec.com/forums/edge-ai/>

IUP Online Hub

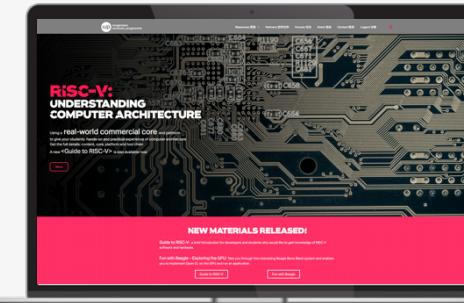
IUP Website

The focal point to access our services is the IUP website: teaching materials, video tutorials, forums, suggested hardware, recommended textbooks, pictures, news, and workshop / event listings.

Joining the IUP

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<http://university.imgtec.com/register/>
2. Activate your account from the verification email
3. Visit the IUP teaching materials page:
<https://university.imgtec.com/teaching-download/>
 - Request the materials you want
 - Tell us what you plan to do
4. Downloads are usually approved within 48 hours

The IUP homepage at:
<https://university.imgtec.com>



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<http://university.imgtec.com/forums/>

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Academic Partners



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