Elementos que conforman la arquitectura del MC68HC11

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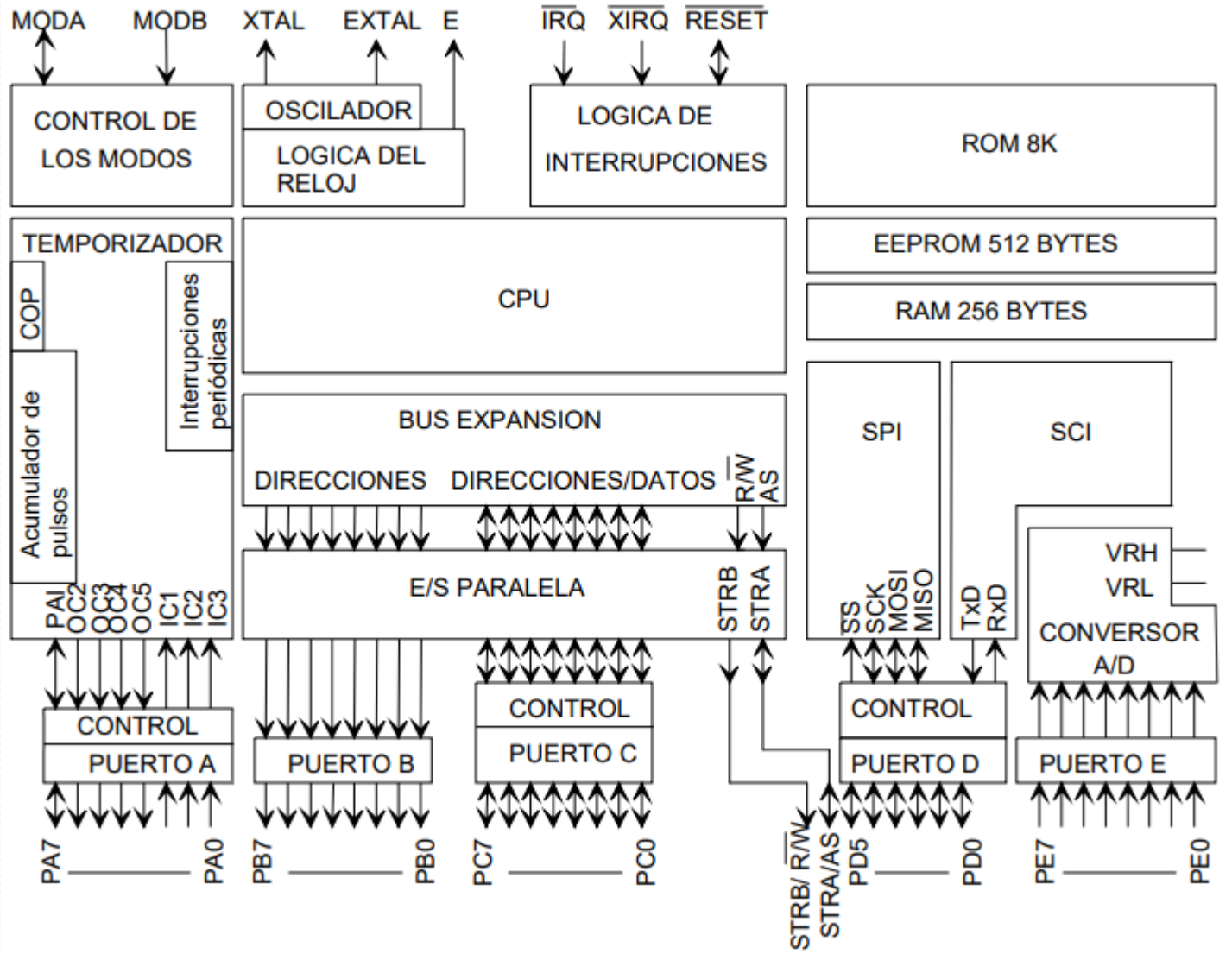
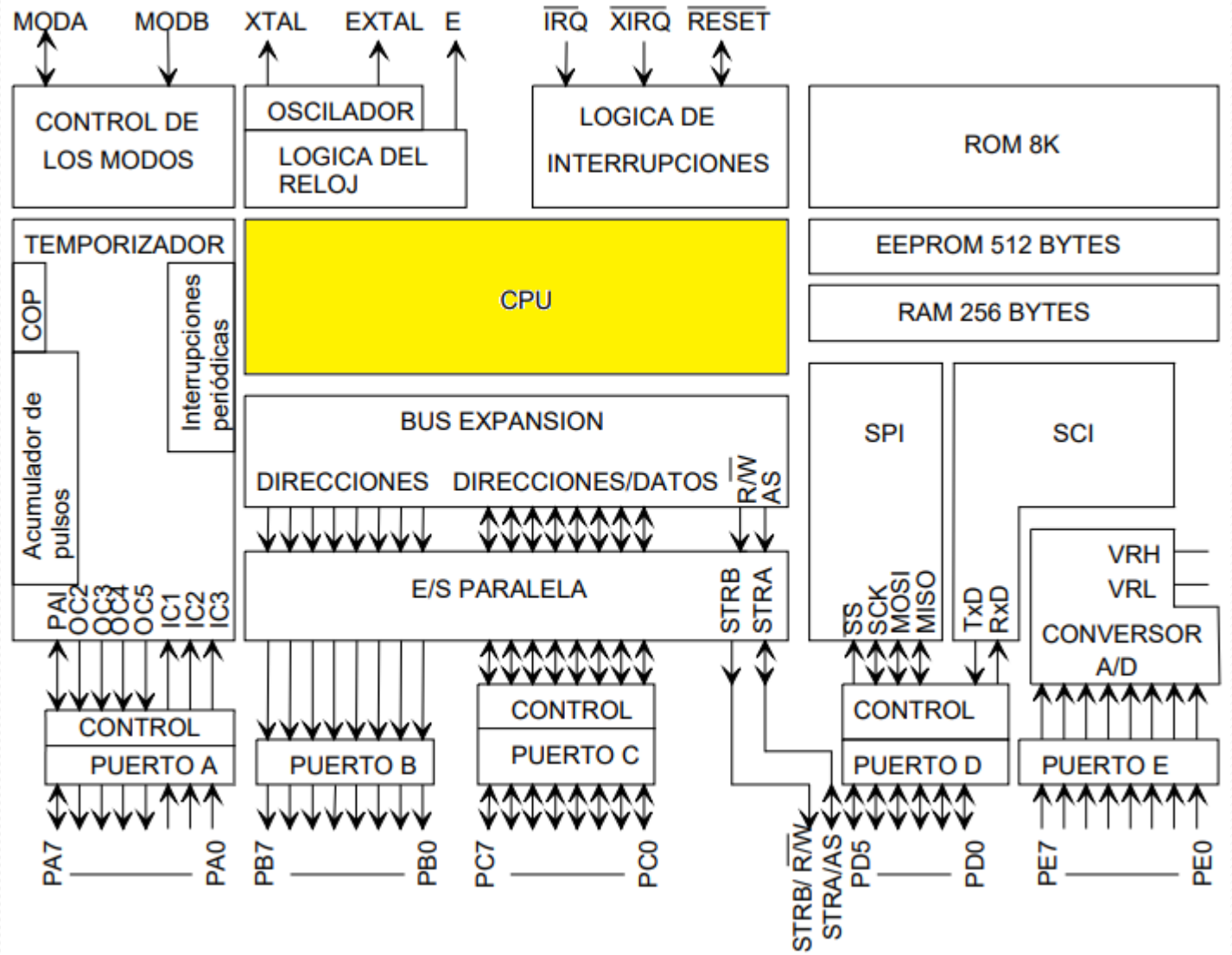
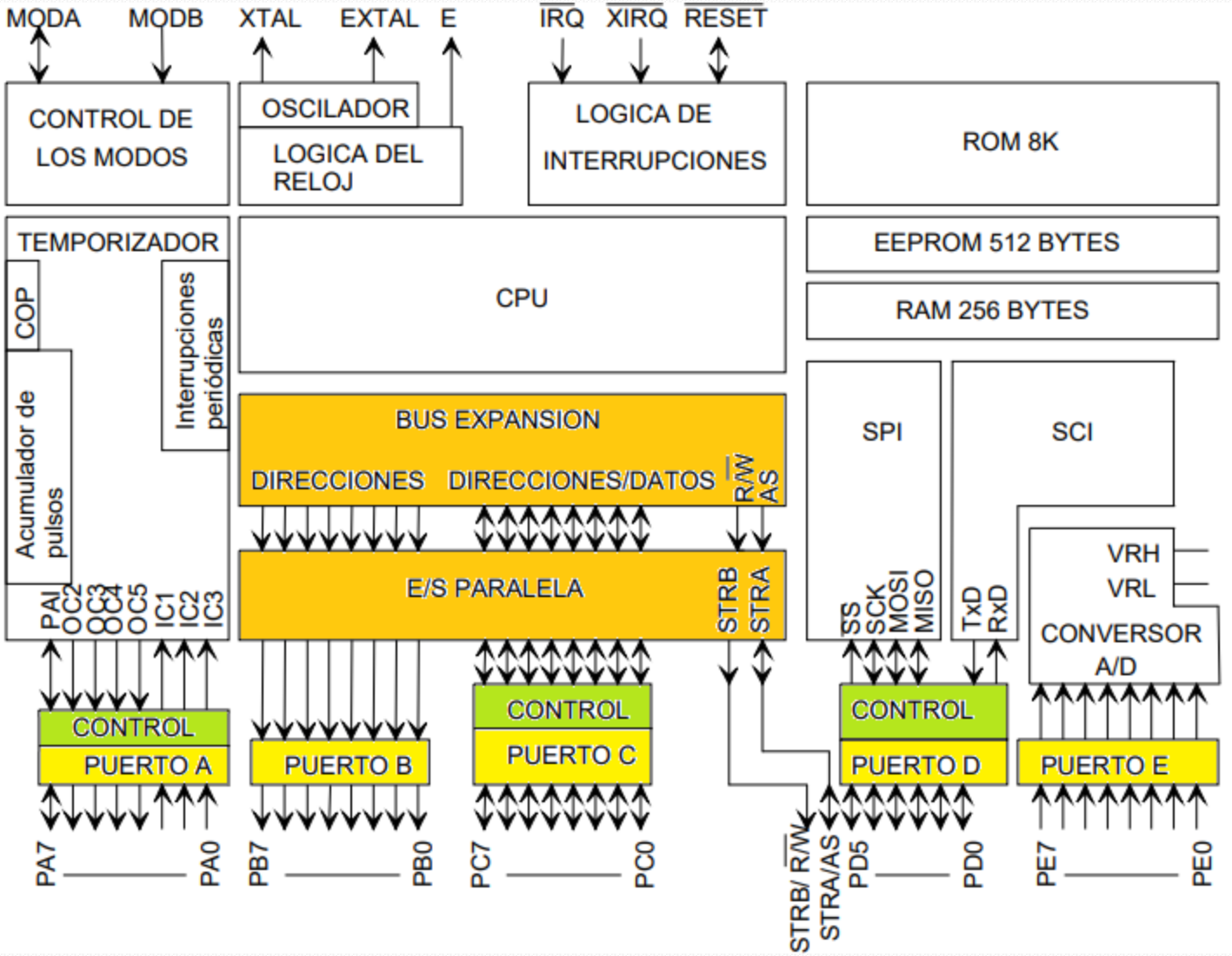
ESTRUCTURA Y PROGRAMACIÓN DE COMPUTADORAS

Diagrama de bloques de la arquitectura del MC68HC11

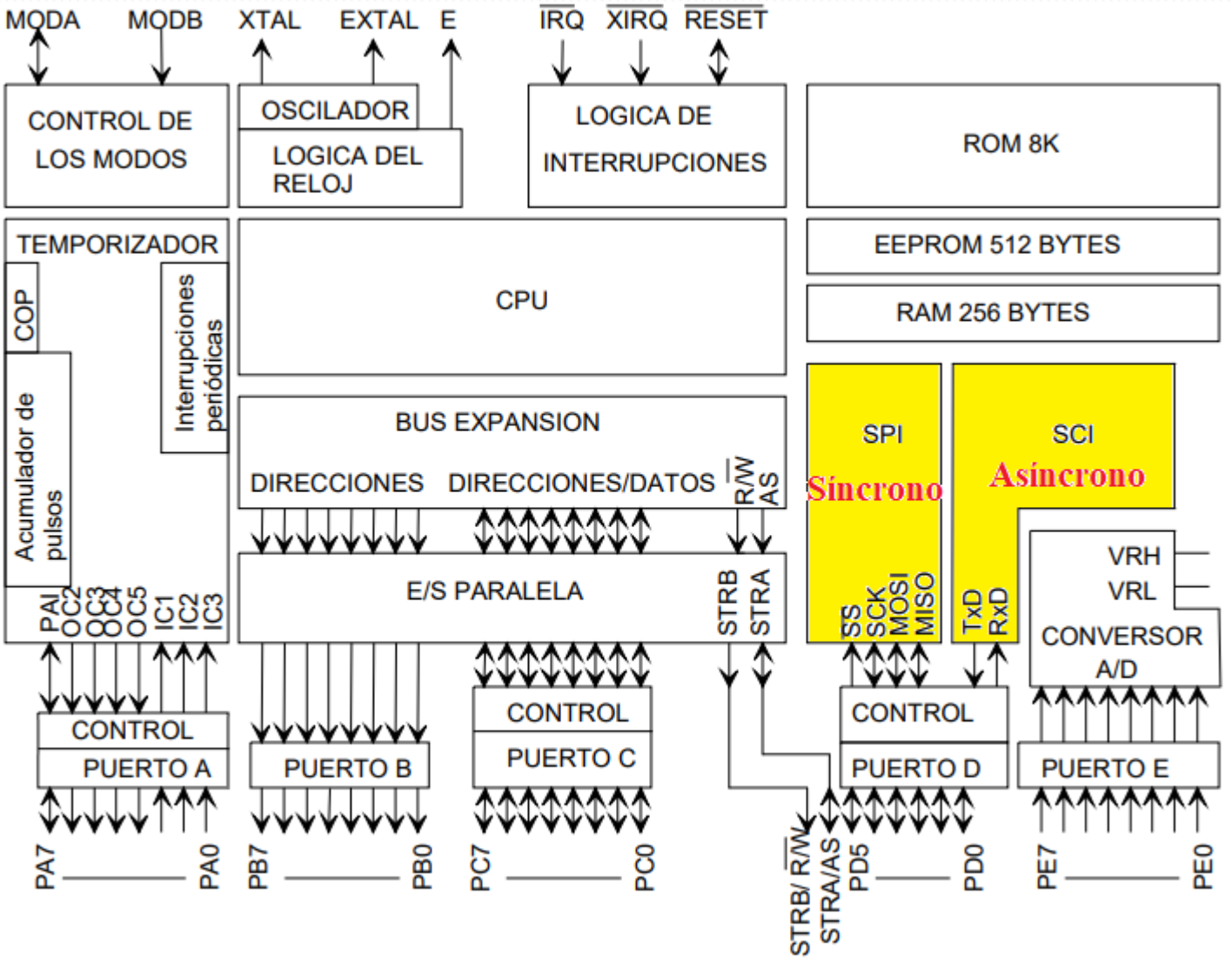


Unidad Central de Procesamiento

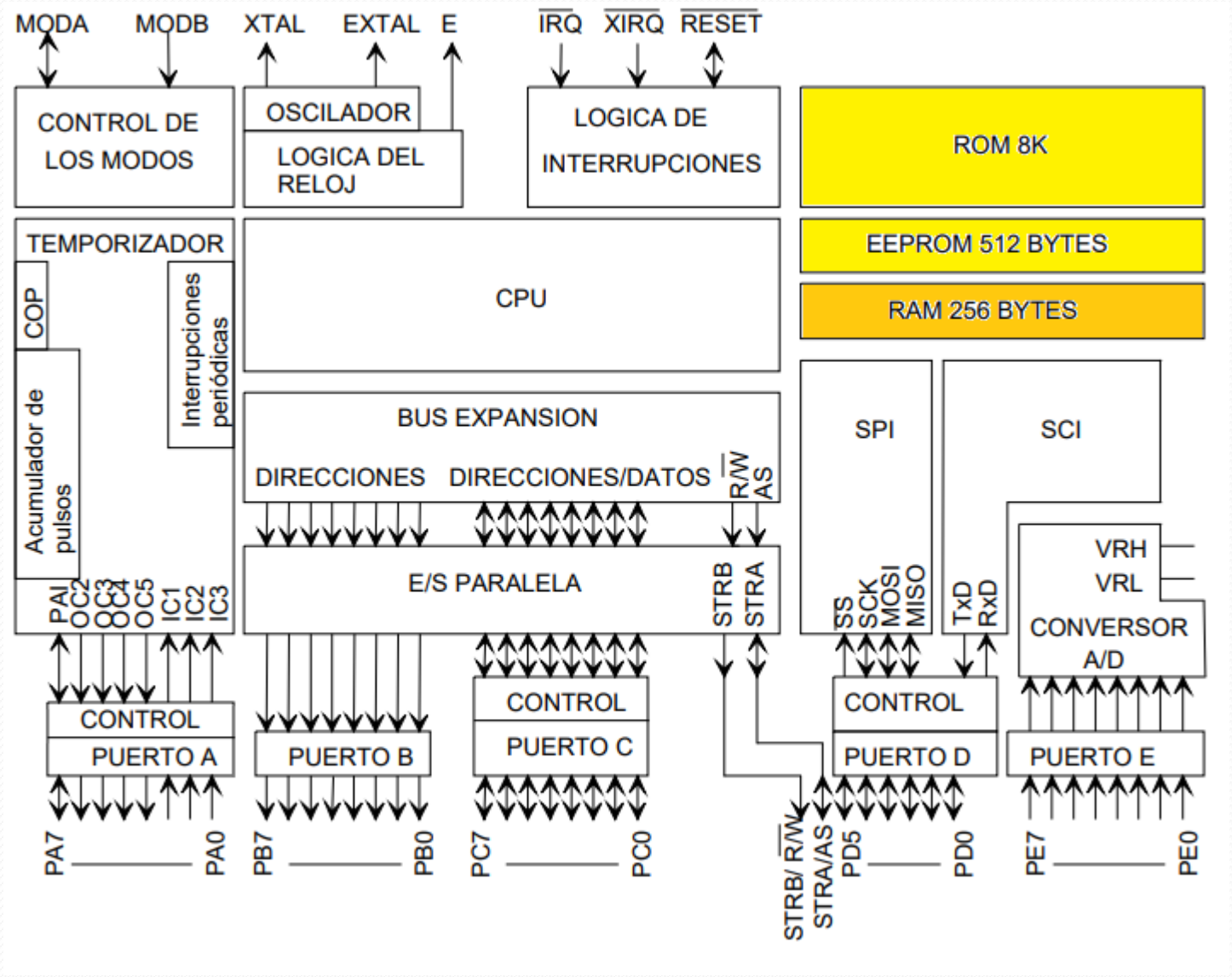



MODA
MODB
XTAL
EXTAL
E
IRQ
XIRQ
RESET
CONTROL DE LOS MODOS
OSCILADOR
LOGICA DEL RELOJ
LOGICA DE INTERRUPCIONES
ROM 8K
TEMPORIZADOR
COP
Interrupciones periódicas
Acumulador de pulsos
PAI
OC2
OC3
OC4
OC5
IC1
IC2
IC3
CPU
EEPROM 512 BYTES
RAM 256 BYTES
BUS EXPANSION
DIRECCIONES
DIRECCIONES/DATOS
R/W
AS
E/S PARALELA
STRB
STRA
SPI
SS
SCK
MOSI
MISO
SCI
TxD
RxD
VRH
VRL
CONVERSOR A/D
CONTROL
PUERTO A
PUERTO B
CONTROL
PUERTO C
CONTROL
PUERTO D
PUERTO E
PA7
PA0
PB7
PB0
PC7
PC0
STRB/ R/W
STRA/AS
PD5
PD0
PE7
PE0

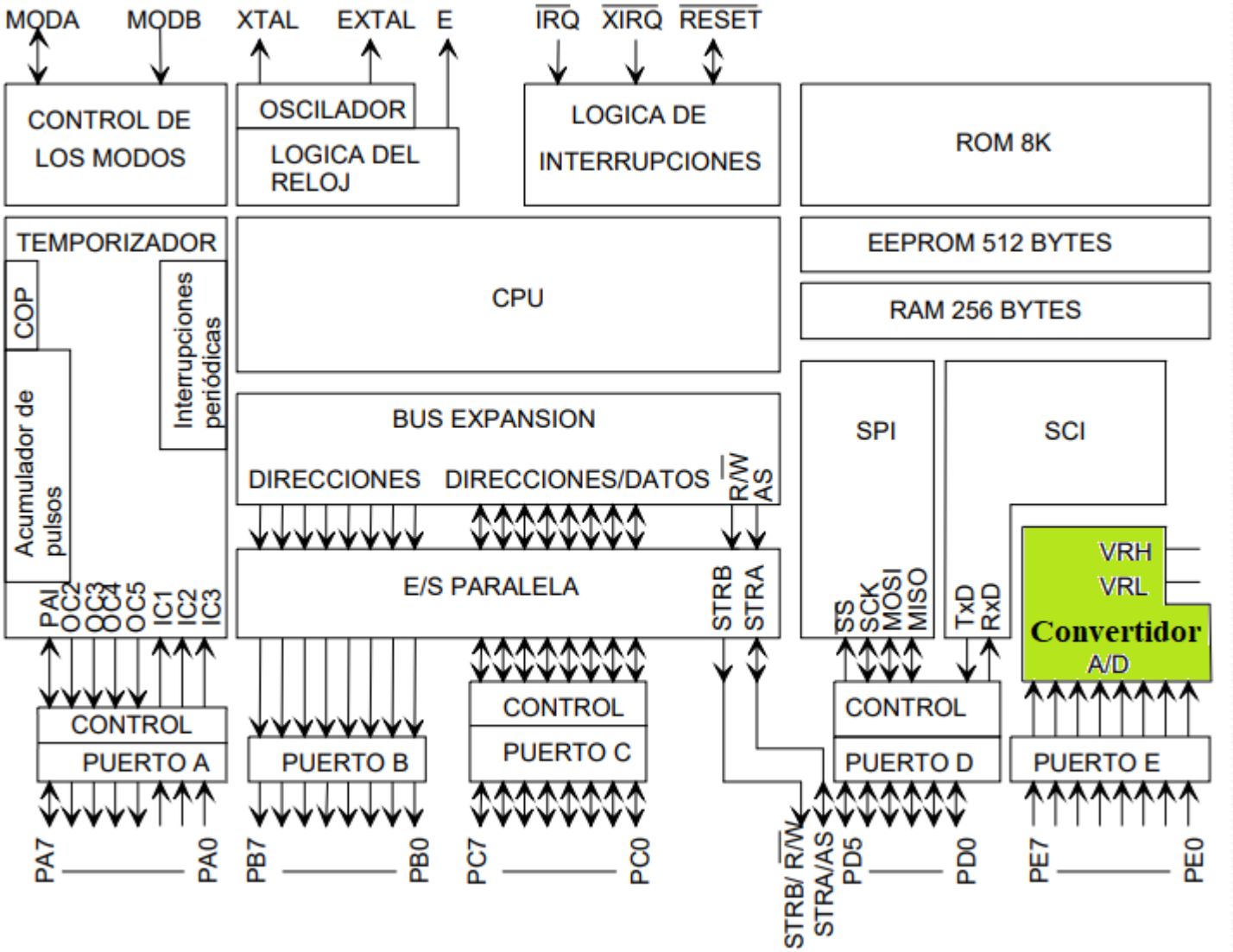
Puertos seriales



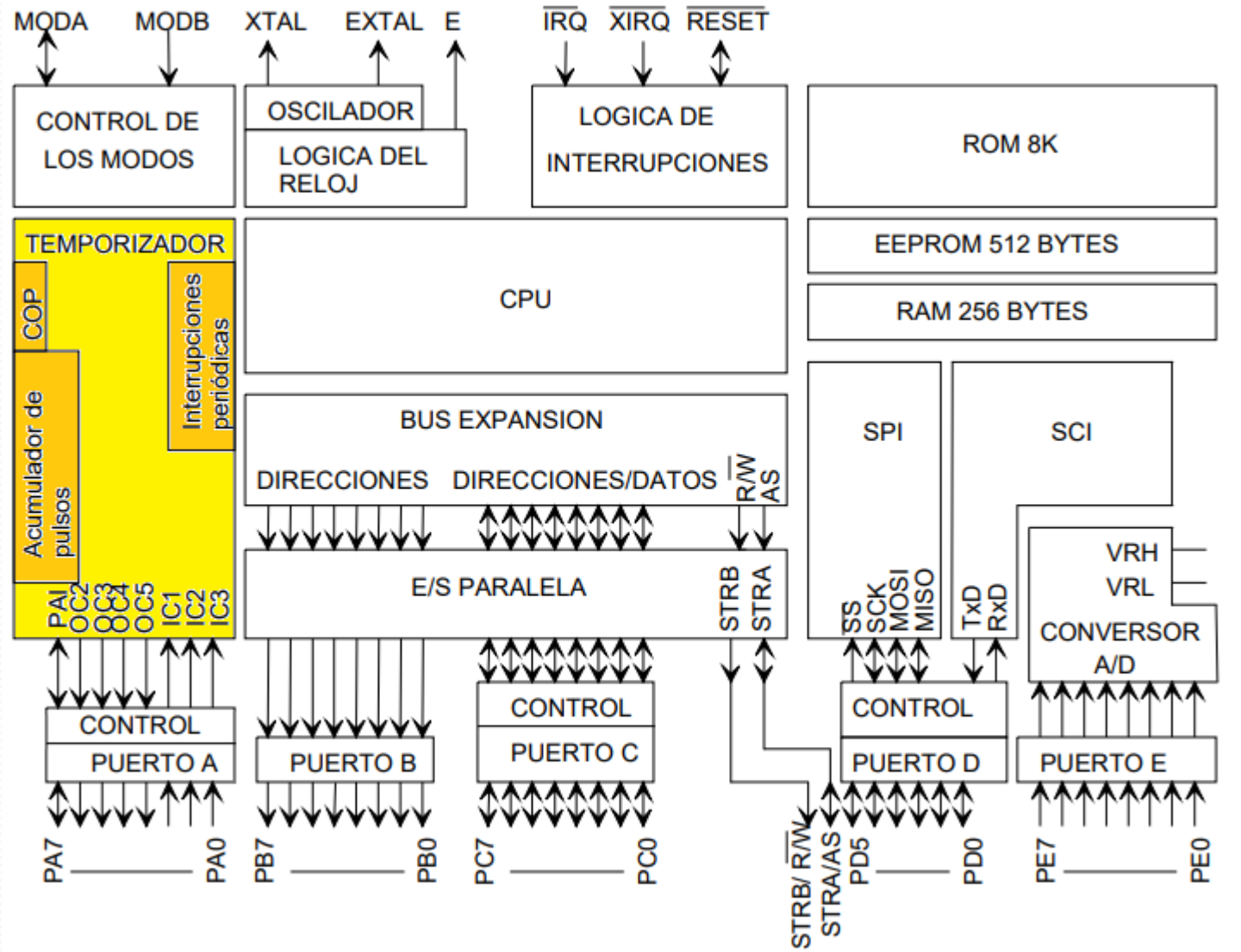
Memoria Interna



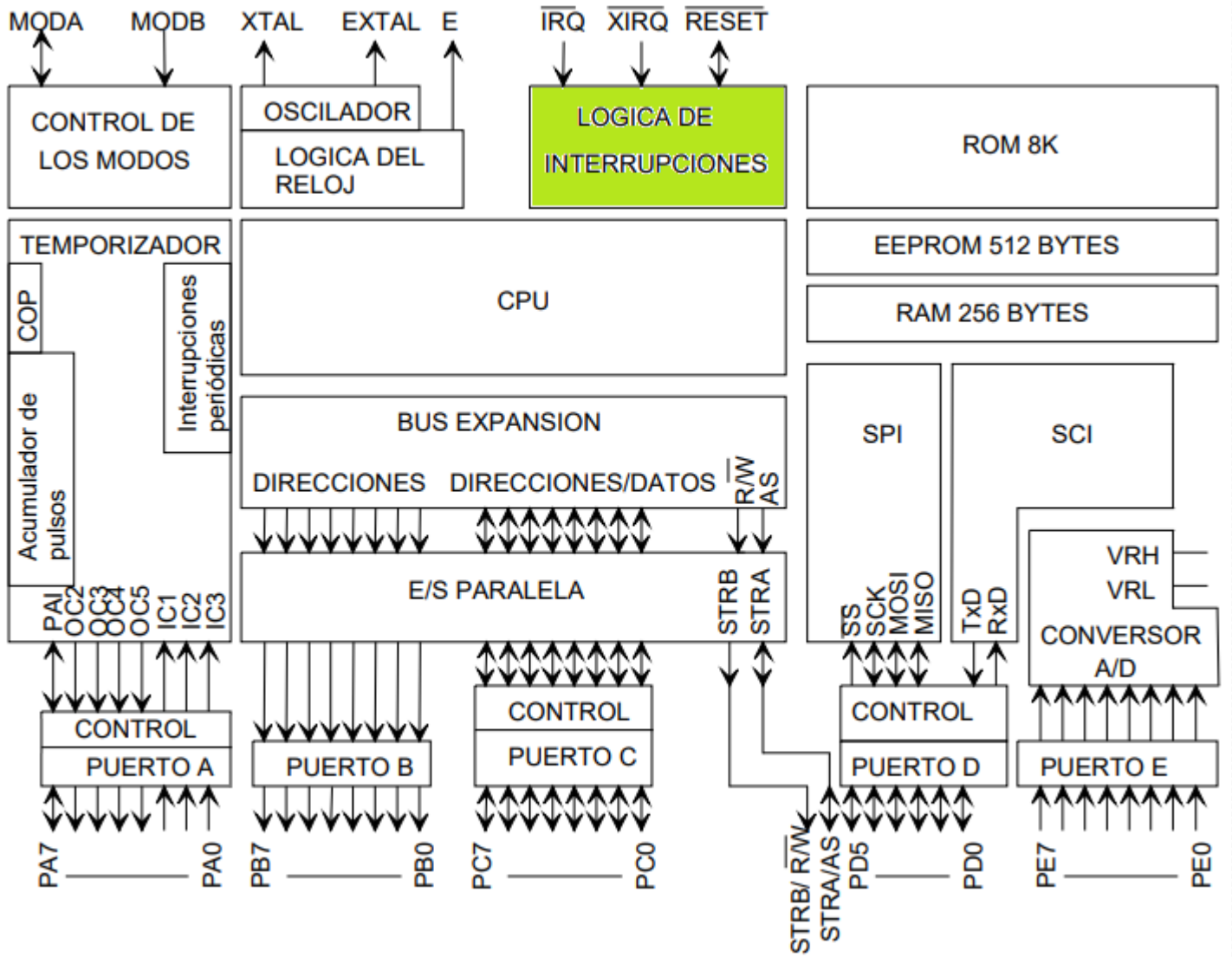
Convertidor Analógico/Digital de 8bits



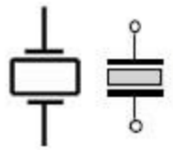
Temporizadores y Contadores

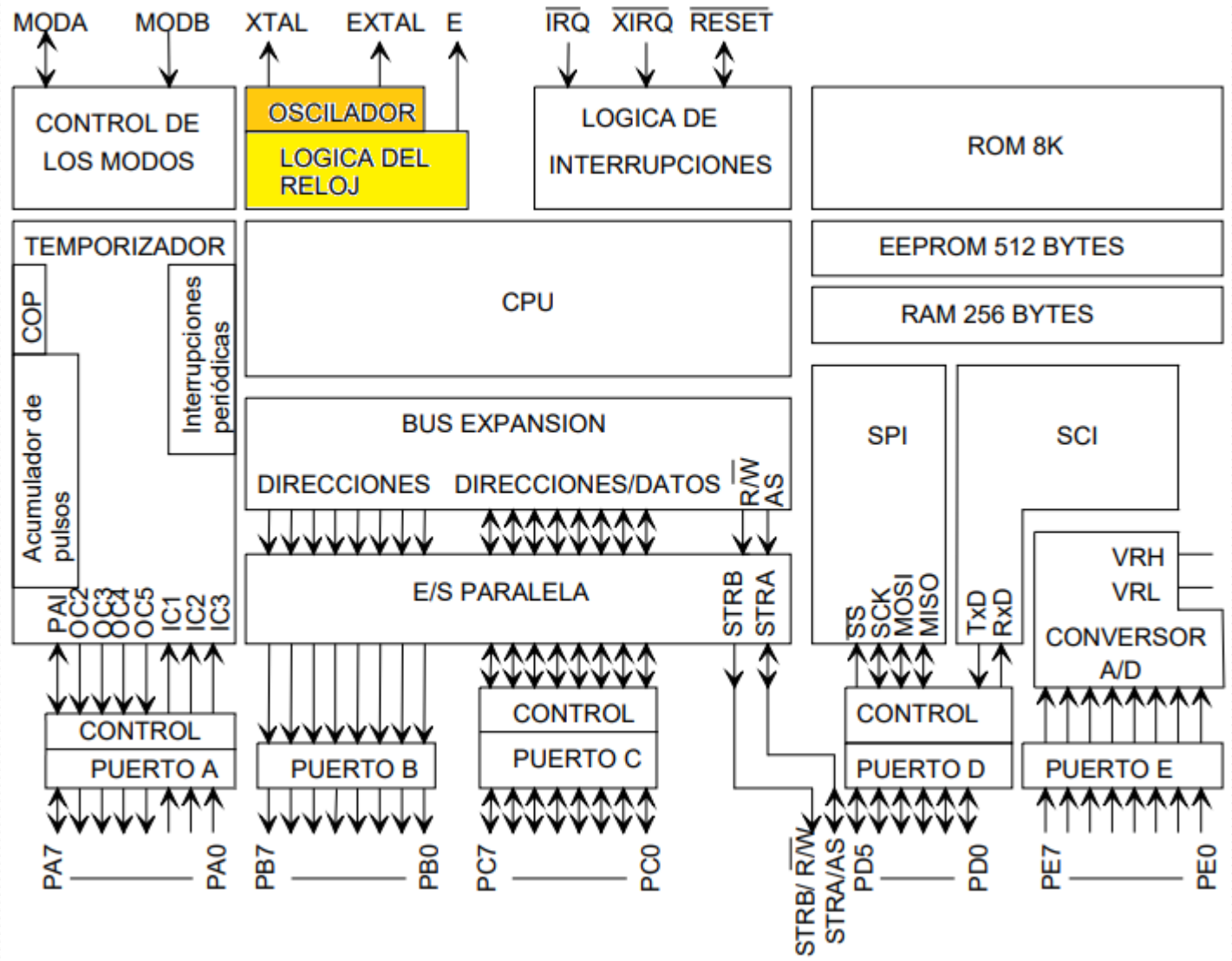


Control de Interrupciones

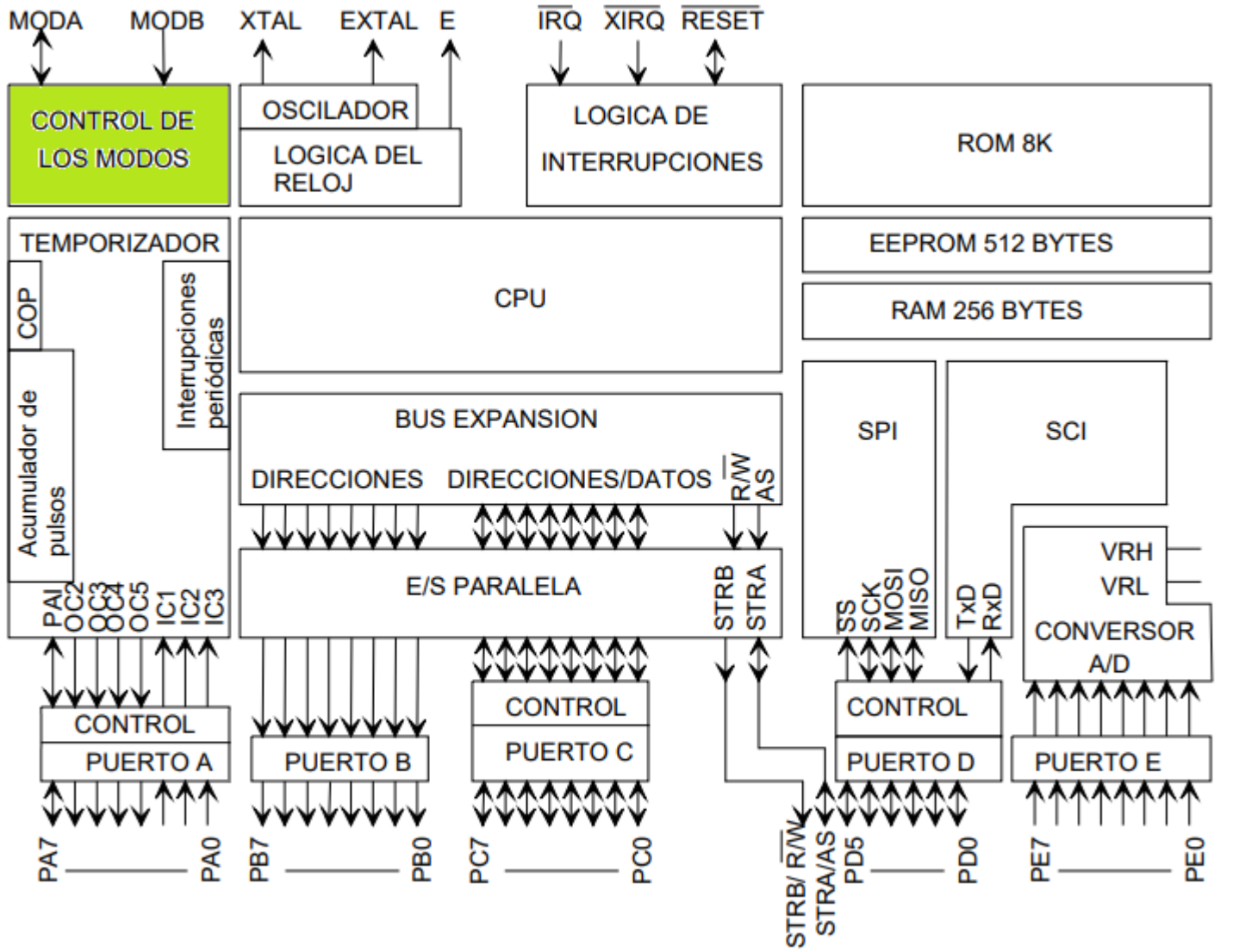


Módulo para generar señal de reloj



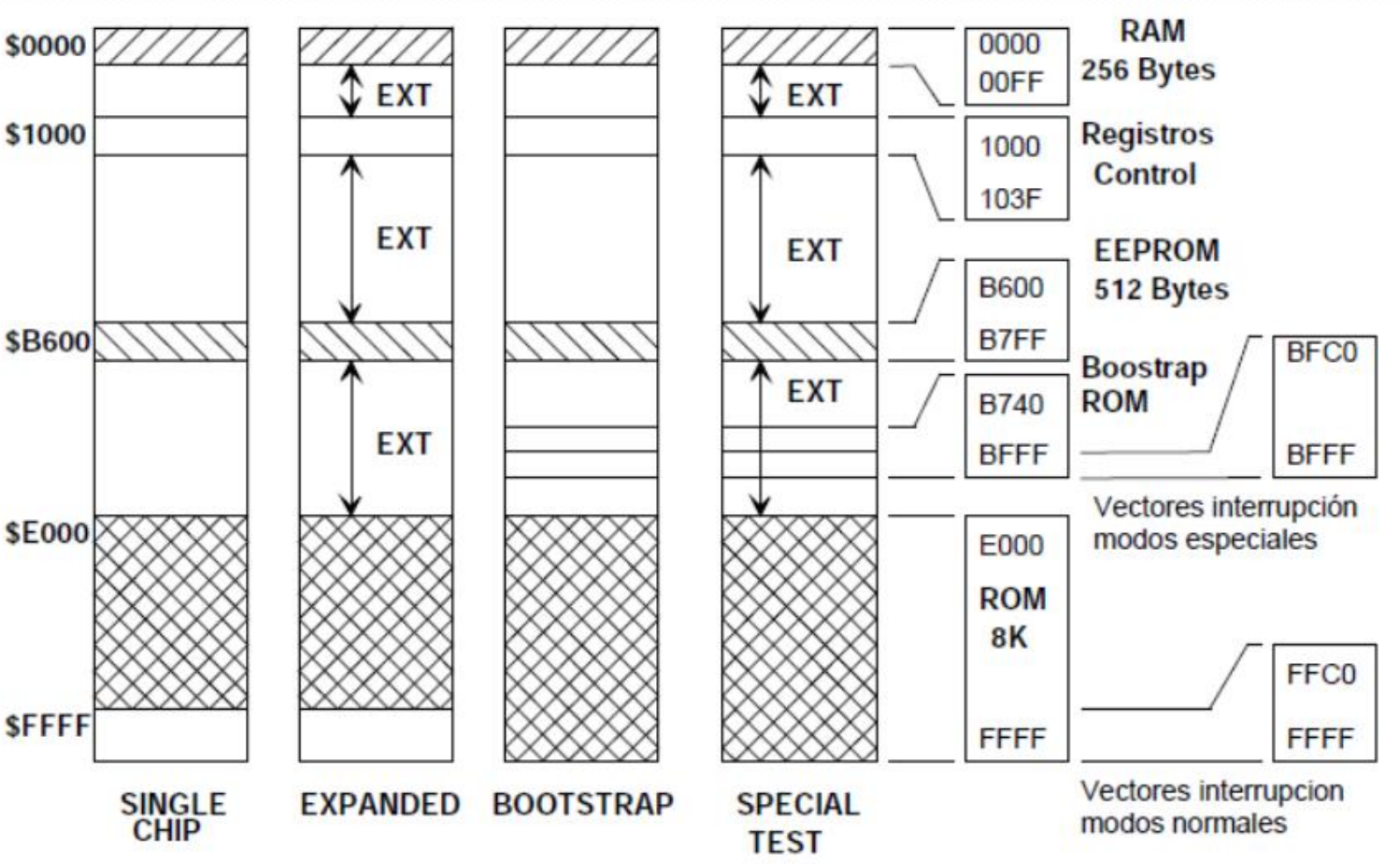


Modos de operación del MC68HC11

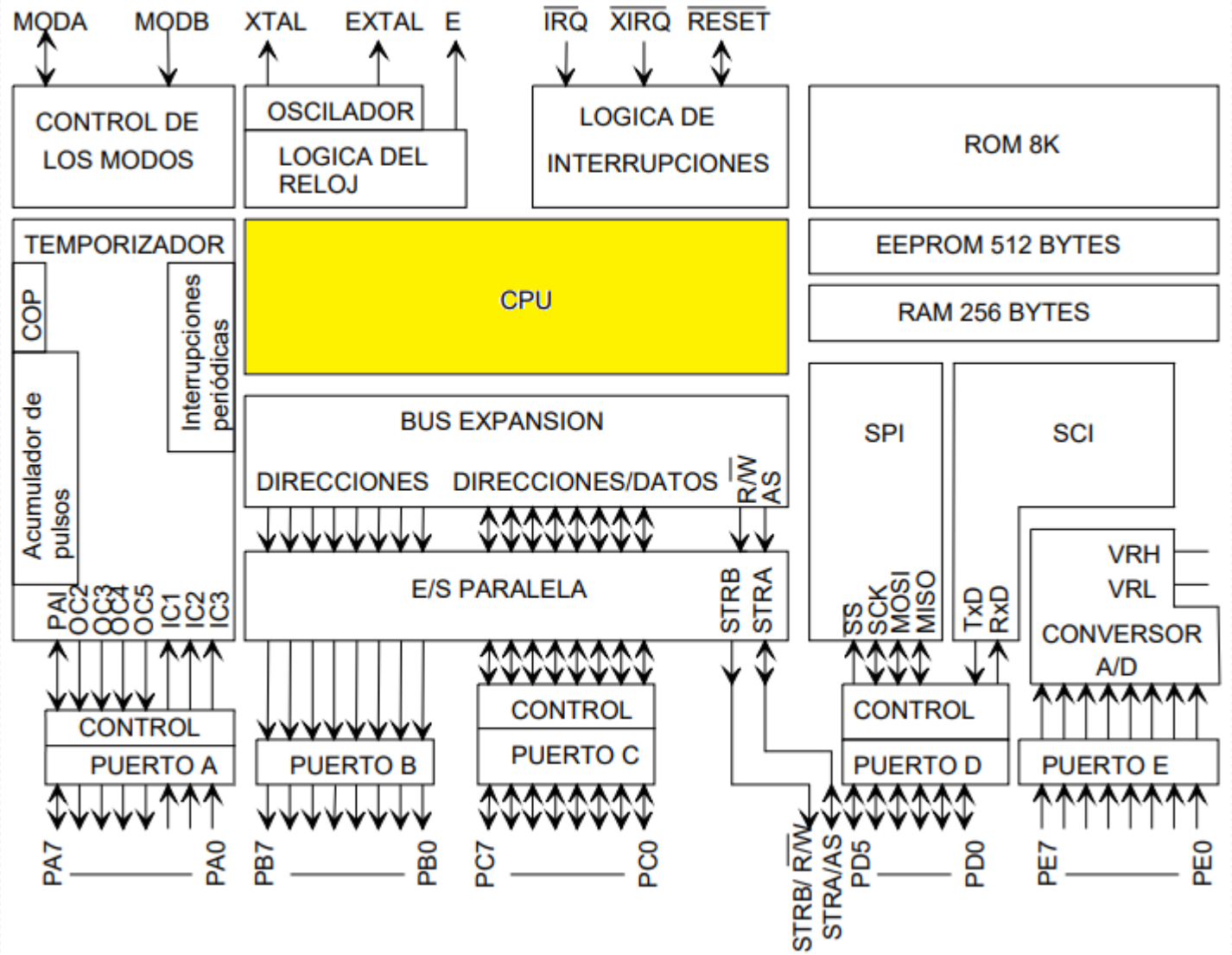


Modos de operación del MC68HC11

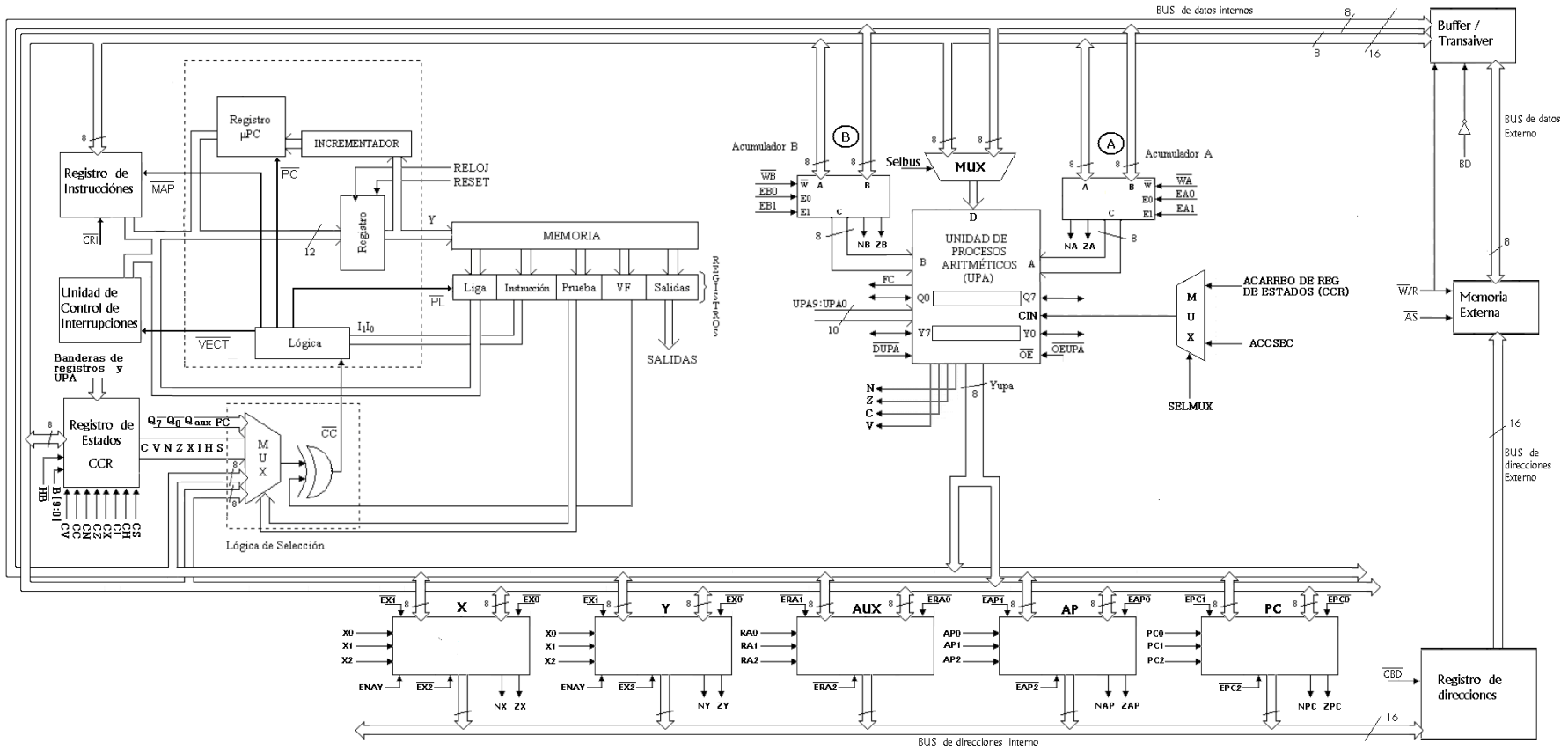
MODA	MODB	
0	0	Single Chip
0	1	Expanded Chip
1	0	Boot Strap
1	1	Special Test



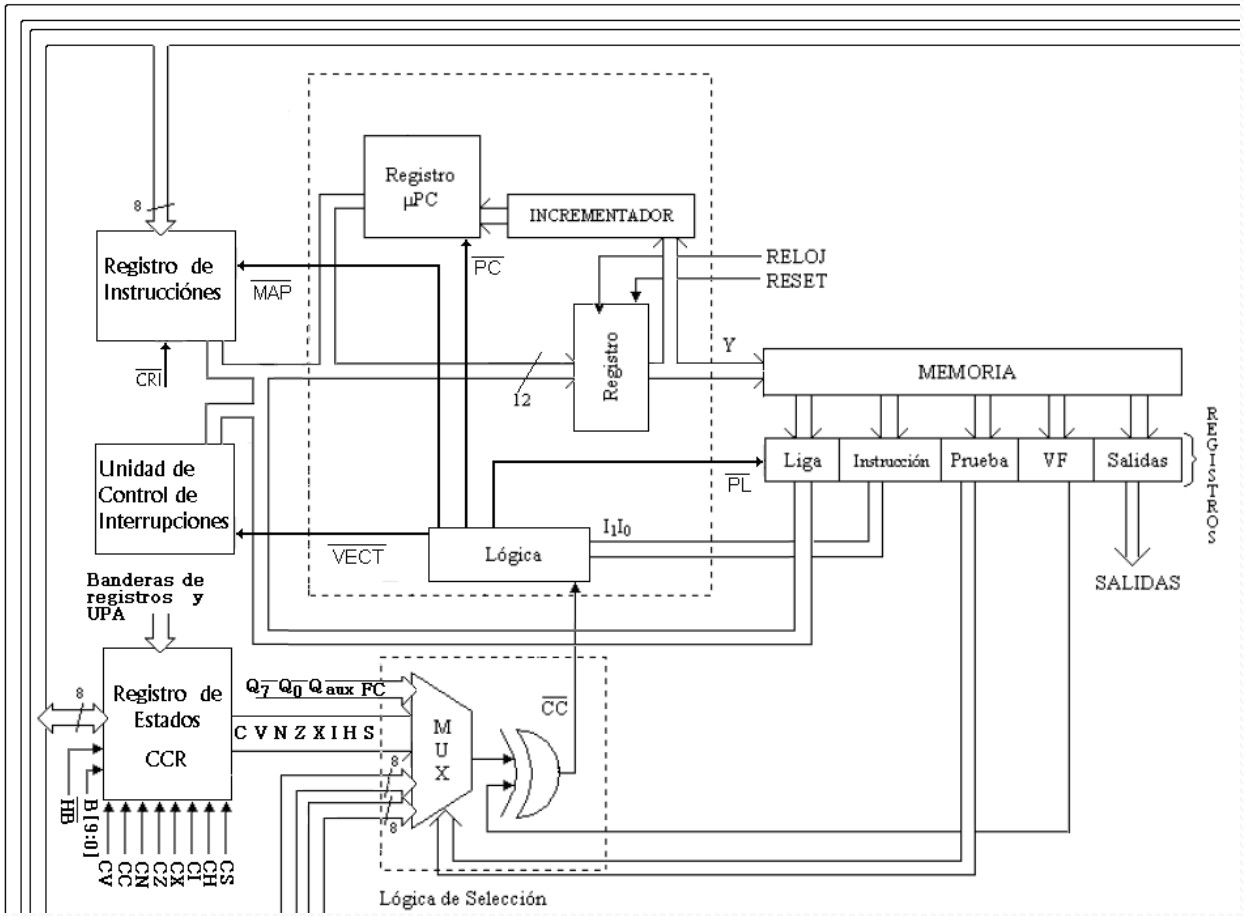
Unidad Central de Procesamiento



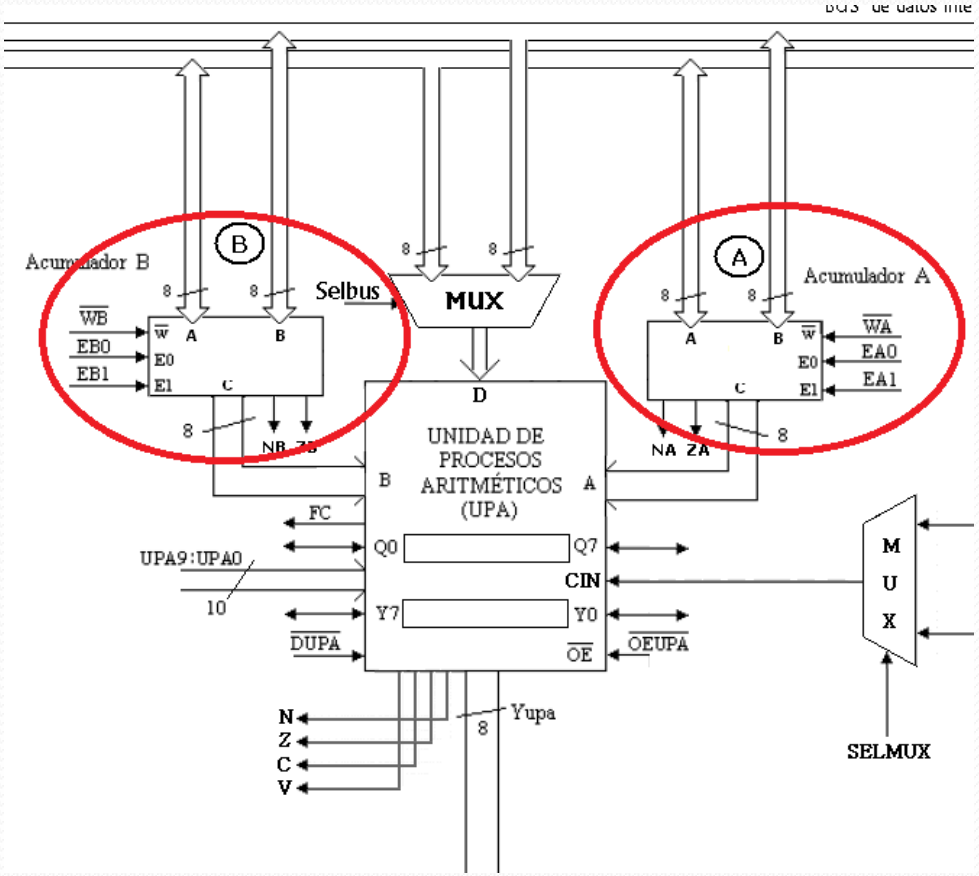
Arquitectura interna del CPU del MC68HC11



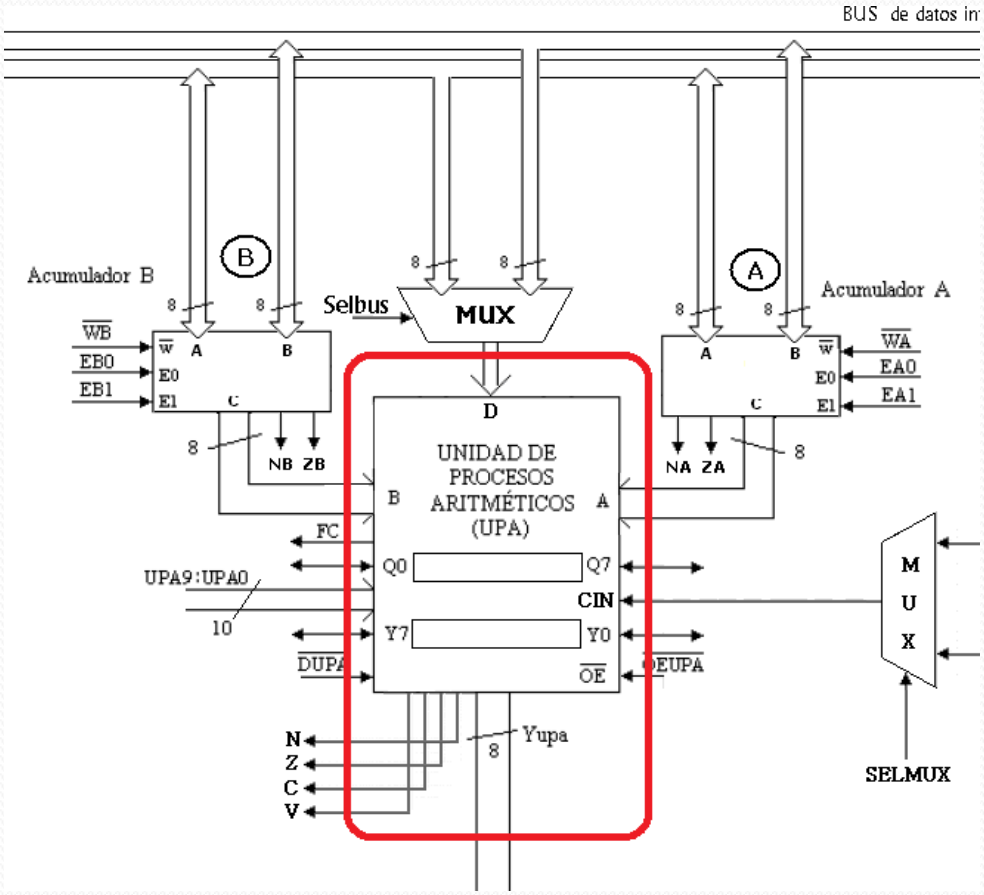
Se puede ver que en el interior del CPU se cuenta con un secuenciador básico



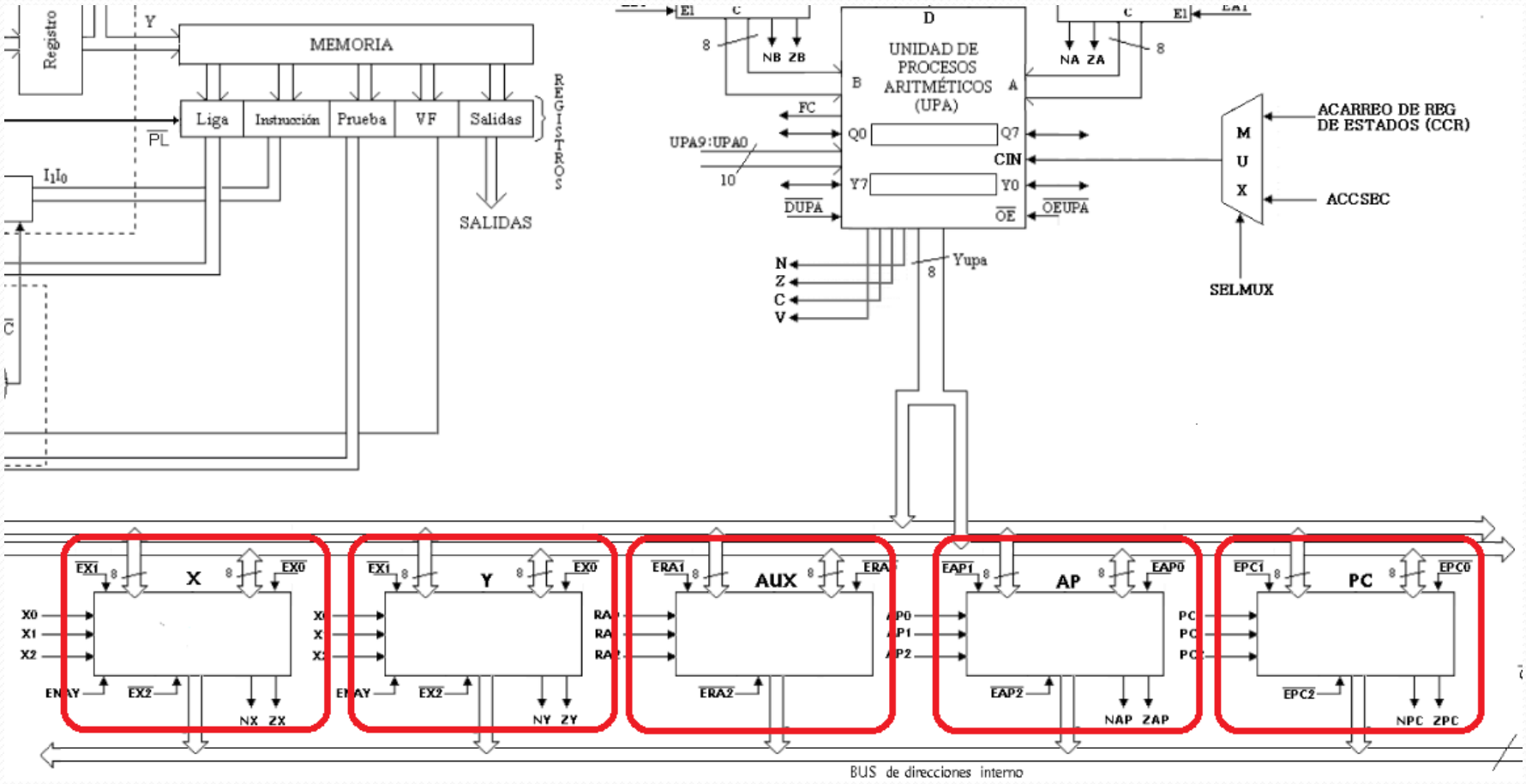
Cuenta con dos registros acumuladores de 8 bits, denotados como “A” y “B”



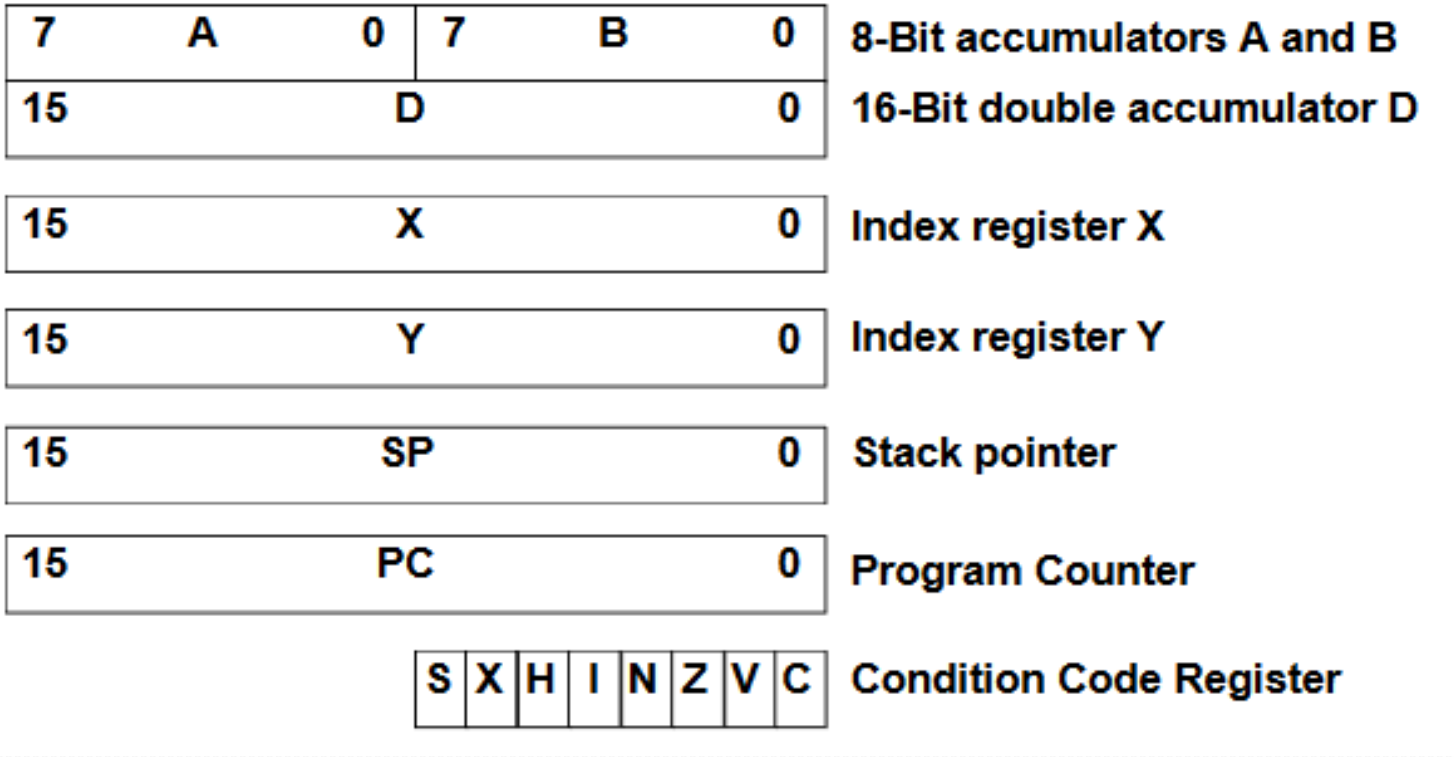
Una Unidad de Procesos Aritméticos de 8 bits



Cinco registros contadores de 16 bits denotados como “X”, “Y”, “AUX”, “AP” y “PC”

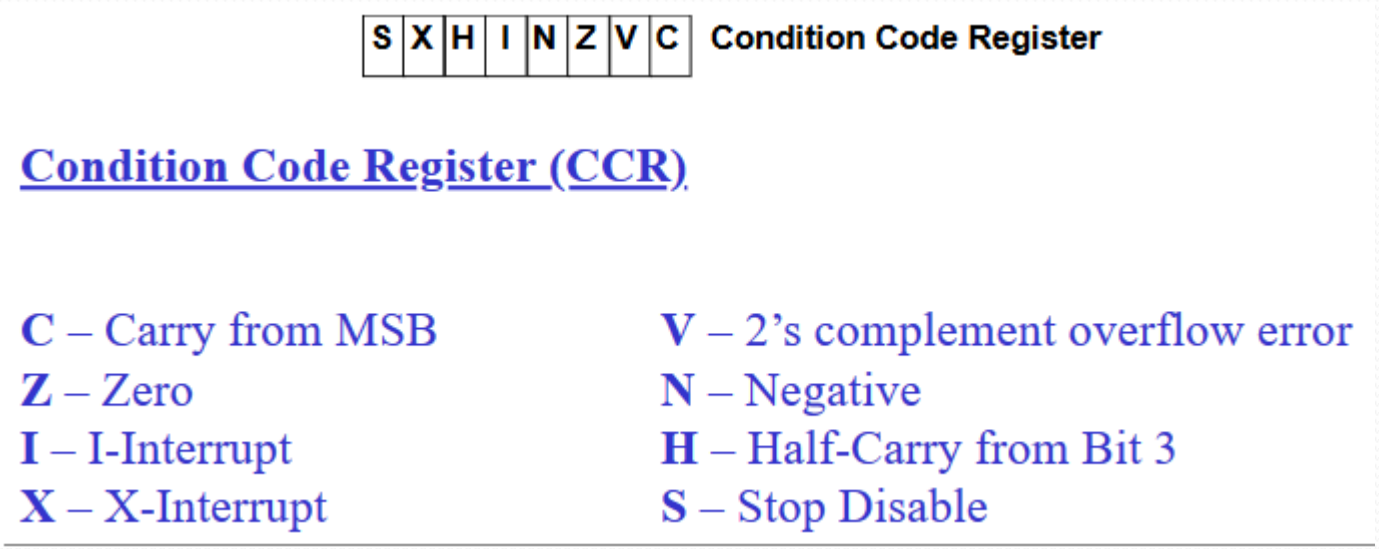


Conjunto de registros del CPU del MC68HC11



Nota: El registro “SP” en español se conoce como “AP” Apuntador de pila

El registro de estados o de condiciones se conoce como CCR.



Nota: Cada uno de sus 8 bits, tiene una función particular