**Generic Multiplier**

**The purpose of this experiment is to write a generic 2s complement multiplier**

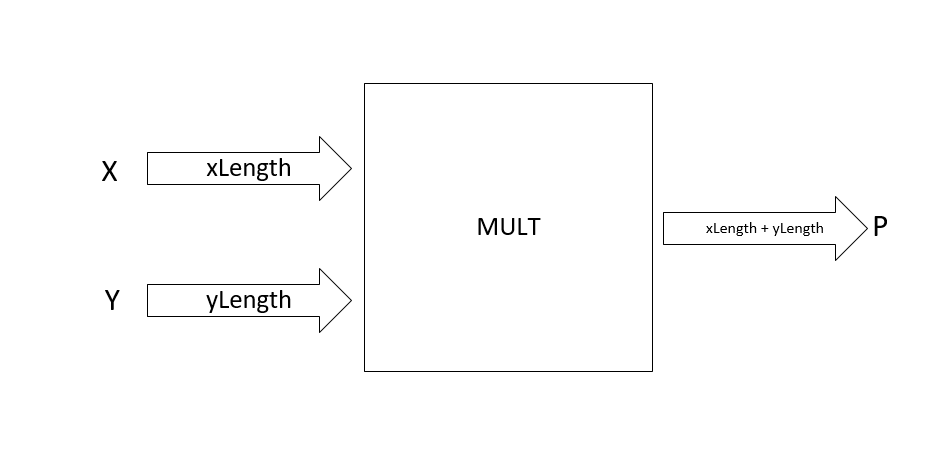
**YOU’RE NAME HERE**

**YOU’RE STUDENT NUMBER HERE**

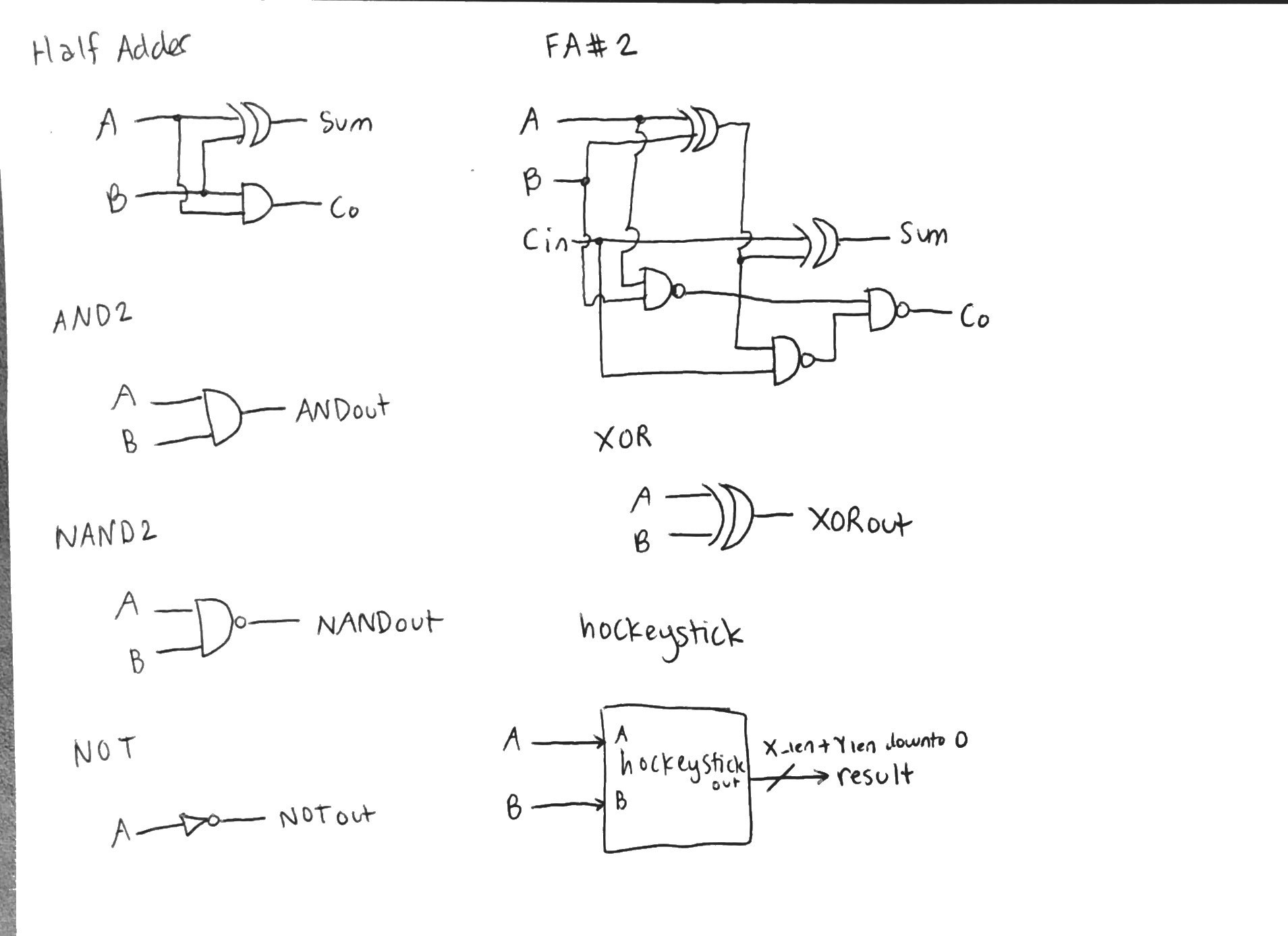
**Project Description:**

In VHDL we made an entity called MULT. MULT takes in X and Y and multiplies them using an array multiplier with the Baugh-Wooley algorithm. It outputs the result as a std\_logic\_vector with a length of Xlength + Ylength.

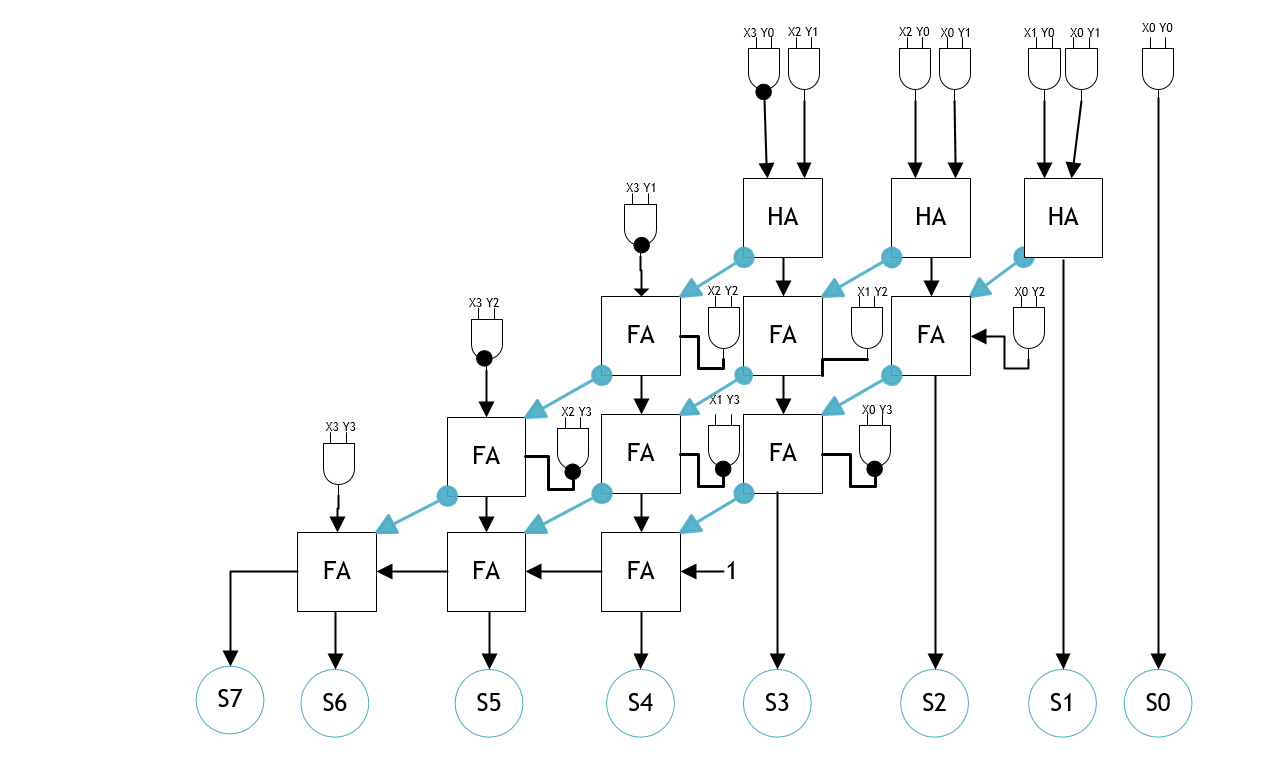
**Block Diagram of the multiply Chip:**



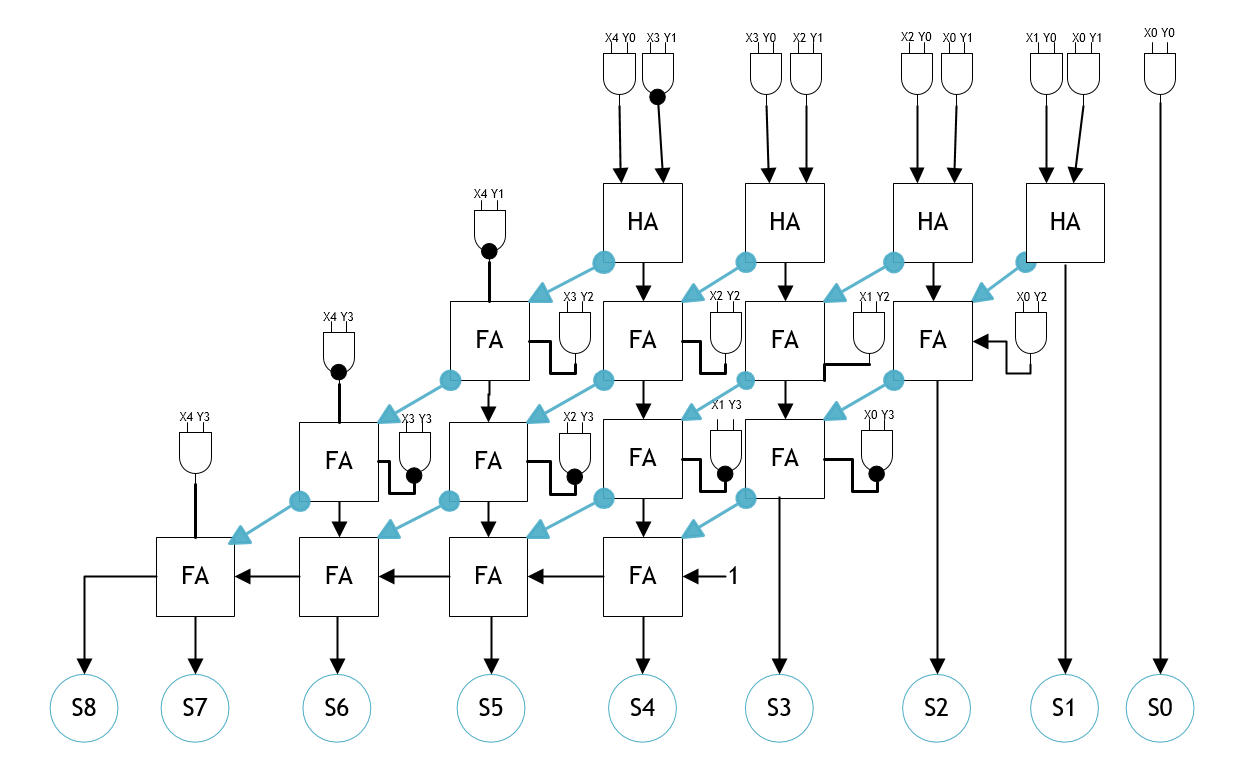
**Gate level design:**



**Design of MULT (4X4)**



**Design of MULT (5X4)**



**MULT VHDL Code:**

**VHDL Test Bench:**