I. Introduction

In the realm of computer architecture, a cache serves as a hardware component that stores recently accessed data with the aim of expediting future requests for that same data. This small and fast type of memory is positioned between the processor and main memory and its primary objective is to reduce the time required to access data from main memory, which is typically slower than accessing data from the cache. As an essential part of modern computer architecture, cache memory has a significant impact on system performance.

As part of our project, we have created a simulator code for an arbitrary n-way set associative cache in C++. Our simulator implements two levels of caches, namely L1 and L2. By reading trace files, the simulator assigns requests to the L1 cache, which in turn sends read/write requests to the L2 cache. The L2 cache interacts with DRAM and both L1 and L2 caches keep track of their own counters such as reads, writes, misses, hits, and so on. Upon completion of the simulation, our program prints the statistics for both caches on the console, as specified in the problem statement.

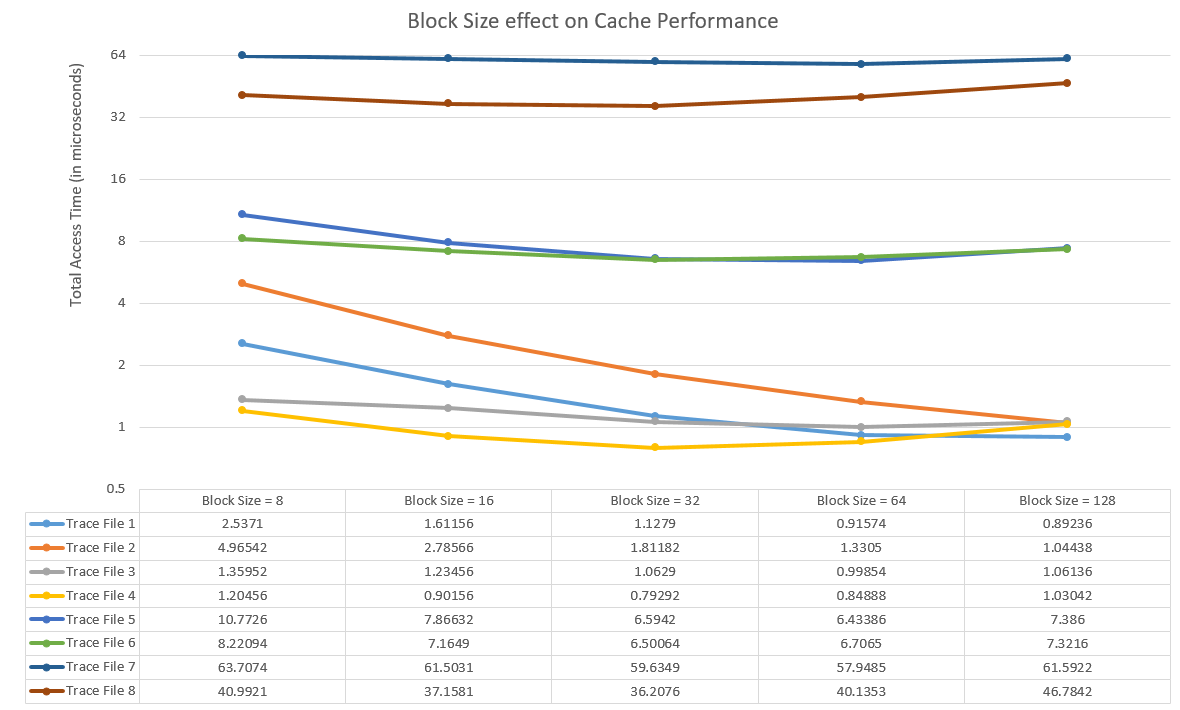
II. Configurable Parameters

The following parameters can be configured in the simulator

1. BLOCKSIZE: Number of bytes in a block/line.
2. L1\_Size: Total bytes of data storage for L1 Cache.
3. L1\_Assoc: Associativity of L1 Cache.
4. L2\_Size: Total bytes of data storage for L2 Cache.
5. L2\_Assoc: Associativity of L2 Cache.

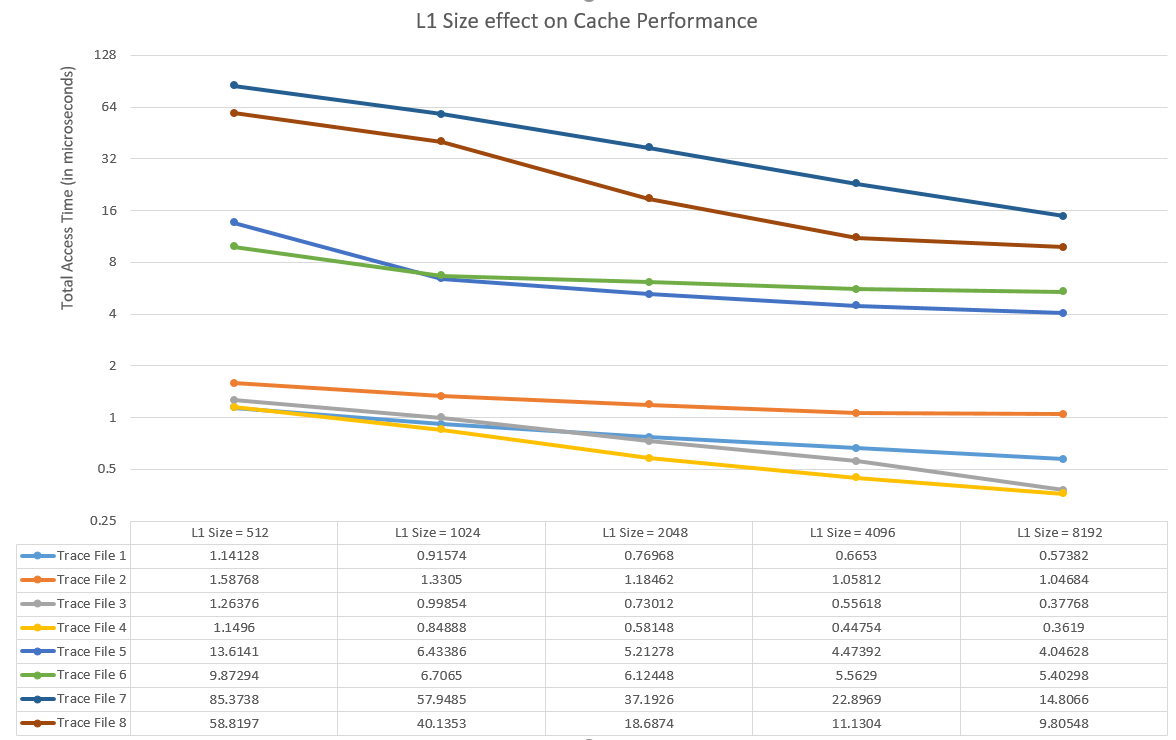
III. Observations

1. Impact of varying BLOCKSIZE on cache access time



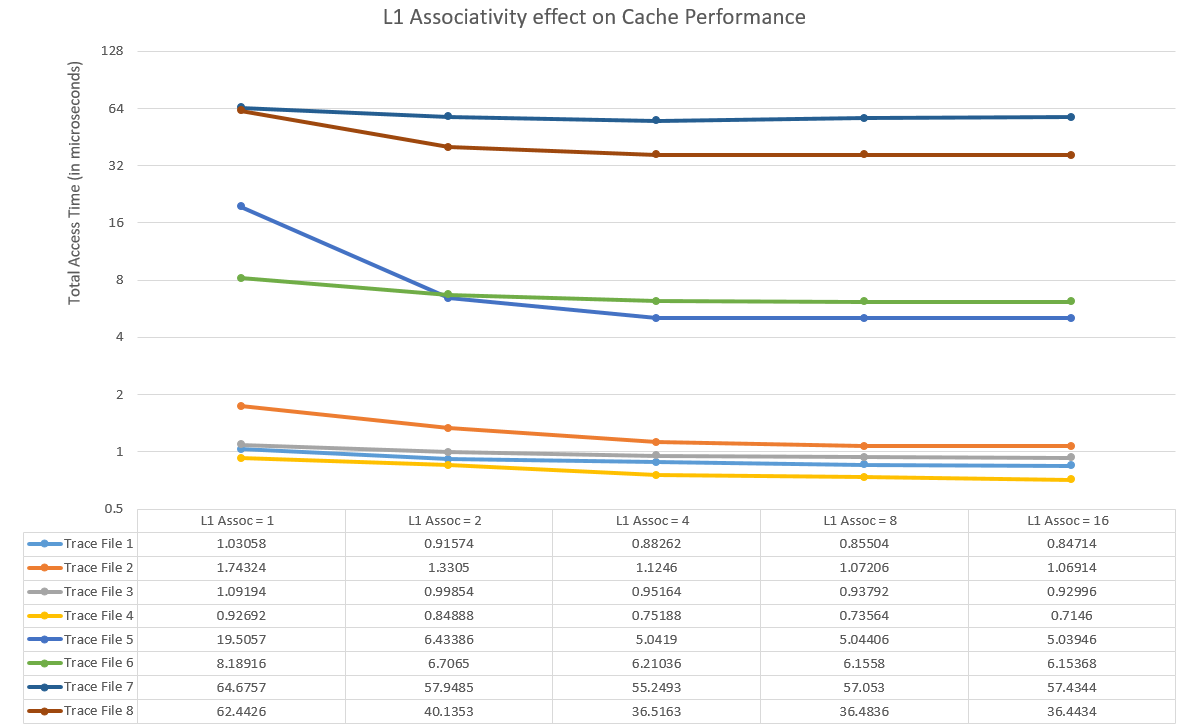
* Increasing block size decreases the number of blocks in cache and reduces compulsory misses.
* However, if block size becomes too large, cache capacity may become a limiting factor.
* As block size increases, cache access time may also increase due to longer transfer times for larger blocks.
* Increasing block size can improve cache hit rate by reducing the number of blocks that must be searched for a given address, but may also increase cache miss rate if there is more data in a block than necessary.
* Smaller block sizes tend to reduce cache miss rate by allowing more fine-grained data placement, but may increase cache overhead due to more frequent tag lookups.

1. Impact of varying L1\_Size on cache access time



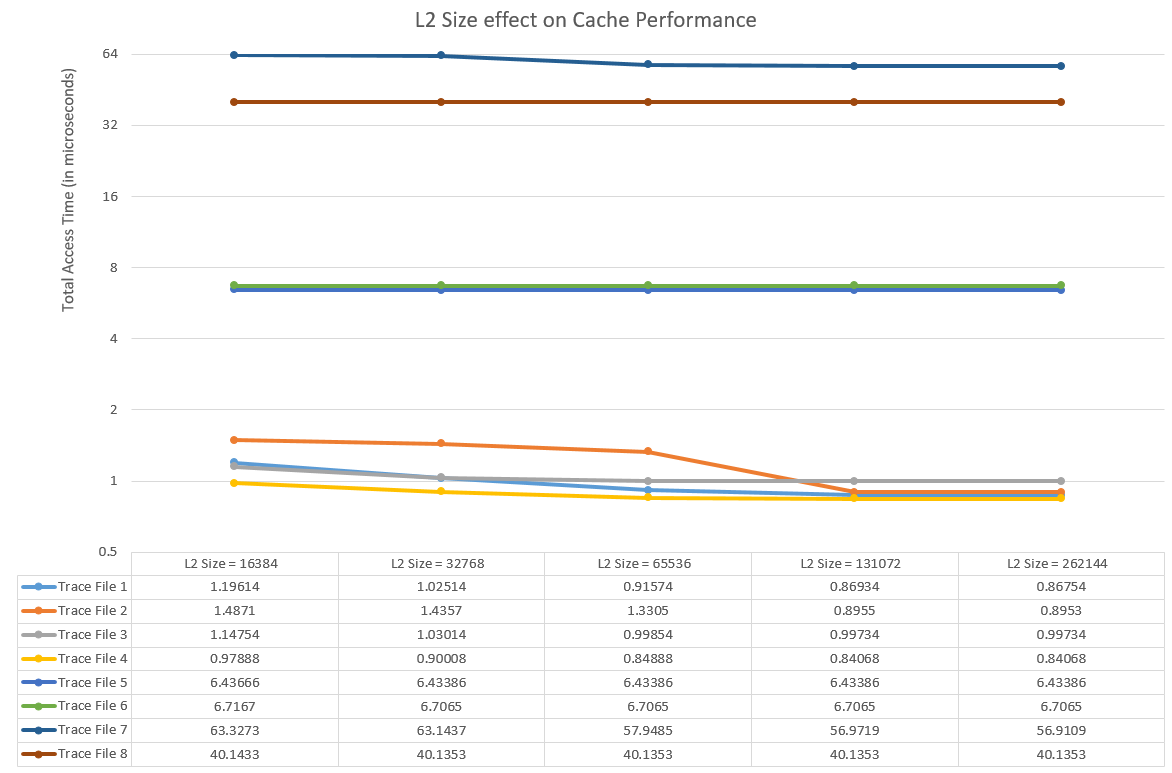
* Increasing L1 cache size reduces miss rates, improving cache access time.
* However, if L1 cache size becomes too large, access time may increase due to longer search times.
* Larger L1 cache sizes tend to improve hit rate and reduce miss rate, but may increase cache access time due to longer search times and tag lookup times.
* Smaller L1 cache sizes tend to have lower hit rates and higher miss rates, but may have faster access times due to smaller search and tag lookup times.
* The optimal L1 size depends on the specific workload and access patterns of the application being run.

1. Impact of varying L1\_Assoc on cache access time



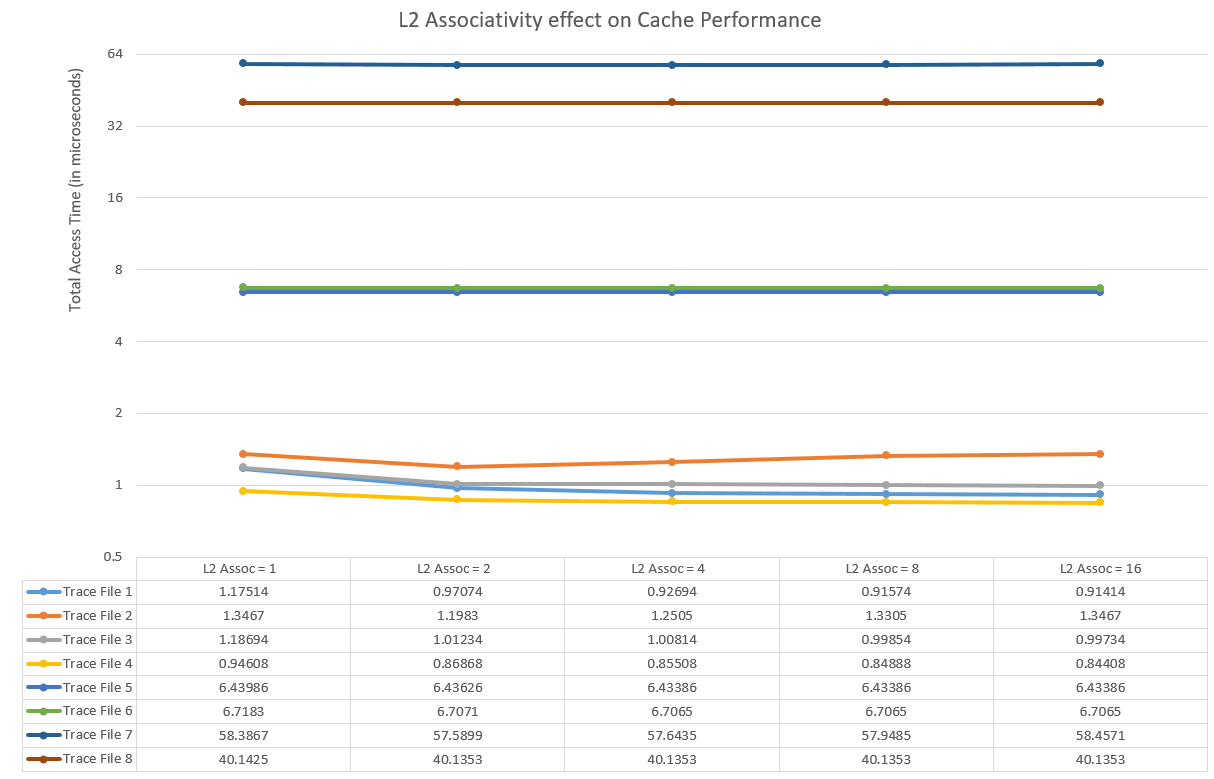
* Increasing L1 associativity reduces conflict misses and improves cache access time.
* However, higher associativity also increases search time.
* Higher L1 associativity tends to improve hit rate by reducing conflict misses, but may also increase cache access time due to longer search and tag lookup times.
* Lower L1 associativity tends to increase conflict misses, but may have faster access times due to shorter search and tag lookup times.

1. Impact of varying L2\_Size on cache access time



* Increasing L2 cache size reduces miss rates, improving cache access time.
* However, if L2 cache size becomes too large, access time may increase due to longer search times.
* Larger L2 cache sizes tend to reduce miss rate by providing a larger secondary cache, but may increase cache access time due to longer search and tag lookup times.
* Smaller L2 cache sizes tend to increase miss rate but may have faster access times due to shorter search and tag lookup times.
* The optimal L2 size depends on the specific workload and access patterns of the application being run.

1. Impact of varying L2\_Assoc on cache access time



* Increasing L2 associativity reduces conflict misses and improves cache access time.
* However, higher associativity also increases search time.
* Higher L2 associativity tends to improve hit rate by reducing conflict misses, but may also increase cache access time due to longer search and tag lookup times.
* Lower L2 associativity tends to increase conflict misses, but may have faster access times due to shorter search and tag lookup times.

IV. References

1. [Computer Organization and Architecture by William Stallings](http://williamstallings.com/COA/COA8e.html)
2. [Cache memory – GeeksforGeeks](https://www.geeksforgeeks.org/cache-memory/)
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4. [Computer Architecture - Carnegie Mellon University](https://www.cs.cmu.edu/~./213/lectures/arch1.pdf)
5. [Cache hierarchy - University of Maryland](https://www.cs.umd.edu/class/sum2003/cmsc311/Notes/Memory/cache.html)