THOMSON COMPONENTS
MOSTEK

ETC2732(Q)-35/45/55

32,768-BIT (4096 x 8) CMOS UV ERASABLE PROM

MEMORY COMPONENTS

The ETC 2732 is a high speed 32K UV erasable and electrically reprogrammable CMOS EPROM ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

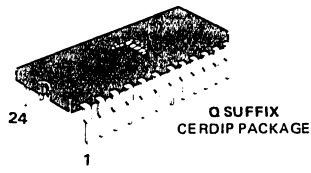
The ETC 2732 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure. This EPROM is fabricated with the reliable, high volume, time proven, P^2 CMOS silicon gate technology.

- CMOS power consumption : 26.25 mW max active power, 0.53 mW max standby power
- 4096 × 8 organization
- Pin compatible to ET 2716, ETC 2716, ET 2732, ET 2764
- Access time down to 350 ns
- Single 5V power supply
- Static - no clocks required
- TTL compatible I/Os during both read and program modes
- Three-state output with OR-tie capability
- Oper. temp. : 0°C, + 70°C ; −20°C, + 70°C (D suffix) ; −25°C, + 70°C (E suffix) ; −40°C, + 85°C (V suffix).

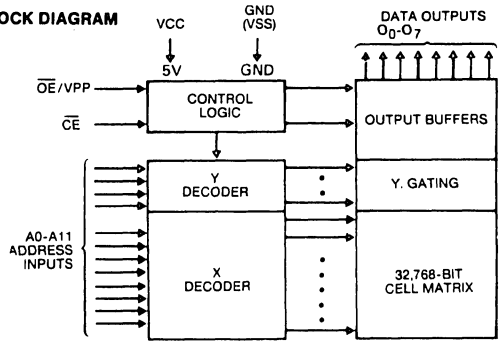
Parameter/Part Number	ETC2732Q-35	ETC2732Q-45	ETC2732Q-55
Access Time (ns)	350	450	500
Active Current (mA at 1 MHz)	5	5	5
Standby Current (mA)	0.1	0.1	0.1

CMOS

(4096 x 8)
32,768 - BIT
UV ERASABLE PROM

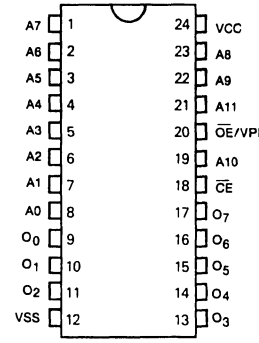


BLOCK DIAGRAM



Mode	Pin Name/Number CE 18	OE/VPP 20	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5V	DOUT
Standby	VIH	Don't Care	5V	Hi-Z
Program	VIL	25V	5V	DIN
Program Verify	VIL	VIL	5V	DOUT
Program Inhibit	VIH	25V	5V	Hi-Z

PIN ASSIGNMENT



PIN NAMES

A0-A11	Address Inputs
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Read RV, Program 25V
V_{CC}	5V
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperature Under Bias	−10°C to + 80°C	Output Voltages with Respect to VSS	VCC + 0.3V to VSS −0.3V
Storage Temperature	−65°C to +125°C	Power Dissipation	1.0W
VPP Supply Voltage with Respect to VSS	26.5V to −0.3V	Lead Temperature (Soldering, 10 seconds)	300°C
Input Voltages with Respect to VSS except VPP (Note 5)	6V to −0.3V		

READ OPERATION (Note 2)

DC OPERATING CHARACTERISTICS TA = 0°C to + 70°C, VCC = 5V ± 5 %, VSS = 0V, (Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
ILI	Input Current	VIN=VCC or GND	–	–	10	μA
ILO	Output Leakage Current	VOUT=VCC or VSS, $\overline{CE}$ = VIH	–	–	10	μA
VIL	Input Low Voltage		−0.1	–	0.8	V
VIH	Input High Voltage	(Note 4)	2.0	–	VCC+1	V
VOL1	Output Low Voltage	IOL=2.1 mA	–	–	0.45	V
VOH1	Output High Voltage	IOH = −400μA	2.4	–	–	V
VOL2	Output Low Voltage	IOL = 0μA	–	–	0.1	V
VOH2	Output High Voltage	IOH = 0μA	VCC−0.1	–	–	V
ICC1	VCC Supply Current Active (TTL Levels)	$\overline{CE}$ = $\overline{OE}$ = VIL Inputs = VIH or VIL Frequency 1 MHz, I/O = 0 mA	–	2	10	mA
ICC2	VCC Supply Current Active (CMOS Levels)	$\overline{CE}$ = $\overline{OE}$ = VIL (Note 4) Inputs=GND or VCC Frequency 1 MHz, I/O = 0 mA	–	1	5	mA
ICCSB1	VCC Supply Current Standby	$\overline{CE}$ = VIH	–	0.1	1	mA
ICCSB2	VCC Supply Current Standby	$\overline{CE}$ = VCC	–	0.01	0.1	mA

AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5V ± 5 %, VSS = 0V, (Unless otherwise specified)

Symbol	Parameter	Conditions	ETC2732Q-35		ETC2732Q-45		ETC2732Q-55		UNIT
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$/PGM=$\overline{OE}$=VIL	–	350	–	450	–	550	ns
t_{CE}	CE to Output Delay	$\overline{OE}$ = VIL	–	350	–	450	–	550	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL	–	150	–	150	–	150	ns
t_{DF}	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL (Note 5)	0	130	0	130	0	130	ns
t_{OH}	Address to Output Hold	$\overline{CE}$/PGM=$\overline{OE}$=VIL	0	–	0	–	0	–	ns

CAPACITANCE (Note 3) (T_A = +25°C, f = 1 MHz)

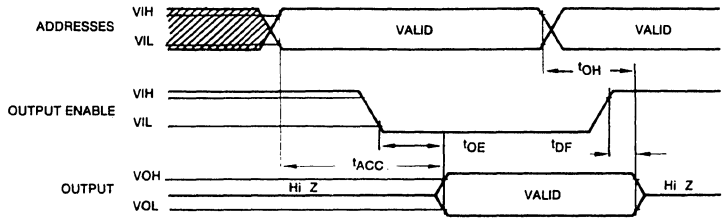
Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	V_{IN} = 0V	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0V	—	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

AC TEST CONDITIONS

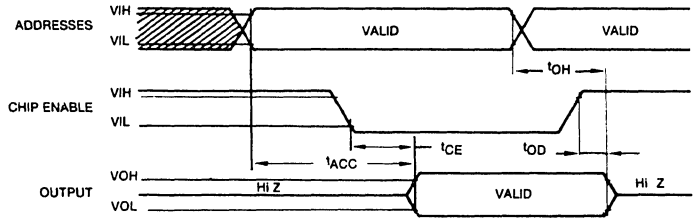
Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	< 20 ns
Output Load	1 TTL Gate and CL=100 PF
Input and Output Timing Reference Levels:	0.8V and 2V

SWITCHING TIME WAVEFORMS

Read Cycle ($\overline{CE}$ = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Note 1 : "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are, not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2 : Typical conditions are for operation at : TA = 25°C, VCC = 5V, VPP = VCC, and VSS=0V.

Note 3 : Capacitance is guaranteed by periodic testing. TA = 25°C, f = 1 MHz.

Note 4 : The inputs (Address, $\overline{OE}$, $\overline{CE}$) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC +0.3V.

Note 5 : The t_{DF} compare level is determined as follows :
High to Hi-Z, the measured V_{OH1} (DC) — 0.10V
Low to Hi-Z, the measured V_{OL1} (DC) + 0.10V

DC PROGRAMMING CHARACTERISTICS (Notes 1 and 2)
TA = +25°C ± 5°C, VCC = 5V ± 5 %, VPP = 25V ± 1V) (Unless otherwise specified)

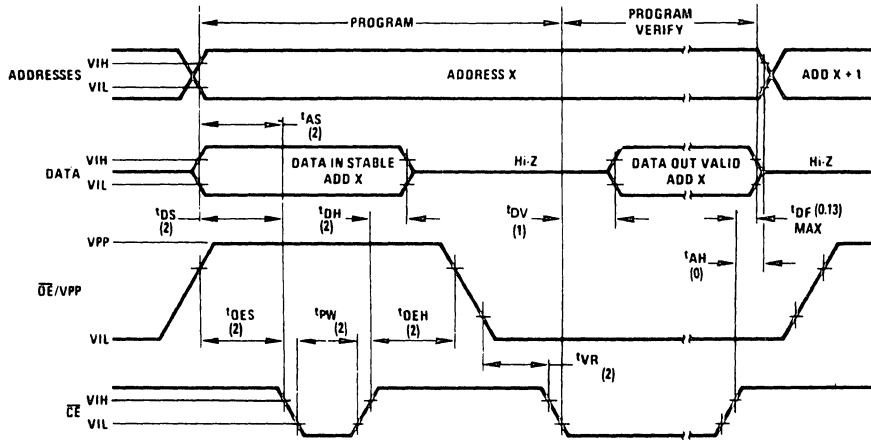
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (All inputs)	$V_{IN} = V_{CC}$ or GND	–	–	10	µA
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA	–	–	0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ µA	2.4	–	–	V
I_{CC}	V_{CC} Supply Current		–	2	10	mA
V_{IL}	Input Low Level (All Inputs)		−0.1	–	0.8	V
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)		2.0	–	$V_{CC}+1$	V
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$	–	–	30	mA

AC PROGRAMMING CHARACTERISTICS (TA = +25°C ± 5°C, VCC = 5V ± 5 %, VPP 25V ± 1V)

Symbol	Parameter	Conditions	Min	Typ	Max	
t_{AS}	Address Set-Up Time		2	–	–	µs
t_{OES}	$\overline{OE}$ Set-Up Time		2	–	–	µs
t_{DS}	Data Set-Up Time		2	–	–	µs
t_{AH}	Address Hold Time		0	–	–	µs
t_{OEH}	$\overline{OE}$ Hold Time		2	–	–	µs
t_{DH}	Data Hold Time		2	–	–	µs
t_{DF}	Chip Enable to Output Float Delay		0	–	130	ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{CE} = V_{IL}$;$\overline{OE} = V_{IL}$	–	–	1	µs
t_{PW}	$\overline{CE}$ Pulse Width During Programming		45	50	55	ms
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50	–	–	ns
t_{VR}	V_{PP} Recovery Time		2	–	–	µs

PROGRAMMING WAVEFORMS

Note : All times shown in parentheses are minimum and in μs unless otherwise specified.
The input timing reference is 0.8V for a V_{IL} and 2V for a V_{IH}.



AC TEST CONDITIONS

V_{CC}	5V ± 5 %
V_{PP}	25V ± 1V
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level Inputs , Outputs	0.8V and 2V

Note 1 : Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. The ETC 2732 must not be inserted into or removed from a board with Vpp at 25 ± 1V to prevent damage to the device.

Note 2 : The maximum allowable voltage which may be applied to the Vpp pin during programming is 26V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across Vpp,Vcc to GND to suppress spurious voltage transients which may damage the device.

FUNCTIONAL DESCRIPTION

DEVICE OPERATION

The five modes of operation of the ETC 2732 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

Read Mode

The ETC 2732 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The ETC 2732 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53mW. The ETC 2732 is placed in the standby mode, by applying a TTL high signal to the $\overline{CE}$ input when in standby mode the outputs are in a high impedance state, independant of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMS are usually used in larger memory arrays, we have provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for.

a)the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION : Exceeding 26.5V on pin 20 (V_{PP}) will damage the ETC 2732.

Initially, and after each erasure, all bits of the ETC 2732 are in the "1" state. Data is introduced by selectively programming "Os" into the desired bit locations. Although only "Os" will be programmed, both "1s" and "Os" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The ETC 2732 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1 µF capacitor be placed across $\overline{OE}/V_{PP}$, and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms active low TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time-either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms.
The ETC 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple ETC 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled ETC 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled.

Program Inhibit

Programming multiple ETC 2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel ETC 2732s may be common. A TTL level program pulse applied to an ETC 2732s $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25 V will program that ETC 2732. A high level $\overline{CE}$ input inhibits the other ETC 2732s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

TABLE I. MODE SELECTION

Mode / Pins	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20	V_{CC} (24)	Outputs (9-11, 13-17)
Read.	V_{IL}	V_{IL}	5	D_{OUT}
Standby	V_{IH}	Don't Care	5	Hi-Z
Program	V_{IL}	V_{PP}	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	5	Hi-Z

ERASURE CHARACTERISTICS

The erasure characteristics of the ETC 2732 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 Å – 4000 Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical ETC 2732 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the ETC 2732 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the ETC 2732 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

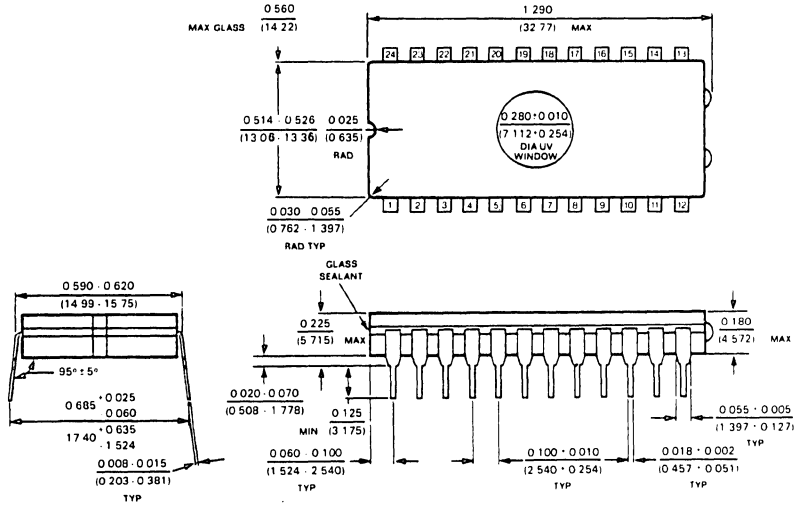
The recommended erasure procedure for the ETC 2732 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm² power rating. The ETC 2732 should be place within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer — the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board traces.

PHYSICAL DIMENSIONS inches (millimeters)



UV Window Cavity Dual-In-Line Package (Q)

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.