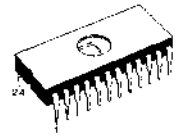
SGS-THOMSON MICROELECTRONICS

ETC2732

32K BIT (4K x 8) CMOS UV ERASABLE PROM

- CMOS POWER CONSUMPTION: 26.25 mW MAX ACTIVE POWER, 0.53 mW MAX STANDBY POWER
- 4096 x 8 ORGANIZZATION
- PIN COMPATIBLE TO M/ET2716, ETC2716, M2732A,
- ACCESS TIME DOWN TO 350 ns
- SINGLE 5V POWER SUPPLY
- STATIC - NO CLOCKS REQUIRED
- TTL COMPATIBLE I/Os DURING BOTH READ AND PROGRAM MODES
- THREE-STATE OUTPUT WITH OR-TIE CAPABILITY
- OPER. TEMP. : 0 to +70°C ; −40 to +85°C (V suffix).



Q
DIP-24
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

DESCRIPTION

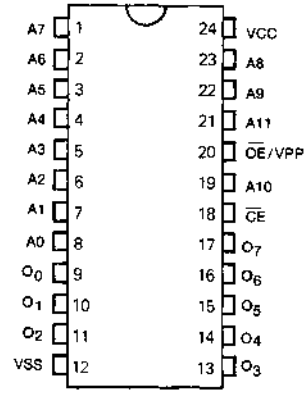
The ETC2732 is a high speed 32K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

The ETC2732 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure. This EPROM is fabricated with the reliable, high volume, time proven, P² CMOS silicon gate technology.

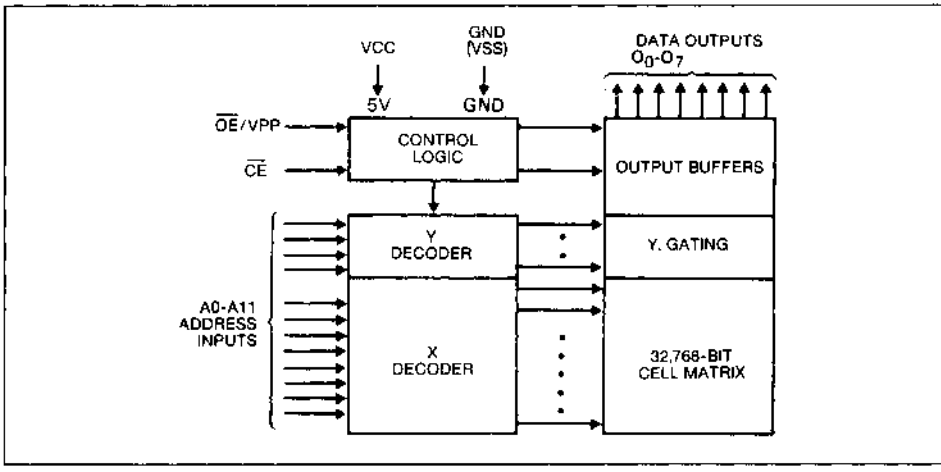
PIN NAMES

A0—A11	ADDRESS INPUTS
O_0—O_7	DATA OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{PP}	READ RV, PROGRAM 25V
V_{CC}	5V
V_{SS}	GROUND

PIN CONNECTIONS



BLOCK DIAGRAM



PIN CONNECTION DURING READ OR PROGRAM

MODE	PIN NAME/NUMBER			
	$\overline{CE}$ 18	$\overline{OE}/V_{PP}$ 20	V_{CC} 24	OUTPUTS 9—11, 13-17
READ	V_{IL}	V_{IL}	5V	D_{OUT}
STANDBY	V_{IH}	Don't Care	5V	Hi-Z
PROGRAM	V_{IL}	25V	5V	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	5V	D_{OUT}
PROGRAM INHIBIT	V_{IH}	25V	5V	Hi-Z

* Symbol in parentheses are proposed JEDEC standard.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{amb}	Temperature Under Bias "V" range	−10 to +80 −50 to +95	°C °C
T_{stg}	Storage Temperature	−65 to +125	°C
V_{PP}	V_{PP} Supply Voltage with Respect to V_{SS}	26.5V to −0.3	V
V_{in}	Input Voltages with Respect to V_{SS} except V_{PP}	6V to −0.3	V
	Output Voltages with Respects to V_{SS}	V_{CC}+0.3V to V_{SS}−0.3V	
P_D	Power Dissipation	1.0	W
	Lead Temperature (Soldering 10 seconds)	300	°C

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are, not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

READ OPERATION

DC CHARACTERISTICS $T_A = 0°C$ to $+ 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, (Unless otherwise specified)[6]

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Units
I_{LI}	Input Current	$V_{IN} = V_{CC}$ or GND	—	—	10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}, $\overline{CE} = V_{IH}$	—	—	10	µA
V_{IL}	Input Low Voltage		−0.1	—	0.8	V
V_{IH}[3]	Input High Voltage		2.0	—	$V_{CC}+1$	V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1$ mA	—	—	0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -400$ µA	2.4	—	—	V
V_{OL2}	Output Low Voltage	$I_{OL} = 0$µA	—	—	0.1	V
V_{OH2}	Output High Voltage	$I_{OH} = 0$µA	$V_{CC}-0.1$	—	—	V
I_{CC1}	V_{CC} Supply Current Active (TTL Levels)	$\overline{CE} = \overline{OE} = V_{IL}$ Input = V_{IH} or V_{IL} Frequency 1MHz, I/O = 0mA	—	2	10	mA
I_{CC2}	V_{CC} Supply Current Active (CMOS Levels)	$\overline{CE} = \overline{OE} = V_{IL}$ (Note 4) Inputs = GND or V_{CC} Frequency 1MHz, I/O = 0mA	—	1	5	mA
I_{CCSB1}	V_{CC} Supply Current Standby	$\overline{CE} = V_{IH}$	—	0.1	1	mA
I_{CCSB2}	V_{CC} Supply Current Standby	$\overline{CE} = V_{CC}$	—	0.01	0.1	mA

AC CHARACTERISTICS $T_A = 0°C$ to C, $V_{CC} = 5V \pm 5\%$ $V_{SS} = 0V$; Unless otherwise specified)[6].

Symbol	Parameter	Test Conditions	ETC2732-3		ETC2732 (-V)		Unit
			Min.	Max.	Min.	Max.	
t_{ACC}	Address to Output Delay	CE/PGM = OE = V_{IL}	—	350	—	450	ns
t_{CE}	CE to Output Delay	$\overline{OE} = V_{IL}$	—	350	—	450	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$/PGM = V_{IL}	—	150	—	150	ns
t_{DF}[4,5]	$\overline{OE}$ or $\overline{CE}$ High to Output Hi-Z	$\overline{CE}$/PGM = V_{IL}	0	130	0	130	ns
t_{OH}	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE} = V_{IL}$	0	—	0	—	ns

CAPACITANCE ($T_A = +25°C$, f = 1 MHz) (Note 2)

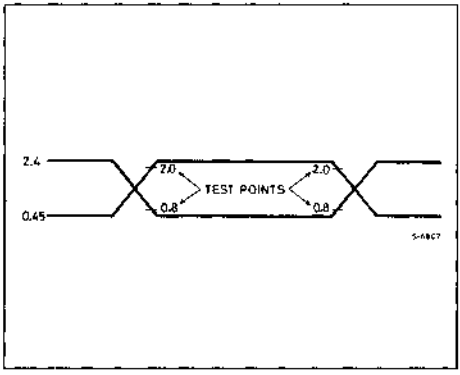
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$		4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$		—	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes 1. Typical conditions are for operation at: TA = 25°C, VCC = VPP = VCC, and VSS = OV.
2. Capacitance is guaranteed by periodic testing. TA = 25°C, f = 1 MHz.
3. The inputs (Address, OE, CE) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC + 0.3 V.
4. The t_{DF} compare level is determined as follows:
High to Hi-Z, the measured V_{OH1} (DC) — 0.10V
Low to Hi-Z, the measured V_{OH1} (DC) + 0.10V
5. T_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ which ever occurs first. This parameter is only sampled, not 100% tested.
6. $T_A = -40°C$ to $+85°C$ for "V" range

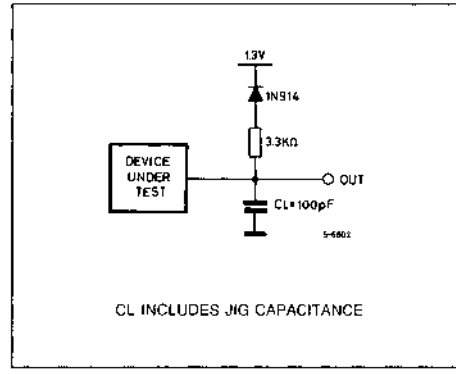
AC TEST CONDITIONS

Output Load:	1 TTL gate and CL = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input pulse levels:	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs, Outputs	0.8V and 2V

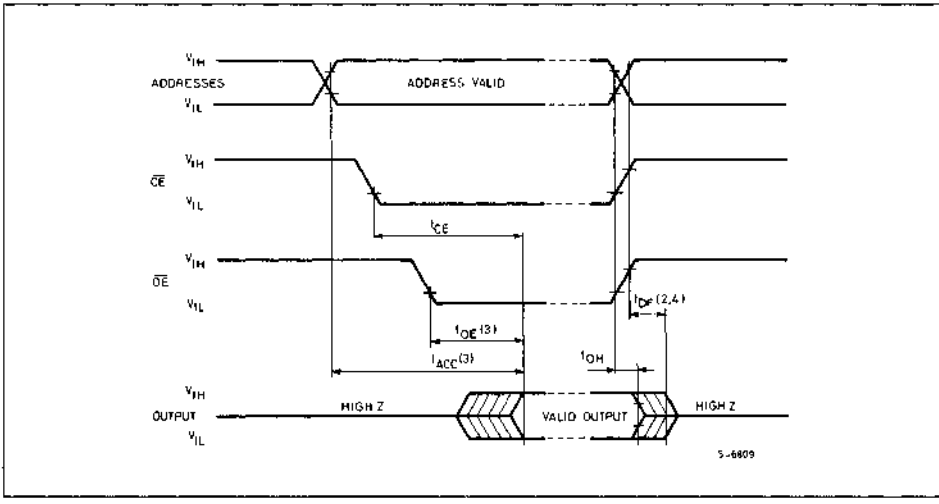
AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT



AC WAVEFORMS



Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The five modes of operation of the ETC 2732 are listed in the Operating Modes table. A single 5 V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}$/Vpp during programming. In the program mode the $\overline{OE}$/Vpp input is pulsed from a TTL level to 25V.

READ MODE

The ETC2732 has two control functions, both of wich must be logically active in order to obtain data at the ouputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The ETC2732 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53mW. The ETC 2732 is placed in the standby mode, by applying a TTL high signal to the $\overline{CE}$ input when in standby mode the outputs are in a high impedance state, independant of the $\overline{OE}$ input.

OUTPUT OR-TYING

Because EPROMS are usually used in larger memory arrays, we have provided a 2-line control function that accomodates this use of multiple memory connection. The 2-line control function allows for.

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

PROGRAMMING

CAUTION: Exceeding 26.5V on pin 20 (V_{PP}) will damage the ETC2732.

Initially, and after each erasure, all bits of the ETC 2732 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The ETC2732 is in the programming mode when the $\overline{OE}$/Vpp input is at 25V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}$/Vpp, and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms active low TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time-either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The ETC 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple ETC 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled ETC 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled.

OPERATING MODES

MODE \ PIN	$\overline{CE}$ (18)	$\overline{OE}$/V_{PP} (20)	V_{CC} (24)	OUTPUTS (9—11, 13-17)
READ	V_{IL}	V_{IL}	5	D_{OUT}
STANDBY	V_{IH}	Don't Care	5	Hi-Z
PROGRAM	V_{IL}	V_{PP}	5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	5	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	5	Hi-Z

PROGRAM INHIBIT

Programming multiple ETC2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel ETC2732s may be common. A TTL level program pulse applied to an ETC2732s $\overline{CE}$ input with $\overline{OE}$/Vpp at 25 V will program that ETC2732. A high level $\overline{CE}$ input inhibits the other ETC2732s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}$/Vpp $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

ERASURE CHARACTERISTICS

The erasure characteristics of the ETC2732 are such that erasure begins to occur when exposed to light with wavelenghts shorter than approximately 4000 Angstroms (A). It should be noted that sunlight and certain types of fluorescent lamps have wavelenghts in the 3000 A - 4000 A range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical ETC 2732 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the ETC2732 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the ETC2732 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the ETC 2732 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (A). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The ETC2732 should be place within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

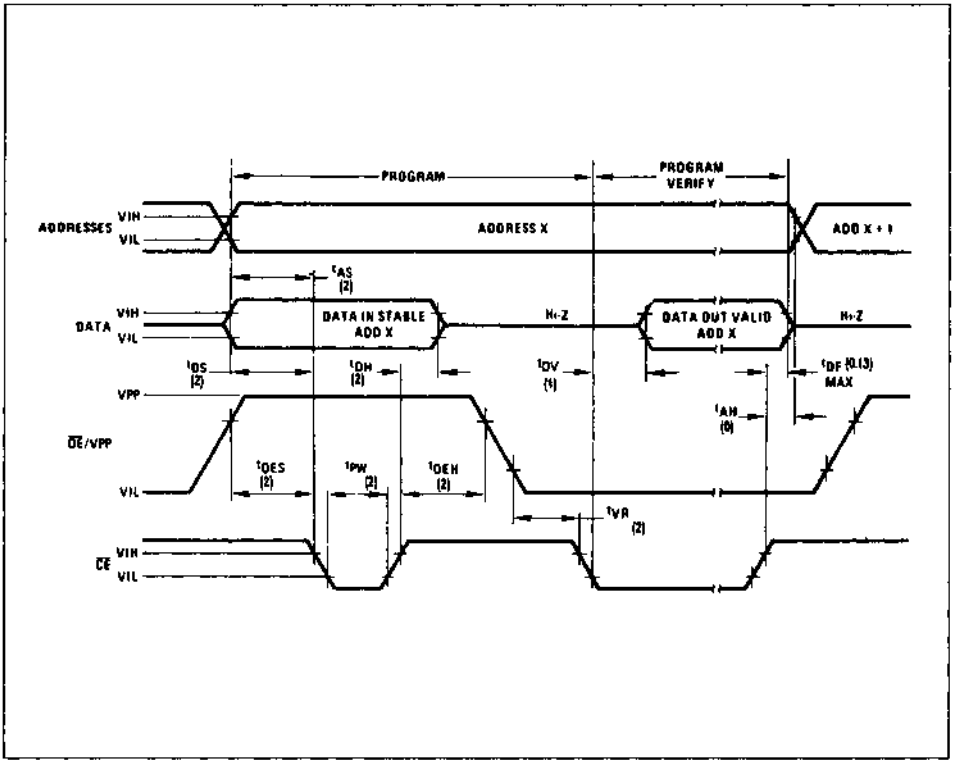
SYSTEM CONSIDERATION

The power swhitching characterics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer - the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltgage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1μF Ceramic capacitor be used an every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7μF bulk electolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

PROGRAMMING WAVEFORMS

Note: All times shown in parentheses are minimum and in μs unless otherwise specified.
The input timing reference is 0.8V for a V_{IL} and 2V for a V_{IH}.

TIMING DIAGRAM



Notes: 1. V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. The ETC 2732 must not be inserted into or removed from a board with Vpp at 25 ± 1V to prevent damage to the device.
2. The maximum allowable voltage with may be applied to the Vpp pin during programming is 26V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

PROGRAMMING OPERATION (1,2)

DC OPERATING CHARACTERISTICS $T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$; Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All inputs)	$V_{IN} = V_{CC}$ or GND	—	—	10	μA
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA	—	—	0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ μA	2.4	—	—	V
I_{CC}	V_{CC} Supply Current		—	2	10	mA
V_{IL}	Input Low Level (All Inputs)		−0.1	—	0.8	V
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)		2.0	—	$V_{CC}+1$	V
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$	—	—	30	mA

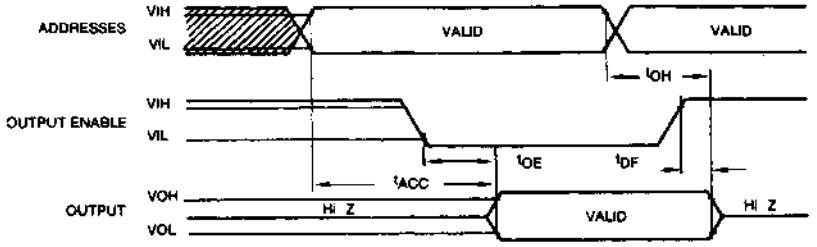
AC CHARACTERISTICS ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, V_{PP} 25V ± 1V).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{AS}	Address Set-Up Time		2	—	—	μs
t_{OES}	$\overline{OE}$ Set-Up Time		2	—	—	μs
t_{DS}	Data Set-Up Time		2	—	—	μs
t_{AH}	Address Hold Time		0	—	—	μs
t_{OEH}	$\overline{OE}$ Hold Time		2	—	—	μs
t_{DH}	Data Hold Time		2	—	—	μs
t_{DF}	Chip Enable to Output Float Delay		0	—	130	ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{CE} = V_{IL}$; $\overline{OE} = V_{IL}$	—	—	1	μs
t_{PW}	$\overline{CE}$ Pulse Width During Programming		45	50	55	ms
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50	—	—	ns
t_{VR}	V_{PP} Recovery Time		2	—	—	μs

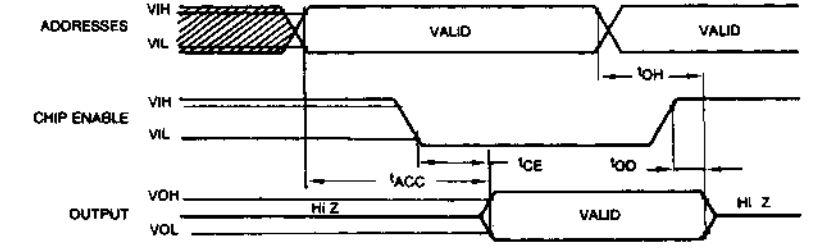
Notes 1. V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. The ETC 2732 must not be inserted into or removed from a board with Vpp at 25 ± 1V to prevent damage to the device.
2. The maximum allowable voltage which may be applied to the Vpp pin during programming is 26V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across Vpp, Vcc to GND to suppress spurious voltage transients which may damage the device.

SWITCHING TIME WAVEFORMS

Read Cycle ($\overline{CE}$ = VIL)



Read Cycle ($\overline{OE}$ = VIL)

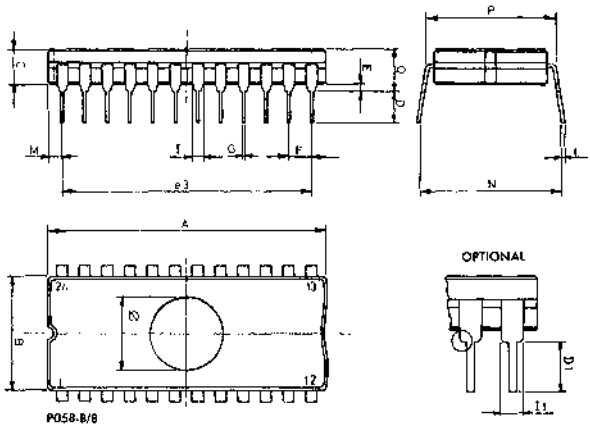


ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ETC2732Q-3	350 ns	5V ± 5%	0 to +70°C	DIP-24
ETC2732Q	450 ns	5V ± 5%	0 to +70°C	DIP-24
ETC2732Q-45-V	450 ns	5V ± 5%	−40 to +85°C	DIP-24

PACKAGE MECHANICAL DATA

24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.30			1.272
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1(1)	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		27.94			1.100	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1(1)	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

Note: 1. Optional see drawing