TMS 2508 JL
FAST 1024-WORD BY 8-BIT
ERASABLE PROGRAMMABLE READ-ONLY MEMORY

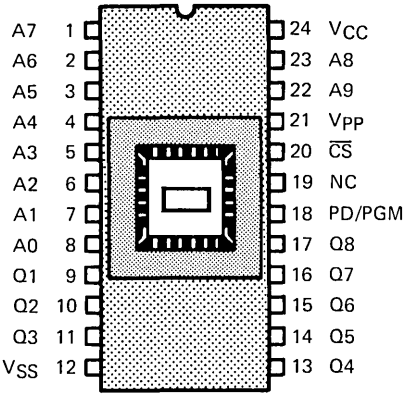
DECEMBER 1979

- **Organization . . . 1K × 8**
- **Single +5 V Power Supply**
- **Pin Compatible with Existing ROMs and EPROMs (8 K, 16 K, and 64 K)**
- **JEDEC Standard Pinouts**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Fast . . . Down to 250 ns**
- **2 Performance Ranges**

	Max Access/Min Cycle
TMS 2508-25	250 ns
TMS 2508-30	300 ns

- **8-Bit Output for Use in Microprocessor-Based Systems**
- **N-Channel Silicon-Gate Technology**
- **3-State Output Buffers**
- **Low Power**
  - **— Active . . . 250 mW Typical**
  - **— Standby . . . 50 mW Typical**
- **Guaranteed dc Noise Immunity with Standard TTL Loads**
- **No Pull-Up Resistors Required**

TMS 2508
24-PIN CERPAK
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A(N)	Address Inputs
$\overline{CS}$	Chip Select
PD/PGM	Power Down/Program
NC	No Internal Connection
Q(N)	Input/Output
V_{CC}	+5 V Power Supply
V_{PP}	+25 V Power Supply
V_{SS}	0 V Ground

description

The TMS 2508 is a high-speed 8192-bit, ultraviolet light erasable, electrically programmable read-only memory. It is fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and Bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for OR tying multiple devices on a common bus.

Both versions operate from a single +5-V supply (in the read mode), making them ideal for use in microprocessor systems. One other (+25 V) supply is needed for programming but all programming signals are TTL level, requiring a single 50-ms pulse. For programming outside the system, existing 5-V EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits for the TMS 2508 is 50 seconds.

Devices are offered in a 600-mil (15.2-mm) cerpak (JL suffix) package rated for operation from 0°C to 70°C.

operation

FUNCTION	PIN	MODE					
		READ	OUTPUT DISABLE	POWER DOWN	START PROGRAMMING	INHIBIT PROGRAMMING	PROGRAM VERIFICATION
PD/PGM	18	V_{IL}	Don't Care	V_{IH}	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IL}
$\overline{CS}$	20	V_{IL}	V_{IH}	Don't Care	V_{IH}	V_{IH}	V_{IL}
V_{PP}	21	+5 V	+5 V	+5 V	+25 V	+25 V	+25 V (or +5 V)
V_{CC}	24	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V
Q	9-11, 13-17	Q	HI-Z	HI-Z	D	HI-Z	Q

read/output disable

When the outputs of two or more TMS 2508's are commoned on the same bus, the output of any one device in the circuit can be read with no interference from the competing outputs of the others. The TMS 2508 whose output is to be read should have a low-level TTL signal applied to the $\overline{CS}$ and PD/PGM pins. All other 2508's in the circuit should have their outputs disabled by applying a high-level signal to at least one of these same pins. (PD/PGM can be left low, but it may be advantageous to power down the device during output disable). Output data is accessed at pins Q1 to Q8. Data can be accessed in 250 or 300 ns = $t_{a(A)}$. (Access time from $\overline{CS}$ is 125 or 150 ns = $t_{a(CS)}$, once the addresses are stable).

power down

Active power dissipation can be cut by 70% by applying a high TTL signal to the PD/PGM pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the TMS 2508 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (= UV intensity X exposure time) is fifteen watt-seconds per square centimeter. A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in about 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state.

start programming

After erasure, logic lows are programmed into the desired locations. A low can be erased only by ultraviolet light. The programming mode is achieved when Vpp is 25 V and $\overline{CS}$ is at V_{IH}. Data is presented in parallel (8 bits) on pins Q1 to Q8. Once addresses and data are stable, a 50 millisecond TTL high-level Pulse should be applied to the PD/PGM pin for each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. More then one TMS 2508 can be programmed when the devices are connected in parallel.

inhibit programming

When two or more TMS 2508's are connected in parallel, data can be programmed into all devices or only chosen devices. Devices not intended to be programmed (i.e., inhibited) should have a low level applied to the PD/PGM pin and a high-level applied to the $\overline{CS}$ pin.

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program verification

A verify is done to see if the device was programmed correctly. It can be done on each location immediately after that location is programmed and can be done at any time. To do a verify V_{PP} may be kept at +25 V.

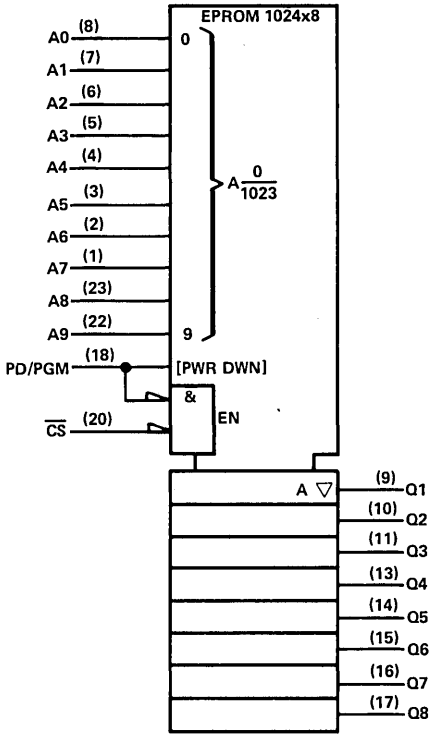
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 6 V
Supply voltage, V_{PP} (see Note 1)	−0.3 to 28 V
All input voltages (see Note 1)	−0.3 to 6 V
Output voltage (operating with respect to V_{SS})	−0.3 to 6 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{SS} (substrate).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}		V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		V_{CC}+1	V
Low-level input voltage, V_{IL}	−0.1		0.8	V
Read cycle time, $t_{c(rd)}$ For TMS 2508-25	250			ns
Read cycle time, $t_{c(rd)}$ For TMS 2508-30	300			ns
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{CC} or V_{PP} is applied so that the device is not damaged.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 25 V (± 1V).

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage*	I_{OH} = −400 μA	2.4			V
V_{OL}	Low Level output voltage*	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 5.25V			10	μA
I_O	Output current (leakage)	V_O = 5.25V			10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25, PD/PGM = V_{IL}			6	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/PGM = V_{IH}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/PGM = V_{IH}		10	25	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{CS}$ = PD/PGM = V_{IL}		50	85	mA

†Typical values are at T_A = 25°C and nominal voltages.
*AC timing measurements made with 50% pattern and at 90% points.

capacitance over recommended supply voltage and operating free-air temperature range f = 1 MHz

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

†All typical values are T_A = 25°C and nominal voltage.

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switching characteristics over full ranges of recommended operating conditions (see note 4)

PARAMETER		TEST CONDITIONS (SEE NOTE 4)	TMS 2508-25			TMS 2508-30			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leq$ 20 ns, $t_f \leq$ 20 ns		180	250		215	300	ns
$t_{a(CS)}$	Access time from chip select				125			150	ns
t_{PVX}	Output not valid from address change		0			0			ns
t_{PXZ}	Output disable time from chip deselect during read only		0		100	0		100	ns
t_{PXZ}	Output disable time from chip deselect during program and program verify				125			150	ns
t_{PXZ}	Output disable time from PD/PGM during standby		0		100	0		100	ns
$t_{a(PD)}$	Access time from power down				250			300	ns

† All typical values are at T_A = 25°C and nominal voltages.

NOTE 4. For all switching characteristics and timing measurements, input pulse levels are 0.8 V to 2.0 V and V_{PP} = 25 V ± 1 V during programming.
All AC and DC measurements are made at 10% and 90% points with a 50% pattern.

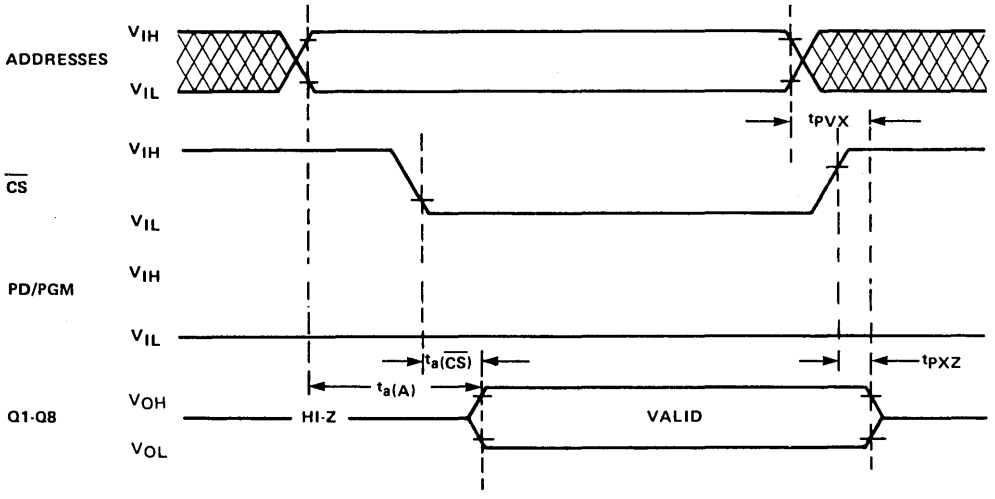
recommended timing requirements for programming T_A = 25°C (see Note 4)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	45	50	55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(CS)}$	Chip-select setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from Vpp	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(CS)}$	Chip-select hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs

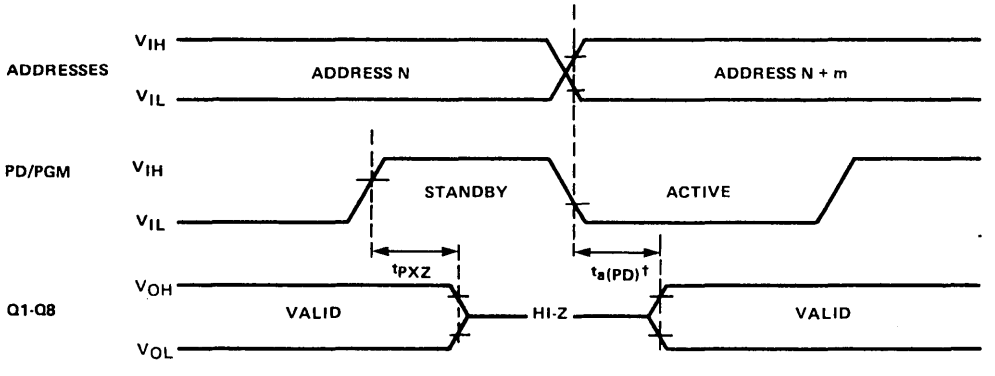
†Typical values are at nominal voltages.

NOTE 4. For all switching characteristics and timing measurements, input pulse levels are 0.8 V to 2.0 V and V_{PP} = 25 V ± 1 V during programming.
All AC and DC measurements are made at 10% and 90% points with a 50% pattern.

read cycle timing



standby mode



NOTE: $\overline{CS}$ must be in low state during Active Mode, "Don't Care" otherwise.
†$t_{a(PD)}$ referenced to PD/PGM or the address, whichever occurs last.

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program cycle timing