Am27C49

65,536-Bit (8192x8) High-Performance CMOS PROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

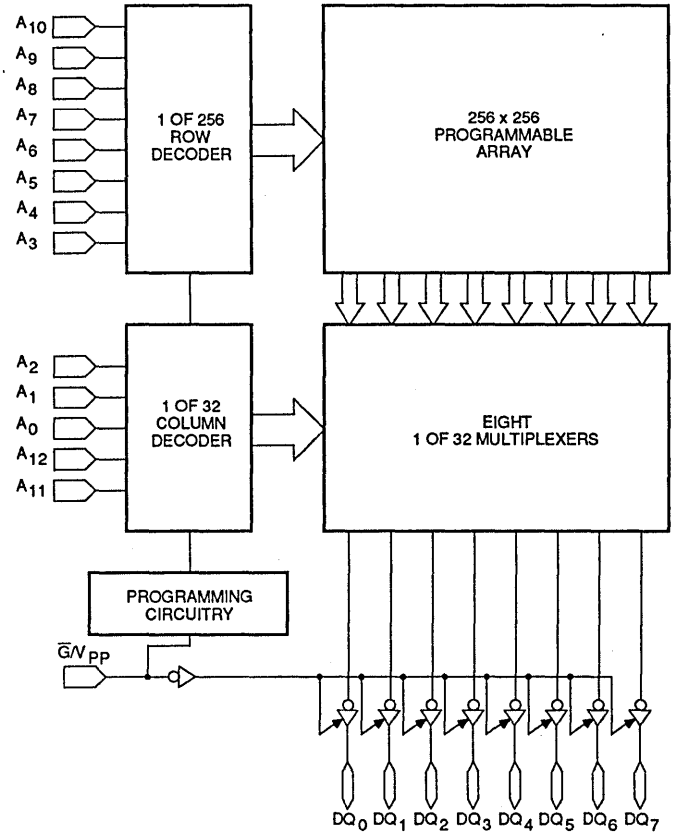
- **High-speed (35 ns)/Low-Power (90 mA) CMOS EPROM Technology**
- **Direct plug-in replacement for Bipolar PROMs — JEDEC-approved pinout**
- **5-Volt ±10% power supplies for both Commercial and Military**
- **UV-erasable and reprogrammable provides exceptionally high programming yields (Typ. > 99.9%)**
- **ESD Immunity > 2000 V**

GENERAL DESCRIPTION

The Am27C49 (8192 words by 8 bits) is a high-speed CMOS programmable read-only memory (PROM).

This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls. This device utilizes proven floating-gate EPROM technology to ensure high reliability, ease of programming, and exceptionally high programming yields.

BLOCK DIAGRAM



09890A-1

Publication # 09890 Rev. B Amendment /0
Issue Date: January 1989

PRODUCT SELECTOR GUIDE

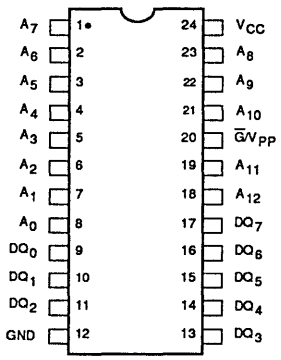
Part Number	Am27C49-35	Am27C49-45	Am27C49-55
Address Access Time	35 ns	45 ns	55 ns
Operating Range	COM'L	COM'L/MIL*	COM'L/MIL*

*** Advance Information—Military Products Only.**

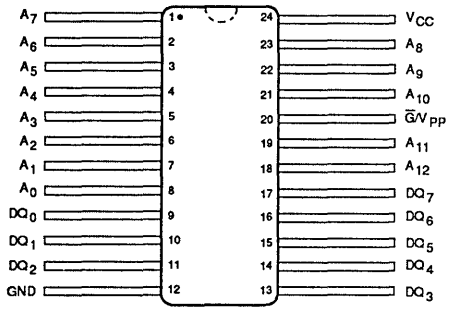
CONNECTION DIAGRAMS

Top View

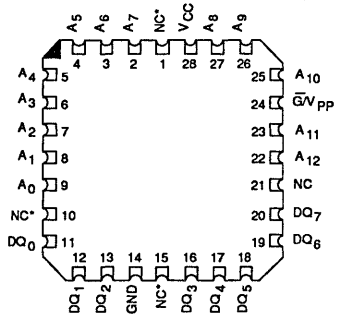
DIPs **



Flatpack



LCC ***



09890A-2

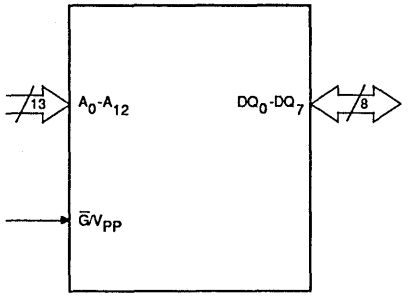
***NC = No Connection**

Note: Pin 1 is marked for orientation.

** Also available in a 24-Pin ceramic windowed DIP. Pinout identical to DIPs.

*** Also available in a 28-Pin ceramic windowed LCC. Pinout identical to LCC.

LOGIC SYMBOL



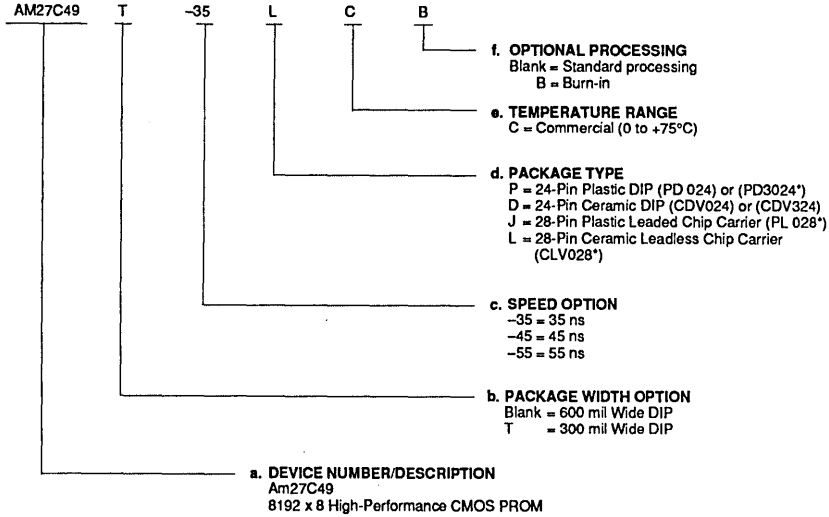
09890A-3

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Package Width Option
c. Speed Option
d. Package Type
e. Temperature Range
f. Optional Processing



* Product version in Development, contact HPP Product Marketing.

Valid Combinations	
AM27C49-35	PC, PCB, DC, DCB, LC, LCB JC, JCB
AM27C49-45	
AM27C49-55	
AM27C49T-35	PC, PCB, DC, DCB
AM27C49T-45	
AM27C49T-55	

Valid Combinations

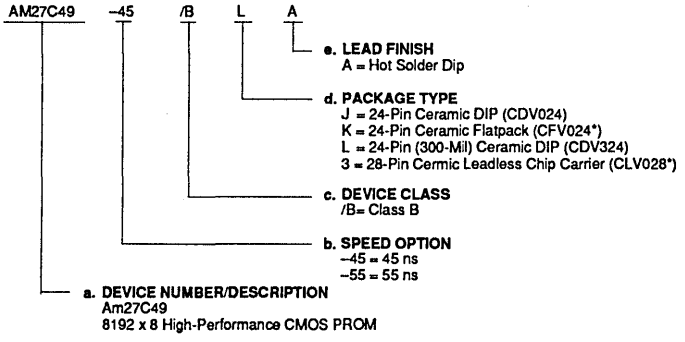
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27C49-45	/BJA, /BLA,
AM27C49-55	/BKA, /B3A

*Preliminary; Package in Development.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

5

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

A_0-A_{12} Address Lines (Inputs)
The 13-bit field presented at the address inputs selects one of 8192 memory locations to be read from.

DQ_0-DQ_7 Data Port (Input/Outputs; Three State)
The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which, when disabled, are in a floating or high-impedance state. These pins provide the data input for programming the memory array.

$\overline{G}/V_{PP}$ $\overline{\text{Output Enable}}$/Programming Power
Provides direct control of the DQ output three-state buffers. When raised to a voltage > 12.0 V, this pin provides the programming power to program the memory array.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65 to +150°C
Ambient Temperature with Power Applied .... –55 to +125°C
Supply Voltage ..... –0.5 V to +7.0 V
DC Voltage Applied to Outputs in
High-Impedance State ..... –0.5 V to +7.0 V
DC Programming Voltage (V_{PP}) ..... 14 V
DC Input Voltage ..... –0.5 V to +7.0 V
Electrostatic Discharge Protection
(per MIL-STD-883 Method 3015.2) ..... > 2000 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) Devices*
Case Temperature (T_C) ..... -55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

* *Military Product 100% tested at T_C = +25°C, +125°C, and –55°C.*

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 1)			0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{CL}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		–1.2		V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V			10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.0 V			–10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max. V_{OUT} = 0.0 V (Note 2)		–20	–90	mA
I_{CEX}	Output Leakage Current	V_{CC} = Max., $V_{\overline{G}}$ = 2.4 V	V_{OUT} = 5.5 V		40	µA
			V_{OUT} = 0.4 V		–40	µA
I_{CC}	Operating Supply Current	V_{CC} = Max. (Note 3)	All Inputs = V_{IH}		90	mA
			All Inputs = V_{IL}			

Notes:
1. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
3. Operating I_{CC} is measured with all inputs except $\overline{G}$ switching between V_{IL} and V_{IH} at a timing interval equal to TAVDQV. The outputs are disabled via $\overline{G}$ held at 3.0 V.

Capacitance*

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C_{IN}	Input Capacitance ($\overline{G}/V_{PP}$)	V_{CC} = 5.0 V, T_A = 25°C	15	pF
	Input Capacitance (All Others)		5	
C_{OUT}	Output Capacitance	V_{IN}/V_{OUT} = 2.0 V @ f = 1 MHz	8	pF

*These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*)

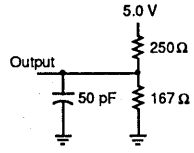
No.	Parameter Symbol	Parameter Description	Am27C49						Unit
			-35		-45		-55		
			COM'L Only		COM'L/MIL		COM'L/MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVDQV	Address Valid to Output Valid Access Time		35		45		55	ns
2	TGHDQZ	Delay from Output Enable HIGH to Output High Impedance		20		25		30	ns
3	TGLDQV	Delay from Output Enable LOW to Output Valid		20		25		30	ns

See Switching Test Circuits.

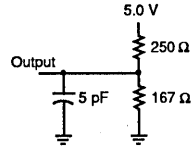
Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in diagram A.
2. TGHDQZ is measured at steady-state HIGH output voltage –0.5 V and steady-state LOW output voltage +0.5 V output levels using the test load in diagram B.

* Subgroups 7 and 8 apply to functional tests.

SWITCHING TEST CIRCUITS



A. Output Load for all AC tests except TGVDQZ



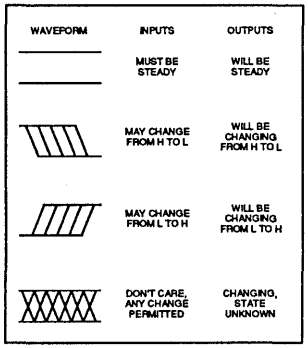
B. Output Load for TGVDQZ

09890A-4

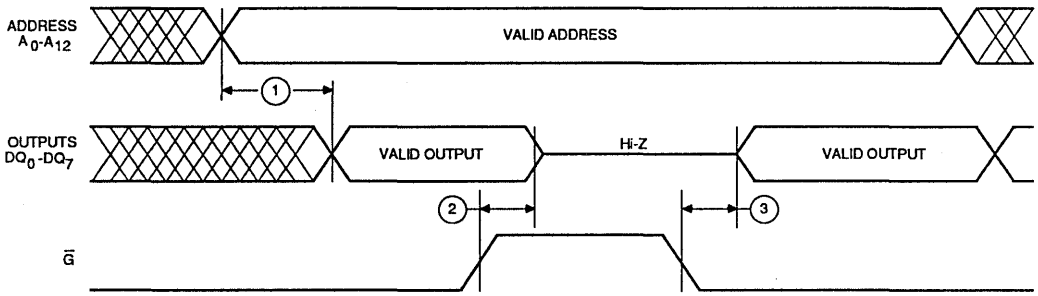
Notes: 1. All device test loads should be located within 2" of device output pin.
2. Load capacitance includes all stray and fixture capacitance.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



KS000010



09890A-5

5

Am27C49 CMOS PROM PROGRAMMING PROCEDURE

Programming Technique

Advanced Micro Devices' high-performance CMOS PROM circuits have been designed to use a programmng algorithm which minimizes the requirements on the programmer, yet allows the circuit to be programmed quickly and reliably. Specifically, the following sequence of events must take place:

1) V_{CC} power is applied to the device;
2) The device outputs are disabled;
3) The appropriate address is selected;
4) The appropriate byte-wide pattern is applied to all outputs;
5) The $\overline{G}/V_{PP}$ pin is pulsed to 13.5 V for 1 ms;
6) The device is enabled and the byte sensed to verify that correct programming has occurred.
7) In the event that the data does not verify, the sequence of 4 through 6 could be repeated up to 25 times;
8) At the conclusion of initial programming, the sequence of 4 and 5 should be repeated for overprogramming using a V_{CC} = 5.0 V, and $\overline{G}/V_{PP}$ pulse width equal to twice the sum of initial programming pulse times;
9) The sequence of 2 through 6 must be repeated for each address to be programmed;
10) At the conclusion of programming, the device should be verified for correct data at all addresses with two V_{CC} supply voltages (V_{CC} = 6.0 and V_{CC} = 4.2 V).

Notes on Programming

1) The unprogrammed or erased state of all enabled outputs is HIGH.
2) All delays between edges are specified from the completion of the first edge to the beginning of the second edge; i.e., not the midpoints (10% or 90% of specified waveform).
3) During t_V, the output may be switched to appropriate loads for proper verification of specified V_{OL} and V_{OH} levels.
4) Due to the potential for fast voltage transitions of the outputs, it is advisable to provide low-impedance connections to the device's V_{CC} and ground pins and to ensure adequate decoupling at the device pins.

Erasure Characteristics

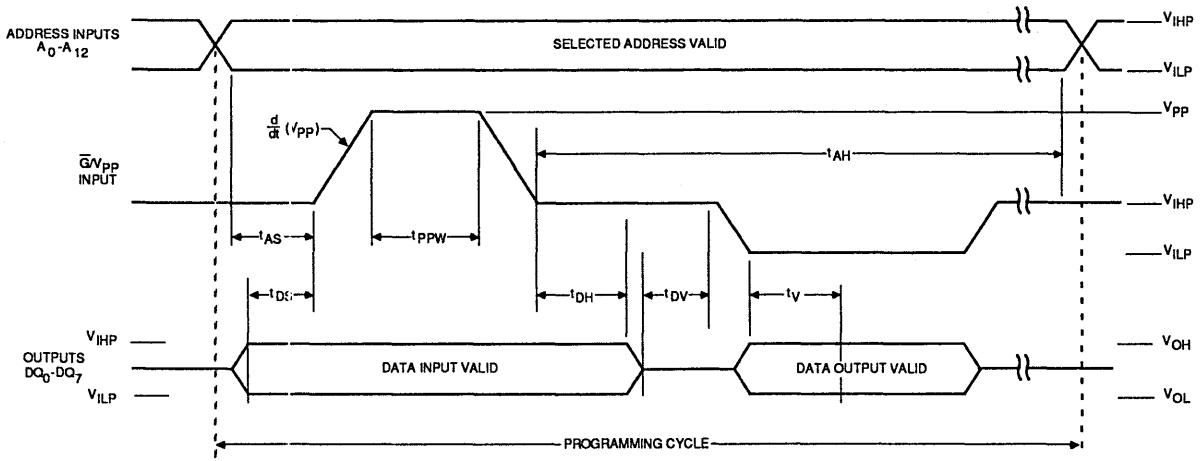
In order to fully erase all memory locations, it is necessary to expose the memory array to an ultraviolet light source having a wavelength of 2537 Angstroms. The minimum recommended dose (UV intensity times exposure time) is 15 Wsec/cm². For a UV lamp with a 12 mW/cm² power rating, the exposure time would be approximately 30 minutes. The device should be located within 1 inch of the source in direct line.

It should be noted that erasure may begin with exposure to light having wavelengths less than 4000 Angstroms. To prevent exposure to sunlight or flourescent lighting from resulting in partial erasure, an opaque label should be afixed over the window after programming.

PROGRAMMING PARAMETERS (T_A = 25°C ±5°C)

Parameter Symbol	Parameter Description		Min.	Max.	Unit
V_{CCP}	Power Supply during Programming	Initial Programming	5.75	6.25	V
		Over-Programming	4.75	5.25	
I_{CCP}	V_{CC} Supply Current during Programming			90	mA
V_{PP}	Programming Voltage		13	14	V
I_{PP}	V_{PP} Supply Current during Programming			30	mA
V_{IHP}	Input HIGH Level during Programming and Verify		2.4	5.5	V
V_{ILP}	Input LOW Level during Programming and Verify		0	0.45	V
V_{OL}	Output LOW Voltage during Verify			0.45	V
V_{OH}	Output HIGH Voltage during Verify		2.40		V
dV_{PP}/dt	Rate of $\overline{G}/V_{PP}$ Voltage Change (Rise and Fall Times)		5	10	V/µs
t_{PPW}	V_{PP} Programming Pulse Width	Initial Programming Pulse	0.95	1.05	ms
t_{AS}	Address Valid to V_{PP} (HIGH) Setup Time		1.0		µs
t_{AH}	V_{PP} (LOW) to Address Change Hold Time		1.0		µs
t_{DS}	Data Valid to V_{PP} (HIGH) Setup Time		1.0		µs
t_{DH}	V_{PP} (LOW) to Data Change Hold Time		1.0		µs
t_{DV}	Delay from Data to Output Enable (LOW) for Verification		1.0		µs
t_V	Delay from Output Enable (LOW) to Verification Strobe		100		ns

PROGRAMMING WAVEFORMS



09890A-6

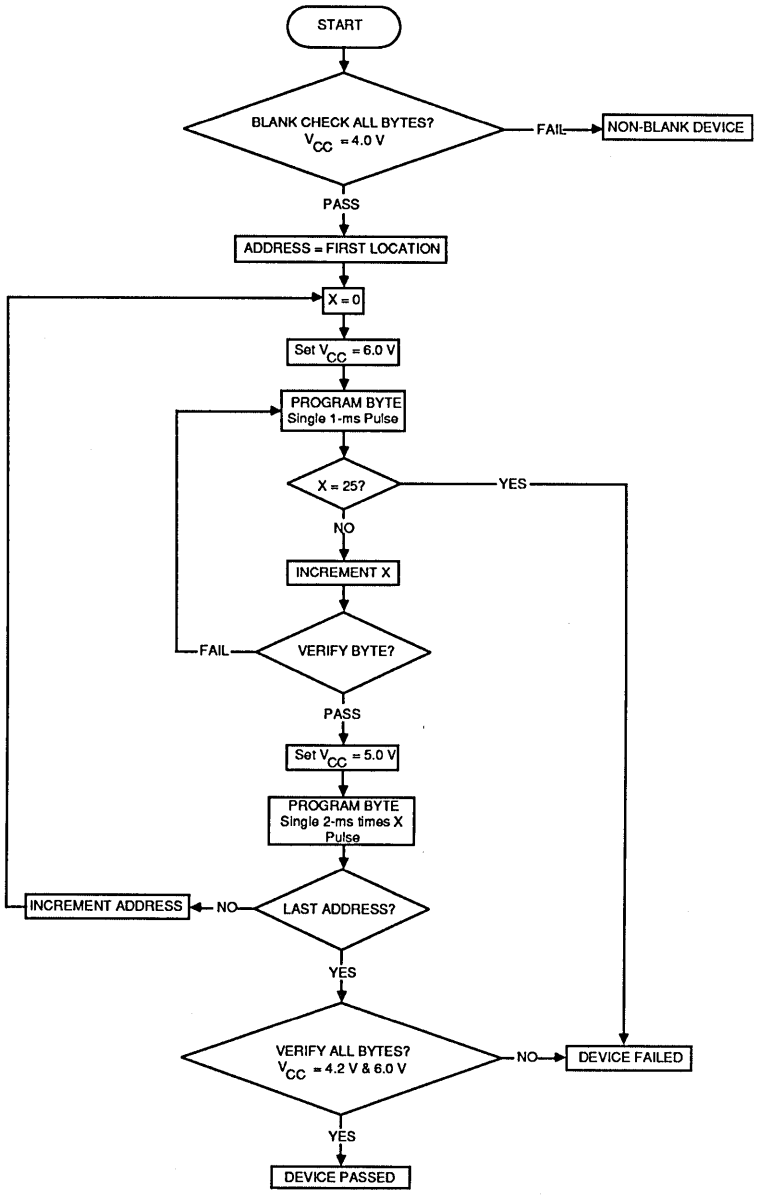


Figure 1. Programming Flow