# Am2732A

4096 x 8-Bit UV Erasable and one-time programmable EPROMs

## DISTINCTIVE CHARACTERISTICS

- Fast access times — 200ns, 250ns, 300ns, 450ns
- New low-cost plastic package for applications not requiring reprogramming
- Low power dissipation
  - 525mW active, 130mW standby
- Three-state outputs
- Pin compatible with Am9233 — 32K-bit ROM
- Separate chip enable and output enable

## GENERAL DESCRIPTION

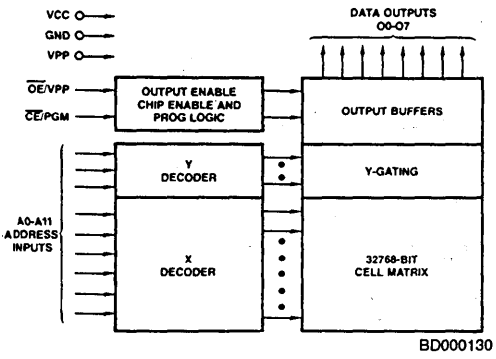
The Am2732A is a 32768-bit UV-light erasable and electrically programmable read-only memory, organized as 4096 words by 8-bits. The standard Am2732A offers an access time of 250ns, allowing operation with high-speed microprocessors without any WAIT state.

To eliminate bus contention in a multiple-bus microprocessor system, Am2732A offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random.

The part is available in an economical plastic package for applications which do not require reprogramming.

## BLOCK DIAGRAM

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## MODE SELECT TABLE

| $\overline{CE}$/PGM (18) | $\overline{OE}$/$V_{PP}$ (20) | Outputs (9–11, 13–17) | Mode |
|---|---|---|---|
| L | L | $D_{OUT}$ | Read |
| H | X | High Z | Standby |
| L | $V_{PP}$ | $D_{IN}$ | Program |
| L | L | $D_{OUT}$ | Program Verify |
| H | $V_{PP}$ | High Z | Program Inhibit |

H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

| Access Times | 200ns | | 250ns | | 300ns | | 450ns | |
|---|---|---|---|---|---|---|---|---|
| Power Supply Tolerance | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% |
| Part Number | Am2732A-2 | Am2732A-20 | Am2732A-2 | Am2732A-25 | Am2732A-3 | Am2732A-30 | Am2732A-4 | Am2732A-45 |

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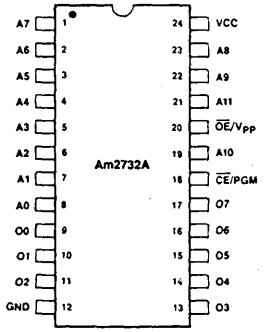
## CONNECTION DIAGRAM
### Top View

**D-24-4**

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Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am2732A-20 D L**

- L — Temperature
  - C – Commercial (0°C to +70°C)
  - I – Industrial (–40°C to +85°C)
  - L – Extended (–55°C to +100°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 24-pin CERDIP w/window
  - P – 24-pin plastic DIP
- Am2732A-20 — Speed Select
  - See Product Select Guide

| Valid Combinations | |
|---|---|
| Am2732A | PC, DC, DI, DL |
| Am2732A-2<br>Am2732A-3<br>Am2732A-4<br>Am2732A-30 | DC, DI, DL |
| Am2732A-20<br>Am2732A-25<br>Am2732A-45 | DC, DI, DL, DM |

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### ERASING THE Am2732A (Does Not Apply to Am2732APC)

In order to erase the Am2732A, it is necessary to expose it to an ultraviolet light source. A dosage of 15 Wseconds/$cm^2$ is required for complete erasing. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537Å) with intensity of 12000$\mu$W/$cm^2$ for 15 to 20 minutes. The Am2732A should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2732A, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer the exposure to fluorescent light and sunlight will eventually erase the Am2732A, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

### PROGRAMMING THE Am2732A

Upon delivery, or after each erasure the Am2732A has all 32768 bits in the "1", or high state. "0"s are loaded into the Am2732A through the procedure of programming.

The programming mode is entered when +21V is applied to the $\overline{OE}$/VPP pin. A 0.1$\mu$F capacitor must be placed across $\overline{OE}$/VPP and ground to suppress spurious voltage transients which may damage the device. The address to be programmed is applied to the proper address pins; 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL low level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. The only requirement is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC low level to the $\overline{CE}$/PGM input is prohibited when programming.

### READ MODE

The Am2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$/VPP) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs 100ns ($t_{OE}$) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

### STANDBY MODE

The Am2732A has a standby mode which reduces the active power dissipation by 75%, from 525 to 130mW (values for 0 to +70°C). The Am2732A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

### OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### PROGRAM INHIBIT

Programming of multiple Am2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2732A's may be common. A TTL level program pulse applied to an Am2732A's $\overline{CE}$/PGM input with VPP at 21V will program that Am2732A. A high-level $\overline{CE}$/PGM input inhibits the other Am2732A's from being programmed.

### PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}$/VPP and $\overline{CE}$ at $V_{IL}$. Data should be verified $t_{DV}$ after the falling edge of $\overline{CE}$.

### SYSTEM APPLICATION FOR Am2732A

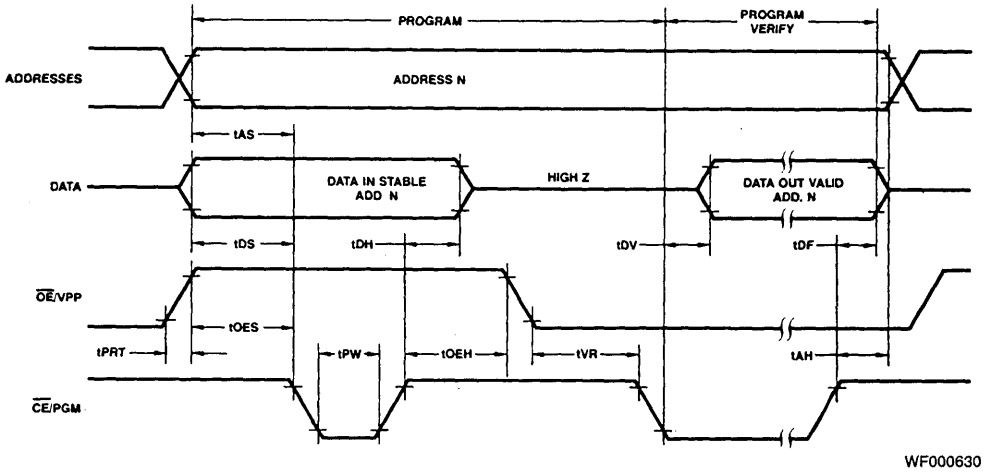
During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1$\mu$F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between $V_{CC}$ and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on Am2732A arrays, a 4.7$\mu$F bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | 10 | µA |
| $V_{OL}$ | Input Low Voltage During Verify | $I_{OL}$ = 2.1mA | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage During Verify | $I_{OH}$ = −400µA | 2.4 | | Volts |
| $I_{CC}$ | $V_{CC}$ Supply Current | | | 100 | mA |
| $V_{IL}$ | Input Low Level (All Inputs) | | -0.1 | 0.8 | Volts |
| $V_{IH}$ | Input High Level (All Inputs Except $\overline{OE}/V_{PP}$) | | 2.0 | $V_{CC}$ +1 | Volts |
| $I_{PP}$ | $V_{PP}$ Supply Current | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$ | | 30 | mA |
| $t_{AS}$ | Address Set-up time | Input $t_R$ and $t_F$ (10% to 90%) = 20ns<br>Input Signal Levels = 0.8 to 2.2V<br>Input Timing Reference Level = 1V and 2V<br>Output Timing Reference Level = 0.8V and 2V | 2 | | µs |
| $t_{OES}$ | Output Enable Set-up Time | | 2 | | µs |
| $t_{DS}$ | Data Set-up Time | | 2 | | µs |
| $t_{AH}$ | Address Hold Time | | 0 | | µs |
| $t_{OEH}$ | Output Enable Hold Time | | 2 | | µs |
| $t_{DH}$ | Data Hold Time | | 2 | | µs |
| $t_{DF}$ | Chip Enable to Output Float Delay | | 0 | 130 | ns |
| $t_{DV}$ | Data Valid From $\overline{CE}$ ($\overline{CE} = V_{IL}$,$\overline{OE} = V_{IL}$) | | | 1 | µs |
| $t_{PW}$ | Program Pulse Width | | 45 | 55 | ms |
| $t_{PRT}$ | Program Pulse Rise Time | | 50 | | ns |
| $t_{VR}$ | $V_{PP}$ Recovery Time | | 2 | | ns |

Note: 1. When programming the Am2732A, it is advisable to connect a 0.1µF capacitor between $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

## PROGRAMMING WAVEFORMS

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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −65°C to +135°C
Voltage on All Inputs/
Outputs (except $V_{PP}$) ..... +6V to −0.3V
Voltage on $V_{PP}$ during
programming ..... +22 to −0.3V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Temperature
Commercial ..... 0°C to +70°C
Industrial ..... −40°C to +85°C
Extended ..... −55°C to +100°C
Military ..... −55°C to +125°C

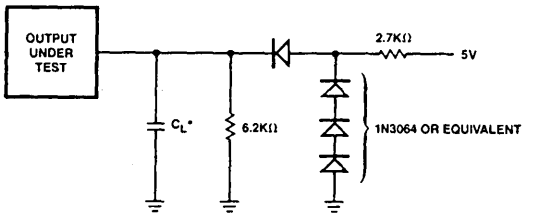
Supply Voltages
Am2732A, -2, -3, -4 ..... +4.75V to +5.25V
Am2732A-20, -25, -30, -40 ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0 to 5.5V | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0 to 5.5V | | | 10 | µA |
| $I_{PP1}$ | $V_{PP}$ Current Read (Note 2) | $V_{PP}$ = 5.5V | | | 1 | mA |
| $I_{CC1}$ | $V_{CC}$ Standby Current (Notes 2, 7) | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$ | | | 25 | mA |
| $I_{CC2}$ | $V_{CC}$ Active Current (Note 2) | $\overline{OE}$ = $\overline{CE}$ = $V_{IL}$ | | | 100 | mA |
| $V_{IL}$ | Input Low Voltage | 0 to 70°C | −0.1 | | +0.8 | Volts |
| $V_{IL}$ | Input Low Voltage | (−40 to +85°C, −55 to +100°C, −55 to +125°C) | −0.1 | | +0.6 | Volts |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$+1 | Volts |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −400µA | 2.4 | | | Volts |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 4 | 6 | pF |
| $C_{IN2}$ | $\overline{OE}$/$V_{PP}$ Input Capacitance | $V_{IN}$ = 0V | | | 20 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | | 12 | pF |

## SWITCHING TEST CIRCUIT

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*Note: $C_L$ = 100pF including jig capacitance.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

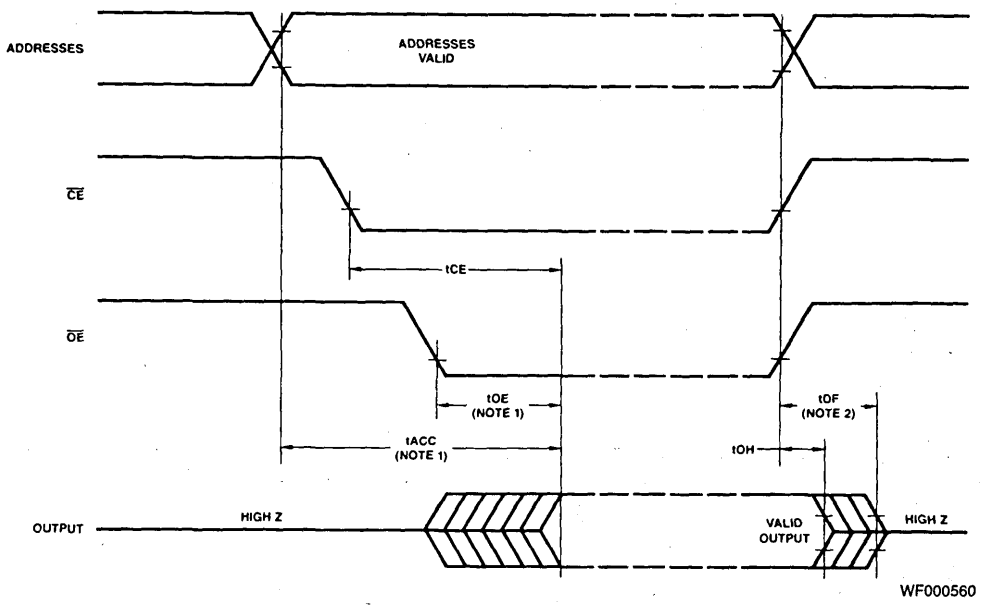
| No. | Symbol | Description | Test Conditions | | Min Values All Types | Maximum Values 2732APC | Maximum Values 2732A-2 2732A-20 | Maximum Values 2732A 2732A-25 | Units |
|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load: 1 TTL gate and $C_L$ = 100pF<br>Input Rise and Fall Times ≤ 20ns<br>Input Pulse levels: 0.45 to 2.4V<br>Timing Measurement Reference Level:<br>Inputs: 0.8V and 2V<br>Outputs: 0.8V and 2V | $\overline{CE} = \overline{OE} = V_{IL}$ | | 250 | 200 | 250 | ns |
| 2 | $t_{CE}$ | $\overline{CE}$ to Output Delay | | $\overline{OE} = V_{IL}$ | | 250 | 200 | 250 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE} = V_{IL}$ | | 100 | 70 | 100 | ns |
| 4 | $t_{DF}$ (Note 4) | Output Enable High to Output float | | $\overline{CE} = V_{IL}$ | | 90 | 60 | 90 | ns |
| 5 | $t_{OH}$ (Note 4) | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occured First | | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | | ns |

| No. | Symbol | Description | Test Conditions | | Min Values All Types | Maximum Values 2732A-3 2732A-30 | Maximum Values 2732A-4 2732A-45 | Units |
|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load: 1 TTL gate and $C_L$ = 100pF<br>Input Rise and Fall Times ≤ 20ns<br>Input Pulse levels: 0.45 to 2.4V<br>Timing Measurement Reference Level:<br>Inputs: 0.8V and 2V<br>Outputs: 0.8V and 2V | $\overline{CE} = \overline{OE} = V_{IL}$ | | 300 | 450 | ns |
| 2 | $t_{CE}$ | $\overline{CE}$ to Output Delay | | $\overline{OE} = V_{IL}$ | | 300 | 450 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE} = V_{IL}$ | | 150 | 150 | ns |
| 4 | $t_{DF}$ (Note 4) | Output Enable High to Output float | | $\overline{CE} = V_{IL}$ | | 130 | 130 | ns |
| 5 | $t_{OH}$ (Note 4) | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever Occured First | | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | ns |

Notes:

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply would then be the sum of $I_{CC}$ and $I_{PP1}$.
3. Typical values are for nominal supply voltages.
4. This parameter is only sampled and not 100% tested.
5. Caution: The 2732A must not be removed from or inserted into a socket or board when $V_{PP}$ or $V_{CC}$ is applied.
6. Unless otherwise specified under Test Conditions, all values apply to the appropriate temperature ranges as defined in Ordering Information of this specification.
7. $I_{CC1}$ limit is 35mA for Am2732APC.

## SWITCHING WAVEFORMS




Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC}$-$t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.