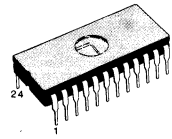
SGS-THOMSON MICROELECTRONICS

ETC2716

16K BIT (2K x 8) CMOS UV ERASABLE PROM

- CMOS POWER CONSUMPTION
- PERFORMANCE COMPATIBLE TO MARKET STANDARD 8-BIT CMOS MICROP.
- 2048 x 8 ORGANIZZATION
- PIN COMPATIBLE TO 2716
- ACCESS TIME DOWN TO 350 ns
- SINGLE 5V POWER SUPPLY
- STATIC - NO CLOCKS REQUIRED
- TTL COMPATIBLE I/Os DURING BOTH READ AND PROGRAM MODES
- THREE-STATE OUTPUT WITH OR-TIE CAPABILITY
- OPER. TEMP. : 0 to + 70°C ; −40 to + 85°C (V suffix).



Q
DIP-24
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

DESCRIPTION

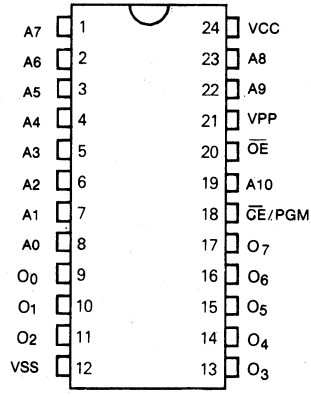
The ETC 2716 is a high speed 16K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

The ETC 2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure. This EPROM is fabricated with the reliable, high volume, time proven, P^2 CMOS silicon gate technology.

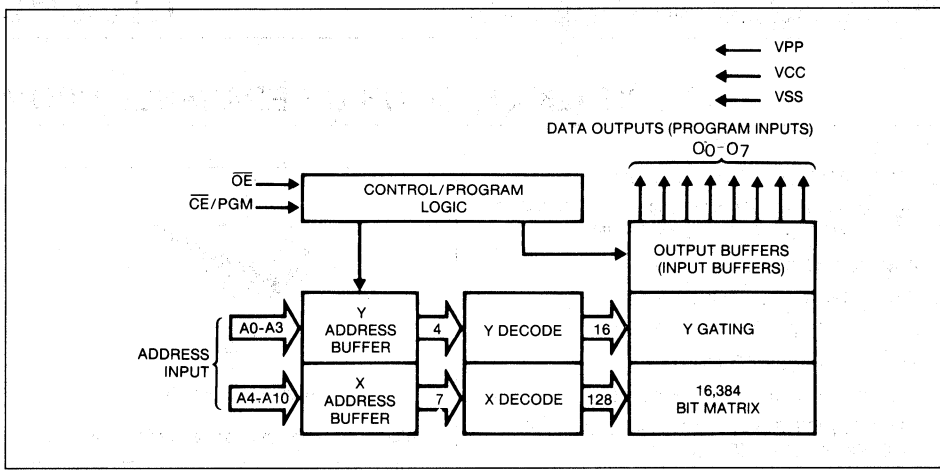
PIN NAMES

A0—A10	ADDRESS INPUTS
O_0—O_7	DATA OUTPUTS
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
V_{PP}	READ 5V, PROGRAM 25V
V_{CC}	5V
V_{SS}	GROUND

PIN CONNECTIONS



BLOCK DIAGRAM



PIN CONNECTION DURING READ OR PROGRAM

MODE	PIN NAME/NUMBER				
	$\overline{CE}$/PGM 18	$\overline{OE}$ 20	V_{PP} 21	V_{CC} 24	OUTPUTS 9-11, 13-17
Read	V_{IL}	V_{IL}	5	5	D_{OUT}
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{amb}	Temperature Under Bias "V" range	−10 to +80 −50 to +95	°C °C
T_{stg}	Storage Temperature	−65 to +125	°C
V_{PP}	V_{PP} Supply Voltage with Respect to V_{SS}	26.5V to −0.3	V
V_{in}	Input Voltages with Respect to V_{SS} except V_{PP}	6V to −0.3	V
	Output Voltages with Respects to V_{SS}	V_{CC} + 0.3V to V_{SS} − 0.3V	
P_D	Power Dissipation	1.0	W
	Lead Temperature (Soldering 10 seconds)	+300	°C

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are, not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

READ OPERATION

DC CHARACTERISTICS $T_A = 0°C$ to $+ 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$ (2), $V_{SS} = 0V$, (Unless otherwise specified)(6)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{LI}	Input Current	$V_{IN} = V_{CC}$ or GND	—	—	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.25V$, $\overline{CE}/PGM = V_{IH}$	—	—	10	μA
V_{IL}	Input Low Voltage		−0.1	—	0.8	V
V_{IH}(4)	Input High Voltage		2.0	—	$V_{CC}+1$	V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1$ mA	—	—	0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -400$ μA	2.4	—	—	V
V_{OL2}	Output Low Voltage	$I_{OL} = 0$ μA	—	—	0.1	V
V_{OH2}	Output High Voltage	$I_{OH} = 0$ μA	$V_{CC}-0.1$	—	—	V
I_{PP1}	V_{PP} Supply Current	$V_{PP} = 5.25V$	—	—	10	μA
I_{CC1}	V_{CC} Supply Current Active (TTL Levels)	$\overline{CE}/PGM$, $\overline{OE} = V_{IL}$ Address = V_{IH} or V_{IL} Frequency 1MHz, I/O = 0mA	—	2	10	mA
I_{CC2}	V_{CC} Supply Current Active (CMOS Levels)	$\overline{CE}/PGM = \overline{OE} = V_{IL}$ (Note 5) Addresses = GND or V_{CC} Frequency 1MHz, I/O = 0mA	—	1	5	mA
I_{CCSB1}	V_{CC} Supply Current Standby	$\overline{CE}/PGM = V_{IH}$	—	0,1	1	mA
I_{CCSB2}	V_{CC} Supply Current Standby	$\overline{CE}/PGM = V_{CC}$	—	0,01	0,1	mA

AC CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$, $V_{SS} = 0V$; Unless otherwise specified)(6).

Symbol		Parameter	Test Conditions	ETC2716-1		ETC2716 (-V)		Unit
Alternate	Standard			Min.	Max.	Min.	Max.	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}/PGM = \overline{OE} = V_{IL}$	—	350	—	450	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$	—	350	—	450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}/PGM = V_{IL}$	—	120	—	120	ns
t_{DF}(5)	TGHQZ	$\overline{OE}$ or $\overline{CE}$ High to Output Hi-Z	$\overline{CE}/PGM = V_{IL}$	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}/PGM = \overline{OE} = V_{IL}$	0	—	0	—	ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE} = V_{IL}$	0	100	0	100	ns

CAPACITANCE(3) $T_A = 25°C$, f = 1 MHz

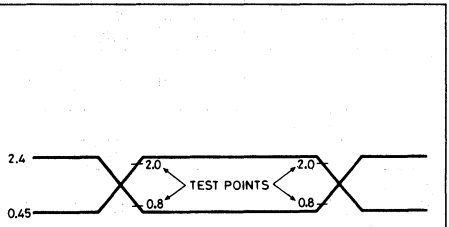
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_O	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes 1. Typical conditions are for operation at: $T_A = 25°C$, $V_{CC} = 5V$, $V_{PP} = V_{CC}$, and $V_{SS} = 0V$.
2. V_{PP} may be connected to V_{CC} except during program.
3. Capacitance is guaranteed by periodic testing. $T_A = 25°C$, f = 1 MHz.
4. The inputs (Address, OE, CE) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC + 0.3V.
5. T_{DF} is specified for OE or CE which ever occurs first. This parameter is only sampled and not 100% tested.
6. $T_A = -40°C$ to $+85°C$ for "V" range

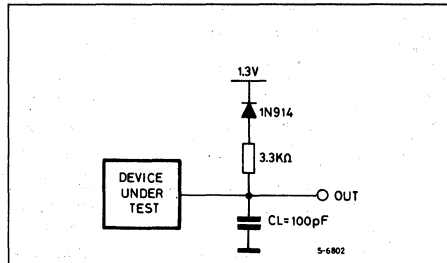
AC TEST CONDITIONS

Output Load: 1 TTL gate and CL = 100 pF
Input Rise and Fall Times ≤ 20 ns
Input pulse levels: 0.45V to 2.4V
Timing Measurement Reference Level
Inputs, Outputs 0.8V and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

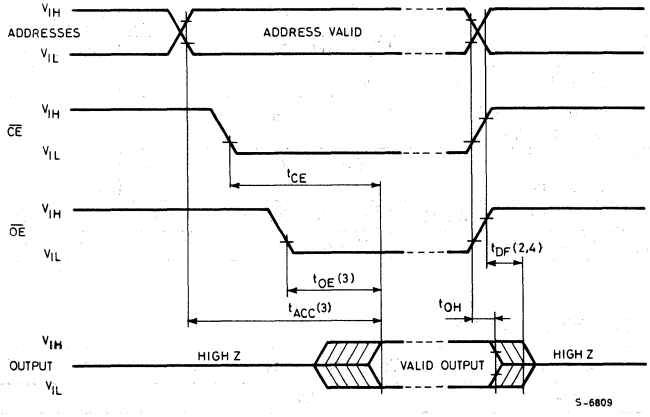


AC TESTING LOAD CIRCUIT



CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS



Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The ETC2716 has 3 modes of operation in the normal system environment. These are shown in Table 1.

READ MODE

The ETC2716 read operation requires that $\overline{OE}$ = V_{IL}, $\overline{CE}$/PGM = V_{IL} and that addresses A_0-A_{10} have been stabilized. Valid data will appear on the output pins after t_{ACC} t_{OE} or t_{CE} times (see Switching Time Wafeforms) depending on which is limiting.

DESELECT MODE

The ETC2716 is deselected by making $\overline{OE}$ = V_{IH}. This mode is independent of $\overline{CE}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{OE}$ = V_{IH}. This allows OR-tying 2 or more ETC2716 for memory expansion.

STANDBY MODE (POWER DOWN)

The ETC2716 may be powered down to the standby mode by making $\overline{CE}$/PGM = V_{IH}. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 0.4% of the normal operating power. V_{CC} must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The ETC2716 is shipped from SGS-THOMSON completely erased. All bits will be at a "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

PROGRAM MODE

The ETC2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels, including the program pulse on chip enable are TTL compatible. The programming sequence is:

With V_{PP} = 25V, V_{CC} = 5V, $\overline{OE}$ = V_{IH} and $\overline{CE}$/PGM = V_{IL}, an address is selected and the desired data word is applied to the output pins. (V_{IL} = "0" and V_{IH} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) *must not* be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. ETC2716 may be programmed in parallel with the same data in this mode.

PROGRAM VERIFY MODE

The programming of the ETC2716 is verified in the program verify mode which has V_{PP} at V_{CC} (see Table II). After programming an address, that same address cannot be immediately verified without an address change (dummy read).

PROGRAM INHIBIT MODE

The program inhibit mode allows programming several ETC2716 simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the ETC2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = V_{IH} will put its outputs in the HI-Z state.

TABLE I. OPERATING MODES (V_{CC} = 5V)

MODE	PIN NAME/NUMBER		
	$\overline{CE}$/PGM 18	$\overline{OE}$ 20	Outputs 9-11, 13-17
Read	V_{IL}	V_{IL}	D_{OUT}
Deselect	Don't Care	V_{IH}	Hi-Z
Standby	V_{IH}	Don't Care	Hi-Z

TABLE II. PROGRAMMING MODES (V_{CC} = 5V)

MODE	PIN NAME/NUMBER			
	$\overline{CE}$/PGM 18	$\overline{OE}$ 20	V_{PP} 21	OUTPUTS 9-11, 13-17
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	25	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	25(5)	D_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	25	Hi-Z

ERASING

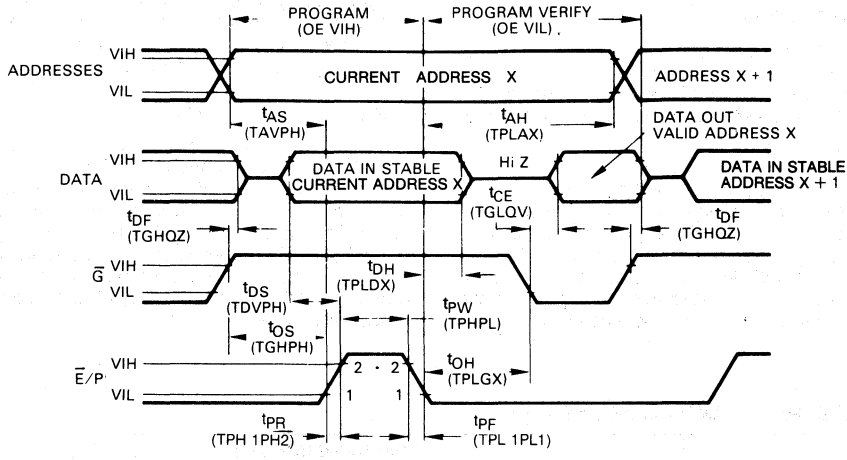
The ETC2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the ETC2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces ICC due to photodiode currents.

An ultraviolet source of 2537A yielding a total integrated dosage of 15 watt-seconds/cm² is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm² power rating is used. The ETC2716 to be erased should be place 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

TIMING DIAGRAM

PROGRAM MODE



Note: Symbols in parentheses are proposed JEDEC standard

PROGRAM OPERATIONS[1,2]

DC AND OPERATIVE CHARACTERISTICS ($T_A = 25°C \pm 5°C$) ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Values			Unit
		Min.	Typ.	Max.	
I_{LI}	Input Leakage Current (Note 3)	—	—	10	μA
V_{IL}	Input Low Level	−0.1	—	0.8	V
V_{IH}	Input High Level (Note 7)	2.2	—	$V_{CC}+1$	V
I_{CC}	V_{CC} Power Supply Current	—	—	10	mA
I_{PP1}	V_{PP} Supply Current (Note 4)	—	—	10	μA
I_{PP2}	V_{PP} Supply Current During Programming Pulse (Note 5)	—	—	30	mA

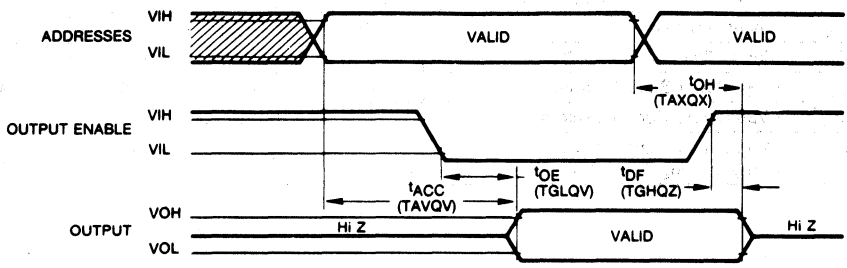
AC CHARACTERISTICS ($T_A = 25°C \pm 5°C$) ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 5V \pm 1V$) (Note 6)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	2	—	—	μs
t_{OS}	$\overline{OE}$ Setup Time	2	—	—	μs
t_{DS}	Data Setup Time	2	—	—	μs
t_{AH}	Address Hold Time	2	—	—	μs
t_{OH}	$\overline{OE}$ Hold Time	2	—	—	μs
t_{DH}	Data Hold Time	2	—	—	μs
t_{DF}	Output Disable to Output Three state Delay	0	—	100	μs
t_{OE}	Output Enable to Output Delay	—	—	120	ns
t_{PW}	Program Pulse Width	45	50	55	ms
t_{PR}	Program Pulse Rise Time	5	—	—	ns
t_{PF}	Program Pulse Fall Time	5	—	—	ns

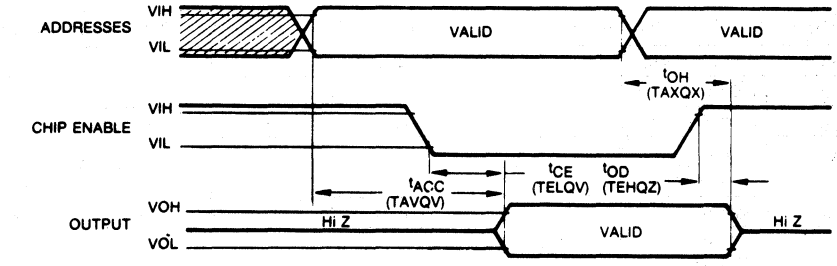
Notes 1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}. To prevent damage to the device it must not be inserted into a board with power applied.
2. Care must be taken to prevent overshoot of the V_{PP} supply when switching to +26V max.
3. $0V \leqslant V_{IN} \leqslant 5.25V$.
4. $CE/\overline{PGM} = V_{IL}$, $V_{PP} = V_{CC}$.
5. $V_{PP} = 26V$.
6. Transition times $\leqslant 20$ ns unless otherwise noted.
7. The inputs (Address, OE, CE) may go above V_{PP} by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to $V_{PP}+0.3V$ to $V_{SS}-0.3V$.

SWITCHING TIME WAVEFORMS

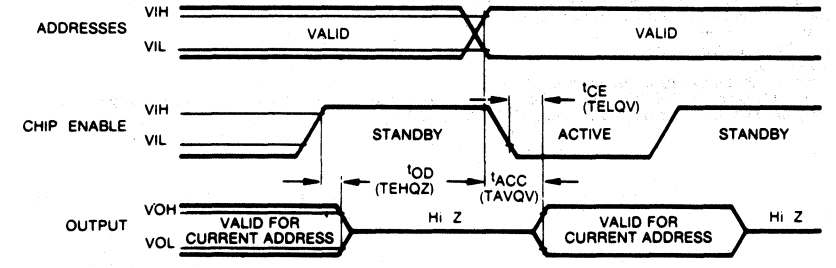
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power-Down Mode ($\overline{OE}$ = VIL)



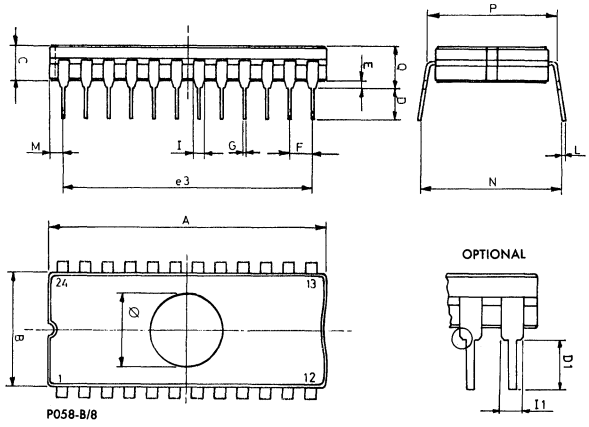
Symbols in parentheses are proposed JEDEC standard

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ETC2716Q	450 ns	5V± 5%	0 to +70°C	DIP-24
ETC2716Q-1	350 ns	5V± 5%	0 to +70°C	DIP-24
ETC2716Q-V	450 ns	5V± 5%	−40 to +85°C	DIP-24

PACKAGE MECHANICAL DATA

24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.30			1.272
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1(1)	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		27.94			1.100	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1(1)	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

Note: 1. Optional see drawing