TMS2516, SMJ2516
16,384-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

DECEMBER 1979 – REVISED AUGUST 1983

- Organization . . . 2048 X 8
- Single +5-V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (16K, 32K, and 64K)
- JEDEC Standard Pinout
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time:

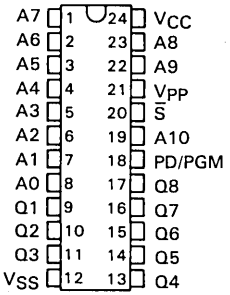
  '2516-35 350 ns
  '2516-45 450 ns

- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Low Power Dissipation:

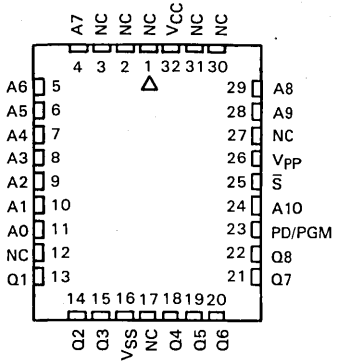
  Active . . . 285 mW Typical
  Standby . . . 100 mW Typical

- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required
- Available in Full Military Temperature Range Version (SMJ2516)

TMS2516 . . . JL PACKAGE
SMJ2516 . . . J PACKAGE
(TOP VIEW)



SMJ2516 . . . FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A(N)	Address Inputs
NC	No Internal Connection
PD/PGM	Power Down/Program
Q(N)	Data Outputs
$\overline{S}$	Chip Select
V_{CC}	+5-V Power Supply
V_{PP}	+25-V Power Supply
V_{SS}	0-V Ground

description

The '2516 series are 16,384-bit, ultraviolet-light erasable, electrically-programmable read-only memories. These devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54/74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 54/74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The '2516 is plug-in compatible with the '4016 16K static RAM.

The TMS2516s are offered in a dual-in-line cerpak package (JL suffix), rated for operation form 0°C to 70°C. The SMJ' devices are offered in a 24-pin dual-in-line ceramic package (J) and in a 32-pad leadless ceramic chip carrier (FG). The J package is designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers, whereas the FG package is intended for surface mounting on solder pads on 0.050-inch (1,27 mm) centers. The FG package offers a three layer rectangular chip carrier with dimensions 0.450 × 0.550 × 0.100 (11,42 × 13,97 × 2,54).

Since these EPROMs operate from a single +5 V supply (in the read mode), they are ideal for use in microprocessor systems. One other (+25 V) supply is needed for programming but all programming signals are TTL level, requiring a single 10-ms pulse. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 20 seconds.

operation

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down	Start Programming	Inhibit Programming	Program Verification
PD/PGM (18)	V_{IL}	Don't Care	V_{IH}	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IL}
$\overline{S}$ (20)	V_{IL}	V_{IH}	Don't Care	V_{IH}	V_{IH}	V_{IL}
V_{PP} (21)	+5 V	+5 V	+5 V	+25 V	+25 V	+25 V (or +5 V)
V_{CC} (24)	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V
Q (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	HI-Z	Q

read/output disable

When the outputs of two or more '2516s are connected to the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. The device whose output is to be read should have a low-level TTL signal applied to the $\overline{S}$ and PD/PGM pins. All other devices in the circuit should have their outputs disabled by applying high-level signals to these same pins. PD/PGM can be left low, but it may be advantageous to power down the device during output disable. Output data is accessed at pins Q1 through Q8. On the '2516-45, data can be accessed in 450 ns and access time from $\overline{S}$ is 150 ns. On the '2516-35, data can be accessed in 350 ns and access time from $\overline{S}$ is 120 ns. These access times assume that the addresses are stable.

power down

Active power dissipation can be cut by 64% by applying a high TTL signal to the PD/PGM pins. in this mode all outputs are in a high-impedance state.

erasure

Before programming, the '2516 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light having a wavelength of 253.7 nm (2537 angstroms). The recommended minimum exposure dose (UV intensity times exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12-milliwatt per-square-centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are in the "1" state (assuming a high-level output corresponds to logic "1"). It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the '2516, the window should be covered with an opaque lid.

start programming

After erasure (all bits in logic "1" state), logic "0's" are programmed into the desired locations. A "0" can be erased only by ultraviolet light. The programming mode is achieved when V_{PP} is 25 V and $\overline{S}$ is at V_{IH}. Data is presented

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in parallel (8 bits) on pins Q1 through Q8. Once addresses and data are stable, a 10-millisecond TTL high-level pulse should be applied to the PGM pin at each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. Several '2516s can be programmed simultaneously when the devices are connected in parallel.

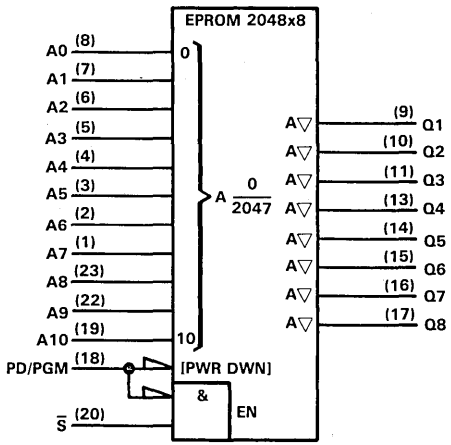
inhibit programming

When two or more devices are connected in parallel, data can be programmed into all devices or only chosen devices. '2516s not intended to be programmed (i.e., inhibited) should have a low level applied to the PD/PGM pin and a high-level applied to the $\overline{S}$ pin.

program verification

A verification is done to see if the device was programmed correctly. A verification can be done at any time. It can be done on each location immediately after that location is programmed. To do a verification, V_{PP} may be kept at +25 V.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions in IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 7 V
Supply voltage, V_{PP} (see Note 1)	−0.3 V to 28 V
All input voltages (see Note 1)	−0.3 V to 7 V
Output voltage (operating, with respect to V_{SS})	−0.3 V to 7 V
Operating free-air temperature range: TMS'	0°C to 70°C
Operating case temperature range: SMJ'	−55°C to 125°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_{SS} (substrate).

recommended operating conditions

PARAMETER	TMS2516-35			TMS2516-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.1		0.8	−0.1		0.8	V
Read cycle time, $t_{c(rd)}$	350			450			ns
Operating free-air temperature, T_A	0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25 V (±1 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS2516			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V			±10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25 V, PD/PGM = V_{IL}			6	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/PGM = V_{IH}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/PGM = V_{IH}		20	30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{S}$ = PD/PGM = V_{IL}		57	100	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage and operating free-air temperature ranges, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TMS2516		UNIT
			TYP‡	MAX	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are T_A = 25°C and nominal voltages.

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switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	TMS2516-35			TMS2516-45			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leq 20$ ns, $t_f \leq 20$ ns		250	350		280	450	ns
$t_{a(S)}$	Access time from chip select				120			150	ns
$t_{a(PR)}$	Access time from PD/PGM			250	350		280	450	ns
$t_{v(A)}$	Output data valid after address change		0			0			ns
$t_{dis(S)}$	Output disable time from chip select during read only‡		0		100	0		100	ns
$t_{dis(S)}$	Output disable time from chip select during program and program verify‡				120			120	ns
$t_{dis(PR)}$	Output disable time from PD/PGM‡		0		100			100	ns

† All typical values are at T_A = 25°C and nominal voltages.
‡ Value calculated from 0.5 volt delta to measured output level.

recommended timing requirements for programming T_A = 25°C (see Note 4)

PARAMETER		TMS2516			UNIT
		MIN	TYP†	MAX	
$t_{w(PR)}$	Pulse duration, program pulse	9		55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(S)}$	Chip-select setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(S)}$	Chip-select hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs

† Typical values are at nominal voltages.
NOTES: 4. Timing measurement reference levels: inputs 0.8 V and 2 V, outputs 0.65 V and 2.2 V.
5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$, $t_{a(S)}$, and t_{dis}, PD/PGM = $\overline{S}$ = V_{IL}.

recommended operating conditions

PARAMETER	SMJ2516-35			SMJ2516-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.5	5	5.5	4.5	5	5.5	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.1		0.8	−0.1		0.8	V
Read cycle time, $t_{c(rd)}$	350			450			ns
Operating case temperature, T_C	−55		125	−55		125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25 V (±1 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	SMJ2516			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V			±10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25 V, PD/PGM = V_{IL}			6	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/PGM = V_{IH}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/PGM = V_{IH}		20	30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{S}$ = PD/PGM = V_{IL}		57	100	mA

† Typical values are at T_C = 25°C and nominal voltages.

capacitance over recommended supply voltage and operating case temperature ranges, f = 1 MHz†

PARAMETER		TEST CONDITIONS	SMJ2516		UNIT
			TYP‡	MAX	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are at T_C = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	SMJ2516-35			SMJ2516-45			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 54 TTL load, $t_r \leq 20$ ns, $t_f \leq 20$ ns		250	350		280	450	ns
$t_{a(S)}$	Access time from chip select				120			150	ns
$t_{a(PR)}$	Access time from PD/PGM			250	350		280	450	ns
$t_{v(A)}$	Output data valid after address change		0			0			ns
$t_{dis(S)}$	Output disable time from chip select during read only‡		0		100	0		100	ns
$t_{dis(S)}$	Output disable time from chip select during program and program verify‡				120			120	ns
$t_{dis(PR)}$	Output disable time from PD/PGM‡		0		100			100	ns

† All typical values are at T_C = 25°C and nominal voltages.
‡ Value calculated from 0.5 volt delta to measured output

recommended timing requirements for programming T_C = 25°C (see Note 4)

PARAMETER		SMJ2516			UNIT
		MIN	TYP†	MAX	
$t_{w(PR)}$	Pulse duration, program pulse	9		55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(S)}$	Chip-select setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(S)}$	Chip-select hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs

† Typical values are at nominal voltages.
NOTES: 4. Timing measurement reference levels: inputs 0.8 V and 2 V, outputs 0.65 V and 2.2 V.
5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$, $t_{a(S)}$, and t_{dis}, PD/PGM = $\overline{S}$ = V_{IL}.

PARAMETER MEASUREMENT INFORMATION

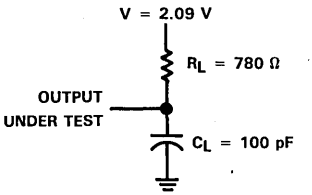
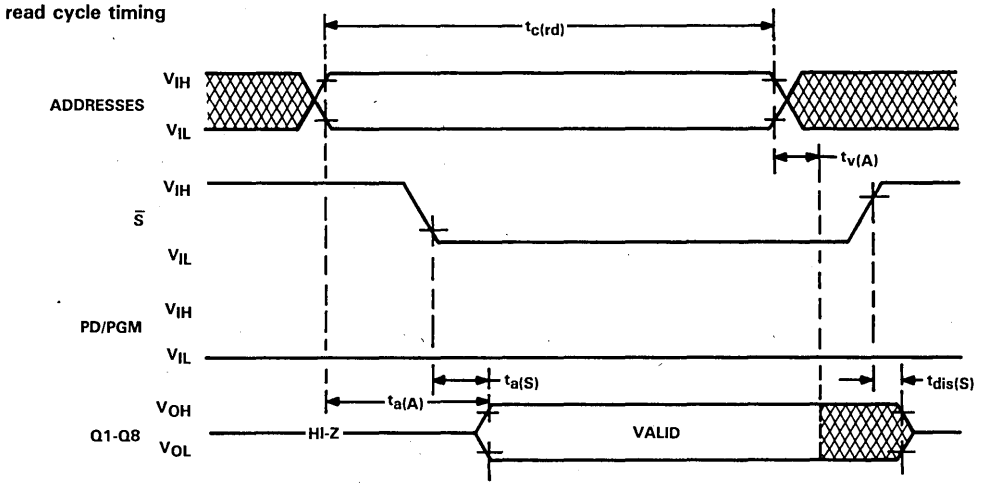
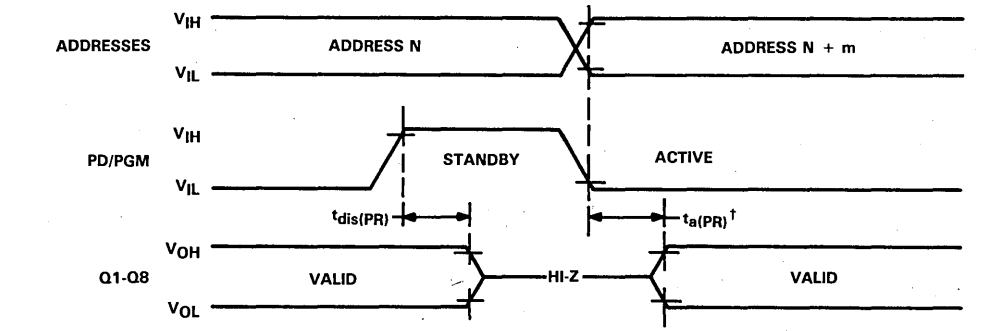


FIGURE 1 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



standby mode



NOTE: $\overline{S}$ must be in low state during Active Mode, "Don't Care" otherwise.
† $t_{a(PR)}$ referenced to PD/PGM or the address, whichever occurs last.

program cycle timing