CY7C261
CY7C263/CY7C264

CYPRESS SEMICONDUCTOR

8192 x 8 PROM Power Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 30 ns (commercial)**
  - **— 35 ns (military)**
- **Low power**
  - **— 550 mW (commercial)**
  - **— 660 mW (military)**
- **Super low standby power (7C261)**
  - **— Less than 200 mW when deselected**
  - **— Fast access: 30 ns**
- **EPROM technology 100% programmable**
- **Slim 300 mil or standard 600 mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2000V static discharge**

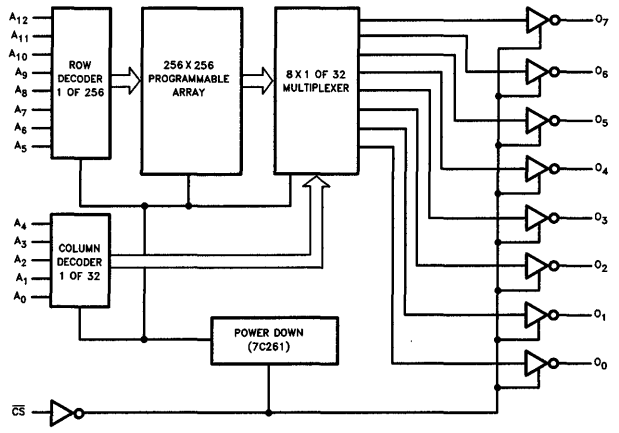
Product Characteristics

The CY7C261, CY7C263 and CY7C264 are high performance 8192 word by 8 bit CMOS PROMs. When deselected, the 7C261 automatically powers down into a low power standby mode. It is packaged in the 300 mil wide package. The 7C263 and 7C264 are packaged in 300 mil and 600 mil wide packages respectively and do not power down when deselected. The reprogrammable CERDIP packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C261, CY7C263 and CY7C264 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS}$. The contents of the memory location addressed by the address lines (A_0–A_{12}) will become available on the output lines (O_0–O_7).

Logic Block Diagram



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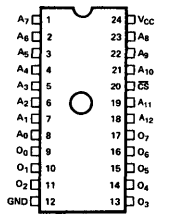
Pin Configurations



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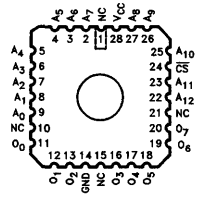

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Selection Guide

		7C261-30 7C263-30 7C264-30	7C261-35 7C263-35 7C264-35	7C261-40 7C263-40 7C264-40	7C261-45 7C263-45 7C264-45	7C261-55 7C263-55 7C264-55
Maximum Access Time (ns)		30	35	40	45	55
Maximum Operating Current (mA)	Commercial	120	100	100	100	100
	Military		120		120	120
Standby Current (mA) (7C261 only)	Commercial	40	30	30	30	30
	Military		30		30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage (Pin 19 DIP, Pin 23 LCC) 13.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latchup Current ..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[5]	−55°C to + 125°C	5V ±10%

3

Electrical Characteristics Over the Operating Range[6]

Parameters	Description	Test Conditions		7C261-30 7C263-30 7C264-30		7C261-35 7C263-35 7C264-35		7C261-40 7C263-40 7C264-40		7C261-45, 55 7C263-45, 55 7C264-45, 55		Units
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	Commercial			2.4		2.4		2.4		V
			Military							2.4		V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	Commercial	2.4								V
			Military			2.4						V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA	Commercial				0.4		0.4		0.4	V
			Military								0.4	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA	Commercial		0.4							V
			Military				0.4					V
V_{IH}	Input HIGH Level[1]			2.0		2.0		2.0		2.0		V
V_{IL}	Input LOW Level[1]				0.8		0.8		0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2								
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−40	+40	−40	+40	−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V	Commercial		120		100		100		100	mA
			Military				120				120	mA
I_{SB}	Standby Supply Current (7C261)	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH} I_{OUT} = 0 mA	Commercial		40		30		30		30	mA
			Military				40				30	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C261, CY7C263 & CY7C264 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. T_A is the "instant on" case temperature.
6. See the last page of this specification for Group A subgroup testing information.

Switching Characteristics Over the Operating Range[5, 6]

Parameters	Description	7C261-30 7C263-30 7C264-30		7C261-35 7C263-35 7C264-35		7C261-40 7C263-40 7C264-40		7C261-45 7C263-45 7C264-45		7C261-55 7C263-55 7C264-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		30		35		40		45		55	ns
t_{HZCS1}	Chip Select Inactive to High Z[8]		25		25		25		30		35	ns
t_{HZCS2}	Chip Select Inactive to High Z (7C261)[8]		30		30		35		45		55	ns
t_{ACS1}	Chip Select Active to Output Valid		20		20		25		30		35	ns
t_{ACS2}	Chip Select Active to Output Valid (7C261)		35		40		45		45		55	ns
t_{PU}	Chip Select Active to Power Up (7C261)	0		0		0		0		0		ns
t_{PD}	Chip Select Inactive to Power Down (7C261)		30		35		40		45		55	ns

AC Test Loads and Waveforms

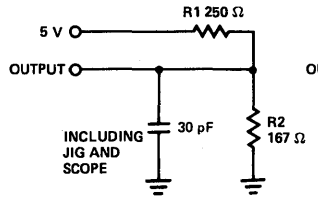

Figure 1a

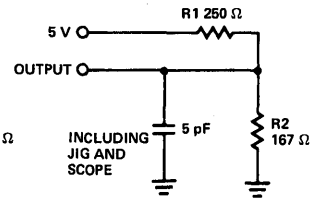

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Figure 1b

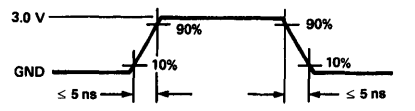

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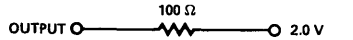
Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



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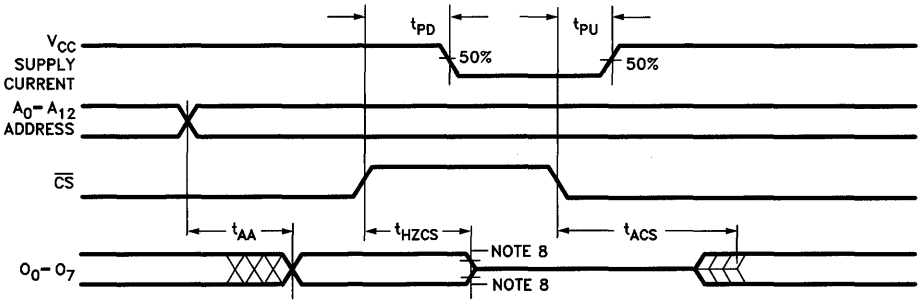

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Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b.*
8. t_{HZCS} is tested using the load shown in *Figure 1b.* The transition time is measured from 1.5V on the CS low to high transition to the output transition through the ±500 mV level respective to the 2.0V bias voltage (V_{THZCSL} = 1.5V, V_{THZCSH} = 2.5V).

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C261 or 7C263 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W×sec/cm^2 is the recommended maximum dosage.

Device Programming

The CY7C261, CY7C263 & CY7C264 all program identically. They utilize an intelligent programming algorithm to assure consistent programming quality. These 64K PROMS use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

Programming Pinout

The Programming Pinout of all three devices are shown in Figure 3 below, and are identical. The programming mode is entered by raising the pin 19 to V_{PP}. In this mode, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched and held in an onboard register, while the lower 8 address bits are presented on the same pins for selecting one of 256 memory bytes. The addressed location is programmed and verified with the application of a $\overline{PGM}$ and $\overline{VFY}$ pulse applied to pins 22 and 23 respectively. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.

Programming And Blankcheck

Addressing During Programming and Blankcheck

Addressing to these devices in all modes of operation other than normal read operation is accomplished by multiplexing the upper 5 address bits with the lower 8. The address designations for the lower 8 addressing bits is AX0 through AX7 and the upper 5 address bits are designated AY8 through AY12. This allows sufficient pins for an intelligent programming algorithm to be implemented without the need to switch high voltage signals during the blankcheck, programming, and verification operation.

Addressing while in these modes is accomplished by placing the upper 5 bits of address on pins 8, 7, 6, 5, and 4 with the least significant bit on pin 8. These address bits are loaded into an onboard register by clocking pin 21, the latch signal, from V_{ILP} to V_{IHP} and back to V_{ILP}. The lower 8 address bits are then placed on pins 8 through 1, with the least significant bit on pin 8. The upper 5 bits remain in the onboard latch until a new value is loaded or power is removed from the device. All 256 bytes addressed by the lower 8 bits may be accessed by sequencing the lower 8 addresses without changing the upper 5 bits or relatching the value in the onboard register.

Blankcheck

Blankcheck is accomplished by performing a verify cycle, sequencing through all memory address locations, where all the data read will be "0"s.

Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing V_{PP} on pin 19. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location as described above, placing the data to be programmed into a location on the data pins, and clocking the $\overline{PGM}$ signal from V_{IHP} to V_{ILP} and back to V_{IHP} with a pulse width of 200 μs. The data is removed from the data pins and the content of the location is then verified by taking the $\overline{VFY}$ signal from V_{IHP} to V_{ILP}, comparing the output with the desired data and then returning $\overline{VFY}$ to V_{IHP}. If the contents are correct, a second overprogram pulse of 4 times the original 200 μs is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200 μs pulse is applied to $\overline{PGM}$ with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the

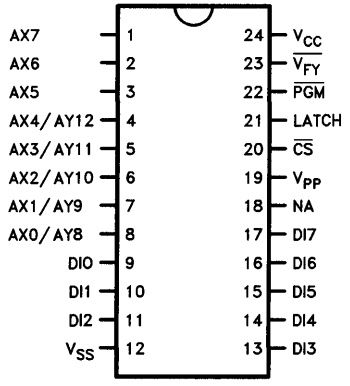


Figure 3. Programming Pinout (DIP Package)

location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed. After all locations are programmed, they should be verified at V_{CCP} = 5.0V.

Operating Modes

Read

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 13 bit field, a chip select, (active LOW), is applied to the $\overline{CS}$ pin, and the contents of the addressed location appear on the data out pins.

Program, Program Inhibit, Program Verify

These modes are entered by placing a high voltage V_{PP} on pin 19, with pins 18 and 20 set to V_{ILP}. In this state, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched into an onboard register, pin 22 becomes an active LOW program ($\overline{PGM}$) signal and pin 23 becomes an active LOW verify ($\overline{VFY}$) signal. Pins 22 and 23 should never be active LOW at the same time. The PROGRAM mode exists when $\overline{PGM}$ is LOW, and $\overline{VFY}$ is HIGH. The VERIFY mode exists when the reverse is true, $\overline{PGM}$ HIGH and $\overline{VFY}$ LOW and the PROGRAM INHIBIT mode is entered with both $\overline{PGM}$ and $\overline{VFY}$ HIGH. PROGRAM INHIBIT is specifically provided to allow data to be placed on and removed from the data pins without conflict.

Blankcheck

Blankcheck mode is identical to PROGRAM VERIFY and is entered in the same manner as described above.

Programming Sequence

The flowchart in Figure 4 is a detailed description of the intelligent programming cycle used to program the devices covered in this specification. Of particular importance are the areas of power sequencing used to enter and exit the programming operation. This flowchart combined with the timing diagrams AC and DC parameters accurately describe this complete operation. Note should be taken of the inner and outer addressing loops which allow 256 bytes to be programmed each time the onboard register containing the upper 5 address bits is loaded.

The timing diagram in Figure 5 contains all of the timing information necessary for describing the relations required for programming the devices covered in this specification. Some of the information pertains to each cycle of programming as specified in the inner loops of Figure 5, some for the outer loop where the upper address is advanced, and some pertains only to entry and exit from the programming mode of operation.

In particular, the timing sequence associated with the Latch signal on pin 21 and addresses AY8 through AY12 pertain only to the outer loop where the upper 5 (N in the flow chart) address bits are incremented.

T_P, T_{PD} and T_{HP} refer to the entry and exit from the programming mode of operation. Note that this is referenced to LATCH, $\overline{PGM}$ and $\overline{VFY}$ operations.

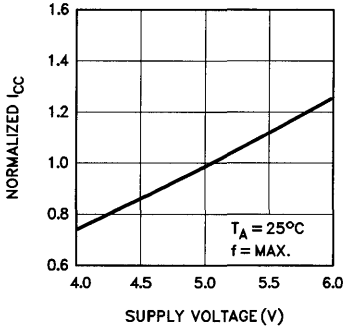
T_{DS}, T_{AS}, T_{AH} and T_{DH} refer to the required setup and hold times for the address and data for $\overline{PGM}$ and $\overline{VFY}$ operations. These parameters must be adhered to, in all operations, including V_{FY}. This precludes the option then of verifying the device by holding the V_{FY} signal LOW, and sequencing the addresses.

Table 1. Operating Modes

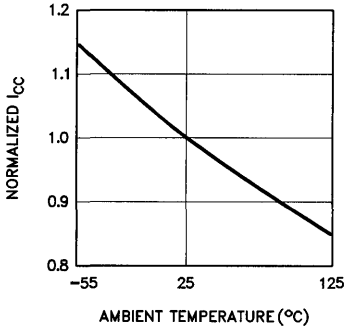
Mode	Pins 1 thru 3 A7–A5, AX7–AX5	Pins 4 thru 8 A4–A0, AX4–AX0 AY12–AY8	Pins 9 thru 11 D0 thru D2	Pins 13 thru 17 D3 thru D7	Pin 18	Pin 19	Pin 20	Pin 21	Pin 22	Pin 23
Read	A7 thru A5	A4 thru A0	DO0 thru DO2	DO3 thru DO7	A12	A11	$\overline{CS}$	A10	A9	A8
Program	AX7 thru AX5	AX4 thru AX0 AY12–AY8	DI_0 thru DI_2 Input	DI_3 thru DI_7 Input	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{ILP}	V_{IHP}
Program Inhibit	AX7 thru AX5	AX4 thru AX0 AY12–AY8	High Z	High Z	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{IHP}	V_{IHP}
Program Verify	AX7 thru AX5	AX4 thru AX0 AY12–AY8	DO0 thru DO2 Output	DO3 thru DO7 Output	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{IHP}	V_{ILP}
Blank Check	AX7 thru AX5	AX4 thru AX0 AY12–AY8	DI_0 thru DI_2 Output	DI_3 thru DI_7 Output	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{IHP}	V_{ILP}

Typical AC and DC Characteristics

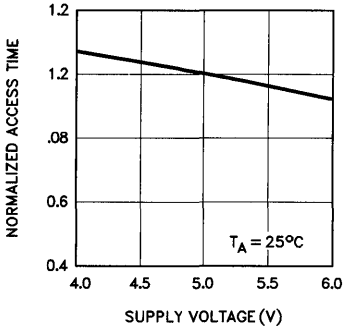
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



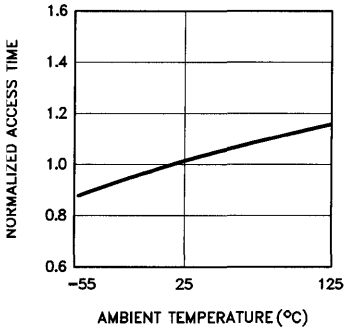
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



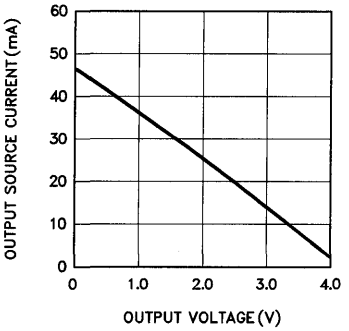
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



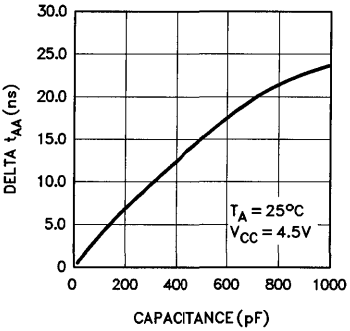
NORMALIZED ACCESS TIME vs. TEMPERATURE



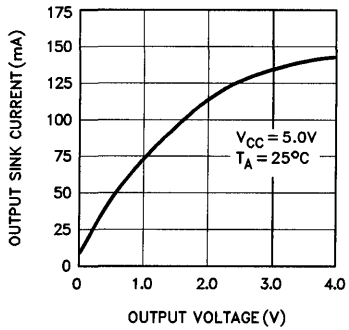
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



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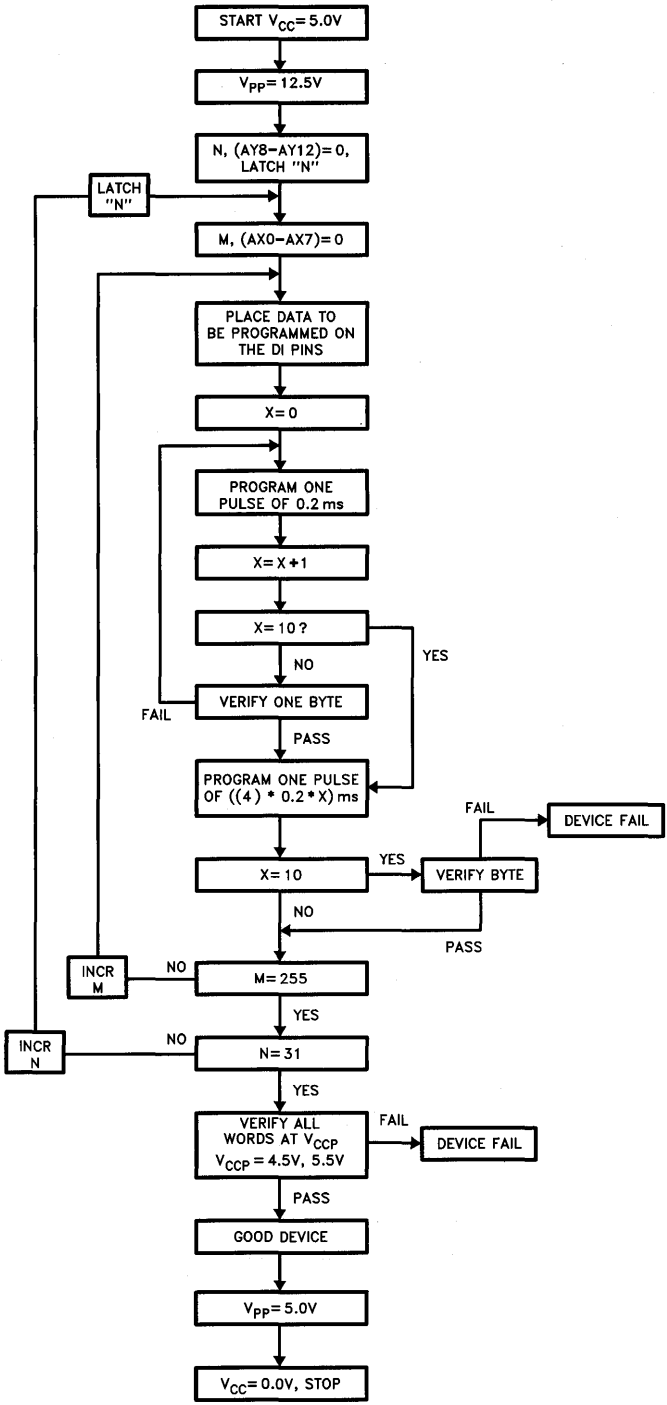

Figure 4. Programming Flowchart

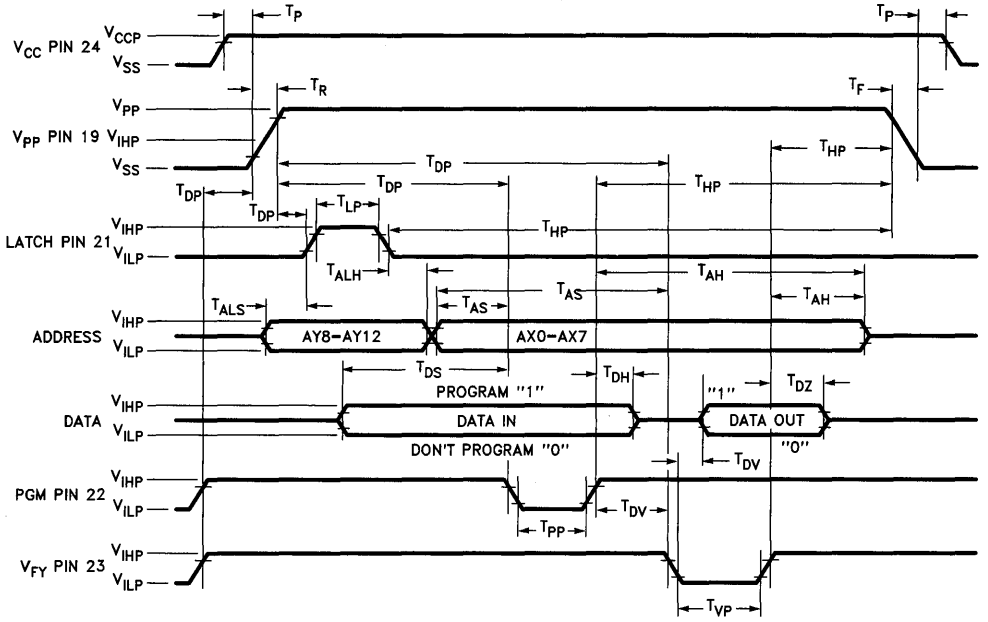

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Figure 5. Programming Waveforms

Note: Power, V_{PP} and V_{CC} should not be cycled for each program verify cycle but remain static during programming.

Table 2. DC Programming Parameters T_A = 25°C

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	12.0	13.0	V
V_{CCP}	Power Supply Voltage During Programming	4.75	5.25	V
I_{PP}	V_{PP} Supply Current		50	mA
V_{IHP}	Input High Voltage During Programming	4.75	5.25	V
V_{ILP}	Input Low Voltage During Programming	−3.0	0.4	V
V_{OH}	Output High Voltage	2.4		V
V_{OL}	Output Low Voltage		0.4	V

Table 3. AC Programming Parameters T_A = 25°C

Parameter	Description	Min.	Max.	Units
T_{AS}	Address Setup Time to $\overline{PGM}/\overline{VFY}$	1.0		μs
T_{AH}	Address Hold Time from $\overline{PGM}/\overline{VFY}$	1.0		μs
T_{DS}	Data Setup Time to $\overline{PGM}$	1.0		μs
T_{DH}	Data Hold Time $\overline{PGM}$	1.0		μs
T_{PP}	Program Pulse Width	0.2	10	ms
$T_{R,F}$	V_{PP} Rise and Fall Time	100		ns
T_{ALS}	Address Setup Time to Latch	1.0		μs
T_{ALH}	Address Hold Time from Latch	1.0		μs
T_{LP}	Latch Pulse Width	1.0		μs
T_{DV}	Delay to Verify	1.0		μs
T_{VD}	Verify to Data Out		1.0	μs
T_{VH}	Data Hold Time from Verify		1.0	μs
T_{VP}	Verify Pulse Width	2.0		μs
T_{DZ}	Verify to High Z		1.0	μs
T_{DP}	Delay to Function	1.0		μs
T_{HP}	Hold From Function	1.0		μs
T_P	Power Up/Down	20.0		ms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C261-30PC	P13	Commercial
	CY7C261-30WC	W14	
	CY7C263-30PC	P13	
	CY7C263-30WC	W14	
	CY7C264-30PC	P11	
	CY7C264-30WC	W12	
	CY7C264-30DC	D12	
35	CY7C261-35PC	P13	Commercial
	CY7C261-35WC	W14	
	CY7C263-35PC	P13	
	CY7C263-35WC	W14	
	CY7C264-35PC	P11	
	CY7C264-35WC	W12	
	CY7C264-35DC	D12	
	CY7C261-35WMB	W14	Military
	CY7C261-35DMB	D14	
	CY7C261-35LMB	L64	
	CY7C261-35QMB	Q64	
	CY7C263-35WMB	W14	
	CY7C263-35DMB	D14	
	CY7C263-35LMB	L64	
	CY7C263-35QMB	Q64	
	CY7C264-35DMB	D12	
	CY7C264-35WMB	W12	
40	CY7C261-40PC	P13	Commercial
	CY7C261-40WC	W14	
	CY7C263-40PC	P13	
	CY7C263-40WC	W14	
	CY7C264-40PC	P11	
	CY7C264-40DC	D12	
	CY7C264-40WC	W12	

Speed (ns)	Ordering Code	Package Type	Operating Range
45	CY7C261-45PC	P13	Commercial
	CY7C261-45WC	W14	
	CY7C263-45PC	P13	
	CY7C263-45WC	W14	
	CY7C264-45PC	P11	
	CY7C264-45DC	D12	
	CY7C264-45WC	W12	
	CY7C261-45WMB	W14	Military
	CY7C261-45DMB	D14	
	CY7C261-45LMB	L64	
	CY7C261-45QMB	Q64	
	CY7C263-45WMB	W14	
	CY7C263-45DMB	D14	
	CY7C263-45LMB	L64	
	CY7C263-45QMB	Q64	
	CY7C264-45DMB	D12	
	CY7C264-45WMB	W12	
55	CY7C261-55PC	P13	Commercial
	CY7C261-55WC	W14	
	CY7C263-55PC	P13	
	CY7C263-55WC	W14	
	CY7C264-55PC	P11	
	CY7C264-55DC	D12	
	CY7C264-55WC	W12	
	CY7C261-55WMB	W14	Military
	CY7C261-55DMB	D14	
	CY7C261-55LMB	L64	
	CY7C261-55QMB	Q64	
	CY7C263-55WMB	W14	
	CY7C263-55DMB	D14	
	CY7C263-55LMB	L64	
	CY7C263-55QMB	Q64	
	CY7C264-55DMB	D12	
	CY7C264-55WMB	W12	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}[2]	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AA}	7,8,9,10,11
t_{HZCS1}[1]	7,8,9,10,11
t_{HZCS2}[2]	7,8,9,10,11
t_{ACS1}[1]	7,8,9,10,11
t_{ACS2}[2]	7,8,9,10,11

Notes:
1. 7C263 and 7C264 only.
2. 7C261 only.

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