Rockwell

R87C32
32K (4K × 8) CMOS UV EPROM

PRELIMINARY

FEATURES

- 4096 x 8 organization
- JEDEC approved pin-out
- Low Power
  —Active: 132 mW (max.)
  —Standby: 525 μW (max.)
- Access times: 350 ns, 450 ns and 550 ns (max.)
- Single 5V power supply
- Static operation, no clocks required
- Inputs and tri-state outputs TTL compatible during both read and program mode
- Pin compatible with INTEL 2732A EPROM and Rockwell R2332B ROM.

ORDERING INFORMATION

Part Number: R87C32__

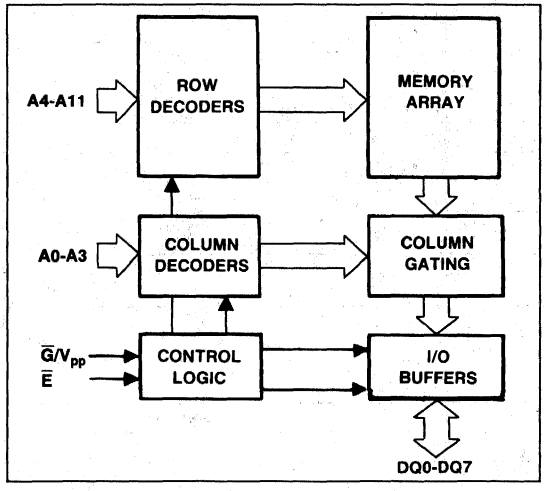
Access Time:
35 = 350 ns
45 = 450 ns
55 = 550 ns

DESCRIPTION

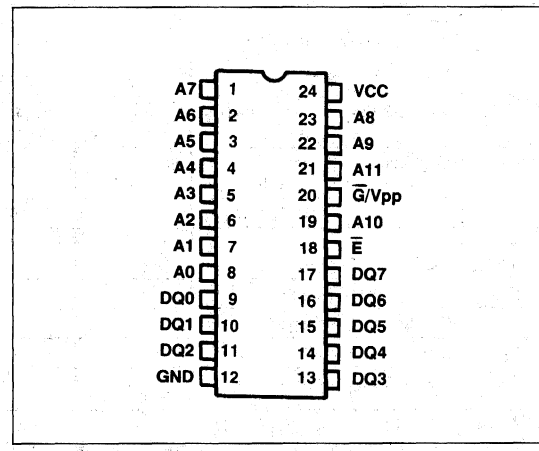
The Rockwell R87C32 is a 4K x 8 (32,768 bits) ultraviolet (UV) light erasable programmable read-only-memory (EPROM). It is manufactured using CMOS technology for low power dissipation in both active and standby operating modes. Single 5V operation allows simple circuit design in runtime environments.

Initially, all bits are in the "1" state. Programming is performed by applying 21V to $\overline{G}$/Vpp and a 50 ms low level pulse to $\overline{E}$ while the desired data is stable on DQ0-DQ7 lines and the address is stable on A0-A11 lines. All bits may be erased to the "1" state by exposure to a UV light source through the transparent window on the top of the device package.

The R87C32 EPROM is ideal for system development or low volume production applications requiring non-volatile memory in either multiple chip or single chip microcomputers with extended bus configurations. The low power requirements especially support applications using the R65C00 CMOS Microcomputer device family.



R87C32 Block Diagram



R87C32 Pin Configuration

A0-A11	ADDRESSES
$\overline{E}$	CHIP ENABLE
$\overline{G}$/Vpp	OUTPUT ENABLE/PROGRAM
DQ0-DQ7	DATA INPUT/OUTPUT

R87C32 Pin Names

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage All, except Vpp during Programming Vpp during Programming	V_{IN}	 −0.3 to V_{CC} +0.3 −0.3 to +22.0	Vdc
Output Voltage	V_{OUT}	−0.3 to V_{CC} +0.3	Vdc
Temperature under Bias	T_A	−10 to +80	°C
Storage Temperature	T_{STG}	−40 to 125	°C
Power Dissipation @ 25°C	P	1.0	W

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Read Mode	Program Mode
V_{CC} Supply Voltage	5V ±5%	5V ±5%
V_{PP} Supply Voltage		21V ±0.5V
Temperature Range	0 to 70°C	0 to 70°C

DC OPERATING CHARACTERISTICS DURING READ

V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4		—	V	I_{OH} = −400 μA
V_{OL}	Output Low Voltage	—		0.45	V	I_{OL} = 2.1 mA
V_{IH}	Input High Voltage	2.0		V_{CC} +0.3	V	
V_{IL}	Input Low Voltage	−0.1		0.8	V	
I_{CC1}	V_{CC} Active Current TTL Level Address Inputs		2	10	mA	$\overline{E}$ = $\overline{G}$ = V_{IL} V_{IN} = V_{IH} or V_{IL} Frequency = 1 MHz, I/O = 0 mA
	CMOS Level Address Inputs		1	7	mA	$\overline{E}$ = $\overline{G}$ = V_{IL} V_{IN} = GND or V_{CC} Frequency = 1 MHz, I/O = 0 mA
I_{CC2}	V_{CC} Standby Current TTL Level Chip Enable		0.1	1	mA	$\overline{E}$ = V_{IH}
	CMOS Level Chip Enable		10	100	μA	$\overline{E}$ = V_{CC}
I_{PP}	V_{PP} Supply Current			30	mA	$\overline{E}$ = V_{IL}, $\overline{G}/V_{PP}$ = V_{PP}
I_{IN}	Input Leakage Current			±10	μA	V_{IN} = 0V to V_{CC}
I_O	Output Leakage Current			±10	μA	V_{OUT} = 0V to V_{CC}
C_I	Input Capacitance[1]			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C f = 1 MHz
C_O	Output Capacitance[1]			10	pF	

Notes:
1. This parameter is periodically sampled and is not 100% tested.

DC OPERATING CHARACTERISTICS DURING PROGRAM

V_{CC} = 5.0V ±5%, T_A = −20°C to 30°C, V_{PP} = 21.0V ±0.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.1		0.8	V	
I_{CC}	V_{CC} Active Current	—		25	mA	$\overline{E}$ = V_{IL}, $\overline{G}$ = 21V
I_{PP}	V_{PP} Active Current	—		30	mA	$\overline{E}$ = V_{IL}, $\overline{G}$ = 21V
I_{IN}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}

AC CHARACTERISTICS DURING READ

V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R87C32-35		R87C32-45		R87C32-55		Unit	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVQV}	Address to Data Valid		350		450		550	ns	$\overline{E} = \overline{G} = V_{IL}$
t_{ELQV}	Chip Enable to Data Valid		350		450		550	ns	$\overline{G} = V_{IL}$
t_{GLQV}[2]	Output Enable to Data Valid		120		120		120	ns	$\overline{E} = V_{IL}$
t_{GHQZ}[3]	Output Enable to High Impedance	0	100	0	100	0	100	ns	$\overline{E} = V_{IL}$
t_{AXQX}	Address to Output Hold	0		0		0		ns	$\overline{E} = \overline{G} = V_{IL}$
t_{EHQZ}	Chip Enable to High Impedance	0	100	0	100	0	100	ns	$\overline{G} = V_{IL}$

Notes:
1. Test Conditions
   Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤20 ns
   Input Pulse Levels: 0.45V to 2.4V
   Timing Measurement Reference Level: Inputs 1V and 2V
   Outputs 0.8V and 2V
2. $\overline{G}$ may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without impact on t_{AVQV}. Data is available at the DQ outputs after a delay of t_{GLQV} from the falling edge of $\overline{G}$, provided that $\overline{E}$ has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.
3. t_{GHQZ}, t_{EHQZ} are specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

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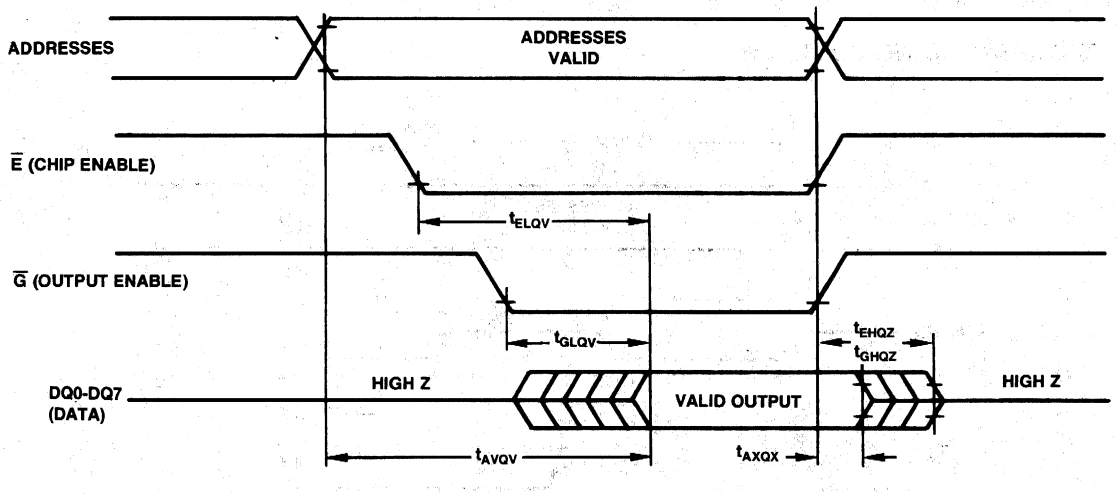
READ TIMING DIAGRAM



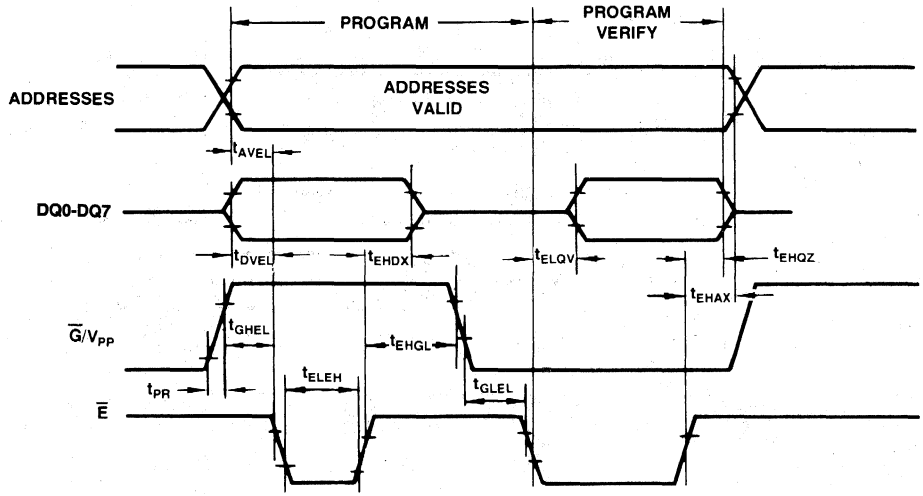
AC CHARACTERISTICS DURING PROGRAM

V_{CC} = 5.0V ±5%, T_A = 20°C to 30°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AVEL}	Address set-up time	2			μs
t_{GHEL}	$\overline{G}$ set-up time	2			μs
t_{DVEL}	Data set-up time	2			μs
t_{EHAX}	Address hold time	0			μs
t_{EHGL}	$\overline{G}$ hold time	2			μs
t_{EHDX}	Data hold time	2			μs
t_{EHQZ}	Output disable to output Hi-Z delay	0		100	ns
t_{ELQV}	Data valid from $\overline{E}$			1	μs
t_{ELEH}	$\overline{E}$ pulse width during programming	45	50	55	ms
t_{PR}	$\overline{G}$ pulse rise time during programming	50			ns
t_{GLEL}	V_{PP} recovery time	2			μs

Notes:
Test Conditions:
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level: Inputs 1V and 2V
Outputs 0.8V and 2V

PROGRAM TIMING DIAGRAM



OPERATING MODES

The Rockwell R87C32 has five modes of operation (see table 1) and is pin compatible with Intel's 2732A.

READ MODE

The read mode is governed by two control pins, $\overline{E}$ and $\overline{G}$. In order to obtain data at the outputs, both $\overline{E}$ and $\overline{G}$ must be V_{IL}. $\overline{E}$ is the power control and should be used for device selection. $\overline{G}$ is the output control and should be used to gate data to the output pins. Valid data will appear on the output pins after T_{AVQV}, T_{GLQV} or T_{ELQV} times, depending on which is limiting.

STANDBY MODE

The standby mode of the R87C32 reduces power dissipation. The R87C32 is placed in the standby mode by making $\overline{E} = V_{IH}$. This is independent of $\overline{G}$ and automatically puts the outputs in their high impedance (High-Z) state.

PROGRAM MODE

The R87C32 is in the program mode when G/V_{PP} is at 21V. The data to be programmed is applied to the data output pins. When the address controls and data are stable, a 50 msec program pulse is applied to the $\overline{E}$ input.

PROGRAM VERIFY MODE

A program verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with $\overline{G}/V_{PP}$ and $\overline{E}$ at V_{IL}. Data should be verified to t_{ELQV} after the falling edge of $\overline{E}$.

PROGRAM INHIBIT MODE

The program inhibit mode allows programming several R87C32 EPROMs simultaneously with different data for each by using $\overline{E}$ to control which devices respond to the program pulse on $\overline{E}$.

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Table 1. Mode Selection

Pin / Mode	$\overline{E}$ (18)	G/V_{PP} (20)	V_{CC} (24)	DQ0-DQ7 (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	No Effect	+5	High-Z
Program	Pulsed V_{IH} to V_{IL}	V_{PP}	+5	D_{In}
Program verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program inhibit	V_{IH}	V_{PP}	+5	High-Z
Note: No Effect = No effect on selection/enable logic, however, no voltage other than logic levels shall be applied.				

ERASURE PROCEDURE

Initially, and after each erasure by ultraviolet light, all bits of the R87C32 are in the "1" state. In Program Mode, "0"s are selectively programmed into the desired bit locations. The only way to change a "0" to a "1" is by ultra-violet light erasure.

The recommended erasure procedure for the R87C32 is exposure to ultra-voilet light wqhich has a wavelength of 2537 Angstroms.

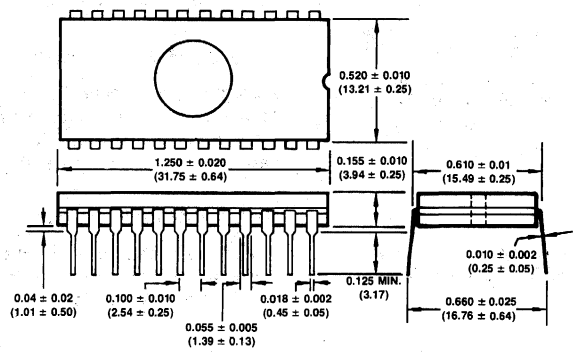
The integrated dose for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is 20 minutes using an ultraviolet lamp with a 12000 uW/cm^2 power rating.

Caution

The erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms. Sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Angstroms range.

PACKAGE DIMENSIONS

24-PIN CERDIP



DIMENSIONS IN INCHES AND (MILLIMETERS)