2048 WORD x 8 BIT EPROM

N CHANNEL SILICON STACKED GATE MOS.

TMM323D
TMM323D-1

DESCRIPTION

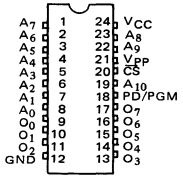
The TMM323D is a 2048 word x 8 bit ultraviolet erasable and electrically programmable read only memory For read operation it requires a single 5-volt power supply only The maximum active power dissipation is 525mW while the maximum standby power dissipation is only 132mW, a 75% savings Programming can be executed by applying 25-volt and 5-volt at the Vpp and Vcc terminals respectively, and applying a TTL level signal at the other input terminals Programming the one bit location requires only a single pulse, and it is possible to program sequentially, individually or at random Under the condition Vpp = 25V, read operation is permitted in the program verify mode, and also programming is inhibitted by selecting the program inhibit mode

The TMM323D is fabricated with the N-channel silicon double layer gate MOS technology and is packaged in a standard 24-pin dual-in-line cerdip package

FEATURES

- Single.5-volt power supply
- Access time TMM323D , 450ns (MAX)
  TMM323D-1, 350ns (MAX)
  Current 100 mA (active)
  25mA (standby)
- Three state output
- Particular bit location programming
- Programs with one 50ms pulse
- Total programming time 100 second
- Inputs and outputs TTL compatible during read and program
- Pin to pin compatible to.2716 type EPROM

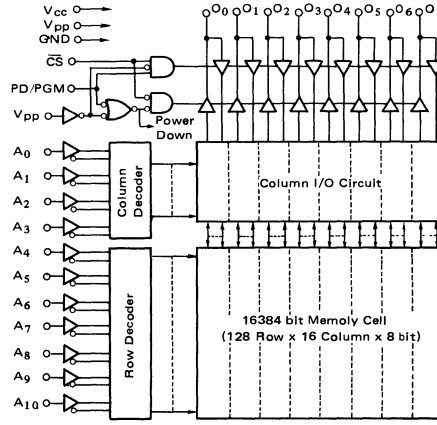
PIN CONNECTION



PIN NAMES

$A_0 - A_{10}$	Addresses
$O_0 - O_7$	Outputs
$\overline{CS}$	Chip Select
PD/PGM	Power down/ Program
Vcc, Vpp	Power Supply
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

PINS / MODE	PD/PGM (18)	$\overline{CS}$ (20)	Vpp (21)	Vcc (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	5V	5V	D out
Deselect	*	V_{IH}	5V	5V	High Z
Power Down	V_{IH}	*	5V	5V	High Z
Program	V_{IH} / V_{IL}	V_{IH}	25V	5V	D in
Program Verify	V_{IL}	V_{IL}	25V	5V	D out
Program Inhibit	V_{IL}	V_{IH}	25V	5V	High Z

* V_{IL} or V_{IH}

MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
V_{CC} Supply Voltage with respect to Ground	V_{CC}	−0 3 ~ +7	V
V_{PP} Supply Voltage with respect to Ground	V_{PP}	−0.3 ~ +26 5	V
All Input Voltages with respect to Ground	V_{IN}	−0 3 ~ +7	V
All Output Voltages with respect to Ground	V_{OUT}	−0 3 ~ +7	V
Power Dissipation	P_D	1 5	W
Soldering Temperature Times	T_{SOLDER}	260·10	°C · sec
Storage Temperature	T_{STG}	−65 ~ +125	°C
Operating Temperature	T_{OPR}	0 ~ 70	°C

READ OPERATION

D.C. and A.C. OPERATING CONDITIONS

PARAMETER	SYMBOL		MIN.	TYP	MAX	UNIT
Power supply	V_{CC} (1, 2)	TMM323D	4 75	5	5 25	V
		TMM323D-1	4 5	5	5 5	V
Power supply	V_{PP} (2)		V_{CC}−0 6	5	V_{CC} + 0 6	V

D.C. and OPERATING CHARACTERISTICS

Ta = 0 ~ 70°C

PARAMETER	SYMBOL	MIN	TYP (3)	MAX	UNIT	CONDITIONS
Input Load Current	I_{LI}			±10	μA	V_{IN} = 5 25V
Output Leakage Current	I_{LO}			±10	μA	V_{OUT} = 5 25V/0 45V
V_{PP} Current (Read)	I_{PP_1}			5	mA	V_{PP} = 5 85V
V_{CC} Current (Standby)	I_{CC_1}		10	25	mA	PD/PGM = V_{IH}, $\overline{CS}$ = V_{IL}
V_{CC} Current (Active)	I_{CC_2}		57	100	mA	PD/PGM = $\overline{CS}$ = V_{IL}
Input Low Voltage	V_{IL}	−0 1		0 8	V	
Input High Voltage	V_{IH}	2 0		V_{CC} + 1	V	
Output Low Voltage	V_{OL}			0 45	V	I_{OL} = 2 1mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA

A.C. CHARACTERISTICS

Ta = 0 ~ 70°C, V_{PP} = V_{CC} ± 0.6V

PARAMETER	SYMBOL	TMM323D		TMM323D-1		UNIT	CONDITIONS
		MIN.	MAX	MIN.	MAX		
Address to Output Delay	t_{ACC_1}		450		350	ns	PD/PGM = $\overline{CS}$ = V_{IL}
PD/PGM to Output Delay	t_{ACC_2}		450		350	ns	$\overline{CS}$ = V_{IL}
Chip Select to Output Delay	t_{CO}		120		120	ns	PD/PGM = V_{IL}
PD/PGM to Output Float	t_{PF}	0	100	0	100	ns	$\overline{CS}$ = V_{IL}
Chip Deselect to Output Float	t_{DF}	0	100	0	100	ns	PD/PGM = V_{IL}
Address to Output Hold	t_{OH}	0		0		ns	PD/PGM = $\overline{CS}$ = V_{IL}

- **A.C. Test Conditions**
- Output Load 1TTL + 100pF
  Input Rise and Fall Times (10% ~ 90%) ≦ 20ns
- Input Pulse Levels V_{IL} = 0.8V, V_{IH} = 2.2V
- Timing Measurement Reference Level Inputs 1V & 2V, Outputs 0 8V & 2V

(Note 4)

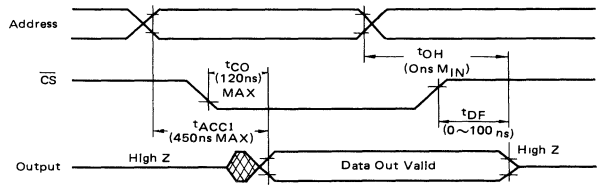
CAPACITANCE

Ta = 25°C, f = 1MHz

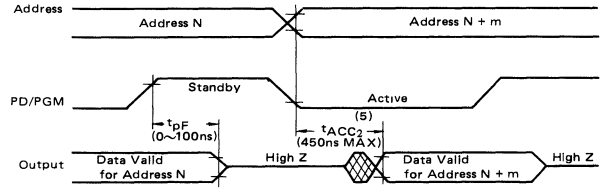
PARAMETER	SYMBOL	LIMITS			UNIT	CONDITIONS
		Min	Typ	Max		
Input Capacitance	C_{IN}		4	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{out} = 0V

TIMING WAVEFORMS (READ)

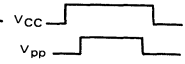
A. Read Mode PD/PGM = V_{IL}



B. Standby Mode $\overline{CS}$ = V_{IL}



Note 1 V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}



2 The V_{PP} terminal is permitted to connect the V_{CC} terminal directly during non-programming

3 Typical values are at Ta = 25°C and nominal supply voltages

4 This parameter is periodically sampled and is not 100% tested

5 The $t_{ACC}2$ is a output data delay time (i e access time) from address or PD/PGM whichever changes late

PROGRAM OPERATION

Ta = 25°C ± 5°C, V_{CC} = 5V ± 5%, V_{PP} = 25V ± 1V (Note 1, 2, 3)

D.C. PROGRAMMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	CONDITIONS
Input Current	I_{LI}			±10	μA	V_{IN} = 5 25V/0 45V
V_{PP} Supply Current	I_{PP_1}			5	mA	PD/PGM = V_{IL}
V_{PP} Supply Current During Programming Pulse	I_{PP_2}			30	mA	PD/PGM = V_{IH}
V_{CC} Supply Current	I_{CC}			100	mA	I_{OUT} = 0 mA
Input Low Level	V_{IL}	−0 1		0 8	V	
Input High Level	V_{IH}	2 0		V_{CC} + 1	V	

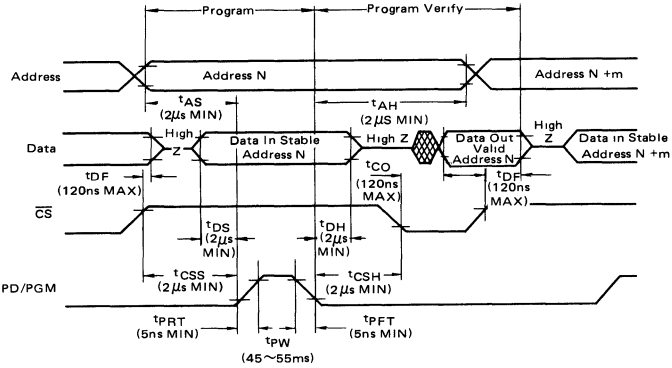
A.C. PROGRAMMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{CS}$ Setup Time	t_{CSS}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
$\overline{CS}$ Hold Time	t_{CSH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Chip Deselect to Output Float Delay	t_{DF}	0		120	ns	PD/PGM = V_{IL}
Chip Select to Output Delay	t_{CO}			120	ns	PD/PGM = V_{IL}
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	5			ns	
Program Pulse Fall Time	t_{PFT}	5			ns	

- **A.C. Test Conditions**
- Input Rise and Fall Times (10% ~ 90%) ≦ 20ns
- Input Pulse Levels V_{IL} = 0.8V, V_{IH} = 2.2V
  Timing Measurement Reference Level Input 1V & 2V, Output 0.8V & 2V

TIMING WAVEFORMS (PROGRAM)

V_{PP} = 25V ± 1V, V_{CC} = 5V ± 5%



Note 1 V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}

2 Sometimes removing the device from socket and setting the device in socket under the condition V_{PP} = 25V ± 1V may destroy its device, so it should be noted during programming

3 V_{PP} supply voltage is permitted up to 26V programming, so the voltage over 26V should not be applied to V_{PP}
Particularly when switching pulse voltage is applied to V_{PP}, also the over-shoot voltage of its pulse should not be exceeded 26-volt

ERASURE CHARACTERISTICS

The TMM323D's memory cell data can be erased by applying light with wavelengths shorter than 4000 Å. (1Å = 10^{-8} cm)
Sunlight and the fluorescent lamps may include 3000 ~ 4000 Å wavelength components

Therefore when used under such lighting for extended periods of time, an opaque seal (Toshiba EPROM Protecting Seal AC 901 etc) will be required to protect the TMM323D Generally, ultraviolet light with a wavelength of 2537 Å is recommended for TMM323D-erasing, and in this case the integrated dose (ultraviolet light intensity [w/cm²] x time [sec]) should be over 15 [w sec/cm²]

When Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1-cm from the lamp surface, erasure should be completed in about 60 minutes

And using a lamp whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes
(In this case the integrated dose should be 12000 [μw/cm²] x (20 x 60) [sec] ≅ 15 [w sec/cm²])

OPERATING INFORMATION

TMM323D-operation-modes are classified into six types, as shown in the following table Each mode can be selected by TTL level signals only The V_{CC} and V_{PP} power supplies required are only 5-volt for read operation, and the V_{PP} power supply required is 25-volt during program operation only.

MODE \ PINS		PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11, 13-17)
Read Operation	Read	V_{IL}	V_{IL}	5V	5V	D out
	Deselect	*	V_{IH}	5V	5V	High Z
	Power Down	V_{IH}	*	5V	5V	High Z
Program Operation	Program	V_{IH} / V_{IL}	V_{IH}	25V	5V	D in
	Program Verify	V_{IL}	V_{IL}	25V	5V	D out
	Program Inhibit	V_{IL}	V_{IH}	25V	5V	High Z

* V_{IL} or V_{IH}

Read Mode

Assuming that PD/PGM = V_{IL} and $\overline{CS}$ = V_{IL}, the output data is available within t_{ACC1} (MAX.) after stabilizing of the address.
And assuming that PD/PGM = V_{IH} or $\overline{CS}$ = V_{IH}, the outputs will become high impedance in state.

When all addresses are in the fixed state and $\overline{CS}$ = V_{IL}, the output data is available within t_{ACC2} (MAX) after the PD/PGM input is changes to V_{IL} from the V_{IH} level (Outputs change to data available state from a high impedance state)

When all addresses are in the fixed state and PD/PGM = V_{IL}, the output data is available within t_{CO} (MAX) after the $\overline{CS}$ input is changed to V_{IL} from the V_{IH} level (Outputs change to data available state from a high impedance state.)

Deselect Mode

Assuming that $\overline{CS}$ = V_{IH}, the outputs will be in a high impedance state So two or more TMM323Ds may be tied together on the same data bus And the $\overline{CS}$ input of the selected chip must be at the V_{IL} level, and that of the other chip must be at the V_{IH} level

Power Down Mode

Assuming that PD/PGM = V_{IH}, the power dissipation will be reduced to one-fourth of normal active power. (i.e. 525mW → 132mW)
Then all outputs will become high impedance in state independent of the $\overline{CS}$ input level

Program Mode

Initially when received by customers all bits of the TMM323D are in the "1" state which is the erased state

Therefore programming is carried out by electrically writing in the "0" state at the desired bit locations

Programming can be completed by applying the TTL level pulse signal with a pulse width of from 45 to 55 ms to PD/PGM input under the condition where V_{PP} = 25V and $\overline{CS}$ = V_{IH}

Programming the TMM323D is permitted in any sequence and also at any particular bit location

But the PD/PGM pulse width applied at one bit location should be over 45ms up to 55ms, and rewriting into the written location is not permitted

When programming is carried out by applying a DC voltage (V_{IH} level) instead of a pulse to the PD/PGM input, erroneous writing may occur sometimes, so a pulse whose recommended width is 50ms should be used in programming.

Programming the same data to two or more TMM 323Ds simultaneously can be accomplished by connecting the respective pins together

Program Verify Mode

In this mode the V_{PP} power supply is 25V

But assuming that PD/PGM = V_{IL} and $\overline{CS}$ = V_{IL}, it can be possible to read written data

For normal read operation, the V_{PP} power supply voltage required is 5V

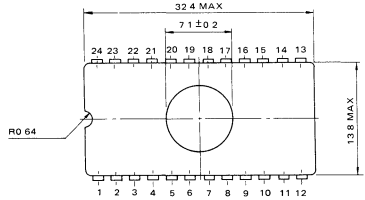
Program Inhibit Mode

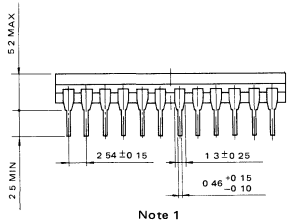
Assuming that PD/PGM = V_{IL} and $\overline{CS}$ = V_{IH} under V_{PP} = 25V, it is able to inhibit the programming

According to the above, programming into two or more TMM323Ds mounted on a board will be possible

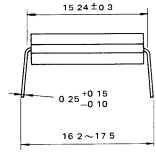
Programming into a desired chip tied on a common bus line independently is possible by connecting all respective inputs except PD/PGM together and applying a pulse to the PD/PGM input of a desired chip and applying DC voltage at the V_{IL} level to the PD/PGM inputs of the other chip.

OUTLINE DRAWINGS





Note 1



Note 2

Note
1 Each lead pitch is 2.54 mm All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 24 leads
2 This value is measured at the end of leads
3 All dimensions are in millimeters

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