4096 WORD x 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE ROM

TMM2732D

N CHANNEL SILICON STACKED GATE MOS

DESCRIPTION

The TMM2732D is a 4096 word x 8 bit ultraviolet light erasable and electrically programmable read only memory For read operation, the TMM2732D's maximum access time is 350 ns, and the TMM2732D operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input The maximum active current is 150 mA and the maximum standby current is 25 mA

For program operation, the programming is achieved by applying a 50 ms active TTL low program pulse to the $\overline{CE}$ input, and it is possible to program sequentially, individually, or at random

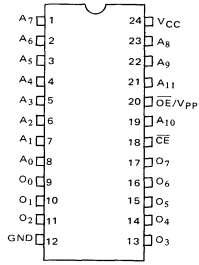
The TMM2732D is fabricated with the N-channel silicon double layer gate MOS technology and is packaged in a standard 24 pin dual in line cerdip package

FEATURES

- Single 5-volt power supply
- Fast access time 350 ns Max
- Power dissipation
  - 150 mA Max (active current)
  - 25 mA Max (standby current)
- Low power standby mode $\overline{CE}$
- Output buffer control $\overline{OE}$
- Fully static operation
- Programs with one 50 ms pulse
- Single location programming
- Total programming time about 200 second
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2732 and ROM TMM2332P

PIN CONNECTION

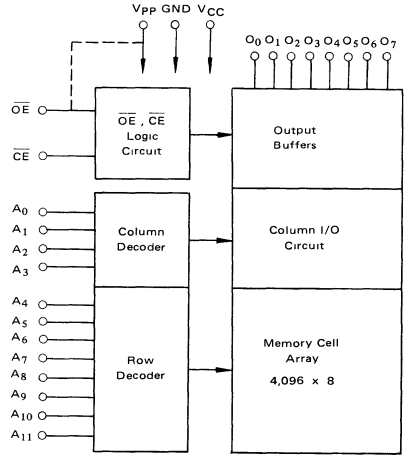
(TOP VIEW)



PIN NAMES

$A_0 \sim A_{11}$	Address Inputs
$O_0 \sim O_7$	Data Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$ / V_{PP}	Output Enable Input/Program Power
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MODE SELECTION

MODE \ PINS (No)	$\overline{CE}$ (18)	$\overline{OE}$ / V_{PP} (20)	V_{CC} (24)	Outputs (9 – 11, 13 - 17)
Read	V_{IL}	V_{IL}	+5V	D_{OUT}
Output Deselect	*	V_{IH}	+5V	High Impedance
Standby	V_{IH}	*	+5V	High Impedance
Program	V_{IL}	V_{PP}	+5V	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5V	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5V	High Impedance

* V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Supply Voltage	–0 3 ~ 7 0	V
$\overline{OE}$ / V_{PP}	Program Supply Voltage	–0 3 ~ 26 5	V
V_{IN}	Input Voltage	–0 3 ~ 7 0	V
V_{OUT}	Output Voltage	–0 3 ~ 7 0	V
P_D	Power Dissipation	1 6	W
T_{SOLDER}	Soldering Temperature Time	260 10	°C sec
T_{STRG}	Storage Temperature	–65 ~ 125	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	V_{CC} Supply Voltage	4 75	5 0	5 25	V
V_{IH}	Input High Voltage	2 0	–	V_{CC} + 1 0	V
V_{IL}	Input Low Voltage	–0 3	–	0 8	V

D.C. and OPERATING CHARACTERISTICS

(Ta = 0 ~ 70°C, V_{CC} = 5V ± 5%, unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{LI}	Input Load Current	V_{IN} = 0 ~ 5 25V	–	–	± 10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 4 ~ 5 25V	–	–	± 10	μA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE}$ = V_{IH}	–	–	25	mA
I_{CC2}	V_{CC} Current (Active)	$\overline{CE}$ = V_{IL}	–	–	150	mA
V_{OL}	Output Low Voltage	I_{OL} = 2 1 mA	–	–	0 4	V
V_{OH}	Output High Voltage	I_{OH} = –400 μA	2 4	–	–	V

A.C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNIT
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	–	–	350	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	–	–	350	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	–	–	120	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$	0	–	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	0	–	100	ns
t_{OH}	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	–	–	ns

A.C. TEST CONDITIONS

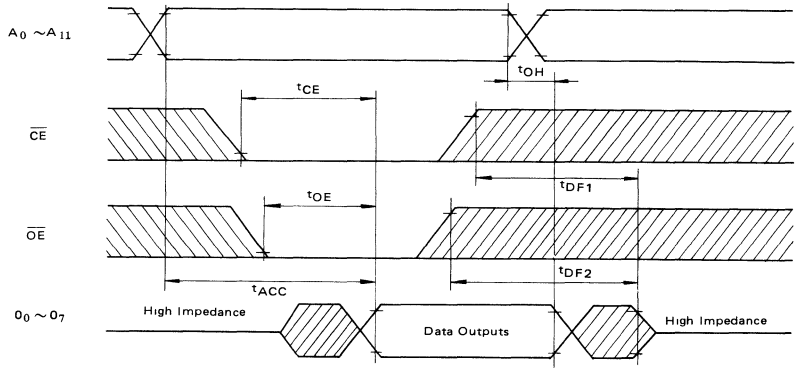
Output Load	1TTL Gate and C_L (100 pF)
Input Pulse Rise and Fall Times	$\leqq$ 20 ns
Input Pulse Levels	0.8 ~ 2.2V
Timing Measurement Reference Level	Inputs 1V and 2V
	Outputs 0.8V and 2V

CAPACITANCE * (Ta = 25°C, f = 1MHz)

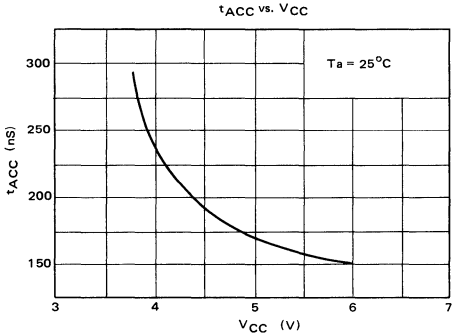
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	–	–	6	pF
C_{IN2}	Input Capacitance ($\overline{OE}/V_{PP}$)	$V_{IN} = 0V$	–	–	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	–	–	12	pF

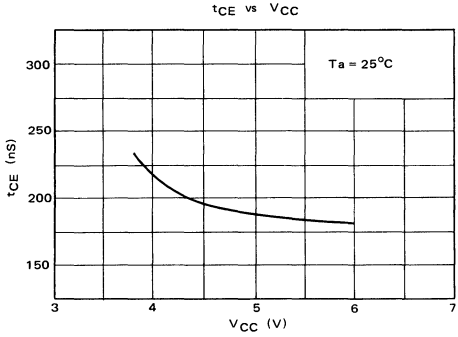
* This parameter is periodically sampled and is not 100% tested

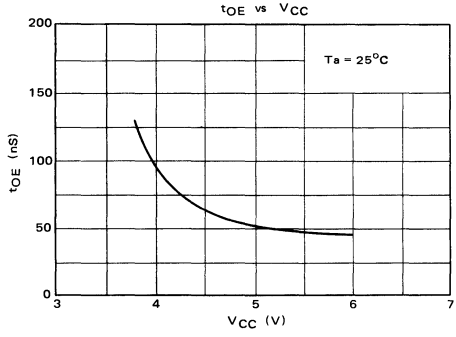
TIMING WAVEFORMS (READ)

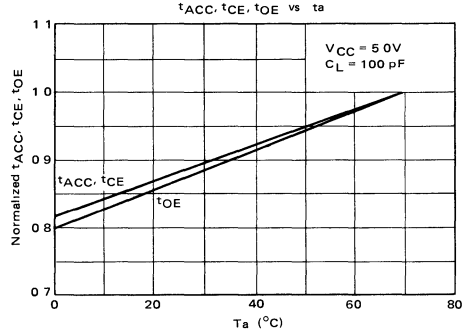


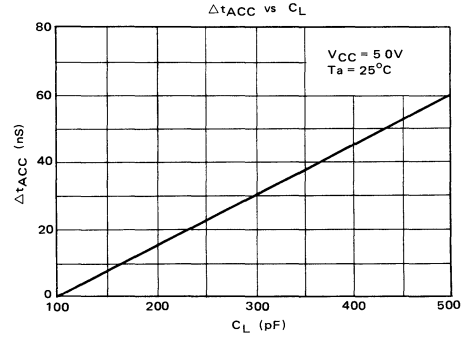
TYPICAL CHARACTERISTICS

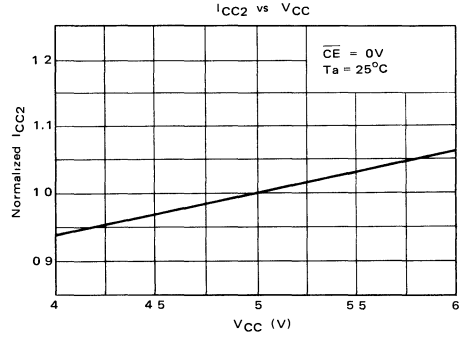


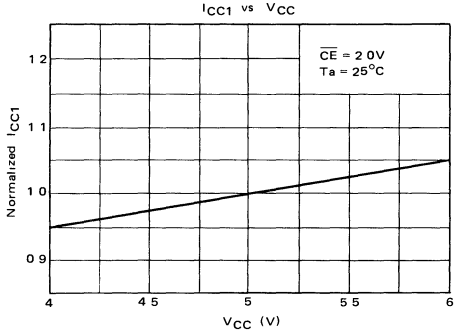


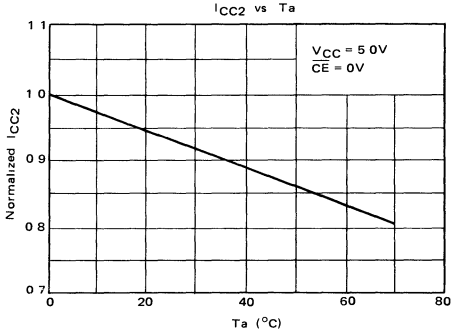


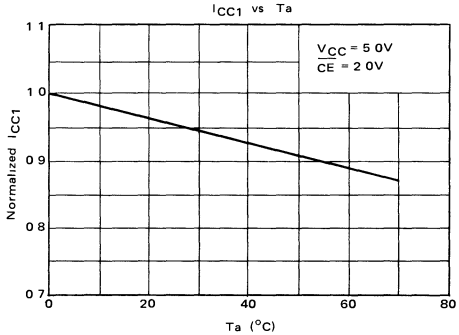


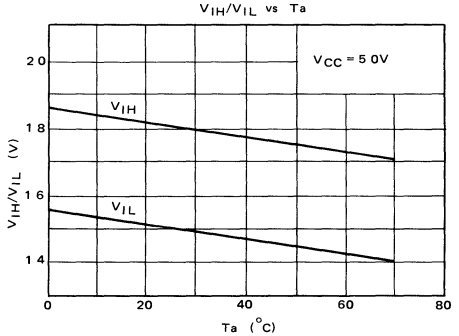





I_{CC1} vs V_{CC}
$\overline{CE}$ = 2.0V
Ta = 25°C
Normalized I_{CC1}
1.2
1.1
1.0
0.9
4
4.5
5
5.5
6
V_{CC} (V)


I_{CC2} vs Ta
V_{CC} = 5.0V
$\overline{CE}$ = 0V
Normalized I_{CC2}
1.1
1.0
0.9
0.8
0.7
0
20
40
60
80
Ta (°C)


I_{CC1} vs Ta
V_{CC} = 5.0V
$\overline{CE}$ = 2.0V
Normalized I_{CC1}
1.1
1.0
0.9
0.8
0.7
0
20
40
60
80
Ta (°C)


V_{IH}/V_{IL} vs Ta
V_{CC} = 5.0V
V_{IH}
V_{IL}
V_{IH}/V_{IL} (V)
2.0
1.8
1.6
1.4
0
20
40
60
80
Ta (°C)

PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage	2 0	–	V_{CC} + 1 0	V
V_{IL}	Input Low Voltage	–0 3	–	0 8	V
V_{CC}	V_{CC} Supply Voltage	4 75	5 0	5 25	V
V_{PP}	Program Input Voltage	24	25	26	V

D.C. PROGRAMMING CHARACTERISTICS

(Ta = 25 ± 5°C, V_{CC} = 5V ±5%, V_{PP} = 25V ±1V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{LI}	Input Current	V_{IN} = 0 ~ 5 25V	–	-	±10	μA
V_{OH}	Output High Voltage	I_{OH} = –400 μA	2 4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2 1 mA	–	–	0 4	V
I_{CC}	V_{CC} Supply Current	–	–	–	150	mA
I_{PP}	V_{PP} Supply Current	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{PP}	–	–	30	mA

A.C. PROGRAMMING CHARACTERISTICS

(Ta = 25 ± 5°C, V_{CC} = 5V ± 5%, V_{PP} = 25 ± 1V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{AS}	Address Set Up Time	2	–	–	μs
t_{OES}	$\overline{OE}$ Set Up Time	2	–	–	μs
t_{DS}	Data Set Up Time	2	–	–	μs
(1) t_{AH}	Address Hold Time	0	–	–	μs
t_{OEH}	$\overline{OE}$ Hold Time	2	–	–	μs
t_{DH}	Data Hold Time	2	–	–	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	–	–	100	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	–	350	ns
t_{PW}	Program Pulse Width	45	50	55	ms
t_{PRT}	V_{PP} Pulse Rise Time	50	–	–	ns
t_{VR}	V_{PP} Recovery Time	2	–	–	μs

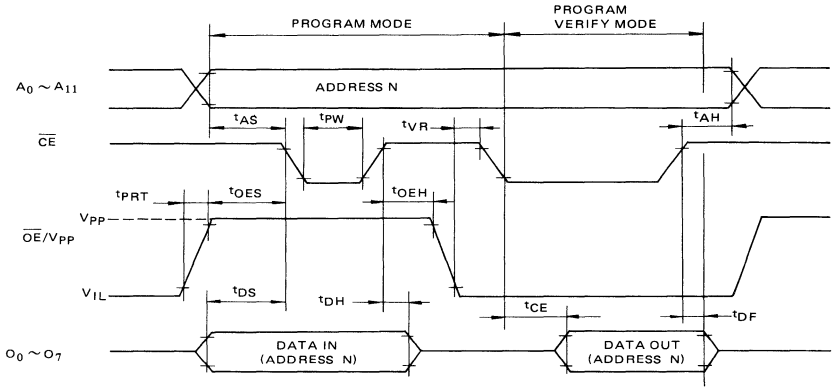
Note (1) t_{AH} (Program Operation 1) = 0 μs min
t_{AH} (Program Operation 2) = 2 μs min
Refer to Timing Waveforms

A.C. TEST CONDITIONS

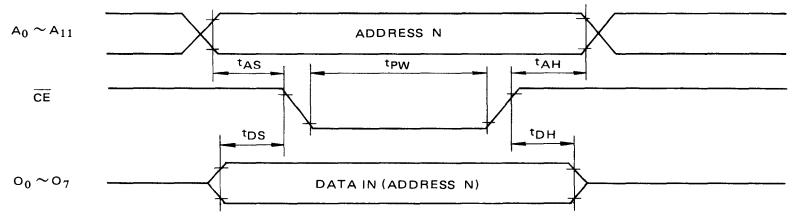
- Input Pulse Rise and Fall Times ≦ 20 ns
- Input Pulse Levels 0 8 ~ 2 2V
- Timing Measurement Reference Level — Inputs 1V & 2V
  Outputs 0 8V & 2 0V

TIMING WAVEFORMS (PROGRAM OPERATION)

Program Operation 1



Program Operation 2 ($\overline{OE}/V_{PP} = V_{PP}$)



NOTE 1 V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}

2 Sometimes removing the device from socket and setting the device in socket under the condition V_{PP} = 25V ± 1V may cause permanent damage to the device

3 The V_{PP} supply voltage is permitted up to 26V for program operation, so the voltage over 26V should not be applied to the V_{PP} input When the switching pulse voltage is applied to the V_{PP} input, the over-shoot voltage of its pulse should not be exceeded 26V

ERASURE CHARACTERISTICS

The TMM2732D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window Then integrated dose (ultraviolet light intensity [w/cm^2] x exposure time [sec]) for erasure should be a minimum of 15 [w sec/cm^2]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1 cm from the lamp surface, the erasure will be achieved within 60 minutes And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm^2] x (20 x 60) [sec] ≅ 15 [w sec/cm^2])

The TMM2732D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å The

sunlight and the fluorescent lamps will include 3000 ~ 4000Å wavelength components Therefore when used under such lighting for extended periods of time, the opaque seals — Toshiba EPROM Protect Seal AC901 — are available

OPERATION INFORMATION

The TMM2732D's six operation modes are listed in the following table Mode selection can be achieved by applying TTL level signal to all inputs except for $\overline{OE}/V_{PP}$ In the read operation mode, a signal 5-volt power supply is required and the levels required for all inputs are TTL

In the program operation mode the $\overline{OE}/V_{PP}$ is pulsed from a TTL level to 25V

MODE \ PINS (NO)		$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	$O_0 \sim O_7$ (9–11, 13–17)
READ OPERATION (Ta = 0 ~ 70°C)	READ	V_{IL}	V_{IL}	+5V	DATA OUTPUT
	OUTPUT DESELECT	*	V_{IH}	+5V	HIGH IMPEDANCE
	STANDBY	V_{IH}	*	+5V	HIGH IMPEDANCE
PROGRAM OPERATION (Ta = 25 ± 5°C)	PROGRAM	V_{IL}	V_{PP}	+5V	DATA INPUT
	PROGRAM VERIFY	V_{IL}	V_{IL}	+5V	DATA OUTPUT
	PROGRAM INHIBIT	V_{IH}	V_{PP}	+5V	HIGH IMPEDANCE

* V_{IH} or V_{IL}

READ MODE

The TMM2732D has two control functions Chip Enable ($\overline{CE}$) controls the operation power and should be used for device selection Output Enable ($\overline{OE}$) controls the output buffers, independent of device selection

Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs within address access time (350 ns max.) after stabilizing of the addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time

Assuming that $\overline{CE} = V_{IL}$ and addresses are stable, the output data is valid at the outputs within t_{OE} (120 ns max) after the falling edge of $\overline{OE}$

OUTPUT DESELECT MODE

Assuming that $\overline{OE} = V_{IH}$ or $\overline{CE} = V_{IH}$, the outputs will be in a high impedance state So two or more TMM2732Ds can be connected together on a common bus line When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode

STANDBY MODE

The TMM2732D has a low power standby mode controlled by $\overline{CE}$ signal By applying a TTL high level signal to the $\overline{CE}$ input, the TMM2732D is placed in the standby mode which reduce the operating current from 150 mA to 25mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ input

PROGRAM MODE

Initially, when received by customers, all bits of the TMM2732D are in the "1" state which is erased state Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming The TMM2732D is set up in the program operation mode when applied the program input voltage (+25V) to the $\overline{OE}/V_{PP}$ input under $\overline{CE} = V_{IH}$

Then programming is achieved by applying a 50 ms active low TTL program pulse to the $\overline{CE}$ input after the addresses and data are stable This program pulse should be a single pulse with 50 ms pulse width per address word, and its maximum value is 55 ms The levels required for the address and data inputs are TTL The TMM2732D can be programmed at any time individually, sequentially, or at random The TMM2732D must not be programmed with a DC signal applied to the $\overline{CE}$ input

PROGRAM VERIFY MODE

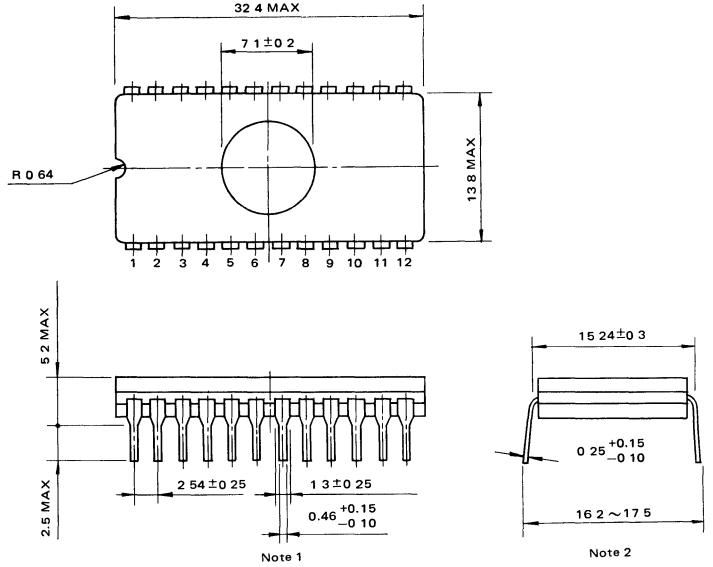
The verify mode is to check that the desired data is correctly programmed on the programmed bits The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL} Data should be verified within t_{CE} (350 ns max) after the falling edge of $\overline{CE}$

PROGRAM INHIBIT MODE

Under the condition that the program input voltage (+25V) is applied to the $\overline{OE}/V_{PP}$ input, a TTL high level $\overline{CE}$ input inhibits the TMM2732D from being programmed

Programming of two or more TMM2732Ds in parallel with different data is easily accomplished That is, all inputs except for $\overline{CE}$ are commonly connected, and the program pulse is applied to the $\overline{CE}$ input of the desired device only and the TTL high level signal is applied to the other devices

OUTLINE DRAWINGS



Note 1 Each lead pitch is 2 54 mm All leads are located within 0 25 mm of their true longitudinal position with respect to No 1 and No 24 leads

2 This value is measured at the end of leads

3 All dimensions are in millimeters