OM-O2 / OM-O2P

Onion Omega2 IoT modules

Data Sheet (Version 1.1)

Onion

Table of Contents

1. Overview

The Onion Omega2 is a Wi-Fi enabled, Linux-based development module, designed specifically for IoT applications. It provides a drop-in, low-power solution ideal for prototyping and building IoT hubs and devices.

It features a MIPS 24KEc processor running at 580 MHz, built-in DDR2 DRAM, flash storage, and a 2.4 GHz 802.11b/g/n Wi-Fi radio. It supports a wide variety of I/O protocols, with dedicated pins for USB 2.0 and ethernet, and 18 pins available to the developer. The module is self-contained and only requires a power supply to operate.

Measuring 42.9x26.4x9.9 mm, the Omega2 is a very small, self-contained, plug and play computing and connectivity device. It is a through-hole device, featuring 32 pins at a 2mm pitch. For prototyping and proof-of-concept work, it can be plugged into any of the Onion Omega2 Docks that provide ports, serial command line access, easy access to I/Os and more. At the next stage of development, custom hardware can be designed to accept the Omega2 depending on the end user's specific needs. Onion also provides the Omega2S, a surface-mount version of the Omega2, designed specifically for high volume production.

By virtue of the pre-loaded Linux operating system, developers can create their own applications using a programming language of their choice, and make use of existing network stacks and a rich set of software packages to implement their desired software functionality.

Key highlights:

- Wi-Fi enabled Linux-based module for IoT applications
- Dual mode 2.4 GHz 802.11 b/g/n Wi-Fi - simultaneously host a WiFi access point and connect to existing WiFi networks
- On-board WiFi antenna & U.FL connector for optional external antenna
- CPU, memory, and flash storage are built-in
- Runs OpenWRT Linux operating system out of the box
- Features USB, ethernet, MicroSD, 2x UARTs, I2C, SPI, GPIOs interfaces
- FCC and CE certified

Highlights on the software and operating system:

- The operating system is based on the OpenWRT Linux distribution
    - Support for modern programming languages: Python (2.7 and 3.6), NodeJS (8.10), GoLang, C, C++, and others
- The default device operating system image includes:
    - Onion's enhanced WiFi driver
    - A package manager (opkg)
    - A lightweight web server (uhttpd) and an extendable Remote Procedure Call daemon (RPCD and ubus)
    - Utilities to control the GPIOs (gpioctl, fast-gpio) and pin multiplexing (omega2-ctrl)
    - The sysfs interface for programmatic control of the hardware interfaces
    - OnionOS, a web-based, graphical user interface for the Omega2 family

The build system for creating an operating system image and software packages is open source, so developers can create their own customized operating system images tailored to their needs. It can be found on GitHub: https://github.com/OnionIoT/source.

Additionally, the source code for many software packages created by Onion can be found on GitHub: https://github.com/OnionIoT

This includes the Omega2 bootloader source code.

Extensive documentation can be found online on the Onion Docs site that describes technical details, software usage, and more.

1.1 Key Features

CPU	
Chipset	MT7688AN
Architecture	MIPS24KEc
Clock Speed	580MHz

Memory	
Flash	16MB (OM-O2) or 32MB (OM-O2P)
DDR2 DRAM	64MB (OM-O2) or 128MB (OM-O2P)

WIFI	
WiFi Protocol	IEEE 802.11 b/g/n
Base Band	2.4GHz
Data Rate	150 Mbit/s
Channel Bandwidth	20/40 MHz
Operation Mode	AP, STA, AP&STA
Encryption Mode	WEP64/128, AES, WPA, WPA2, WAP
On-board Antenna	2 dBi directional chip antenna
Antenna Connector	U.FL connector for optional external antenna

Interfaces	
Ethernet	1 (10M/100M)
USB 2.0 Host	1
SPI	1
I2C	1
I2S	1
UART	**2**
PWM	**2**
GPIO	**Up to 18**
SD	1x MicroSD slot *(OM-O2P only)*

Power Supply Requirement	
DC Input	3.3V
No-load Running Current	200±40mA
Peak Current Requirement	800mA sadfdsf

Operation Conditions	
Ambient Temperature	-10°C ~ 55 °C
Storage Temperature	-20°C ~ 80° C
Operating Humidity	10%-95%RH (Non-Condensing)
Storage Humidity	5%-95%RH (Non-Condensing)

Physical Specifications	
Dimensions	42.9*26.4*9.9 mm
Packaging	Through-hole
Pin Pitch	2mm
Total Pins	32

Additional specifications and operating details for the microprocessor in the Omega2 can be found in the Mediatek MT7688 Datasheet

1.2 Variants

Model	Name	RAM	Flash	Packaging
OM-O2	Omega2	64 MB	16 MB	Through-hole
OM-O2P	Omega2+	128 MB	32 MB	Through-hole

1.3 Differences from Omega2S Module

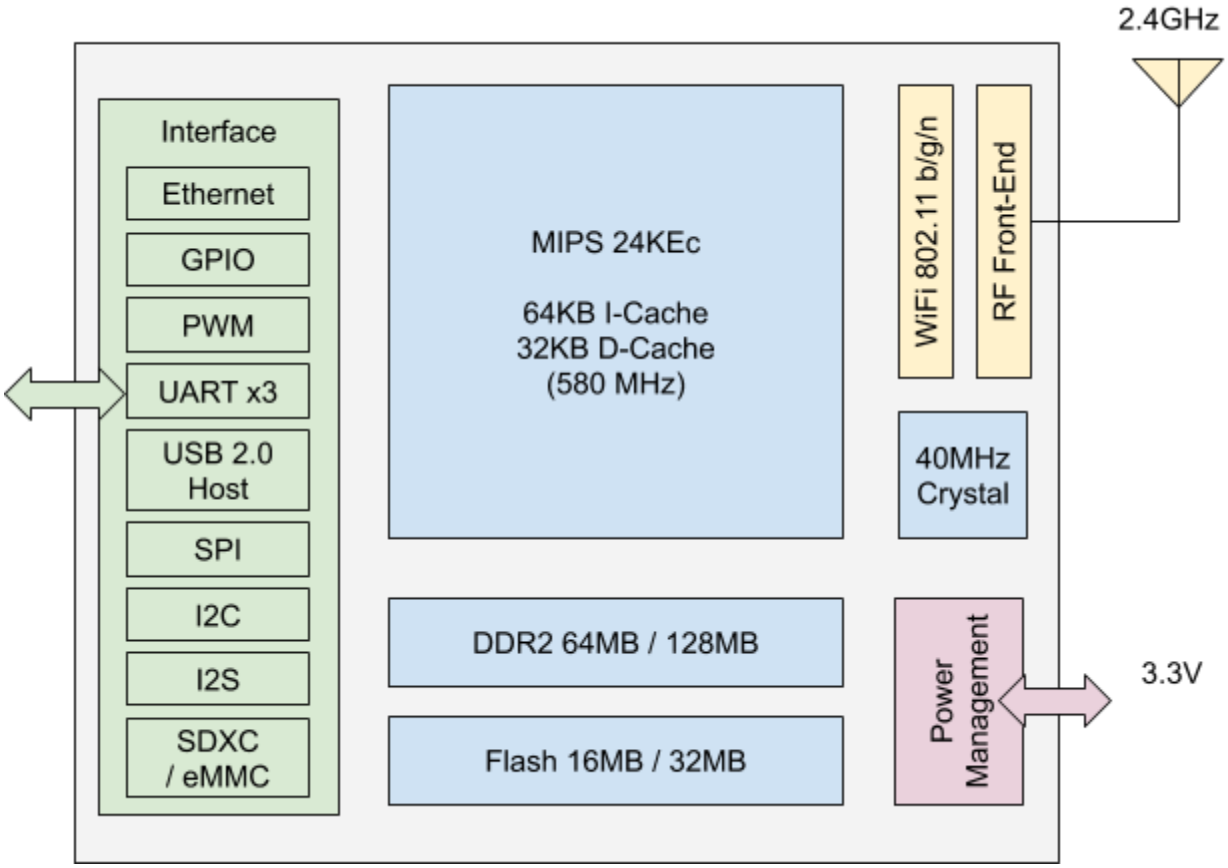
The Onion Omega2S is the surface-mount packaged version of the Omega2, designed specifically for high volume production due to its low profile, extended feature-set, and production friendly design.

The specific differences from the Omega2 are as follows:

- Surface-mount module form-factor
- Low profile, measuring 34x20x2.8 mm

- 63 total pins compared to 32 pins on Omega2
- Pins for SD/eMMC are available on the pinout - no MicroSD slot
- Features 3 UARTs, compared to 2 on the Omega2
- Features 4 PWM channels, compared to 2 on the Omega2
- Exposes SPI Chip-Select 0 (CS0) pin
- No on-board antenna - features Antenna signal pin and U.FL connector
- No on-board system status LED - features system status pin for connection to external LED

1.4 Block Diagram



2. Features

2.1 CPU

The processor is based on the MIPS architecture, it is a MIPS 24KEc, little-endian, 32-bit RISC core that operates at 580 MHz with a 64 KB Instruction Cache and 32 KB Data Cache.

2.2 Memory

Features on-board 16-bit DDR2 DRAM memory operating at 400 MHz

- Omega2 features 64 MB memory
- Omega2+ features 128 MB memory

2.3 Flash

Features on-board SPI flash storage that contains the bootloader, Linux OS, and WiFi calibration data.

- Omega2 features 24-bit addressed 16 MB flash storage
- Omega2+ features 32-bit addressed 32 MB flash storage

2.4 WiFi

The Omega supports 2.4 GHz IEEE 802.11 b/g/n WiFi with a maximum 150 Mbps PHY data rate. The embedded RF front-end is 1T1R, meaning that it is used for both transmitting and receiving by virtue of time-multiplexing.

The Omega's WiFi interface can simultaneously host its own WiFi Access Point while connecting to another WiFi network.

2.4.1 Antenna

The Omega2 features an on-board ceramic surface-mount chip antenna, it is a 2 dBi directional antenna.

The Omega2 also features a male, surface-mounted U.FL connector for use with external antennas. To exclusively use an external antenna, the device must be modified by removing a 0Ω resistor. Find the full procedure outlined in this article.

2.5 Interfaces

Describing the interfaces available on the Omega2 modules.

2.5.1 USB

There is one (1) USB 2.0 host controller available on dedicated pins.

Note 1: *A 5V power source needs to be supplied to the USB client device to properly operate.*
Note 2: *Special care needs to be taken to ensure the high-speed USB data lines are impedance matched when routing custom hardware for use with the Omega2.*
Note 3: *Use of an ESD protection device is recommended.*

2.5.2 SPI

One (1) SPI interface is available. The interface supports half-duplex transmissions and can operate in host-mode only. The maximum SPI clock frequency is 40 MHz.

The SPI interface features two Chip Select signals. The processor communicates with the on-board flash storage using the SPI protocol. The flash storage occupies SPI Chip Select 0, external devices can be connected to SPI Chip Select 1.

Note: *External devices connected to the SPI bus can affect the boot sequence under certain conditions. See section* ***3.3.2 - SPI Pins*** *for details.*

2.5.3 I2C

There is one (1) I2C controller available. The interface can operate in host-mode only. Standard (100kbps) and fast mode (400kbps) are supported. The I2C logic level is 3.3V.

2.5.4 I2S

The Omega2S has one (1) I2S interface available.

The I2S interface consists of two separate cores, a transmitter and receiver. Both can operate in either master or slave mode.

2.5.4.1 Features

- I2S transmitter / receiver, configurable as master or slave
- As slave: 24-bit data, sampling rates up to 192 kHz
- As master: 16-bit data, sampling rates of 8 kHz, 16 kHz, 22.05 kHz, 44.1 kHz, and 48 kHz
- Stereo audio data transfer
- 32-byte FIFO for transmission
- GDMA access
- 12 Mhz bit clock from external source (when in slave mode)

2.5.5 SDIO/eMMC

The Omega2+ (OM-O2P) features a spring-loaded slot for MicroSD cards on the bottom of the device. The Omega2 supports the SDXC specification for SD cards, with a maximum capacity of 2 TB and a maximum transfer speed of 300 MB/s.

2.5.6 Ethernet

The Omega2 has a single 10/100M Ethernet integrated PHY.

It is recommended that typical ethernet magnetics be used, however for very short runs (<5m) a

simpler approach using capacitive decoupling is possible. See the Omega2S reference schematic for details.

2.5.7 UART

There are two (2) 2-pin Serial UARTs available. The UART logic level is 3.3V.
The default bootloader and operating system use UART0 to provide serial command line access.

Note: *Both UARTs are UART Lite controllers that do not feature hardware flow control.*

2.5.7.1 Features

- All standard baud rates up to 345,600 b/s
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick or no parity
- 16-byte receive buffer
- 16-byte transmit buffer
- Loopback control for link fault isolation

2.5.8 PWM

There are two (2) PWM channels available. The maximum PWM signal frequency is 40 MHz.

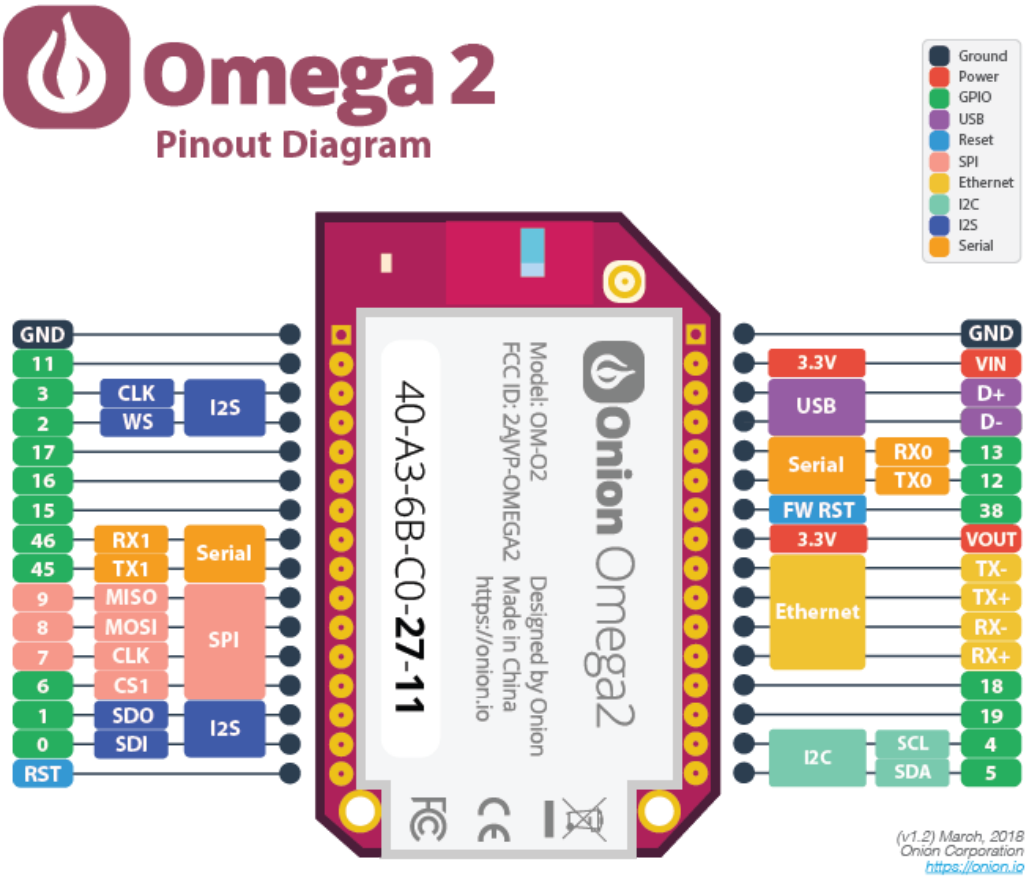
2.5.9 GPIO

Most pins on the module can be configured to operate as GPIO pins. The GPIO logic level is 3.3V and the pins can source or sink a maximum 8mA of current.

See the pin assignment section for details on GPIO capable pins.

3. Pin Definition

3.1 Pin Assignment



No	Name	I/O	Description
1	GND	I	Ground
2	GPIO_11	I/O	General Purpose I/O
3	GPIO_3 / I2S_CLK	I/O	General Purpose I/O / I2S Clock
4	GPIO_2 / I2S_WS	I/O	General Purpose I/O / I2S Word Select (also known as LRCLK - left/right clock)
5	GPIO_17	I/O	General Purpose I/O / 10/100 PHY Port #1 RXN
6	GPIO_16	I/O	General Purpose I/O / 10/100 PHY Port #1 RXP
7	GPIO_15	I/O	General Purpose I/O / 10/100 PHY Port #1 TXN
8	GPIO_46 / UART_RXD1	I/O	General Purpose I/O / UART1 Lite RXD
9	GPIO_45 / UART_TXD1	I/O	General Purpose I/O / UART1 Lite TXD
10	SPI_MISO	I	SPI Master Input/Slave Output
11	SPI_MOSI	O	SPI Master Output/Slave Input
12	SPI_CLK	O	SPI Clock
13	SPI_CS1 / GPIO6	O	SPI Chip Select 1 / General Purpose I/O
14	GPIO_1 / I2S_SDO	I/O	General Purpose I/O / I2S Data Output
15	GPIO_0 / I2S_SDI	I/O	General Purpose I/O / I2S Data Input
16	HW_RST		Hardware Power On Reset - Active Low Performs hard reset (power-cycle) of the CPU
17	I2C_SDA / GPIO_5	I/O	General Purpose I/O / I2C Data
18	I2C_SCL / GPIO_4	I/O	General Purpose I/O / I2C Clock
19	GPIO_19 / PWM_CH1	I/O	General Purpose I/O / PWM Channel 1
20	GPIO_18 / PWM_CH0	I/O	General Purpose I/O / PWM Channel 0
21	RXI_P0	I	10/100 PHY Port #0 RXP

22	RXI_N0	I	10/100 PHY Port #0 RXN
23	TXO_P0	O	10/100 PHY Port #0 TXP
24	TXO_N0	O	10/100 PHY Port #0 TXN
25	3.3V VOUT	O	3.3V Power Out
26	GPIO_38 / SW_RST	I/O	General Purpose I/O / Default User Button - Programmed to trigger a reboot in Onion Firmware - Active High
27	GPIO_12 / UART_TXD0	I/O	General Purpose I/O / Serial UART0 Lite TXD
28	GPIO_13 / UART_RXD0	I/O	General Purpose I/O / Serial UART0 Lite RXD
29	USB_DM	I/O	USB Port0 Differential Data -
30	USB_DP	I/O	USB Port0 Differential Data +
31	3.3V VIN	I	3.3V Power Supply
32	GND	I	Ground pin

Note：

The pins marked **Red** can affect system boot. See Section 3.2.1 for more details.

3.2 Special Pins

Information on pins with unique properties

3.2.1 - System Boot Pins

There are five (5) pins that affect the boot sequence of the device. The pins fall into two categories:

1. Pins that must be left **floating** at boot time. They cannot be pulled up or pulled down, or else the Omega cannot boot
2. Pins that must be **floating or pulled down** at boot time. They cannot be pulled up, or else the Omega cannot boot

Once the Omega has booted, these pins can be used normally.

No	Name	I/O	Description	Boot Time
9	GPIO_45 / UART_TXD1	I/O	General Purpose I/O / UART1 Lite TXD	Must be **floating**

14	GPIO_1 / I2S_SDO	I/O	General Purpose I/O / I2S Data Output	Must be **floating** or **pulled-down**
13	SPI_CS1	O	SPI Chip Select 1	Must be **floating**
12	SPI_CLK	O	SPI Clock	Must be **floating**
27	GPIO_12 / UART_TXD0	I/O	General Purpose I/O / Serial UART0 Lite TXD	Must be **floating** or **pulled-down**

3.2.2 - SPI Pins

The Omega's processor communicates with the on-board flash storage using the SPI protocol. It's physically connected as Chip Select 0 on the Omega's SPI bus. Since there are two SPI Chip Select signals it's possible to connect an additional SPI device to the Omega using Chip Select 1.

As such, the SPI communication pins - CLK, MOSI, and MISO - GPIOs 7, 8, and 9 **cannot be used as regular GPIOs**. Connecting non-SPI circuitry to these pins may prevent your Omega from booting or cause other damage to your unit.

No	Name	I/O	Description
13	SPI_CS1	O	SPI Chip Select 1
12	SPI_CLK	O	SPI Clock *Cannot be used as a regular GPIO*
10	SPI_MISO	I	SPI Master Input/Slave Output *Cannot be used as a regular GPIO*
11	SPI_MOSI	O	SPI Master Output/Slave Input *Cannot be used as a regular GPIO*

3.2.3 - Reset Pins

There are two reset pins:

No	Name	I/O	Description
26	GPIO_38 / SW_RST	I/O	General Purpose I/O / Default User Button - Programmed to trigger a reboot in Onion Firmware - Active High
16	HW_RST_N		Hardware Power On Reset - Active Low Performs hard reset (power-cycle) of the CPU

The **SW_RST** pin acts as the soft-reset on the Omega2. This is actually GPIO38 which is configured in the Onion Omega2 firmware to be the programmable user button input. By

default, the input is configured to be **active-high** and will **trigger a reboot of the Operating System**.

The **HW_RST_N** pin acts as the hard-reset on the Omega2. This input is **active-low**, and, when triggered, will perform a **hard reset (ie a power-cycle) of the CPU**.

3.2.4 - Power Supply Pins

There are two power pins on the Omega2: one serves as a power supply input, and the other, a power supply output:

No	Name	I/O	Description
31	3.3V VIN	I	3.3V Power Supply Input
25	3.3V VOUT	O	3.3V Power Output

Note: No power supply filtering capacitors are required when using the Omega modules.

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power supply voltage	Vcc		3.63	V
Input pin voltage	Vin	GND - 0.3 V	Vcc + 0.3 V	V
DC current through any digital I/O pin (except supplies)	Ipin		8	mA
Storage Temperature	Tstg	-20	80	˚C

4.2 Operating Conditions

Operation beyond the specified operating conditions can affect device reliability.

Parameter	Symbol	Min	Typical	Max	Units
Power supply voltage	Vcc	2.97	3.3	3.63	V
Input pin voltage range	Vin	-0.3		3.3	V
Digital pin low level input voltage	Vil	-0.3		0.8	V
Digital pin high level input voltage	Vih	2		3.6	V
Digital pin low level output voltage	Vol			0.4	V
Digital pin high level output voltage	Voh	2.4		3.3	V
Operating Temperature	Topr	-10		55	˚C

4.3 Power Consumption

State	Peak Current	Typical Current	Units
Booting	180	170	mA
Idle & Connected to WiFi network	190	170	mA
Idle & WiFi radio turned off	130	130	mA
Actively downloading files through WiFi	310	260	mA
Actively downloading files through WiFi, CPU at full load	400	310	mA

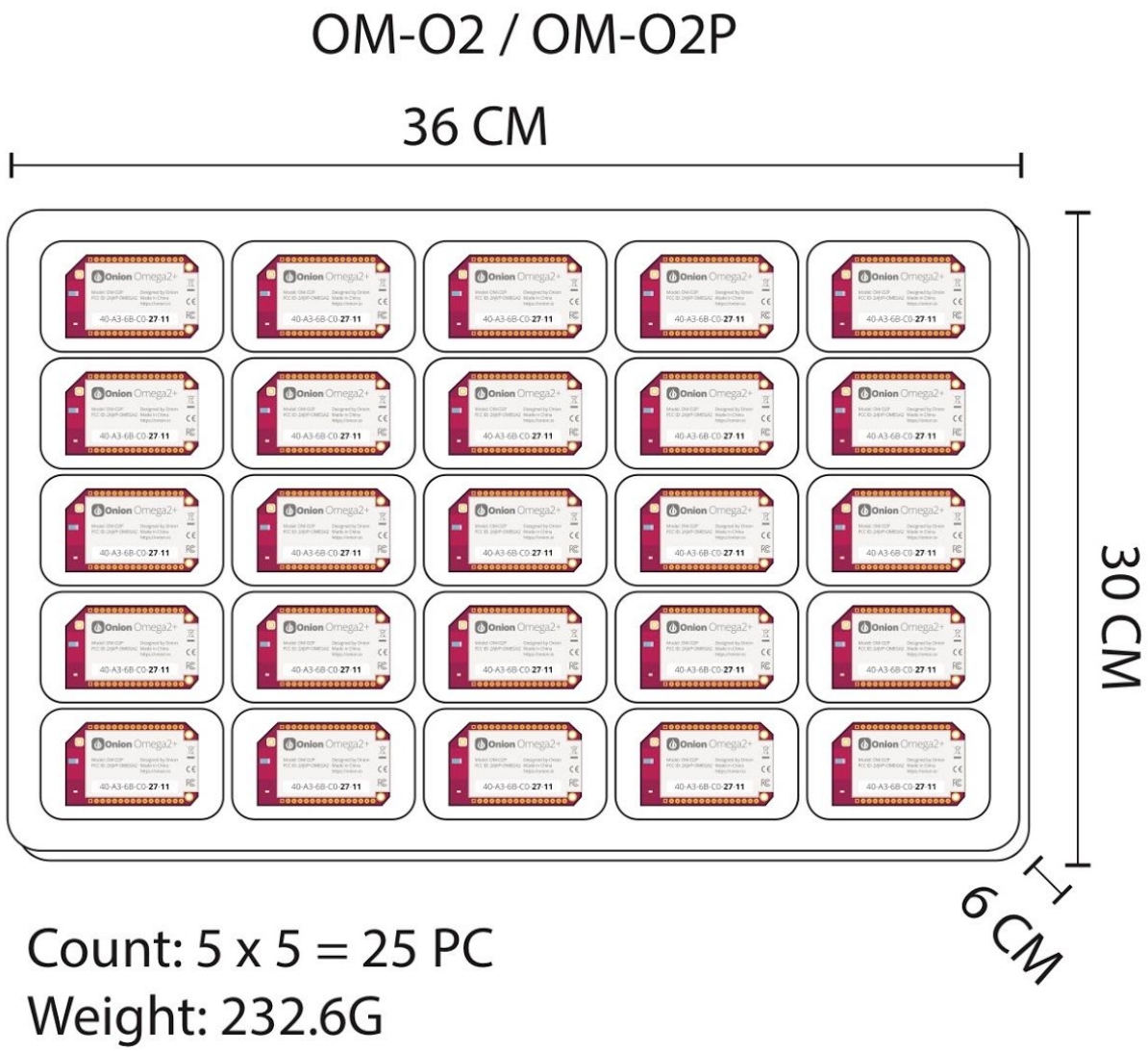
Note: All current measurements correspond to Vcc of 3.3V.
Note: These numbers are not based on exhaustive testing and should be used as reference values

5. Mechanical Specifications

5.1 Mechanical Drawing

Mechanical drawings are available for download.

5.2 Packaging Details



6. Additional Resources

6.1 Omega2 Online Documentation

Extensive documentation for the Omega2 family is hosted online. This documentation also applies to the Omega2.

It can be found here: http://docs.onion.io/

6.2 More Resources

Resources like Application Notes, Footprint files, and more can be found on GitHub: https://github.com/OnionIoT/Omega2

7. Datasheet Revision History

Revision	Date	Description
1.1	August 1, 2019	Added packaging details
1.0	April 1, 2019	Initial release