ECE 165 Project: 8-bit Carry Look Ahead Adder

Youssef Georgy A17214316
Michael Hawkins A17234954
Johnathan Tinajero A16454558

The design challenge for this project is to create an 8-bit adder that has faster performance than the synthesized one created in Lab 4. It is important to strengthen our understanding of the course materials by figuring out what allows for an adder to work at higher frequencies and have faster performances while conserving power consumption.

Some architectures are not optimal for speed because they have to calculate each bit of the sum in order meaning it has to wait for each carry to propagate in order to allow sum bits to generate. That process leads to large propagation delay. A ripple carry adder is a prime example of the process described.

The design our group chose is a carry look adder and we believe it performs better than an 8 bit ripple carry adder because carry signals are now in parallel allowing for the sum bits to be generated without having to wait for the carry to propagate. This allows us to have a lower propagation delay leading to faster speeds while also optimizing power consumption.

An innovative aspect of our work is that we decided to stray away from the typical combinational logic and decided to create our own versions of combinational logic by reducing the sizing and altering the gates to achieve even greater speeds.

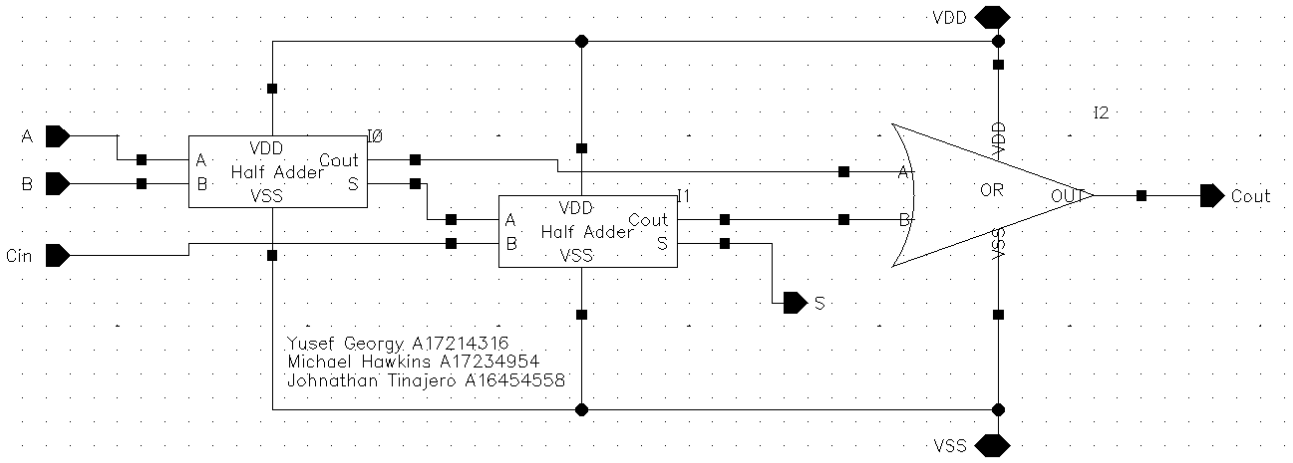
After creating our CLA adder, we brainstormed a way to have a higher clocked frequency threshold and we decided that we would use the CLA adder and implement it into a carry skip adder. That would help reduce critical path delay because of the ability of bypassing carriers. Unfortunately, it did not pan out at the end as for some reason we could not figure out the reason our clocked results were abnormal.

A future iteration that can be incorporated into our design (if looking to enhance clock frequencies of the carry look ahead adder) is pipelining. If pipelining is used effectively then the design should be able to work at higher clock frequencies while also having lower propagation delay. Another suggestion is doing what we tried and implementing the carry look adder into a carry skip adder which would improve the circuit performance as described in our inability to get it to work.

We worked cooperatively for every step during Office Hours in JACOBS EBU1 4307.

Acknowledgements:

Thank you to each TA as they all helped during this project.



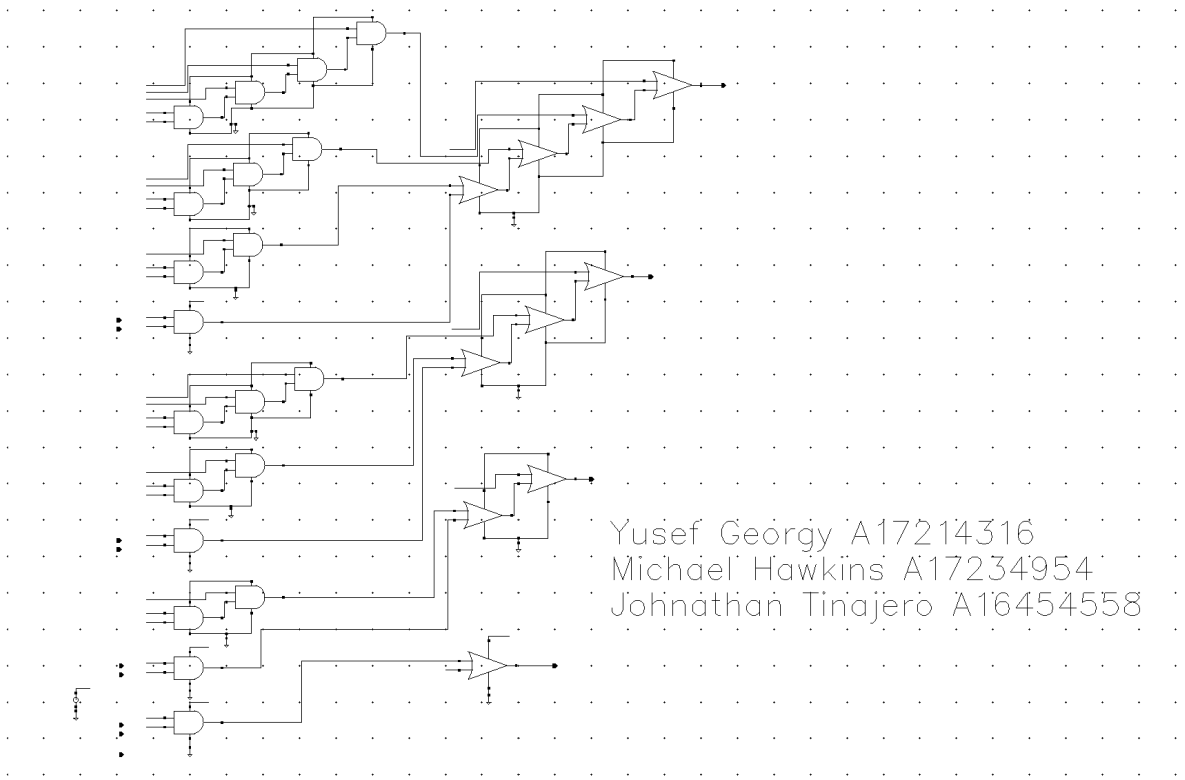


FIGURE 1: Full Adder and Carry Look Ahead Adder

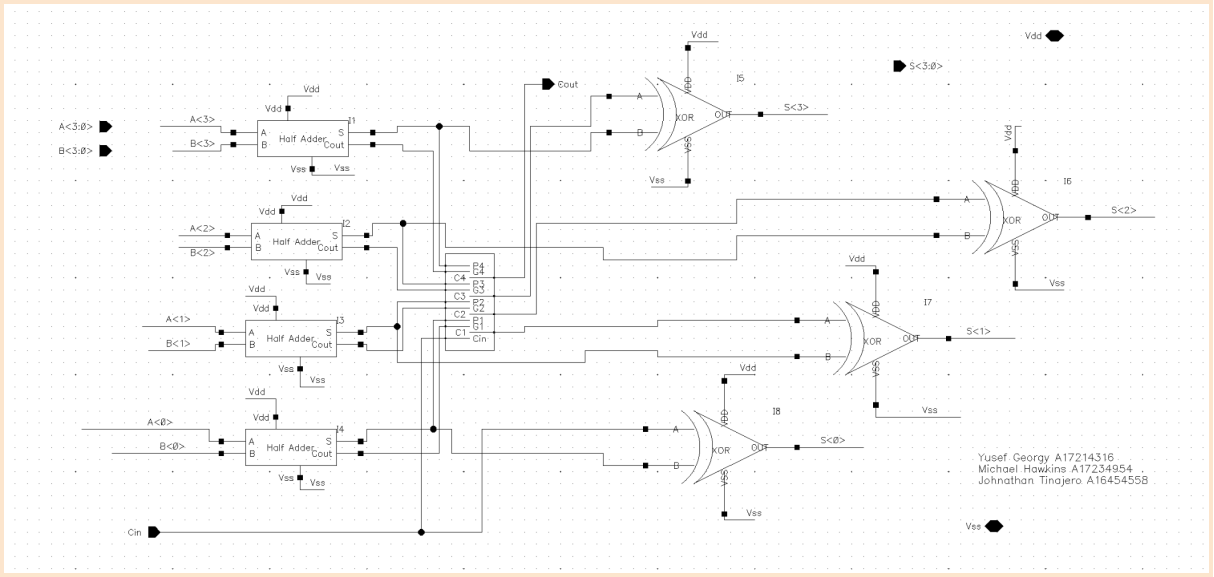


FIGURE: 4-bit Adder Schematic

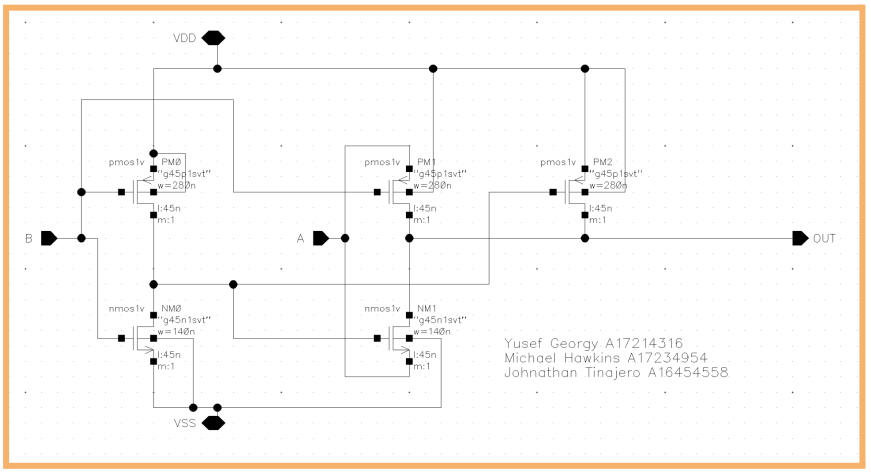


FIGURE: Custom OR

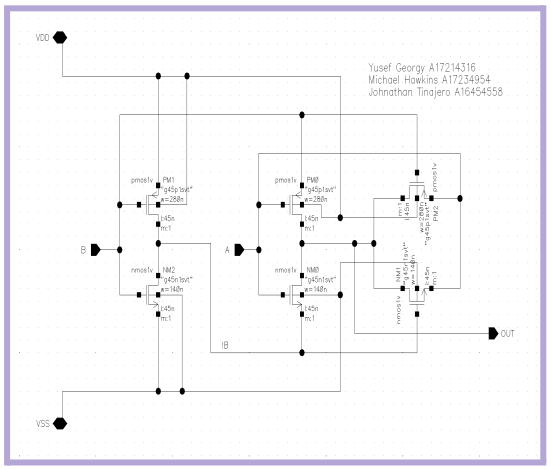


FIGURE: Custom XOR

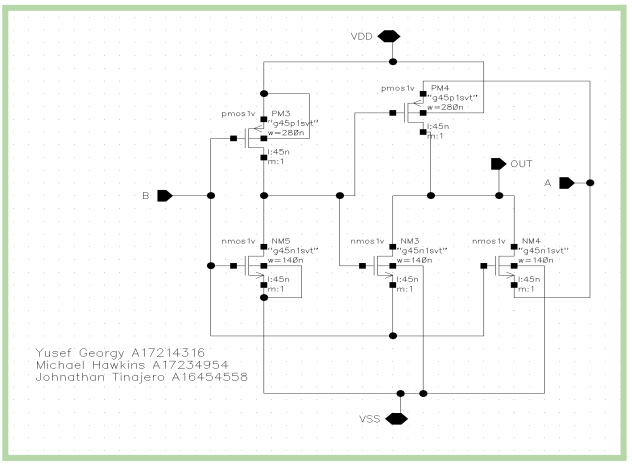


FIGURE: Custom AND

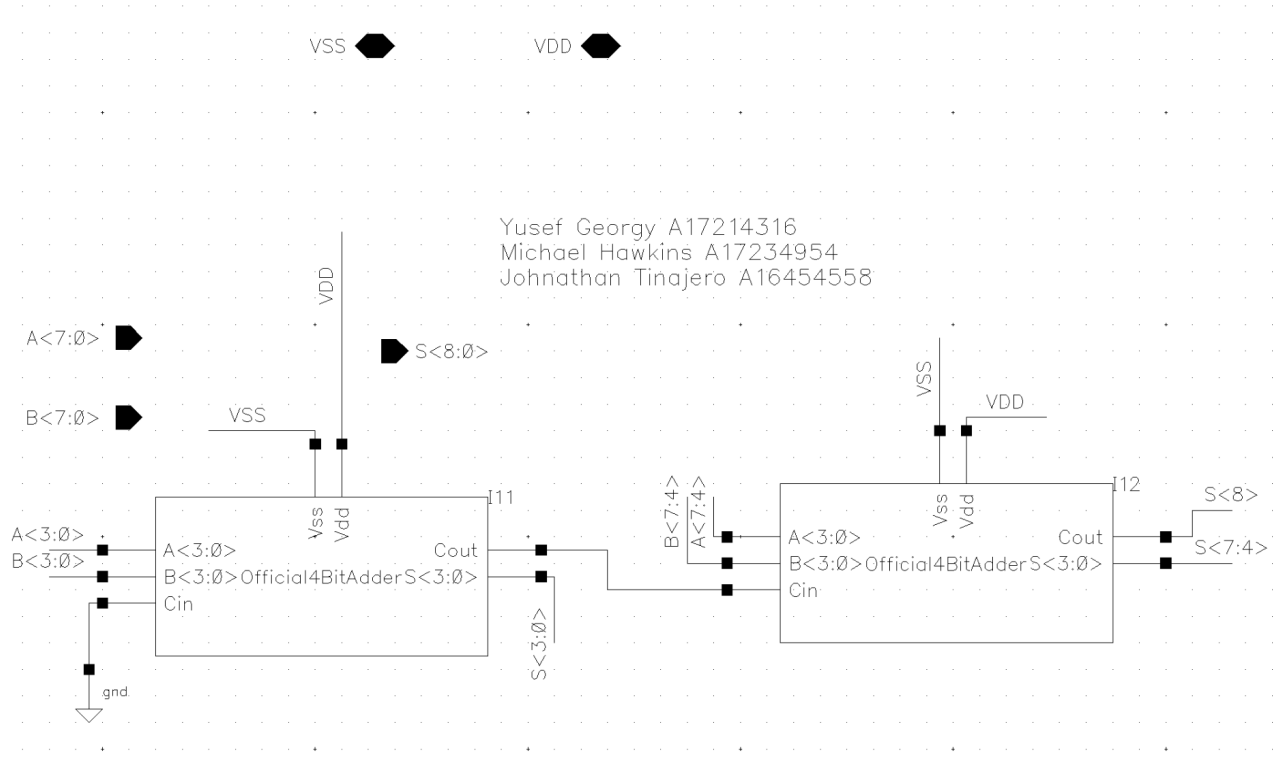


FIGURE: 8-BIT ADDER

5th Page: OPTIONAL Layout of 8 bit adder

FIGURE: N/A

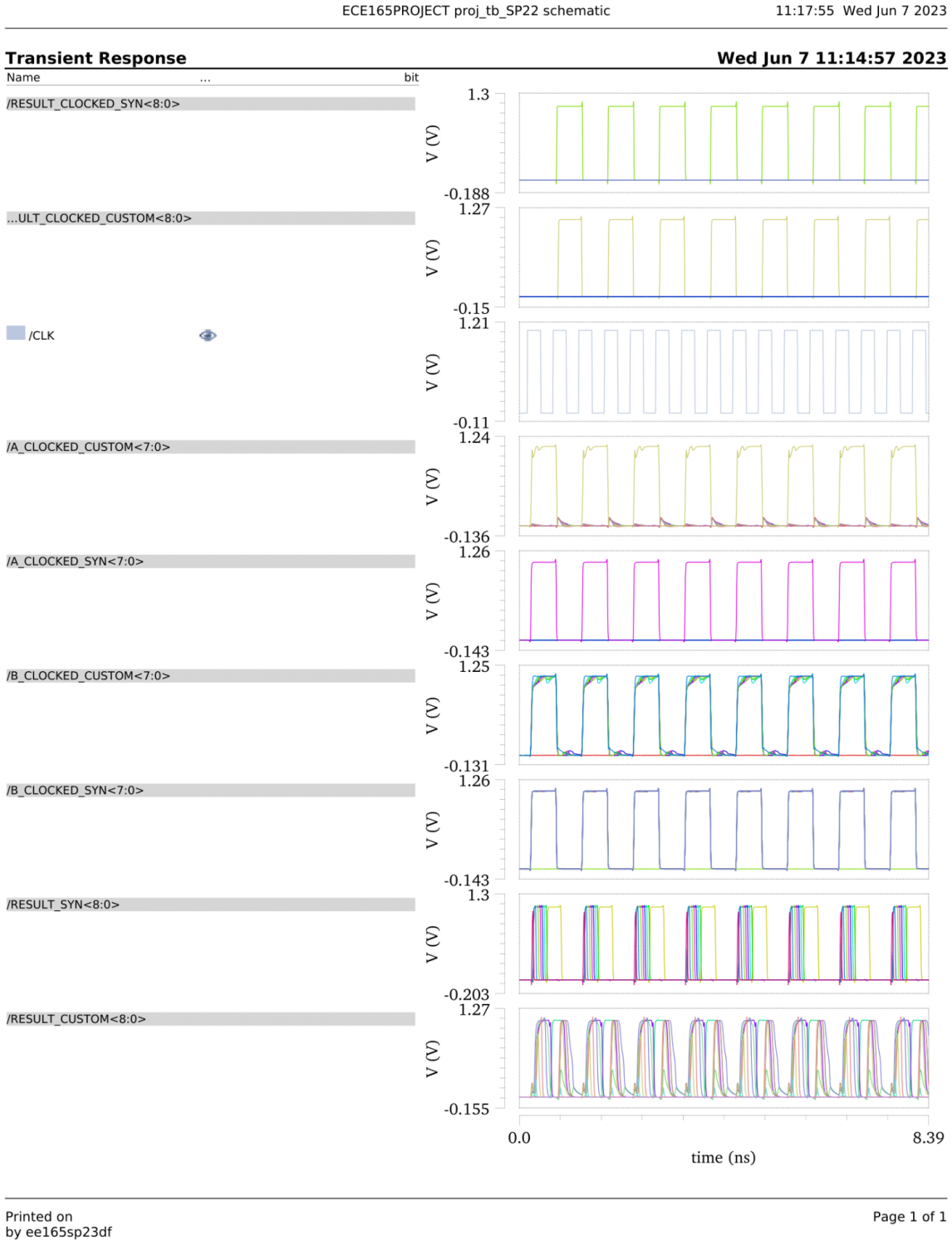
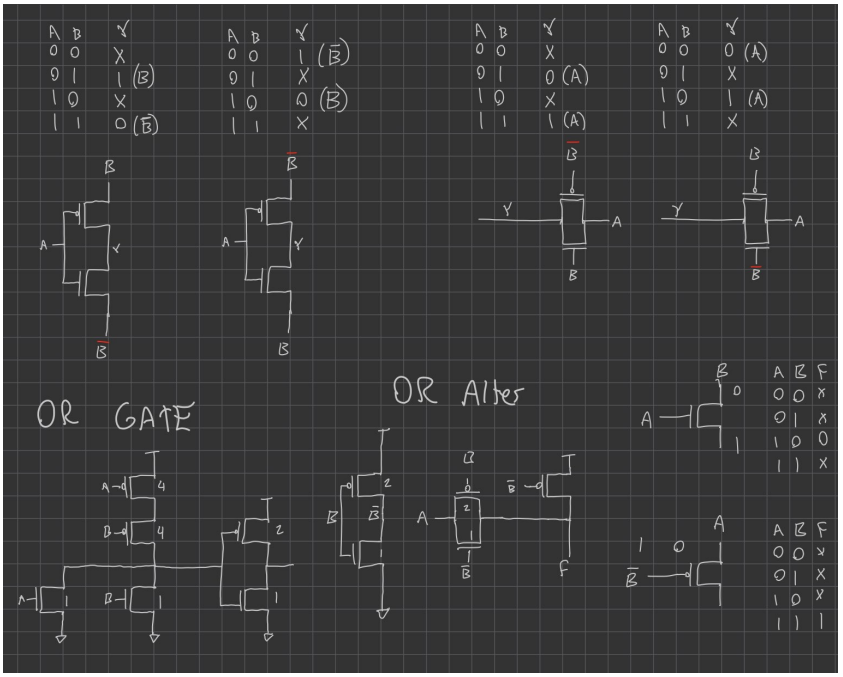
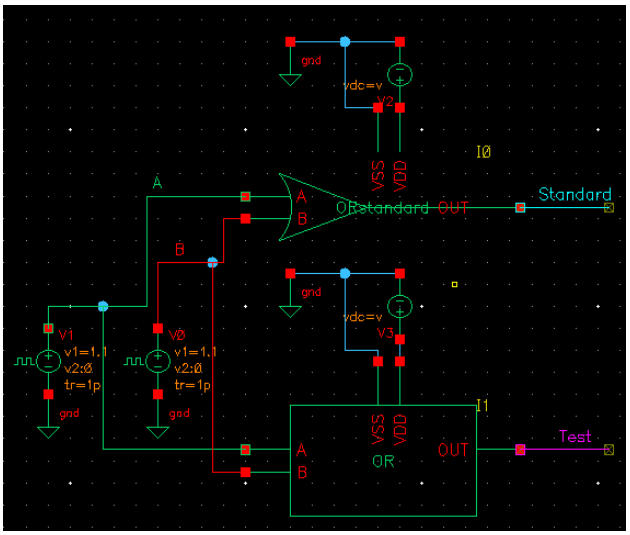


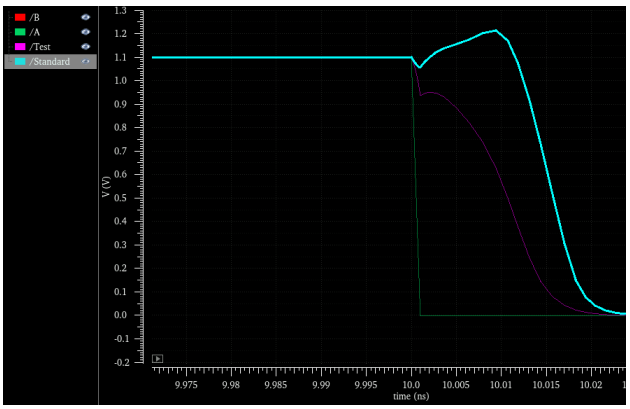
FIGURE: Simulation Result

	Place+route schematic	Custom design schematic
		Performance f
f_{max}	2.3 GHz	1.9 GHz
Power consumption @ f_{max}	608.4 μW	11.86 μW
Energy per operation @ f_{max}	2.65×10^{-13} J	6.24×10^{-15} J
		Performance for VDD
Power consumption @ 1 GHz	74 μW	6.24 μW
Energy per operation @ 1 GHz	7.4×10^{-14} J	6.241×10^{-15} J
		Other importa
Adder architecture	Ripple-carry	Carry Look ahead
Core area	103.968 μm^2	—
Critical input pair (i.e., A=?, B=?)	00000001 01111111	01010101 10101010
Transistor types used (e.g., VTL, VTG)	VTG	VTG

FIGURE: Table of Results







To increase the performance of our circuit, we sought out alternative circuit designs for the OR and AND gates. Some of the brainstorming is shown above, such as how logic can be pulled from an NMOS and PMOS with different configurations while still pulling strong 0s and 1s. One configuration involved the OR gate when the PMOS with a $\overline{B}$ on the gate was using 0 for A and 1 for B, resulting in F being 1. The source and drain of that PMOS flipped resulting in a large power draw, so the A was replaced with VDD which was a better configuration anyways. This was found though testing the configuration with a standard OR gate design and observing the voltage drop of the output for that configuration.