Design Project

Due: Tuesday, December 5th, 5:00 PM

Your first big project at Triton Industries, Inc. is redesigning a sensor interface using a new technology. The schematic (from a previous project) is shown in Figure 1. Due to time-to-market constraints, your manager insists you do not change the circuit's architecture. Your focus is to properly size all of the MOSFETs and resistors to meet the following objectives:

Parameter	Specification
Technology	0.18 µm CMOS (Nominal)
Operating temperature	25 °C
Supply voltage (V_{DD})	1.8 V
Output load (C_L)	10 pF
Input common-mode range	0.2 – 0.8 V
Common-mode output voltage	0.4 – 1.4 V
Power dissipation	≤ 2.5 mW (minimize)
DC small-signal gain	≥ 70 dB
Unity gain bandwidth	≥ 30 MHz
Phase margin	≥ 65°
Gain margin	≥ 15 dB
Current mirror "*m*" factor	≤ 20
L_{min} (current mirrors)	≥ 1 µm
Gate overdrive voltage (V_{OV})	≥ 150 mV

You must size each device to meet the specifications (Table 1). You must provide the supporting documentation and calculations (as outlined below). For simplicity, you are **not** required to verify the design across PVT variations. In practice, this would be the next logical step after getting the "nominal" design working. You may work on this project alone or in teams of two. Each team must submit one project report *EXACTLY* as specified below. You are encouraged to discuss the design problem with other groups, but your implementation *must be unique*. Under **NO** circumstances should you exchange computer files with other teams; this would violate the student honor code and will be submitted to the academic integrity office.

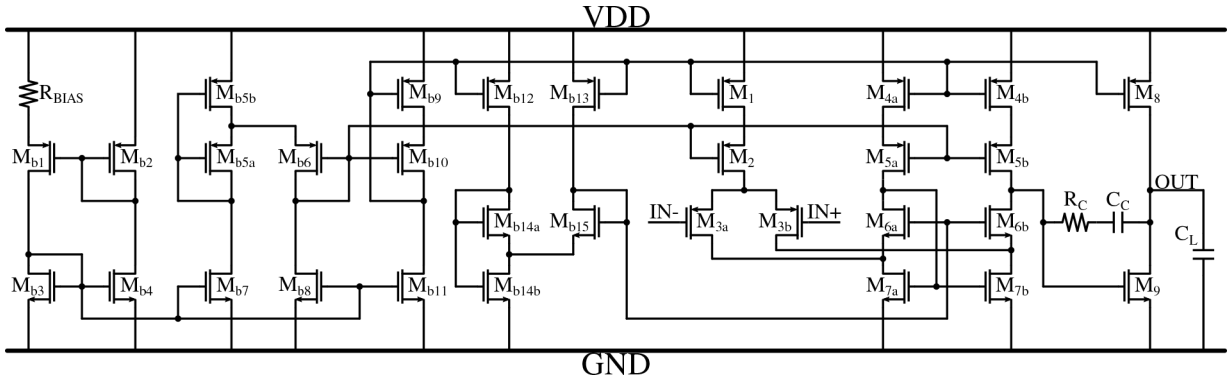

Figure 1 – Amplifier architecture

This project involves a great deal of plain old labor; it takes a significant amount of time to determine suitable design choices, run the necessary simulations, and clearly document your work. Don't delay getting started! There is minimal homework, so you should have lots of time. The lab computers have been known to slow down or be unavailable at the worst possible times (*i.e.* when the projects are due). We will be largely unsympathetic to pleas for extensions arising from such problems.

Suggested Design Flow

1) Read this *entire* document thoroughly and find a project partner. If you need help, check on Piazza.
2) Familiarize yourself with the schematic in Figure 1. Analyze how the key blocks interact. Draw simplified half-circuit schematics (differential- and common-mode). This will allow you to identify the main "knobs."
3) Set up a MATLAB script/Excel sheet that allows you to optimize your design iteratively without repetitive "Spice Monkeying." Identify the key variables you will focus on; calculate important time constants based on reasonable design choices.
4) Simulate your design in SPICE and compare the results to your hand calculations. Inspect and track down discrepancies. If your circuit does not work, double-check your schematic and operating point. (Do not just blame your problems on SPICE!) Be thorough in checking your assumptions and calculations.
5) Begin to write your report (see below) at least *several days before the deadline*. Your grade will strongly depend on the quality of your write-up, not just the power consumption of your design. Writing an insightful, well-documented report showing how you got the best results is a marketable skill that can distinguish you from others in the job market.

Design Hint: The first design that you simulate does not (and probably should not) look exactly like the final circuit (*i.e.,* there is no need to implement the complete biasing circuit in the beginning). Start by using a simplified (idealized) current source for biasing. Once your idealized design works, it is straightforward to translate it into the final version that complies with all the constraints. (Note: Sometimes, it helps to add estimated load impedances such that there is no significant difference when you replace the ideal loads.)

Project Report

Your team is required to prepare a single report. Reports must be submitted online through Canvas and a hard copy in class. *We will not grant any extensions.* Reports must use Arial 12 pt. font with 1" margins.
Page 0: Cover page. Clearly indicate the names of the team members, including PID and email.
Page 1: Outline of your design. How did you approach this problem? What were your key design choices?
Page 2: Schematic of your final design with component values (*i.e.,* W/L, R, etc.) Node voltages and bias currents (from .op) are clearly labeled. Component values should be listed next to the components, and currents next to the branches. Annotate all transistors with their gate overdrive voltage. (**No lookup tables**!)
Page 3-6: Calculate key design parameters, such as g_m, bias currents, etc. (This is the most important part of your report!) Compare the most relevant hand calculations with the final SPICE values in a table and discuss the discrepancies. **Make sure to include your power dissipation** (calculation and simulated). The lowest power designs will NOT automatically score the highest. The methodology is far more important.
Page 7: Bode plot simulation results. Clearly annotate achieved DC gain, bandwidth, and phase margin. Annotate your hand-calculated values on the same plot. (Make sure ALL plots are clearly legible.)
Page 8: Transient simulation results for a 10 μV_{pp} sinusoid at 20 Hz.
Page 9: Comments and conclusions. Convey any issues you had and or anything you learned (or didn't learn) from the project. You may also comment on how you would improve the architecture (not required).

SPICE Submission: We will provide a submission script to validate your circuit's performance.

Grading: Design flow, insight, and optimization strategy – 50%, Write-up – 10%**,** Specs and practicality of circuit – 20%**,** Power consumption – 20%