ECE 164 – Analog Integrated Circuit Design

Sensor Interface Redesign

Triton Industries, Inc.

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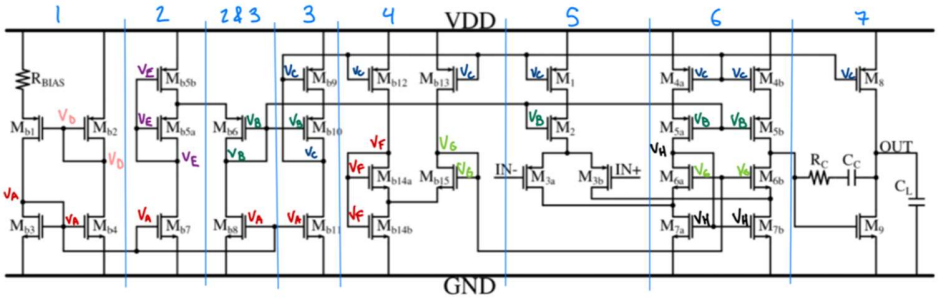
Design Outline



To properly re-design the sensor interface, we initially broke the circuit up into subcircuits with specific characteristics and functions covered in lectures. These subcircuits were: Constant G_m (1), Current Mirror Bias (2, 3, 4), Folded Cascode (5,6), Compensation Network (7), and a Common Source amplifier (7). Most of our components are MOSFETs, so MATLAB scripts with parameters of MOSFET equations like overdrive voltage and drain current were created.

Values for k_n', k_p', and λ were taken from the homework for calculations. Initially, we designed each circuit to meet a V_{ov} of 200 mV for every transistor to meet specifications and give enough room to keep all transistors in saturation. Additionally, we made some assumptions such as setting every V_t to 400 mV and every length to 1µm to standardize calculations. As we proceeded to the CS amplifier, we decided on setting the output to 900 mV to keep both transistors in saturation. Afterwards, we calculated gm_9 using our desired phase margin and gain bandwidth. From this we determined the approximate current for the corresponding g_m and started sizing the CS amplifier accordingly.

Then we began to size the Folded Cascode circuit and Current Mirror Bias circuit to meet the voltages needed for the CS amplifier. In particular, we chose voltages at nodes that would keep with the 200 mV overdrive voltage and limit the V_{ds} in case we would need to correct for currents later. We also took into consideration that some widths would need to be larger in order to achieve parameters for mirroring, so we preemptively raised widths for mirrored transistors connected to the CS amplifier. This was because we found that our $\frac{W}{L}$ ratios calculated in the CS amplifier were quite large and would get larger when optimizing.

For the constant G_m circuit, we wanted to size the two lengths within a ratio and ensure that the voltage from the circuit would keep the Current Mirror Bias circuit M_{b7}, M_{b8}, and M_{b11} within saturation. We verified the operation of the constant G_m circuit and began to optimize the circuit by raising widths for transistors M_9, M_8, and lowered M_3 until parameters were reached and power dissipation was lowered.

Schematic

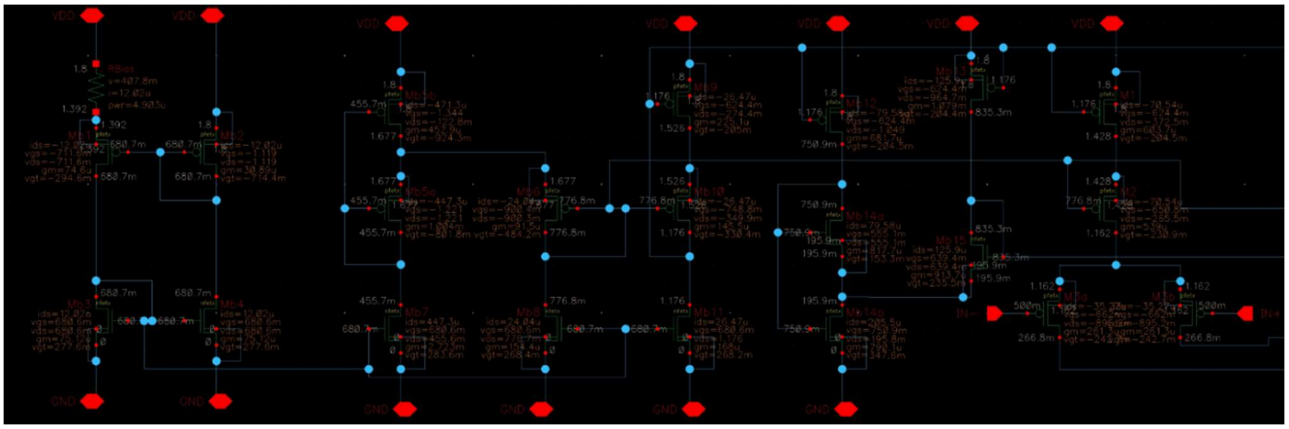


Figure1: Left Side of Design Circuit (Currents, Vov, Node Voltages)

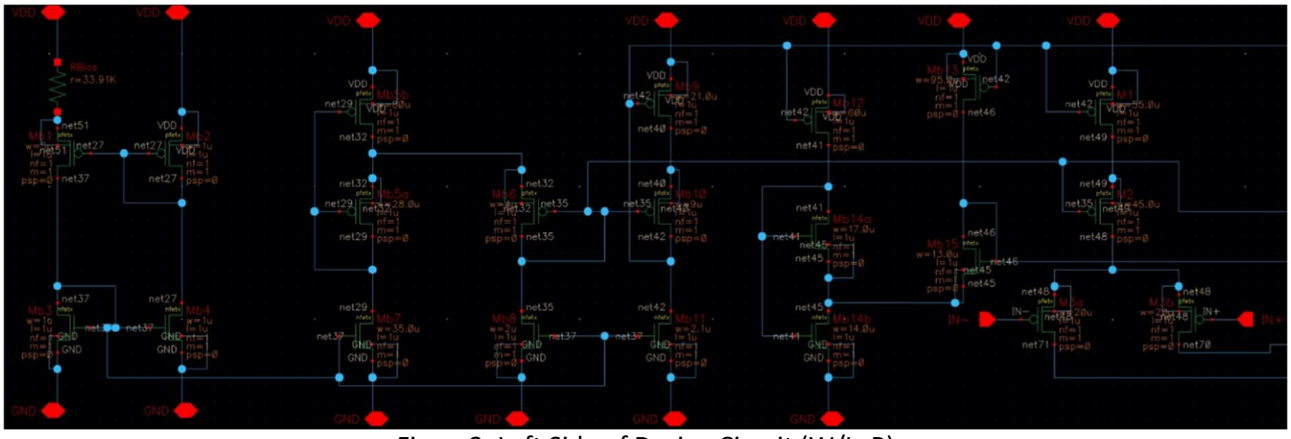


Figure2: Left Side of Design Circuit (W/L, R)

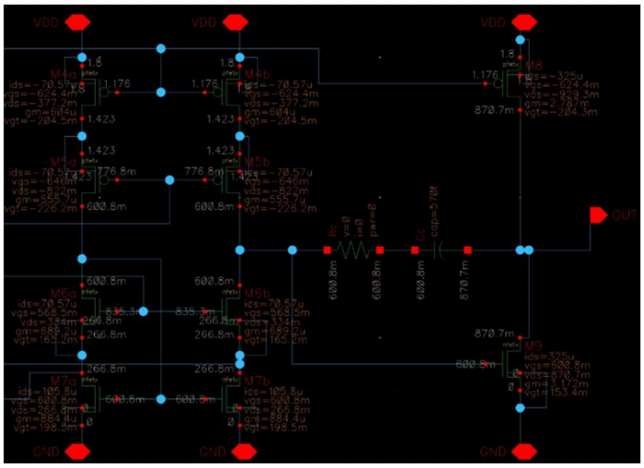


Figure3: Right Side of Design Circuit (Currents, Vov, Node Voltages)

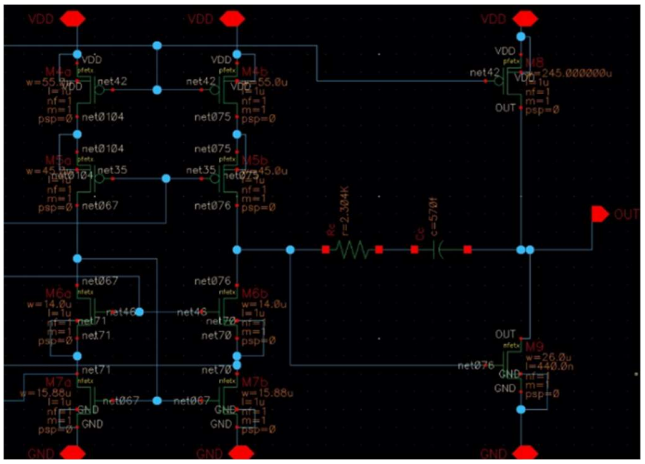
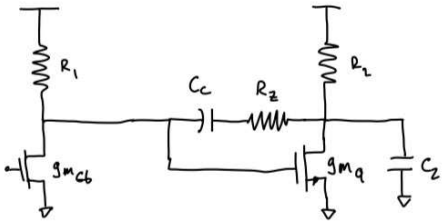


Figure4: Right Side of Design Circuit (W/L)

Common Source & Compensation Network



$$A_{dc} = A_{v_1} A_{v_2} = g_{m_a} R_1 g_{m_q} R_2$$

$$\omega_{p1} \approx -\frac{1}{C_c g_{m_q} R_2 R_1} \qquad \omega_c = GBW = \omega_{p_1} A_v = \frac{g_{m_6}}{C_c}$$

$$\omega_{p_2} = -\frac{g_{m_q}}{C_2} \qquad PM = 90° - \tan^{-1}\left(\frac{\omega_c}{\omega_{p_2}}\right)$$

$C = 550\ f$ PM = 65° Unity Gain BW = 60 MHz

$$\omega_{p_2} = \frac{60\,MHz \times 2\pi}{\tan(25°)} = 808.46E6\ rad/s$$

$$g_{m_q} = \omega_{p_2} \cdot C_2 = 808.46E6\ \frac{rad}{sec} \times 5\times10^{-12} = 4.04\ mS$$

$V_{OV} = 200\ mV$

$K = 20$

$$I_{D_{Mq}} = \frac{g_{m_q} V_{ov}}{2} = 404.23\ \mu A \qquad I_{M_{6B}} = I_{D_6}/k = 404.23\ \mu A/20 = 20.21\ \mu A$$

$$I_D = \tfrac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2 (1 + \lambda V_{DS})$$

$\lambda = .1 \qquad V_{DS} = .9\ V$

$$\Rightarrow \left(\frac{W}{L}\right) = \frac{2\, I_{Dq}}{k_n' V_{ov}^2 (1+\lambda V_{DS})} \Rightarrow \frac{2(404.23\mu A)}{(270\mu A/V^2)(.2)^2(1+.1\times.9)} = 68.68$$

$W_q = 31\ u$ $L_q = .45\ u$ $\left(\frac{W}{L}\right)_q = 68$

$$\omega_{p_1} = \frac{1}{C_c g_{m_q} R_2 R_1} = \frac{1}{(5E{-}12)(4.04mS)(24.738k)(494.8k)}$$

$$= 4.0444E3\ rad/s$$

$$R_2 = \frac{1}{\lambda i_{D_q}} = \frac{1}{.1\cdot(404.23\mu A)} = 24.738k\Omega$$

$$R_1 = \frac{1}{\lambda i_{mirror}} = \frac{1}{.1(20.21\mu A)} = 494.8k\Omega \qquad g_{m_6} = \frac{2(20.21mA)}{.2} = 202.1\mu S$$

$A_{V_1} = g_{m_{CG}} R_1 = (202.1\mu S)(494.8k\Omega) \approx 100 \approx 40dB$

$A_{V_2} = g_{m_4} R_2 = (4.04mS)(24.738k) \approx 100 \approx 40dB$

$A_V = A_{V_1} A_{V_2} = 40+40 = 80dB \geq 69dB$ ✓

Power ≤ 2.5 mW

$\rightarrow I_{tot} = \frac{P}{V} = \frac{2.5mW}{1.8V} = 1.38mA$

$\rightarrow I_{tot} \leq 1.39mA$

aiming for $\rightarrow I_{tot} \leq 1.25mA$

$\approx 10\%$ guardband

$PM = 90° - \tan^{-1}\left(\frac{\omega_c}{\omega_{P_2}}\right)$

$65° = 90° - \tan^{-1}\left(\frac{\omega_c}{808.4656 \frac{rad}{s}}\right)$

$\tan(25°) = \frac{\omega_c}{808.4656 \frac{rad}{s}}$

$\omega_c = 60$ MHz

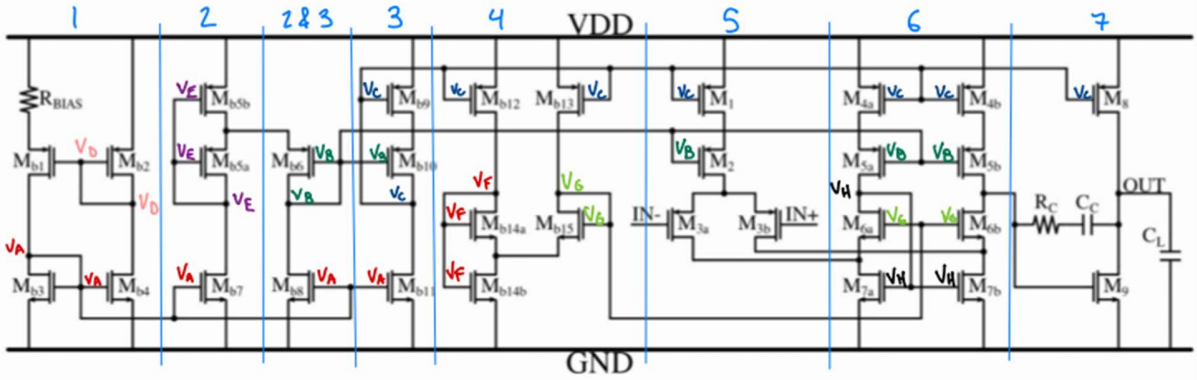
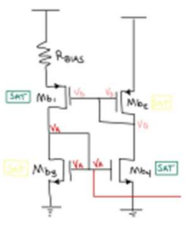


Figure 1 – Amplifier architecture

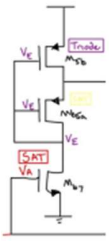



```
%Mosfet Parameters
kn = 267.2e-6; kp = 49.1e-6; lambda = .1;
%Voltages, Components
Vdd = 1.8; Vtn = .43; Vtp = .38;

%Use .7 Vds drop, 5-1 sizing ratio, Budget 12.5uA for R_bias,Mb1,Mb3
Vov_Mb1 = .3; Vov_Mb3 = .3; Id_Mb1_Mb3 = 12.5e-6;
%Budget 12.5uA for Mb2,Mb4
Vov_Mb2 = .7; Vov_Mb4 = .3; Id_Mb2_Mb4 = 12.5e-6;
R_bias = (Vdd - 2*.7)/ Id_Mb1_Mb3;
%Neglecting Channel length to simplify calculations, so Vds = 0
Vds_Mb1 = 0; Vds_Mb2 = 0; Vds_Mb3 = 0; Vds_Mb4 = 0;
WL_Mb1 = (2*Id_Mb1_Mb3)/(kp*Vov_Mb1^2*(1+lambda*Vds_Mb1));
WL_Mb2 = (2*Id_Mb2_Mb4)/(kp*Vov_Mb2^2*(1+lambda*Vds_Mb2));
WL_Mb3 = (2*Id_Mb1_Mb3)/(kn*Vov_Mb3^2*(1+lambda*Vds_Mb3));
WL_Mb4 = (2*Id_Mb2_Mb4)/(kn*Vov_Mb4^2*(1+lambda*Vds_Mb4));
```

Id_Mb1_Mb3	1.2500e-05
Id_Mb2_Mb4	1.2500e-05
kn	2.6720e-04
kp	4.9100e-05
lambda	0.1000
R_bias	3.2000e+04
Vdd	1.8000
Vds_Mb1	0
Vds_Mb2	0
Vds_Mb3	0
Vds_Mb4	0
Vov_Mb1	0.3000
Vov_Mb2	0.7000
Vov_Mb3	0.3000
Vov_Mb4	0.3000
Vtn	0.4300
Vtp	0.3800
WL_Mb1	5.6574
WL_Mb2	1.0391
WL_Mb3	1.0396
WL_Mb4	1.0396

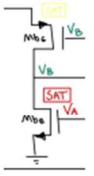
Spec	Hand Calc	Sim	Discrep
R_{BIAS}	32k	33.91k	6%
$(W/L)_{61}$	5.68	5	1.3%
$(W/L)_{62}$	1.04	1	4%
$(W/L)_{63}$	1.04	1	4%
$(W/L)_{64}$	1.04	1	4%




```
%Budgetting 475uA for Current in Mb5b
%Budgetting 450uA for Current in Mb5a, Mb7
%Mosfet Parameters
kn = 267.2e-6; kp = 49.1e-6; lambda = .1;
%Voltages, Components
Vdd = 1.8; Vtn = .43; Vtp = .38;
Vov_Mb7 = .3; Vov_Mb5a = .8; Vov_Mb5b = .9;
Id_Mb5a_Mb7 = 450e-6; Id_Mb5b = 475e-6;
%Neglecting Channel length to simplify calculations, so Vds = 0
%besides Mb5b because of triode
Vds_Mb5b = 0.125; Vds_Mb5a = 0; Vds_Mb7 = 0;

WL_Mb7 = (2*Id_Mb5a_Mb7)/(kn*Vov_Mb7^2*(1+lambda*Vds_Mb7));
WL_Mb5a = (2*Id_Mb5a_Mb7)/(kp*Vov_Mb5a^2*(1+lambda*Vds_Mb5a));
WL_Mb5b = Id_Mb5b/(kp*(Vov_Mb5b*Vds_Mb5b - .5*Vds_Mb5b^2));
```

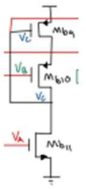
Id_Mb5a_Mb7	4.5000e-04
Id_Mb5b	4.7500e-04
kn	2.6720e-04
kp	4.9100e-05
lambda	0.1000
Vdd	1.8000
Vds_Mb5a	0
Vds_Mb5b	0.1250
Vds_Mb7	0
Vov_Mb5a	0.8000
Vov_Mb5b	0.9000
Vov_Mb7	0.3000
Vtn	0.4300
Vtp	0.3800
WL_Mb5a	28.6405
WL_Mb5b	92.4096
WL_Mb7	37.4251




```
%Budgetting 25uA for Current in Mb6, Mb8
Vov_Mb6 = .48; Vov_Mb8 = .27; Id_Mb6_Mb8 = 24e-6;
%Neglecting Channel length to simplify calculations, so Vds = 0
Vds_Mb6 = 0; Vds_Mb8 = 0;

WL_Mb6 = (2*Id_Mb6_Mb8)/(kp*Vov_Mb6^2*(1+lambda*Vds_Mb6));
WL_Mb8 = (2*Id_Mb6_Mb8)/(kn*Vov_Mb8^2*(1+lambda*Vds_Mb8));
```

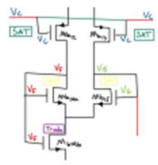
Vov_Mb6	0.4800
Vov_Mb8	0.2700
Vtn	0.4300
Vtp	0.3800
WL_Mb6	3.8895
WL_Mb8	2.2589



```
%Budgetting 25uA for Current in Mb9, Mb19, Mb11
Vov_Mb9 = .21; Vov_Mb10 = .33; Vov_Mb11 = .27; Id_Mb9_Mb11 = 26e-6;
%Neglecting Channel length to simplify calculations, so Vds = 0
Vds_Mb9 = 0; Vds_Mb10 = 0; Vds_Mb11 = 0;

WL_Mb9 = (2*Id_Mb9_Mb11)/(kp*Vov_Mb9^2*(1+lambda*Vds_Mb9));
WL_Mb10 = (2*Id_Mb9_Mb11)/(kp*Vov_Mb10^2*(1+lambda*Vds_Mb10));
WL_Mb11 = (2*Id_Mb9_Mb11)/(kn*Vov_Mb11^2*(1+lambda*Vds_Mb11));
```

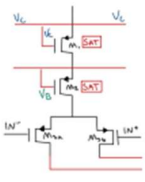
Vov_Mb10	0.3300
Vov_Mb11	0.2700
Vov_Mb9	0.2100
Vtn	0.4300
Vtp	0.3800
WL_Mb10	8.6030
WL_Mb11	2.3615
WL_Mb9	21.2441




```
%Budgetting 75uA for Current in Mb12, Mb14a
%Budgetting 125uA for Current in Mb13, Mb15a -> 200u in Mb14b
Vov_Mb12 = .21; Vov_Mb14a = .16; Id_Mb12_Mb14a = 75e-6;
Vov_Mb13 = .21; Vov_Mb15 = .23; Id_Mb13_Mb15 = 125e-6;
Vov_Mb14b = .35; Id_Mb14b = 200e-6; Vds_Mb14b = .2;
%Neglecting Channel length to simplify calculations, so Vds = 0
Vds_Mb12 = 0; Vds_Mb13 = 0; Vds_Mb14a = 0; Vds_Mb15 = 0;

WL_Mb12 = (2*Id_Mb12_Mb14a)/(kp*Vov_Mb12^2*(1+lambda*Vds_Mb12));
WL_Mb13 = (2*Id_Mb13_Mb15)/(kp*Vov_Mb13^2*(1+lambda*Vds_Mb13));
WL_Mb14a = (2*Id_Mb12_Mb14a)/(kn*Vov_Mb14a^2*(1+lambda*Vds_Mb14a));
WL_Mb15 = (2*Id_Mb13_Mb15)/(kn*Vov_Mb15^2*(1+lambda*Vds_Mb15));
WL_Mb14b = Id_Mb14b/(kn*(Vov_Mb14b*Vds_Mb14b - .5*Vds_Mb14b^2));
```

Vov_Mb12	0.2100
Vov_Mb13	0.2100
Vov_Mb14a	0.1600
Vov_Mb14b	0.3500
Vov_Mb15	0.2300
Vtn	0.4300
Vtp	0.3800
WL_Mb12	60.0376
WL_Mb13	96.9838
WL_Mb14a	19.0050
WL_Mb14b	14.9701
WL_Mb15	14.8569

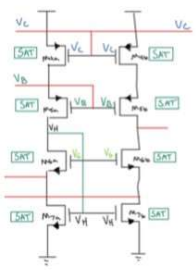



```
%Budgetting 70uA for Current in M1, M2
%Budgetting 35uA for Current in M3a, M3b
Vov_M1 = .21; Vov_M2 = .23; Id_M1_M2 = 70e-6;
Vov_M3a = .25; Vov_M3b = .25; Id_M3a_M3b = 35e-6;
%Neglecting Channel length to simplify calculations, so Vds = 0
Vds_M1 = 0; Vds_M2 = 0; Vds_M3a = 0; Vds_M3b = 0;

WL_M1 = (2*Id_M1_M2)/(kp*Vov_M1^2*(1+lambda*Vds_M1));
WL_M2 = (2*Id_M1_M2)/(kp*Vov_M2^2*(1+lambda*Vds_M2));
WL_Mb3a = (2*Id_M3a_M3b)/(kp*Vov_M3a^2*(1+lambda*Vds_M3a));
WL_Mb3b = (2*Id_M3a_M3b)/(kp*Vov_M3b^2*(1+lambda*Vds_M3b));
```

Vov_Mb12	0.2100
Vov_Mb13	0.2100
Vov_Mb14a	0.1600
Vov_Mb14b	0.3500
Vov_Mb15	0.2300
Vtn	0.4300
Vtp	0.3800
WL_Mb12	60.0376
WL_Mb13	96.9838
WL_Mb14a	19.0050
WL_Mb14b	14.9701
WL_Mb15	14.8569

	Spec	Hand Calc	Sim	Discrep
$(W/L)_{b5a}$		28.64	28	2.3%
$(W/L)_{b5b}$		92.41	80	15.5%
$(W/L)_{b7}$		37.43	35	6.9%
$(W/L)_{b6}$		3.89	4	2.8%
$(W/L)_{b8}$		2.26	2	13%
$(W/L)_{b9}$		21.2	21	1%
$(W/L)_{b10}$		8.6	9	4.4%
$(W/L)_{b11}$		2.36	2.1	12.4%
$(W/L)_{b12}$		60	60	0%
$(W/L)_{b13}$		97	95	2.1%
$(W/L)_{b14a}$		19	17	11.8%
$(W/L)_{b14b}$		15	14	7.1%
$(W/L)_{b15}$		14.9	13	14.6%
$(W/L)_{M1}$		64.7	55	17.6 %
$(W/L)_{M2}$		53.9	45	19.8%
$(W/L)_{3A}$		22.8	20	14 %
$(W/L)_{3B}$		22.8	20	14%

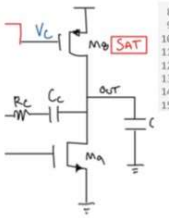


```
%Budgetting 70uA for Current in M4a, M4a, M5a, M5b, M6a, M6b
%Budgetting 105uA for Current in M7a, M7b
Vov_M4a = .21; Vov_M4b = .21; Vov_M5a = .23; Vov_M5b = .23;
Vov_M6a = .17; Vov_M6b = .17; Id_M4a_M6b = 75e-6;
Vov_M7a = .2; Vov_M7b = .2; Id_M7a_M7b = 105e-6;
%Neglecting Channel length to simplify calculations, so Vds = 0
Vds_M4a = 0; Vds_M4b = 0; Vds_M5a = 0; Vds_M5b = 0;
Vds_M6a = 0; Vds_M6b = 0; Vds_M7a = 0; Vds_M7b = 0;

WL_M4a = (2*Id_M4a_M6b)/(kp*Vov_M4a^2*(1+lambda*Vds_M4a));
WL_M4b = (2*Id_M4a_M6b)/(kp*Vov_M4b^2*(1+lambda*Vds_M4b));
WL_M5a = (2*Id_M4a_M6b)/(kp*Vov_M5a^2*(1+lambda*Vds_M5a));
WL_M5b = (2*Id_M4a_M6b)/(kp*Vov_M5b^2*(1+lambda*Vds_M5b));
WL_M6a = (2*Id_M4a_M6b)/(kn*Vov_M6a^2*(1+lambda*Vds_M6a));
WL_M6b = (2*Id_M4a_M6b)/(kn*Vov_M6b^2*(1+lambda*Vds_M6b));
WL_M7a = (2*Id_M7a_M7b)/(kn*Vov_M7a^2*(1+lambda*Vds_M7a));
WL_M7b = (2*Id_M7a_M7b)/(kn*Vov_M7b^2*(1+lambda*Vds_M7b));
```

Vov_M4a	0.2100
Vov_M4b	0.2100
Vov_M5a	0.2300
Vov_M5b	0.2300
Vov_M6a	0.1700
Vov_M6b	0.1700
Vov_M7a	0.2000
Vov_M7b	0.2000
Vtn	0.4300
Vtp	0.3800
WL_M4a	55.4193
WL_M4b	55.4193
WL_M5a	46.2002
WL_M5b	46.2002
WL_M6a	15.5399
WL_M6b	15.5399
WL_M7a	17.7769
WL_M7b	17.7769

Spec	Hand Calc	Sim	Discrep
$(W/L)_{4A,4B}$	55.4	55	.7%
$(W/L)_{5A,5B}$	46.2	45	2.7%
$(W/L)_{6A,6B}$	15.5	14	10.7%
$(W/L)_{7A,7B}$	17.8	15.88	12.1%



```
%Budgetting 325uA for Current in M8, M9
Vov_M8 = .2; Vov_M9 = .16; Id_M8_M9 = 325e-6;

%Neglecting Channel length to simplify calculations, so Vds = 0
Vds_M8 = 0; Vds_M9 = 0;

WL_M8 = (2*Id_M8_M9)/(kp*Vov_M8^2*(1+lambda*Vds_M8));
WL_M9 = (2*Id_M8_M9)/(kn*Vov_M9^2*(1+lambda*Vds_M9));
```

Vds_M8	0
Vds_M9	0
Vov_M8	0.2000
Vov_M9	0.1600
Vtn	0.4300
Vtp	0.3800
WL_M8	239.3075
WL_M9	68.7102

Spec	Hand Calc	Sim	Discrep
$(W/L)_{M8}$	239.3	245	.2%
$(W/L)_{M9}$	69	$\frac{2C}{4H} = 59$	16.9%

$$I_{tot} = I_{D_{M3}} + I_{D_{M4}} + I_{D_{M7}} + I_{D_{M8}} + I_{D_{M11}} + I_{D_{M14B}} + I_{D_{M7A}} + I_{D_{M7B}} + I_{D_{M9}}$$

$$= 12.5\mu A + 12.5\mu A + 450\mu A + 24\mu A + 26\mu A + 200\mu A + 105\mu A + 105\mu A + 329\mu A$$

$$= 1.26\,mA \qquad P = 1.26\,mA \cdot 1.8V = 2.268\,mW$$

Spec	Hand Calculation	Simulation	Discrepancy ≤20% calculation, ok
Phase Margin	65°	66.14°	+1.14°
Gain Margin	——	15.78 dB	——
DC Gain	80 dB	79.72 dB	-.28 dB
Unity Gain Bandwidth	60 MHz	61.39 MHz	+ 1.39MHz
Power Dissipation	2.268 mW	2.275 mW	+ 7 μW

Bode Plot

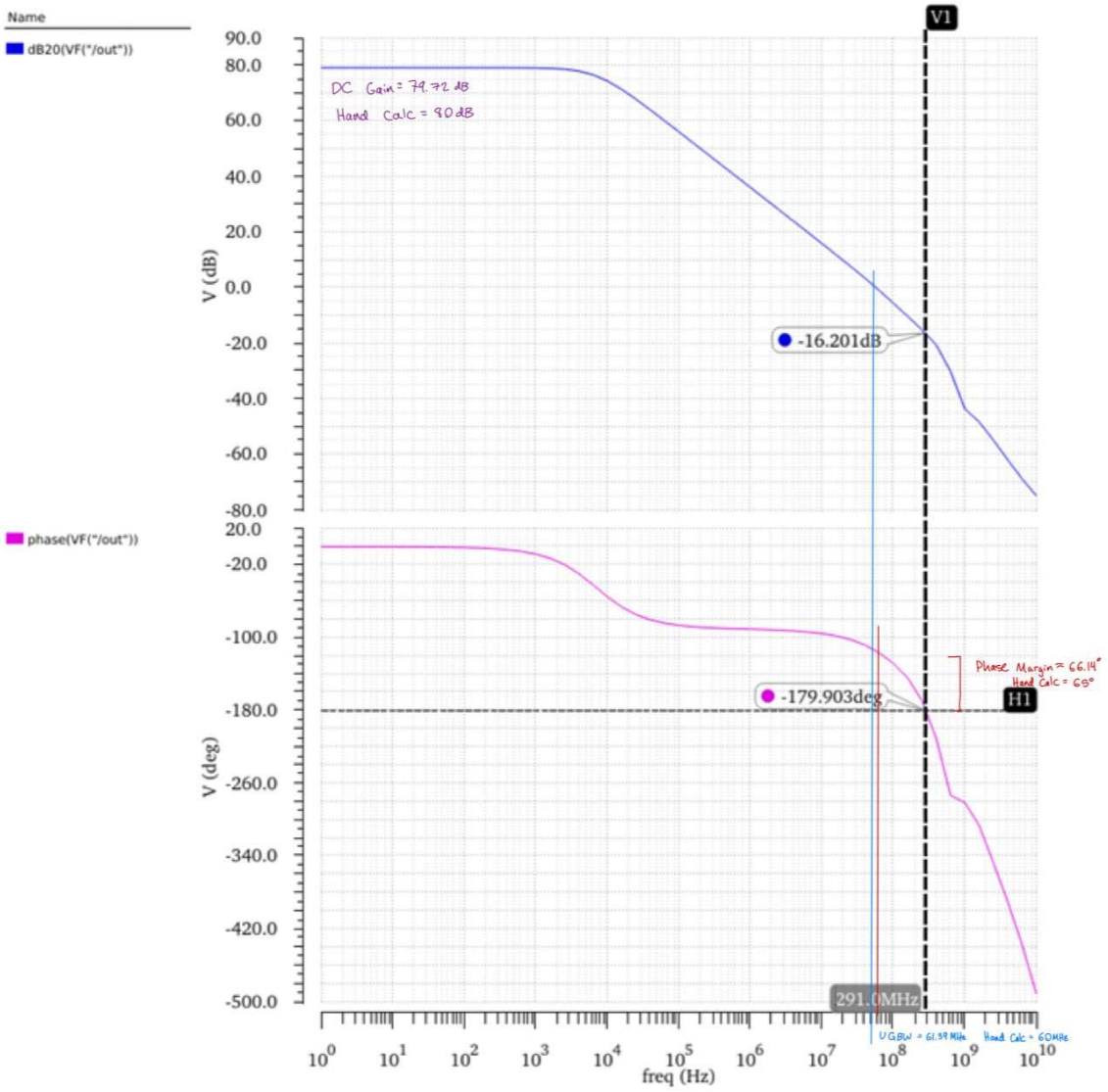


Figure4: Bode Plot Simulation

1	dB20(VF("/out"))	wave	☑	☐
2	phase(VF("/out"))	wave	☑	☐
3	phaseMargin(VF("/out"))	65.22	☑	☐
4	gainMargin(VF("/out"))	-16.21	☑	☐
5	gainBwProd(VF("/out"))	66.48M	☑	☐
6	unityGainFreq(VF("/out"))	60.77M	☑	☐
7	bandwidth(VF("/out") 3 "low")	7.13K	☑	☐
8	dB20(value(VF("/out") 0))	79.37	☑	☐
9	(VDC("/vdd") * IDC("/V3/PLUS") * -1)	2.275m	☑	☐
10	V3/PLUS		☐	☑

Transient Simulation

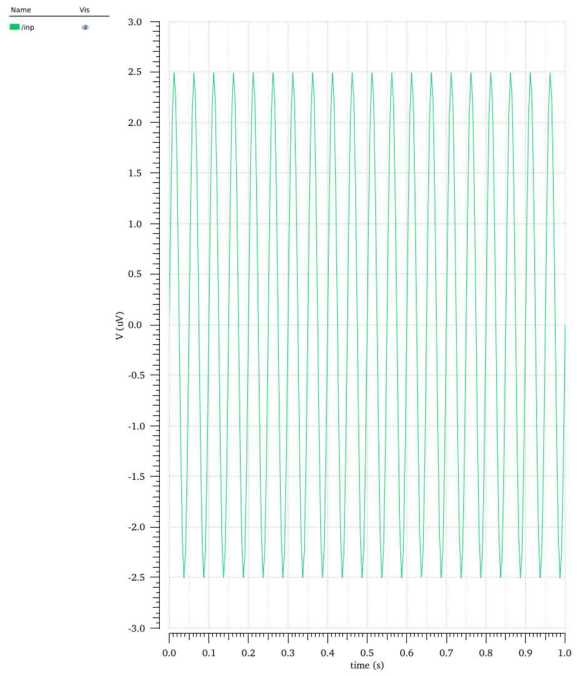


Figure5: Input Transient Simulation

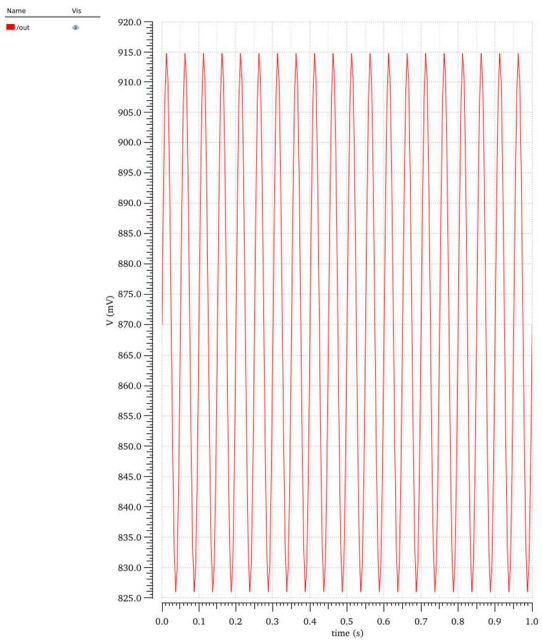


Figure6: Output Transient Simulation

These graphs are based on differential inputs of 2.5 μV_P and -2.5 μV_P using a sine wave source (Figure5). This source was used because we wanted to view the differential voltage across the sensor interface we created. To accomplish this, we needed to half the voltage coming into each side and place a negative voltage for the negative input. This voltage simulated a 10 μV_{PP} sine wave on the input and the resulting output is in figure 6. Placing a 5 µV source in a common mode configuration would yield us a similar type of result, however the magnitude of the final graph would not be as significant. Since we are using a sensor interface, we believe that the differential mode analysis of the transient response would be more beneficial as a result and is posted above.

Comments & Conclusions

The project followed quite closely to hand calculations for most of the project. However, for the project to be optimized properly, the project required V_{OV}s to be driven down to their limit of 150 mV. In order to accomplish this in the overall circuit we considered raising lengths for certain transistors to minimize the $\frac{W}{L}$ ratios and lower the widths of most transistors since the 'm' factor for mirroring transistors would soon be an issue. After this, we sized the transistors in the common source amplifier. We expected the voltage at the gate of the pMOS to increase and the widths and lengths of both transistors to increase. As of now, the nMOS in the common source amplifier is at the lowest voltage value to be within specifications for the given g_m value. Our circuit has some room to adjust on the AC specifications and could benefit from this, but it would require a lot of manipulation throughout the circuit.

The lessons we learned from this project was that hand calculations can only take you so far without making assumptions on values needed to solve. This was a logical step that significantly reduced the time it takes to get valuable results but also allowed us to make small changes faster. At a certain point, the width and length values of transistors would have to be non-integer values to maximize the lowest possible power output.

In order to make these changes, it seemed that parametric analysis was not a tool in order to iterate quickly. Also, the tool had caused a disk error as well as a rare malformed lock-stake issue which prevented one partner from using Cadence. This required extensive debugging through Piazza and using clsAdminTool and has yet to be resolved.