Flashlamp Annealing for Improved Ferroelectric Junctions

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Abstract

Popular Science Summary

A New Frontier of Computing

We all recognize the feeling of panic when your computer crashes and you realize you forgot to save your progress for the past couple of hours. In this scenario you wait for the computer to boot again and assess what you have lost. Imagine instead the computer booting instantly and you find yourself exactly where you left off. With an emerging technology in computer design this could become the new reality.

The basic idea behind the fundamental building block of your electronic devices, known as the transistor, has since its invention in the 1960s been largely unchanged. The design which proved most successful is known as the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and is by far the most common design even to this day due to its cheap manufacturing process and its ability to be scaled down to ever smaller devices. However, in the last decade one has started to reach the limits of the MOSFET design, primarily due to limited scalability, and alternative designs are actively being explored.

A promising design is the Ferroelectric Tunnel Junction (FTJ) which utilizes the small dimensions of the transistor to its advantage where electrons tunnel through a thin barrier. This barrier is then manipulated to either allow electrons though or not, resulting in the characteristic transistor functionality. In addition to being intrinsically small, the ferroelectric barrier allows the transistor to be toggleable where the state of the transistor is maintained even though power is lost. This ability means that electronic devices utilizing this design does not have to be booted up, as all transistors are already set to the desired state. Additionally, as power is only consumed as transistors are being toggled between states, these devices could reduce power consumption lengthening the battery life across all devices.

However, for this to become the new reality of computers, the FTJ design must be improved further to prove as an effective alternative to the MOSFET design. One limiting factor is believed to be the interfaces of the ferroelectric barrier layer. Utilizing a new technique known as Flash-Lamp Annealing (FLA) the processing of the ferroelectric barrier layer can be made up to 10 000 times faster which could

significantly improve the interfaces. This as the material can set much faster resulting in better defined interfaces. If successful, this could be a crucial step for this new transistor design to become a viable alternative to MOSFETs and bring in a new frontier of computing.

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Mål: Redogör för varför III-V är intressant. Direkt bandgap, lägre DOS –> FTJ

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Frågor att besvara:

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- Vilka defekter ser vi med respektive metod?

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5.1 Flashlamp Intensity and Film Temperature

Crystalization of the hafnia films using the flash lamp annealing (FLA) technique does not immediately reveal the temperature achieved in the films. Due to the short time frames and the geometry of the FLA setup, one must simulate the achieved temperature in the film from the compositional structure of the samples and the measured peak backside temperature during annealing. Furthermore, the experiment parameters of preheating temperature and flash duration are crucial for the simulations and are throughout this work set to 250 °C and 5 ms respectively. Figure **??** shows the resulting film temperature depending on flash intensity with the choosen set parameters.

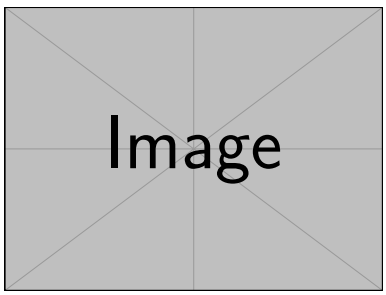

Figure 5.1: Figure showing how flashintensity relates to the peak-temperarure of the films through simulations. From this figure onwards we can then stick to Peak Temperature instead of Flash Intensity.

Explain in detail the figure above here and conclude the subsection. What type of figure can I expect here??

5.2 Sample Specifications and Characterization

In addition to the samples of focus in this work, samples were processed using RTP as the annealing method in paralell with FLA samples. These samples proves as

a point of comparison for the characterization of the FLA samples throughout the work. The RTP samples were annealed at a temperature of 600 °C for 30 seconds. Through the electrical characterization described in Section **??** the remnant polarization (P_r), coercive field (E_c) and endurance were measured and tabulated in table **??**.

Table 5.1: Electrical characteristics for the RTP reference samples measured using a cycling voltage of 3 V.

PUND and Endurance			
Remnant Polarization	P_r	29.03 ± 0.21	$\mu C/cm^2$
Coercive Field	E_c	1.23 ± 0.18	MV/cm
Endurance		0.23 ± 0.11	10^5 cycles

The processing of the FLA samples are outlined in Section **??**. For the first FLA series, hereby denoted sample series 1, the flash intensity was varied between 15-32.5 J/cm^2 to reach different peak temperatures in the film. The film deposition and annealing conditions for these samples are summarized in table **??**.

Table 5.2: Selected processing conditions for sample series 1.

Sample Number		1	2	3	4	5
HZO						
Growth Temperature	[°C]	200	200	200	200	200
Film Thickness	[nm]	10	10	10	10	10
FLA						
Preheat Temperature	[°C]	250	250	250	250	250
Flash Intensity	[J/cm^2]	**15**	**20**	**25**	**30**	**32.5**
Number of Flashes		1	1	1	1	1

Resulting electrical characterization from sample series 1 are shown in figure **??**. Samples annealed with an intensity less than 25 J/cm^2 did not show any ferroelectric behaviour and are hence omitted from some of the figures. As shown in figure **??**a and b the PUND characteristics show ferroelectric behaviour with a strong dependance on peak film temperature. However, for higher peak temperatures these characteristics decline to both weaker polarization response and higher coercive fields which is undesireable. The peak PUND performance at 30 J/cm^2 does not reach the characteristics of the RTP references outlined in table **??** which shows that the energy deposited during the annealing process is not enough to crystalize the entire HZO film while not inducing other effects to reduce the ferroelectric response.

Although reduced PUND characteristics were found for these samples, figure **??**c show an increased endurance for the flash annealed samples compared to

the RTP reference.

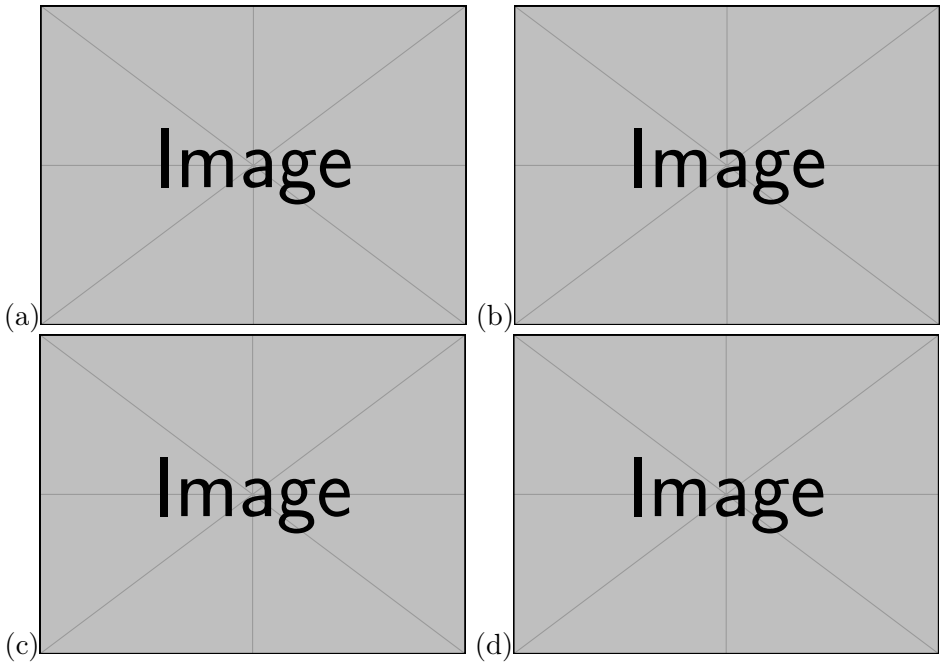

Figure 5.2: Figure showing all measured data from an intensity-varied batch. Low-doped subtrate, 200C ALD, HZO 1:1, 250C preheat, 5ms flash. RTP reference is included for Endurance and Defect Density.

Chapter 6
Conclusion

Mål: Wrap it up. Lägg fram de främsta resultaten/ideerna och ge tips på hur man kan undersöka vidare.

References

[1] R. Athle, "Development of ferroelectric hafnium oxide for negative capacitance field effect transistors," *LUP Student Papers*, 2019.