Kevin Keegan **Dublin, Ireland** kevinkeegans@gmail.com
www.linkedin.com/in/kevin-keegan-engineer +353-876428470

Summary

Electronic Engineer with 5 years of industry experience.
Currently a senior member of the digital design team in the AMS group at AMD.
1st Class Honours Masters degree in Electronic & Computer Engineering from University College Dublin.
Experienced with **System Verilog, Python, C, Linux**.
Interested primarily in Digital Signal Processing & and RTL design.

Technical Skills

- **Languages/Tools**: Verilog, System Verilog, Python, Bash, MATLAB, C, Git, Perforce, LaTeX.
- **Operating Systems**: Proficient in Linux and Windows environments.
- **Digital Design**: Experienced in:
  - Frontend RTL Design
  - Power/Area & Timing Optimization
  - CDC Techniques
  - Real Number Modelling
  - Digital Down Converter Implementations
  - Linting (spyglass)
- **Digital Signal Processing**: Knowledgeable in:
  - Spectrum Analysis
  - Digital Filtering
  - Digital Communication Theory

Professional Experience

- **AMD, Wireless and Wired Group** Dublin, Ireland
  Senior Digital Design Engineer *May 2021 – Present*
  - ASIC Front-End Digital Design
  - Played a key role as one of the lead design engineers on the ADC in RFSOC
  - Block Owner for the Digital Down Converter
  - Implemented new features for a highly configurable system of polyphase decimation filters
  - Led the design of a complex equalizer
  - Successfully integrated and brought up a channelizer
  - Implemented digital blocks responsible for calibrating various components in the analog portion of the ADC.
  - Mentored interns in 2022 & 2023, overseeing their progress on a filter design project
  - Implementing real number models of analog blocks in System Verilog to aid digital verification
  - Provided extensive support to the verification team & other design engineers
  - Developed a Python script to enhance the team's analysis of the ADC's performance,

- **Dialog Semiconductor, ASIC & IP Division** — Dublin, Ireland
  Digital Design Engineer — *Jan 2020 – April 2021*
  - Front-End Digital Design
  - Designed a CIC based anti-aliasing filter
  - Developed scripts to automatically generate a Verilog implementation of a frequently redesigned block, along with its System Verilog testbench.

- **Susquehanna International Group (SIG)** — Dublin, Ireland
  Market Data Engineer — *Sept 2018 – Nov 2019*
  - Monitoring and maintaining critical market data systems.
  - Pcap file analysis via Wireshark/tshark
  - Developed validation tools to test new software before pushing to production.
  - Implemented a system in Python & Bash to archive daily market data recordings from company colocations to a central archive.
  - On call work. When on call, I was the first point of contact for issues regarding SIG's market data infrastructure.

- **Intel Corporation, Internet of Things and Wearables Group** — Kildare, Ireland
  Physical Design Engineer Intern — *Jan 2017 – Aug 2017*
  - Developed a tool in TCL to automate the design, layout & routing of a custom CMOS block.

- **University College Dublin** — Dublin, Ireland
  Voluntary Teaching Assistant — *Sept 2015 – Nov 2015*
  - Voluntary Teaching Assistant in weekly laboratories for the engineering module, EEEN20010 Computer Engineering I: Data Structures and Algorithms through C.

- **FireEye, Inc.** — Dublin, Ireland
  Software Engineer Intern — *May 2015 - July 2015*
  - Developed BASH scripts to facilitate and automate product testing.
  - Built a customized, kickstarted centOS distro to include the configurations and packages necessary for running & testing a company product.

Education

- **University College Dublin** — Dublin, Ireland
  Master of Engineering in Electronic & Computer Engineering; 1st Class Honours — *Sept 2016 – Sept 2018*
  - **GPA**: 3.84/4.2
  - **UCD Intel Masters Scholarship**: Awarded by Intel to top five students entering ME program.

- **University of California Los Angeles** — Los Angeles, CA
  Exchange - Electrical & Electronic Engineering; ***GPA: 3.18/4.0*** — *Jan 2016 – Jun 2016*

- **University College Dublin** — Dublin, Ireland
  Bachelor of Science in Electrical & Electronic Engineering; 1st Class Honours — *Sept 2013 – Sept 2016*
  - **GPA**: 4.09/4.2
  - **Entrance Scholar**: Awarded to top academic achievers entering UCD from secondary school.

- **Coláiste Eoin** — Dublin, Ireland
  Irish Leaving Certificate; ***Points: 595*** — *Sept 2007 – Jun 2013*